Design and Implementation of a Solar Buck MPPT Charge Controller

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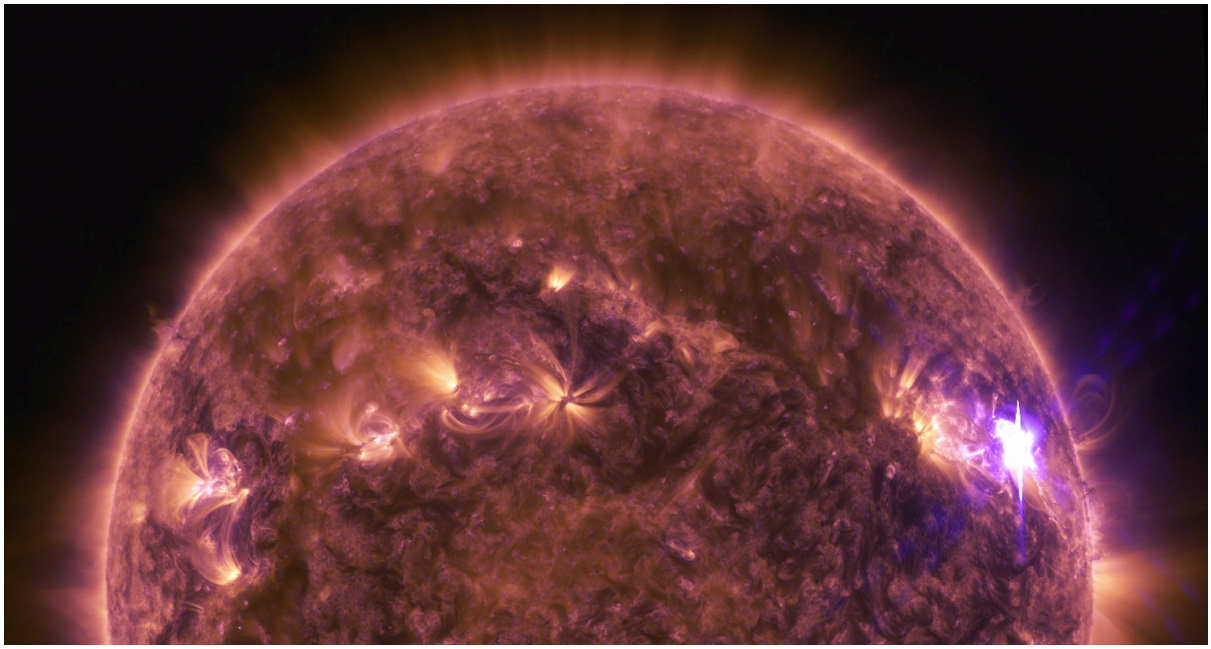
1 Introduction



Our sun is the centre of our solar system and the source of all life on Earth. Within its core, the pressure reaches an estimated 2.60GPa at a searing 15 million Kelvin, which results in an environment where light atoms such as hydrogen may overcome the electric force and fuse into helium via proton-proton chain reactions (with some help of quantum tunnelling) [1]. As a result of this process, approximately 700 million tonnes of hydrogen is fused into 695 million tonnes of helium per second. The resulting difference in mass, or "*mass defect*", is converted to energy. Via Einstein's famous equation, and given this occurs on a per-second basis, we can approximate the power created in this process:

$$P_{sun} \approx mc^2t = (5 \times 10^9 \text{ kg } \cdot (2.98 \times 10^8 \text{ m} \cdot \text{s})^2 \cdot 1 \text{ s }) = 4.4402 \times 10^{26} \text{ W}$$

This immense power is equivalent to detonating 400 billion 1 Megaton nuclear bombs every second [2]. A fraction of this energy, after radiating 1 astronomical unit of (mostly) empty space, (150 million km) electromagnetic waves bombard Earth's upper atmosphere delivering approximately 15 petawatts (15×10^12 W) of power. Harnessing this free and abundant energy then becomes a technical challenge. How can we, as engineers, design systems that convert natures generosity into stable, usable power? This project

explores one answer. Detailing the design, implementation, and testing of a Maximum Power Point Tracking (MPPT) solar charge controller based on a buck converter topology. The controller is designed for use with AGM lead-acid batteries and integrates real-time monitoring, fault handling, and embedded control via ESP32 microcontroller.

2 Project Overview

- **Voltage Input:** Solar panel (18–40V nominal)
- **Input Current Maximum:** 10A
- **Output:** 12V AGM battery (charge voltage up to 14.4V)
- **Control:** MPPT algorithm (Perturb and Observe)
- **MCU:** ESP32-S3 with FreeRTOS
- **Power Stage:** Buck converter with external MOSFETs

3 System Architecture

Synchronous Buck Converter

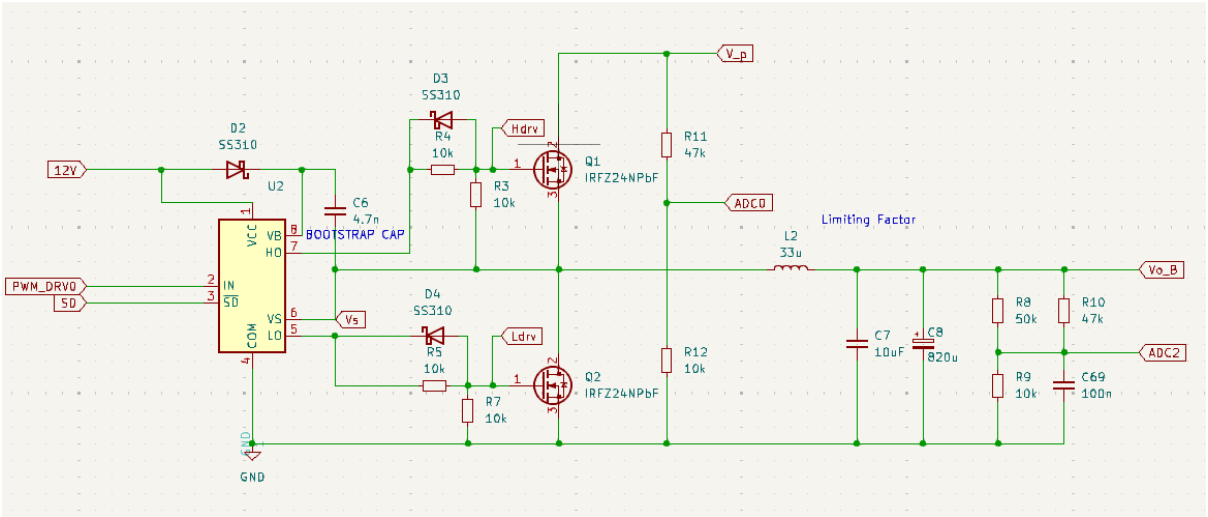


Figure 1: Main Synchronous Buck

A synchronous buck converter, shown in Figure [1] is a type of DC-DC converter used to step down voltage efficiently. It operates similarly to a basic (non-synchronous) buck converter but replaces the catch diode with a second controlled switch—usually a MOSFET. This second switch (called the *low-side switch*) is synchronised with the main *high-side switch* to improve efficiency, especially at higher currents.

- When the high-side MOSFET is on, current flows from the input through the inductor to the output, storing energy in the magnetic field of the inductor.
- When the high-side switch turns off, the low-side MOSFET turns on. This allows the inductor current to continue flowing to the output, but now through the low-side switch instead of a diode.

By replacing the diode with a MOSFET, conduction losses are reduced (since the MOSFET has a lower voltage drop than a diode), making synchronous buck converters more efficient than their asynchronous counterparts. However, the control circuitry is more complex because it must ensure that both switches are never on at the same time (to avoid *shoot-through*).

They are widely used in applications like CPUs, FPGAs, and battery-powered devices where both efficiency and size are important.

3.1 Block Diagram

3.2 Key Hardware Components

Component	**Description**	**Part Number**
MCU	Control unit running MPPT	ESP32-S3
Power Stage	Buck topology power converter	IRFZ44N, IRS2184
ORing Controller	OVLO, UVLO, Reverse Polarity Protection	LM74502,TPH2R608NH
Current Sensing	Hall-effect sensor	ACS712
Voltage Sensing	Resistor divider + filtering	Custom
Display (optional)	OLED/I2C interface	SSD1306
Peripheral Power Management	V_{in} to 5V regulated	XL7005, AZ1117-5.0

4 MPPT Algorithm

4.1 Perturb and Observe

The algorithm samples voltage and current from the panel, computes power, and perturbs the duty cycle to maximise the extracted power.

$$P(t) = V_{\text{panel}}(t) \cdot I_{\text{panel}}(t)$$

$$\text{If } P(t) > P(t-1) \Rightarrow \text{Continue in same direction, else reverse}$$

5 Firmware Implementation

Firmware is implemented on an ESP32-s3-Wroom microcontroller using the esp-idf development environment. The ESP32-s3 contains two Xtensa dual-core 32 bit LX7 microprocessors with 384KB of ROM and 512KB of SRAM [5].

5.1 RTOS Architecture

Tasks are divided as follows:

- `mppt_task`: Runs the control loop every 100 ms
- `adc_task`: Samples current and voltage
- `fault_monitor_task`: Detects overcurrent, undervoltage conditions
- `ui_task`: Updates display or serial output

5.2 Code Snippet: MPPT Control Loop

```
        void mppt_task(void *params) {
            while(1) {
                float voltage = get_panel_voltage();
                float current = get_panel_current();
                float power = voltage * current;

                if (power > prev_power) {
                    duty ++;
                } else {
                    duty --;
                }
                set_pwm_duty(duty);
                prev_power = power;
                vTaskDelay(pdMS_TO_TICKS(20));
            }
        }
```

Listing 1: MPPT Control Logic

6 Theoretical Analysis

Prior to PCB design, theoretical analysis and simulation was completed to validate component selection for the main buck converter. Peripheral buck converters were designed via TI. The following specifications were used to analyse the system.

Parameter	**Limit**	**Rationale**
Switching Frequency	50kHz	Balance switching losses and allowable ripple
PV Input Voltage	15V< V_{in} <50V	MOSFET, UVLO Limit
PV Input Current	0< I_{in} <10A	Currently limited by inductor
Duty Range	0.3< D <0.95	Limited by V_{in} max and ESP32
Duty Resolution	1024 Bits	ESP32 Limit
Output Voltage Minimum	14V	Lead-Acid Charging

1. **Inductor Sizing:** The inductor is one of the main design factors in any switching converter. Considerations were made firstly to ensure constant current-mode operation over all operational parameters. The minimum inductance necessary was evaluated using the parameters in Table 2. Firstly, the minimum inductance required to sustain was found via the relation

$$L_{min} = \frac{T}{2}\frac{V_{out}}{I_{out}}(1 - D)$$

Solving for this equation over the full operating cycle via Matlab gave the characteristic curve in Figure [2], evaluated over maximum input current.

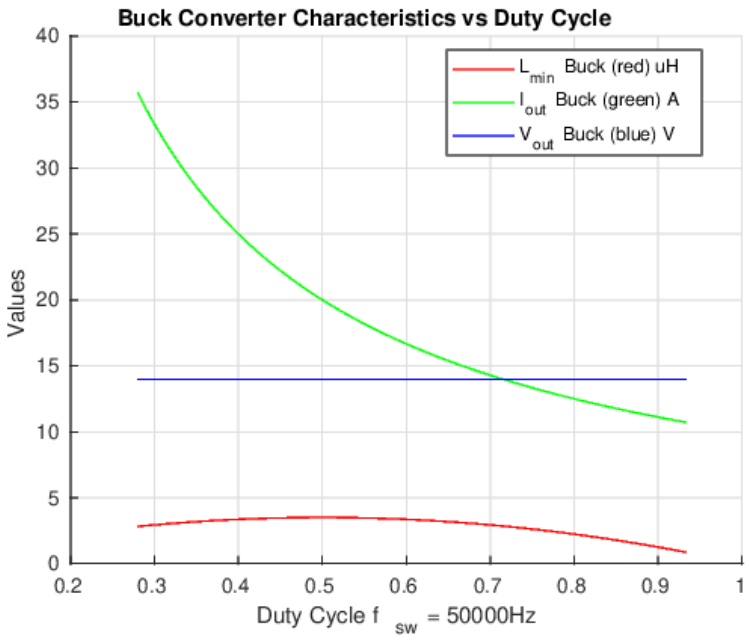


Figure 2

In order to evaluate the inductor ripple current, we must first evaluate the duty cycle, as is standard for PWM driven buck converters, we will assume CCM. We will also assume an output voltage of 14V, which is sufficient to charge lead-acid batteries.

$$D_{min} = \frac{14}{50} = 0.28$$
$$\triangle i_L = \frac{(v_o t_{off})}{L} = \frac{(14)(0.28/50 \times 10^3)}{33 \times 10^{-6}} = 6.101A$$

Note that this ripple value is relatively large at the worst-case operating point. Further design considerations may be necessary when charging.

2. **Input Capacitor Sizing:** Bulk capacitance on the input of the buck converter allows for energy storage. The energy stored in the capacitors can be used to maintain the current within the inductor on duty cycle changes. Thus, two large 1mF capacitors were put in parallel on the input.

3. **Output Capacitor Sizing:** The output capacitor acts as an AC short, which in turn reduces the effects of the inductor ripple $\triangle i_L$. Too large of a ripple on output also constrains the controller due a need to track a large output voltage setpoint. As a result, a design ripple of 0.05V was set. In order to maintain a ripple voltage of 0.05V on output, we solve the equation:

$$\triangle V_o = \frac{\triangle i_L t_{off}}{8C} + \triangle i_L R_{esr}$$

Where R_{esr} is assumed to be small enough such that the additional ripple is negligible.

$$C = \frac{\triangle i_L t_{off}}{8 \triangle V_o}$$
$$C = \frac{6.101(\frac{0.28}{50 \times 10^3})}{8(50 \times 10^3)} = 85.4\mu\text{F}$$

100μF capacitors were deemed sufficient.

4. **MOSFETs:** For a synchronous buck topology, the MOSFETs need to be selected to optimise trade-offs between switching losses. The IRFZ24NPbF was selected.

ID	**Maxima**	G_c	V_{th}	R_{DS}	RT (ns)	FT (ns)
IRFZ24	55V & 17A	5.3nC	2-4V	7mΩ	34	27

Using these values, we can analyse the power losses. Given FET rise time: $t_r = 34\,\text{ns}$ and FET fall time: $t_f = 27\,\text{ns}$, we can evaluate the highside FET switching losses:

$$\begin{aligned} P_{sw} &= \frac{1}{2} V_{on} I_{on} f_s (t_{on} + t_{off}) \\ &= \frac{1}{2}(50)(10)(50 \times 10^3)(61 \times 10^{-9}) = 0.76W \end{aligned}$$

When the low-side FET switches, it switches full output load current and output voltage, so, for the maximum power case,

$$\begin{aligned} I_{on} = I_o &= \frac{10}{0.28} = 35.7A \textbf{ Exceeds limit!} \\ P_{sw} &= \frac{1}{2} V_{on} I_{on} f_s (t_{on} + t_{off}) \\ &= \frac{1}{2}(15)(35.7)(50 \times 10^3)(61 \times 10^{-9}) = 0.82W \end{aligned}$$

Conduction losses are non-negligible, however are minimised by the small R_{DS}.

Conduction losses are estimated below for the limits of duty cycle (recall $0.28 < D < 0.95$):

$$\begin{aligned} P_{HS(on)} &= R_{DS} I_{in}^2 D = 7 \times 10^{-3}(10^2)(0.28) = 0.196W \\ &= 7 \times 10^{-3}(10^2)(0.95) = 0.665W \\ P_{LS(on)} &= R_{DS} I_{out}^2 (1 - D) = 7 \times 10^{-3}(\frac{10}{0.28})^2(0.28) = 2.5W \\ &= 7 \times 10^{-3}(\frac{10}{0.95})^2(0.95) = 0.73 \end{aligned}$$

5. **TODO:** Estimate the theoretical efficiency of the converter assuming only conduction and switching losses.

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} = \frac{1600 - 3.5}{1600} = 99.7\%$$

This is far too high of an efficiency. Inductor conduction losses would also contribute to reducing the efficiency.

6. **IRS2184 MOSFET Driver and Gate Drive**

The IR2104 is used to prototype as the 8-lead DIP package was readily available, however since it has been replaced with the IRS2184 due to the IRS2184's reduced dead time, fall time, and rise time, allowing for the possibility of firmware alterations of switching frequencies.

ID	Rise Time	Fall Time	Dead Time	Current Source/Sink
IR2104	170ns	90ns	520ns	0.13/0.27A
IRS2184	60ns	40ns	500ns	1.4/1.8A

6.1 Backflow Protection

In order to prevent backflow current, an ORING controller is used in line with the power trace.

LM74502H ORing Controller

The LM7450H is an ORING controller with a range of safety features, listed below:

- **Overvoltage Protection:** An internal comparator with reference $V_{OVR} = 1.25$V is fabricated within the IC. By designing a resistive divider, we can set an overvoltage.

$$V_{OV} = \frac{(R_1 + R_2)V_{OVR}}{R_2}$$

- **Reverse Voltage Protection:** Use of back-to-back n-channel MOSFETs on the conduction path prevent component damage from reverse polarity inputs.
- **Backflow Current Protection:** The SRC pin is connected to the source of the external N-channel MOSFET, and the gate is driven by an internal charge pump relative to this node. During night-time or low irradiance conditions, the input voltage (panel side) falls below the output (battery side), preventing the charge pump from developing sufficient voltage above the under-voltage lockout (UVLO) threshold. As a result, the gate is not driven high enough to turn on the MOSFET, and backflow current is blocked through the body diode of the MOSFET.

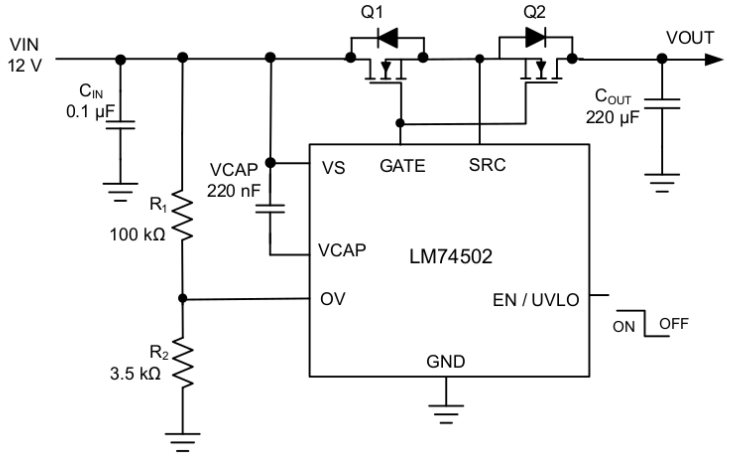


Figure 3: Taken from lm74502 Datasheet: Typical Application Circuit

With the LM74502H ORing Controller, it was deemed that the conduction power loss was insignificant and did not need additional heatsinking so long as $R_{DS(on)} < 5m\Omega$,

which would result in $P < 10^2(5 \times 10^{-3})$=0.5 W maximum conduction dissipation. The **TPH2R608NH** SMD N-channel MOSFET met this criteria.

ID	Maxima	G_c	V_{th}	R_{DS}
TPH2R608NH	75V & 150A	28nC	2-4V	7mΩ

7 Simulation Results

Initial Simulation

The circuit of Figure [4] was simulated to confirm theoretical calculations at the lowest output voltage of 15V, and validate the successful operation of an equivalent circuit of the LM74502 backflow controller.

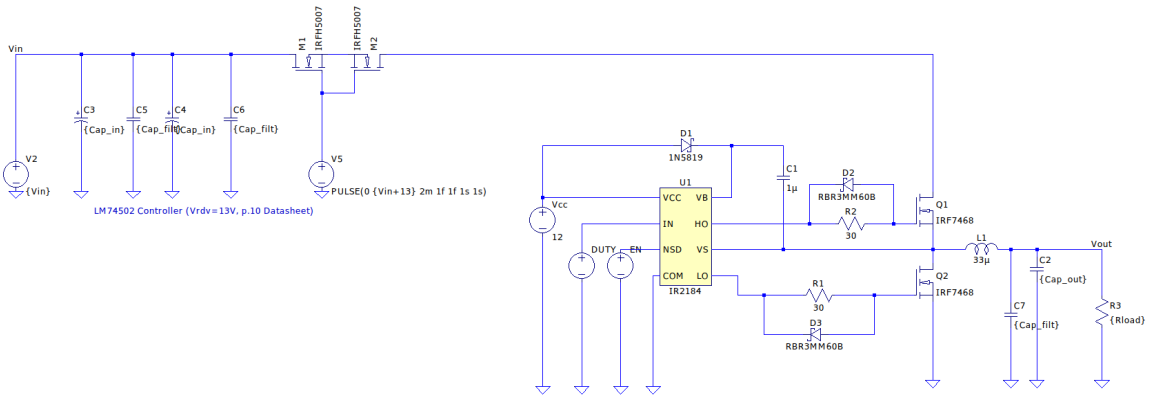


Figure 4: Simulated Powerstage

Table 6: Simulation Values and Design Rationale

Parameter	Limit / Range	Design Rationale
V_{in}	15< V_{in} <50V	Design operational range
V_{out}	14V	Minimum Charging Voltage
Inductor Ripple	6.05A@ D=0.28 , 0.5A @ D=0.95	
Output Voltage Ripple	0.15V@ D=0.28, 0.023V@ D=0.95	
Efficiency	0.95 @ D=0.28, 0.98 @ D=0.95	

Practical Solar Panel Simulation

In order gain an understanding of the MPPT's normal operating parameters, a simple solar panel model was derived. Using a temperature dependent solar panel model derived from [6] chapter 27, shown in Figure

Which was used to replicate the TSM-PC05 solar panel. The V-I curve of the model closely replicated the V-I curve of taken from the datasheet of the solar panel at different

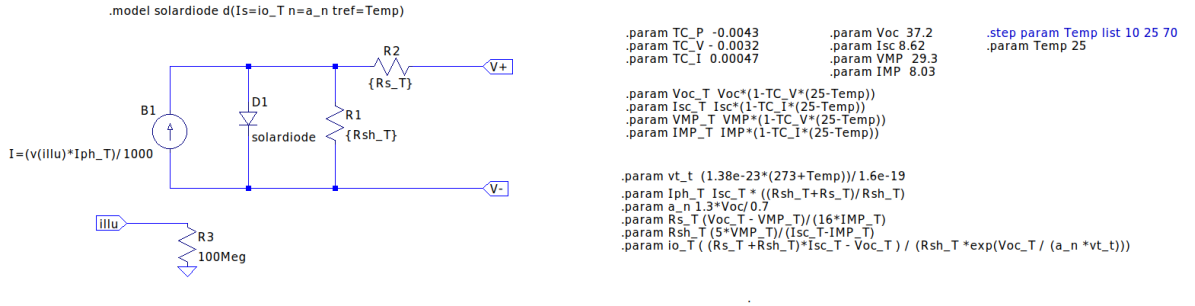


Figure 5: Solar Cell Model

irradiance levels (specifically 200, 600, and 1000 W/m^2), as can be seen in Figure [6] and Figure [7]

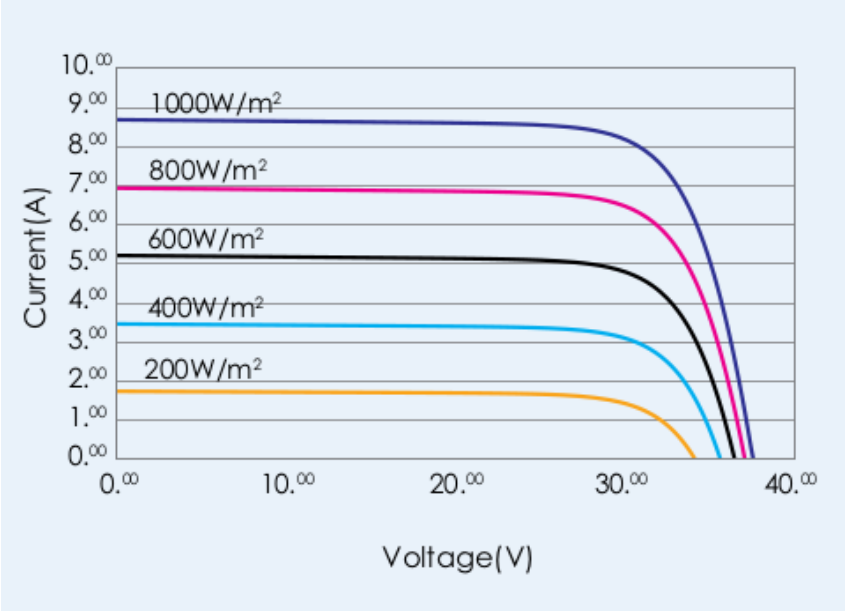


Figure 6: IV Curve of PV module TSM-245 PC05

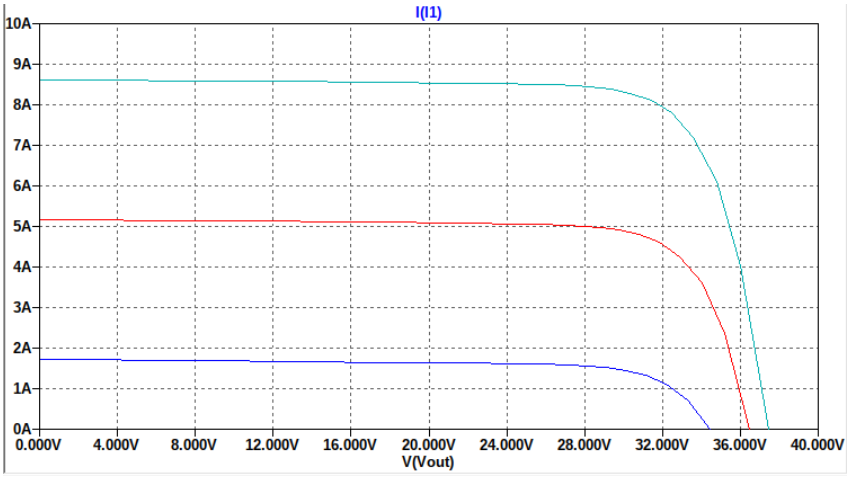


Figure 7: IV Curve of Simulated PV Module

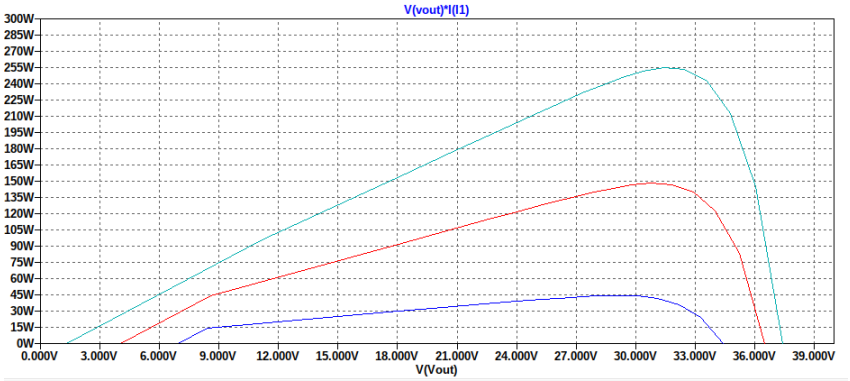


Figure 8: Replicated Power Curve

Which provide accurate results within one decimal place. This model was then used with the buck converter model to confirm the design adheres to the circuits operational maximums when connected to the solar panel. In order to simulate the circuit in Figure [9] at the the MPP, the procedure was followed:

1. Find the maximum power point (V_{MPP}, I_{MPP}) from the simulated circuit in Figure [7], which was found to be 255W at $V_{MPP} = 32$V and $I_{MPP} = 7.96$A, slightly above the datasheet values.

2. Assuming efficiency $\eta = 1$, solve for output load resistance required to evaluate the circuit at the specified power point:

$$R_{load} = \frac{V_{out}^2}{P} = \frac{14^2}{230.4} = 0.76\Omega$$

   The output voltage being 14V such that maximum ripple current and voltage can be evaluated at the smallest duty cycle (largest off time).

3. Solve for D, given $V_{in} = 32$V and $V_{out} = 14$V, the duty cycle is 0.4375.

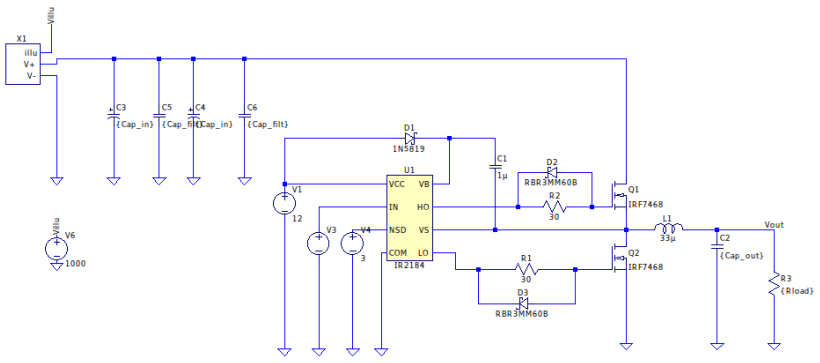


Figure 9: Synchronous Buck Power Stage with Solar Input

The key simulation parameters are evaluated below:

Table 7: Simulation Values and Design Rationale @ 1kW/m^2

Parameter	**Limit / Range**	**Design Rationale**
V_{in}	32	Maximum Power Point
V_{out}	14V	Minimum Charging Voltage
Inductor Ripple	4.8A @ D = 0.4375	
Output Voltage Ripple	0.1V@ D=0.4375	
Efficiency	0.86 @ D=0.4375	
Avg. Output Current	15A	

It was found at this maximum power point, all simulation parameters remained the absolute maximum of the design specification.

All simulation models can be found within the GitHub repository.

8 Initial PCB Design

Initial PCB design consists of a synchronous buck power stage that is digitally controlled via an ESP32-s3.

- Four-layer PCB, KiCad layout
- Thick traces for high-current paths
- Heatsinking for power MOSFETs
- Thermal Relief Vias
- Additional i2c and debugging ports.
- CANbus transceiver for future work with BMS systems.

Screenshots top and bottom layer of the first PCB prototype are shown in Figures [10, 11].

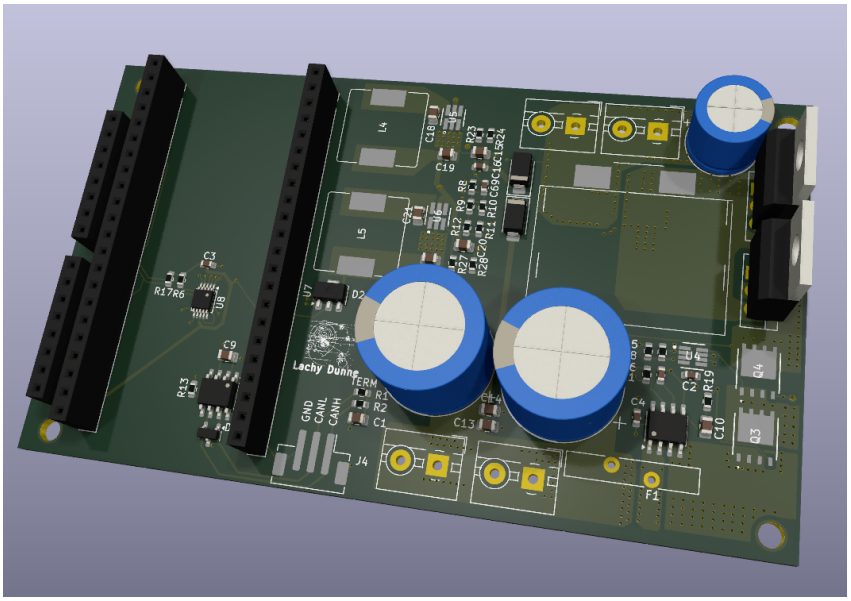


Figure 10: Prototype PCB Layout: Top Layer

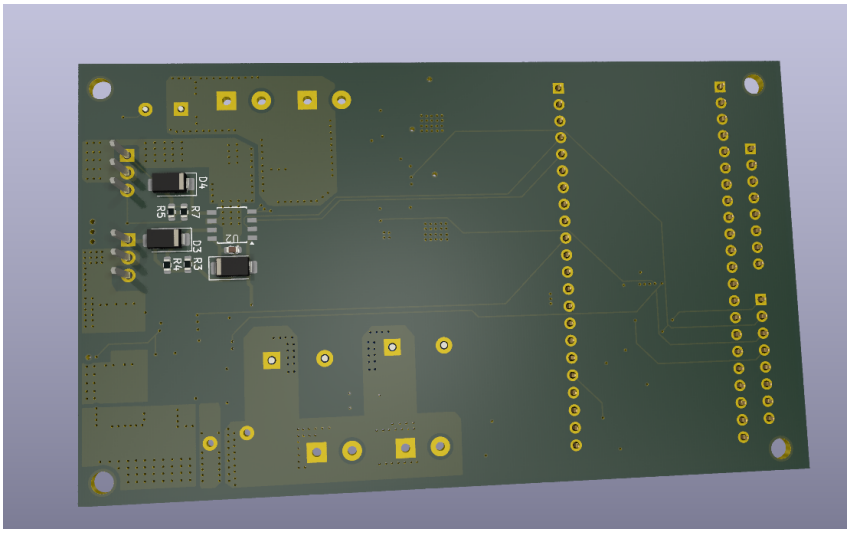


Figure 11: Prototype PCB Layout: Bottom Layer

9 Testing and Results

In order to validate the buck converter working, a list of tests have been devised and are to be evaluated once the hardware is assembled and the software is flashed.

Physical Requirements

ID	Description	Rationale	Ver
PHY-001	Device shall operate from 12 V DC input.	Power standardisation.	Tes
PHY-002	MCU Power $<$ 500mW	Continuous operation.	Mea
PHY-003	PCB Fills should be minimum 20mm for 10A input current		

Functional Requirements

ID	Description	Rationale	Verification
FUN-001	System shall log PV data every 10 seconds.	Ensures timely monitoring.	Test
FUN-002	System shall transmit data wirelessly.	Remote monitoring.	Demonstration

Performance Requirements

ID	Description	Rationale	Verification
PER-001	System shall have an uptime of 99.5%.	Reliability for mission success.	Analysis
PER-002	Response time shall not exceed 500 ms.	Ensures responsiveness.	Test
PER-003	Signal Strength Minimum -50dBi at 20m	Ensure user receives alerts	Test
PER-004	Failures must be detected in $<$ 3s	Robust repsonses	Test

9.1 Test Setup

- Bench power supply simulating solar panel
- 12V AGM battery load
- Oscilloscope to monitor switching waveform

9.2 Results Summary

Test	Expected	Observed
Input Voltage Range	15–40V	**TODO**
Output Voltage	13.8–14.4V	
Max Current	10A	
Desired Charging Current	1A	
Efficiency	85%	

10 Future Work

- Implement more advanced MPPT (Incremental Conductance)
- Add Bluetooth telemetry using ESP32
- Expand to multi-panel input and higher voltage ranges

11 Conclusion

This project demonstrates a functional, efficient MPPT controller using a buck converter and real-time embedded control. It serves as a foundation for further exploration into smart solar systems and low-cost energy harvesting.

Appendix

Formulas and Nomenclature

References

[1] Serway: Physics for Scientists and Engineers with Modern Physics, Third Edition.

[2] M. Freer: Institute of Physics: Nuclear Fusion Explained

[3] Texas Instruments: Web Bench power designer

[4] P. Horowitz & W. Hill: The Art of Electronics 3

[5] ESP32-S3-WROOM-1 Datasheet Version 1.5

[6] Power Electronics: Devices, Drivers, Applications, and Passive Components. Barry Williams.