NVIDIA Jetson Nano

Thermal Design Guide

TDG-09383-001_v1.4 | December 2020

Document History

TDG-09383-001_v1.4

Version	Date	Description of Change
1.0	February 1, 2019	Initial Release
1.1	March 4, 2019	• Minor changes throughout this thermal design guide • Added reference to the platform adaptation guide for customizing fan control.
1.2	August 12, 2019	• Updated thermal values in Table 2-1. • Updated "Tegra X1 Shutdown Temperature" section (Section 4.5).
1.3	June 26, 2020	Updated Table 3-1 with eMMC description
1.4	December 3, 2020	Added Chapter 4 on thermal design guidelines

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Chapter 1. Introduction

This document is the thermal design guide (TDG) for the NVIDIA® Jetson Nano™ (699-13448-0002-xxx) product.

The purpose of this thermal design guide is to provide the system-level thermal, mechanical and qualification requirements for the Jetson Nano.

Refer to the Jetson Nano module data sheet for detailed drawing and module dimensions.

1.1 Customer Requirements

The customer requirements are as follows:

- Customers are responsible for reading and understanding this entire thermal design guide.
- Customers are responsible for implementing a thermal solution that maintains the NVIDIA® TEGRA® X1 temperatures below the specified temperatures in Table 2-1 under the maximum thermal load and system conditions for their use case.
- Customers are responsible for designing a system that delivers enough power to the Jetson Nano to sustain the maximum thermal load for their use case.
- Customers are responsible for qualification of the Jetson Nano in their system and are responsible for any issues related to failure to qualify the product properly.

1.2 Definitions

This section describes terminology that will be referenced throughout this thermal design guide.

1.2.1 Total Module Power

The total module power (TMP) represents the average board power dissipation while the system is running the target workload under the worst-case conditions in steady state. System designs must be capable of providing enough cooling for the Jetson Nano when operating at the TMP level.

1.2.2 Jetson Nano

Figure 1-1 provides a topside view of the Jetson Nano while Figure 1-2 provides the backside view.

Figure 1-1. Jetson Nano – Topside View

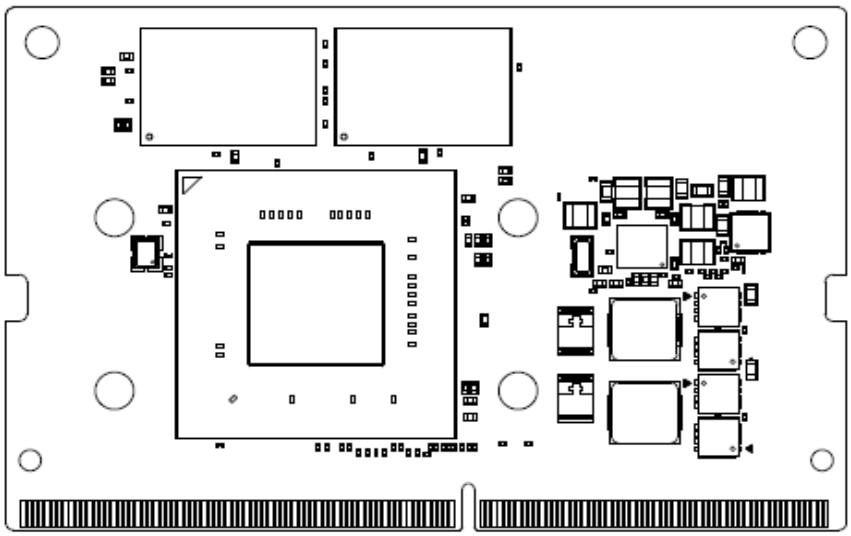
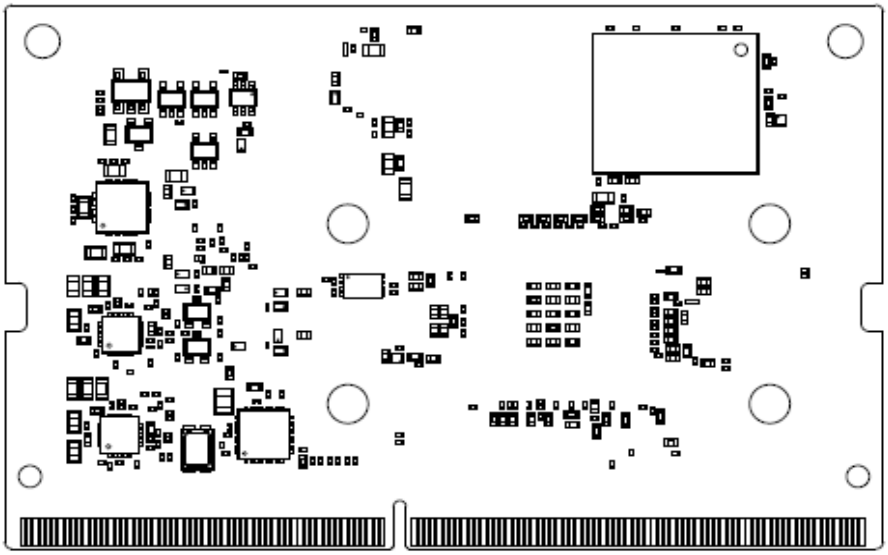


Figure 1-2. Jetson Nano – Backside View



The thermal solution of the customer's system design should attach to the module directly. Mounting holes are provided on the PCB to enable attachment of the customer's thermal solution. More details are provided in Section 3.2 "Mechanical Information." Customer's system thermal solution must provide adequate cooling to maintain all the components on the PCB including the Tegra X1 below the maximum temperature specifications as detailed in Section 2.1 and Section 3.1.

1.2.3 Tegra X1 Temperature

The Tegra X1 junction temperature (T_j) represents the Tegra X1 die temperature read from any of the internal temperature sensors. The on-die thermal sensors are used for high-temperature T_j management and many other temperature-dependent functions. Details regarding the software thermal mechanisms are described in Chapter 5.

Chapter 2. Specifications

2.1 Thermal Specifications

On Tegra X1, there are multiple on-die temperature sensors that are placed close to dominant hotspots for high accuracy measurements of junction temperature. A built-in hardware controller is used to read the sensors and engage thermal protection mechanisms. Chapter 5 contains the details related to these sensors and the associated thermal protection mechanisms. The specifications in Table 2-1 must be followed in order to maintain the performance and reliability of the Jetson Nano module.

Table 2-1. Jetson Nano Thermal Specifications

Parameter	Value	Units
Maximum Tegra X1 operating temperature[1]	T.cpu = 97	°C
	T.gpu = 97.5	°C
Tegra X1 shutdown temperature[2]	T.cpu = 102.5	°C
	T.gpu = 103	°C

Notes:

[1]The Tegra X1 maximum operating temperature is the temperature below which the product will operate at the specified clock speeds. Software will apply clock speed reductions once this temperature is reached. Note that power fluctuations that induce T_j fluctuations above these thresholds will cause temporary clock reductions. See Section 5.1 for details.

[2]The Tegra X1 will shut down the Jetson Nano module once any of these software-imposed temperature limits are reached to maintain the reliability of the Tegra X1. See Section 5.5 for details.

Chapter 3. Design Guidance

This chapter provides design guidance to meet the Jetson Nano module specifications.

3.1 Thermal Information

The design goal for system thermal management is to keep the Tegra X1 temperature below the limits specified in Section 2.1.

3.1.1 Jetson Nano Thermal Performance

The Jetson Nano module is not equipped with a system level thermal solution to dissipate the TMP thermal load into the ambient environment. It is the customer's responsibility to design an adequate thermal solution to maintain all the component temperatures below the de-rated limits as specified in Table 3-1. Figure 3-2 provides a map of the component placement on the Jetson Nano PCB as listed in Table 3-1. The thermal resistance network for the system thermal solution can be represented with the following equation:

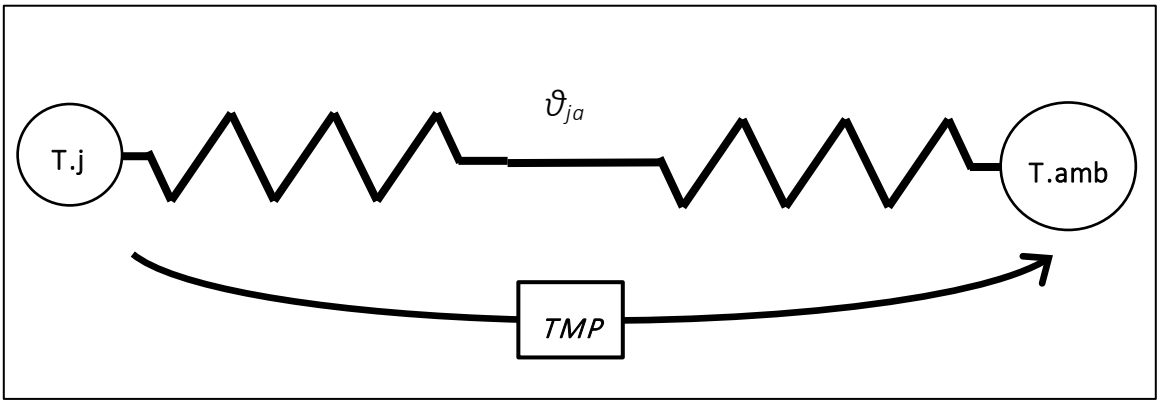
$$\theta_{12} = \frac{T_1 - T_2}{P}$$

Where:

θ_{12}	The thermal resistance between Point 1 and Point 2
T_n	The temperature at Point *n*
P	The heat load (i.e; dissipated power) transferred between Points 1 and 2

A simple example of a thermal resistance network is shown in Figure 3-1, where θ_{ja} represents the thermal resistance from T_j to the ambient of the system thermal solution. The thermal resistance of the system thermal solution may include multiple components including, but not limited to, thermal interface material, heat spreaders, and heat sinks.

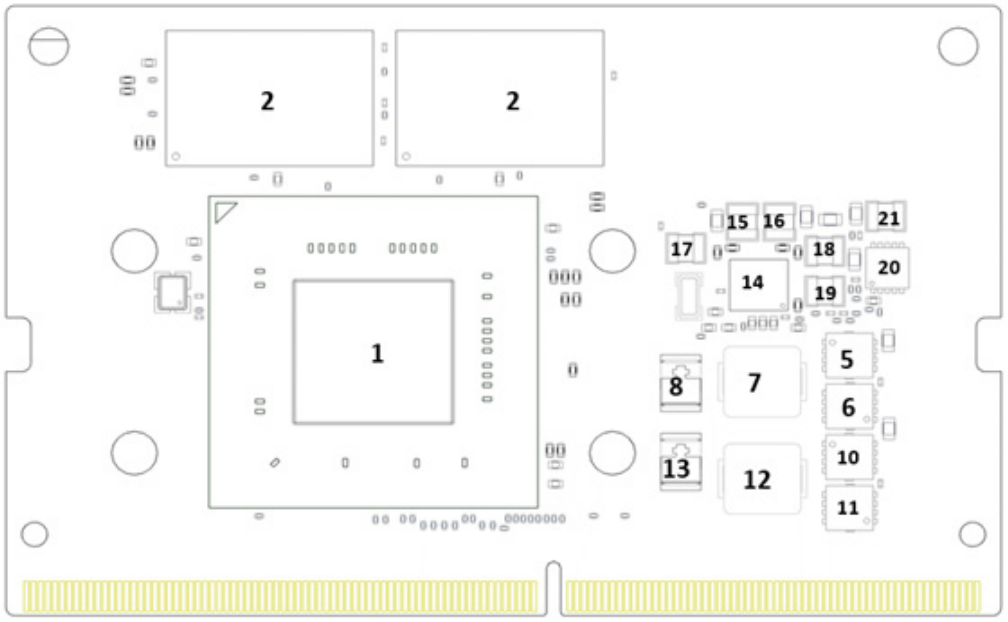
Figure 3-1. Thermal Resistance Network



Jetson Nano enables a wide variety of applications that may exercise different components on the module. The variation between applications will cause variation in heat loads on the different components on the Jetson Nano and hotspots in different logical partitions of the Tegra X1. While the system thermal solution will help to spread the heat and make the thermal performance as consistent as possible, different applications will have different levels of thermal performance. The more evenly the module power is distributed across the Jetson Nano the higher the thermal performance will be.

Figure 3-2. Component Placement Map for Jetson Nano

Top Side



Bottom Side

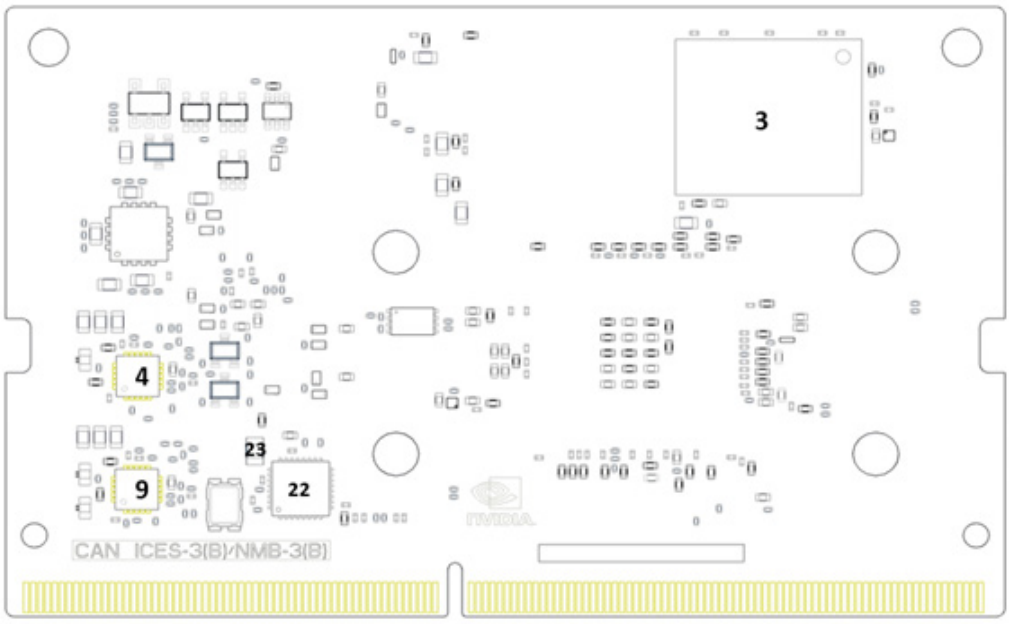


Table 3-1. Jetson Nano Thermal Performance

Components that will be contacted and need to be monitored

Components that need to be monitored and may require contact with thermal solution

Miscellaneous

Comp # on Map	REFDES(s)	Description	Qty	Thermal Specifications
				Tcase
(Number)	*(Name)*		*(Count)*	*(°C)*
1	U7	TEGRA X1	1	Refer to Table 2-1
2	M1, M2	LPDDR4 Memory	2	85
3	U513	eMMC	1	95
4	U530	CPU Voltage Regulator	1	115
5	Q2	CPU HS MOSFET	1	115
6	Q5	CPU LS MOSFET	1	115
7	L29	CPU Inductor	1	100
8	C1217	CPU Output POSCAP	1	85
9	U526	GPU Voltage Regulator	1	115
10	Q1	GPU HS MOSFET	1	115
11	Q8	GPU LS MOSFET	1	115
12	L30	GPU Inductor	1	100
13	C344	GPU Output POSCAP	1	85
14	U4	PMIC	1	85
15	L4	PMIC SOC Inductor A	1	100
16	L11	PMIC SOC Inductor B	1	100
17	L3	PMIC VDD_DDR_1V1 Inductor	1	100
18	L12	PMIC VDD_PRE_REG_1V35 Inductor	1	100
19	L13	PMIC VDD_1V8 Inductor	1	100
20	U32	VIN->3V3 Supply Regulator	1	115
21	L31	VIN->3V3 Supply Inductor	1	100
22	U41	ENET	1	95
23	L502	ENET Reg Inductor	1	85

The components to be monitored above should be instrumented to measure case temperature while the system is running heavy use case loads and in the maximum temperature environment the system will have to be operated in. If any component exceeds the specified thermal specifications changes will be required:

- Maximum environmental temperature lowered.
- Maximum use cases reduced to lower device temperatures.
- Thermal solution required for the devices that exceed thermal specification.

WARNING: If devices other than the SoC contact the heat sink (through TIM material), they must still be instrumented to ensure the case temperature is not higher due to heat from the heat sink due to SoC heat being transferred to the other device.

The required system thermal performance can be determined based on the ambient temperature conditions and TMP level required by the customer. Consider the following example:

$$T.amb = 55°C$$

$T.cpu = 93°C$ (Targeting $4°C$ T.cpu headroom to account for sensor inaccuracy and possible T_j fluctuations resulting from workload variation)

$$P_{TMP} = 10W$$

The heat sink thermal performance requirement for the above conditions.

$$\rightarrow \theta_{ja} = \frac{93°C - 55°C}{10W} = \mathbf{3.8}\frac{°C}{W}$$

So, in this example, a 3.8 °C/W thermal solution is expected to be sufficient to maintain the Tegra X1 within the maximum temperature specification as detailed in Table 2-1. In addition to this, the customer is responsible to verify all other components of the module within their maximum temperature specifications as detailed in Table 3-1.

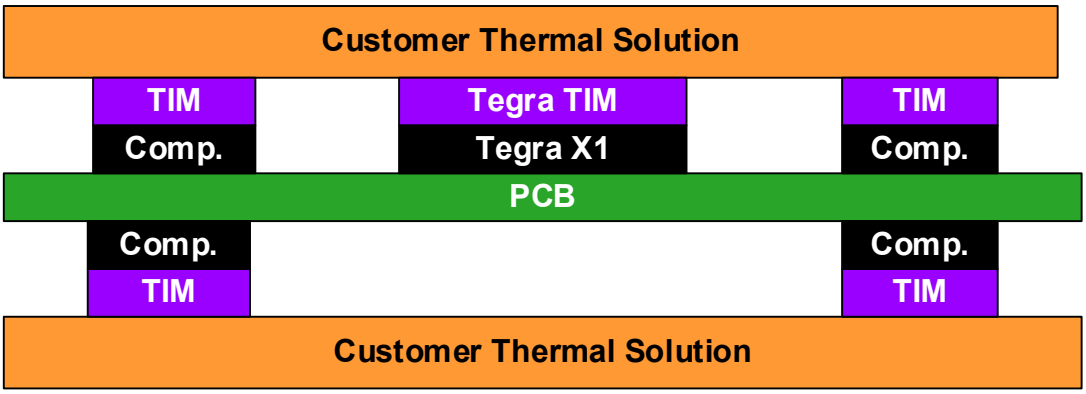
3.1.2 Jetson Nano Thermal Design Details

The customer is responsible for the following items:

- Thermal Solution – A system thermal solution capable of cooling the appropriate amount of TMP for the target workload.
- HS_TIM – The customer is responsible for providing the thermal interface material between the Jetson Nano module and customer's system level thermal solution. For best thermal performance, the TIM should provide low thermal impedance within the mechanical, reliability, and cost constraints of the customer's product.
- Maximum Temperature - To ensure that the maximum Tegra X1 operating temperature is less than the value specified in Table 2-1, and the maximum component temperatures on the PCB must not exceed the value specified in Table 3-1.

Example thermal stack up is shown in Figure 3-3.

Figure 3-3. Thermal Stack-Up Schematic



3.1.3 Customer Thermal Solution

The customer's thermal solution is the mechanical element that interfaces to the Jetson Nano module and provides cooling. A variety of thermal solution configurations are possible depending on the customer's chassis design. In all cases, however, the following recommendations are applicable:

- Good contact of the thermal solution to the Tegra X1 is critical for maximizing the thermal performance of the Jetson Nano. The Tegra X1 consumes the majority of the TMP.
- Customer must determine if system thermal solution needs to contact all / select components on the PCB to make sure that they are maintained within the maximum temperature specifications listed in Table 2-1 and Table 3-1.

3.1.4 Temperature Cycling

Long-term reliability of all solder interconnects is negatively impacted by temperature cycling. It is the customer's responsibility to minimize the component's exposure to temperature cycling and to not exceed that which the component is qualified. NVIDIA's graphics and core logic components are qualified to JEDEC standard JESD47.

Note: NVIDIA recommends that customers refer to JESD94.01 (*Application Specific Qualification Using Knowledge Based Test Methodology*) for more information.

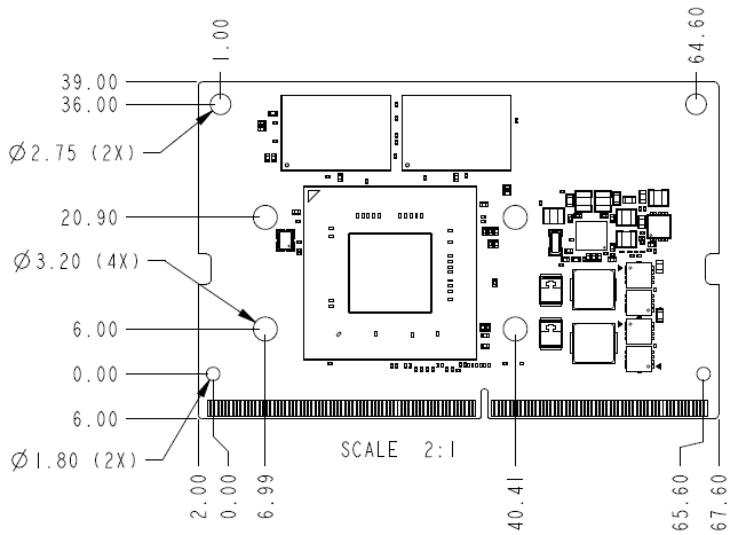
3.2 Mechanical Information

Refer to the Jetson Nano module Mechanical drawing for the exact module dimensions to determine how to interface the module board with the system thermal solution and ensure mechanical compatibility.

3.2.1 Heat Sink Mounting Guidelines

As noted in the thermal section, the mechanical design of the system must ensure good contact between the thermal solution, Tegra X1 and the module board. The module board is provided with mounting holes to accommodate mounting options for a suitable heat sink.

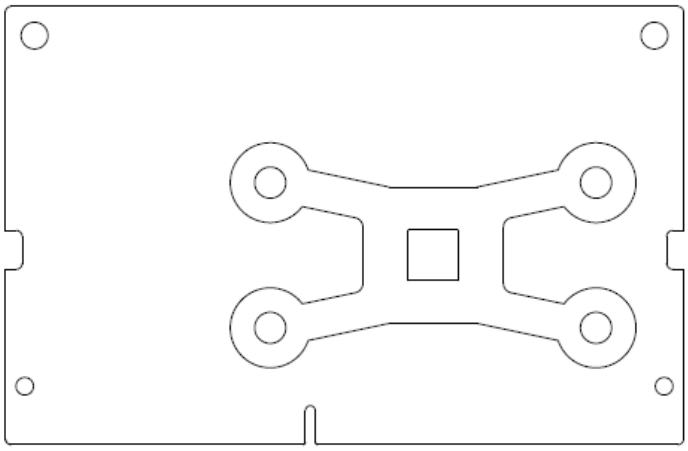
Figure 3-4. Module Board with Mounting Features



The following guidelines should be followed to ensure good mechanical and thermal contact between the chassis thermal solution and the Module board.

- Four holes (Ø 3.2mm) are provided near the Tegra X1 and two holes (Ø 2.75mm) on the edge opposite to edge connector.
- All holes are NPTH with annular ground pads. These holes can be used for system mount as well as Heatsink mount based on individual customer design intents.
- Shoulder screws can be used for all mounting hole locations to prevent thread damaging the board.
- Maximum Pressure on Tegra X1 should not exceed 60 psi
- Module board should not bow or bend to cause more than 500 micro-strain within 5mm of the Tegra X1.
- There is a keep-out area behind the module board to allow for back plate to support the board while heatsink is mounted from top side.
- Figure 3-5 illustrates where module provides room for backplate should the design require a backplate to assist in stiffening the board and for mounting/locking features. The outline shows the keep-out area for the back plate on backside of the module.

Figure 3-5. Module Board PCB Back Support Keepout Area



3.2.2 Assembly Guidelines

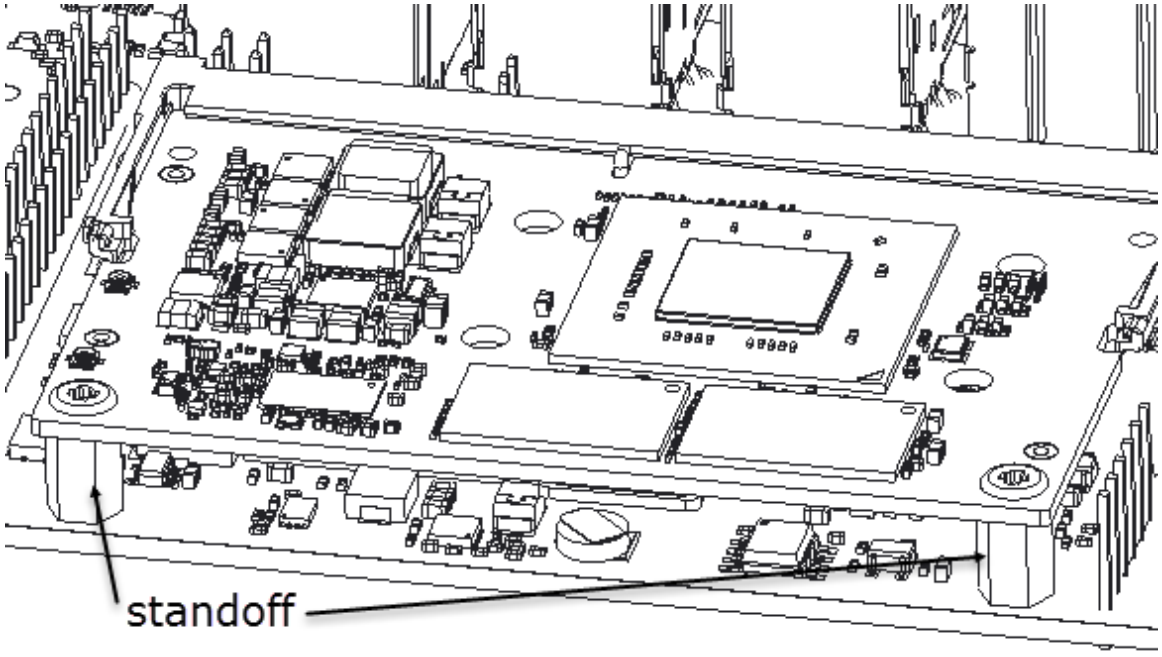
The Jetson Nano comes with JEDEC standard 260 DDR4 SODIMM 0.5MM pitch edge connector and are provided to interface with 260 PIN DDR SODIMM SOCKET WITH 0.5MM PICTH, based on SO-018.

Orientation of the unit is to be aligned with the connector and secured to the baseboard as shown in Figure 3-6. Suggested hardware for mounting the module to the baseboard is use of standoff between the two board, anchored with screw on each board.

Here are some suggested assembly guidelines.

1. Assemble the heat sink and fan if needed on the module board.
2. Install the Jetson Nano module
   a). Baseboard with suitable standoff for as per SoDIMM connector height defined
   b). Insert module at an angle of 25-35 degree into the SODIMM connector.
   c). Arc down the module board until it latches to the SODMM connector
   d). Secure the Jetson Nano module to the baseboard with screws onto the standoff/spacer. Figure 3-6 shows use of two standoff and screws to secure the module to the system/base- board.

Figure 3-6. Jetson Nano System Assembly Example on System Board



Chapter 4. Thermal Design Guidelines

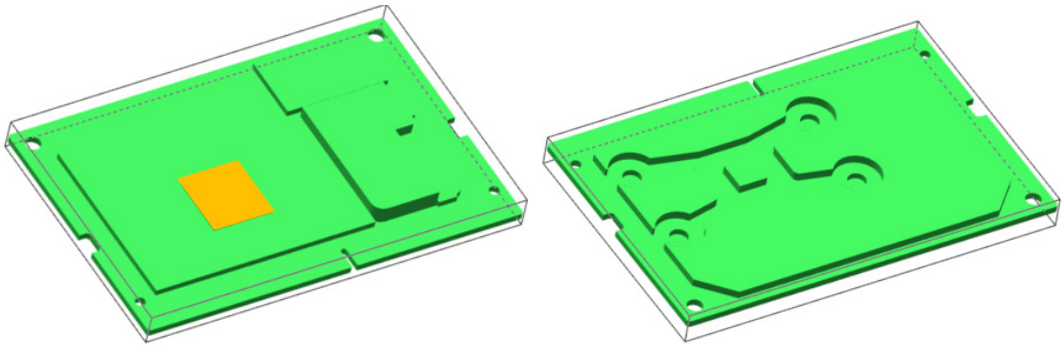
4.1 3D Component Envelope

NVIDIA provides a 3D CAD file (STP format) of the Jetson Nano module on the downloads section of the "NVIDIA Developers Website."

> **Jetson Nano 3D CAD STEP Model (P3448)**	B01	2020/03/05

It provides a 3D CAD model that shows an envelope that the board components will not exceed. Any heat sink should be designed to not intrude into the envelope. The heat sink should be referenced to the SoC DIE area (highlighted).

Figure 4-1. Jetson Nano System 3D CAD Envelope View



4.2 Heat Sink Design

There are typically 2 types of heat sink attachments:

- DIE referenced
- PCB referenced.

The following sections show the differences between the 2 types. Jetson Nano should use a DIE referenced design. The SoC is the main component that should be contacted and provided with a thermal solution. Other components should not require any thermal solution but can be provided if necessary.

For components other than SoC, customers should make sure that they do not exceed the maximum temperature limit specification provided in Table 3-1.

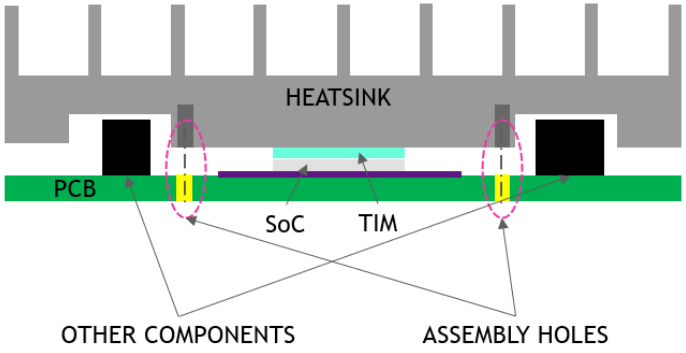
WARNING: Adding thermal material to components other than the SoC may increase their case temperature due to heat transfer from the SoC and they may exceed their maximum limits.

4.2.1 DIE Referenced

The DIE referenced heat sink attachment is the preferred design for Jetson Nano.

- Heat sink contact is referenced to TOP of SoC DIE.
- Use nearby mounting holes to minimize board flex.
- Springs (if used - not shown) may be located either above the heat sink or below the PCB.
- Bondline typically controlled by achievable pressure, TIM compressibility and/or TIM filler particle size.
- Better control of pressure applied at the DIE.

Figure 4-2. Preferred DIE Referenced Heat Sink Example

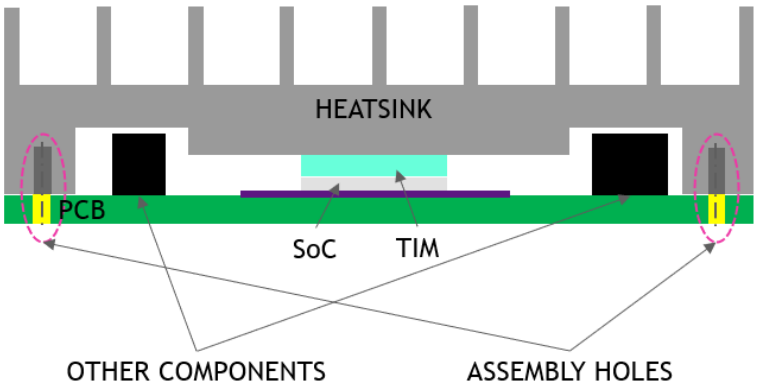


4.2.2 PCB Referenced

The PCB referenced heat sink attachment is not the preferred design for Jetson Nano.

- Tolerance loop includes (at least) the package height and heat sink base height.
- TIM thickness determined by tolerance stack up.
- Optionally uses corner mounting holes in PCB.
- Up to 10x the TIM bond line thickness of a DIE-refenced design.
- May cause PCB warpage due to tolerance deltas.

Figure 4-3. Not Preferred PCB Referenced Heat Sink Example



4.3 Heat Sink Assembly Guidelines

This section discusses the heat sink assembly guidelines for Jetson Nano.

4.3.1 DIE Pressure

For all types of heat sinks the amount of pressure applied to the SoC DIE is critical. If too much pressure is applied the DIE may crack. The pressure must be applied evenly across the DIE.

> **!** CAUTION: During assembly to maintain a constant pressure – do not completely tighten the heat sink mounting screws on one corner at a time, but instead do small adjustments on each screw in a round robin manner.

For Jetson Nano, the maximum pressure that can be applied to the Tegra X1 SoC DIE is 60 PSI.

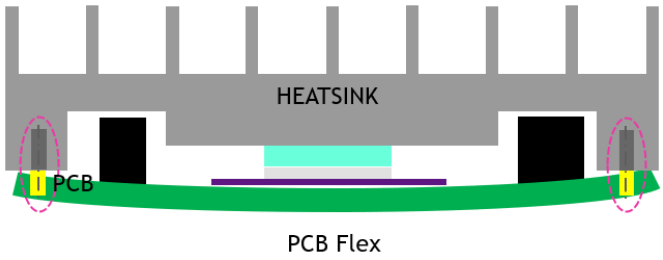
4.3.2 PCB Flex

The amount of DIE pressure combined with the heat sink attachment may cause the PCB to flex in some circumstances. If the board flexes too much this may cause a variety of issues.

- PCB failure
- Component ball and pin cracks

For Jetson Nano, the amount of flex (bow or bend) of the PCB board should cause more than 500 micro-strain within 5 mm of the Tegra X1 SoC.

Figure 4-4. PCB Flex



4.4 Thermal Material

For best thermal transfer, a thin bondline TIM material should be used between the SoC DIE and the thermal solution.

- Uniform thickness of this TIM material is required to provide consistent thermal results.
- DIE referenced design will help enable a thin bondline between SoC and heat sink.
- Jetson Nano Developers Kit uses a 50 um thick layer of thermal grease.

For other components (if needed), a compressible TIM material (GAP pads) can be used between the thermal solution and other components. Customers should request Force vs Deflection curves from gap filler vendors of their choice based on their design requirements and use adequate compression force.

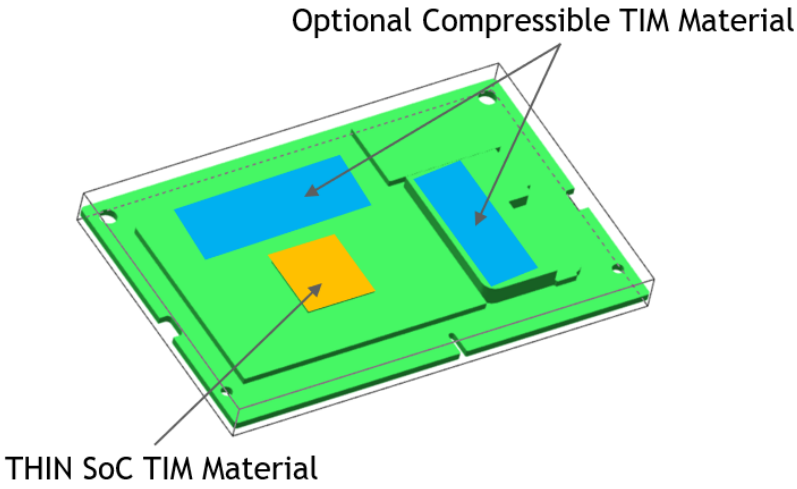
If used, ensure compression force does not create pressure greater than recommended on the SoC DIE or cause PCB warpage beyond the allowable limit.

4.5 Recommended Solution

Design a DIE referenced thermal solution based on the 3D CAD model provided. Jetson Nano Developers Kit uses a 50 um thick layer of thermal grease with thermal conductivity of 6.0 W/m °K.

Do not exceed the maximum supported pressure on the SoC DIE. If absolutely required use compressible TIM material (GAP fillers) for other component contact to fill the gap between the heat sink and the component, while ensuring other components do not exceed their rated specification.

Figure 4-5. Recommended TIM Placement



Chapter 5. Thermal Management

5.1 Temperature Monitoring

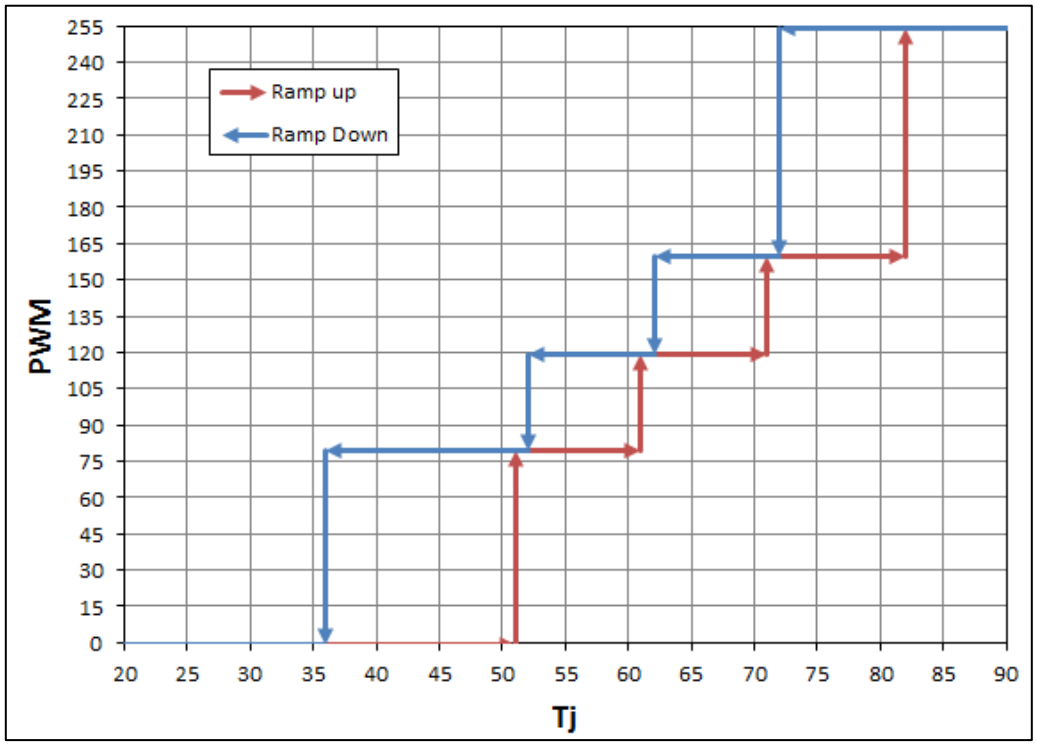
The Tegra junction temperature can be directly read from sysfs nodes, as shown in the following example. Note that the name of each temperature zone is noted in the type node and that the temperature values are reported in units of m °C.

```
cat /sys/devices/virtual/thermal/thermal_zone1/type
cpu-therm
# cat /sys/devices/virtual/thermal/thermal_zone1/temp
35000
```

5.2 Fan Control

The Jetson Nano can be configured to control a system fan. Pulse width modulation (PWM) output and tachometer input are supported. Jetson Nano has configurable fan control of step-based speed control with hysteresis, as shown in Figure 5-1.

Figure 5-1. Fan Control Algorithm



The default fan curve settings are listed in Table 5-1. Note that PWM is configured on a 2^8 scale, with 255 being equivalent to 100% duty cycle.

Table 5-1. Default Fan Control Parameters

CPU Temperature (°C)	PWM	Hysteresis[1] (°C)
51	80	15
61	120	9
71	160	9
82	255	10

Note:

[1]The hysteresis set for each trip point must be greater than the previous trip point. For example, 82 °C – 10 °C = 72 °C, which is greater than the 160 PWM trip point at 71 °C.

Custom fan settings can be implemented if needed. Refer to the *Platform Adaptation and Bring-up Guide* for details.

5.3 Tegra X1 SoC Maximum Operating Temperature

The recommended operating temperature limit is the threshold at which the module will operate without performance reduction. These temperatures are listed in Table 2-1 and cannot be adjusted. The customer's tolerance for performance reduction should determine the amount of T_j operating headroom in the thermal solution design to accommodate the temperature sensor accuracy of ± 3 °C.

Software thermal management operates as follows:

- When the measured temperature is at or below the operating temperature threshold, software T_j thermal management is not engaged and the system is free to vary the system frequencies and voltages.
- When the measured temperature reaches the thermal management threshold, the internal thermal sensors generate an interrupt to software. At this point the software thermal management algorithm engages and begins periodically performing the following operations:
  - Polling temperature.
  - Running a thermal management control algorithm to calculating the throttle degree, indicating the amount of throttling to apply during the next time period.
  - Throttling the system to the level of throttling indicated by the throttling control algorithm. Throttling is applied through limits on the clock frequency of high-power units such as the CPU and graphics processing unit (GPU). Higher throttling degree results in lower frequency limits. DVFS policies operate within these frequency limits.
- Software thermal management remains in operation until the Tegra X1 temperature has returned to a value below the throttling threshold and throttling degree has returned to zero.

Note: Power fluctuations that induce T_j fluctuations above the software thermal management thresholds will cause temporary clock reductions. Power fluctuations in the target workload should be evaluated for their potential to cause temperature to fluctuate above the software threshold.

5.4 Tegra X1 Hardware Thermal Throttling

In the event that software thermal management is not able to maintain the Tegra X1 temperature, then hardware thermal throttling will engage in an attempt to prevent thermal shutdown. To help avoid thermal shutdown conditions without being overly conservative, Tegra X1 has hardware-engaged clock throttling mechanisms that are used as a last resort to prevent shutdown conditions. This will lower the Tegra X1 temperature, but it will also significantly reduce the overall Tegra X1 performance. The Tegra X1 throttle settings cannot be altered. These settings are implemented by NVIDIA to meet safety and reliability standards.

5.5 Tegra X1 Shutdown Temperature

Tegra X1 is rated to operate at a junction temperature not-to-exceed 105 °C. Tegra X1 has hardware shutdown mechanisms that enforce this limit by automatically halting the system when this temperature is exceeded.

The shutdown temperature should not be reached at any time during normal operation, but it may occur if cooling system components are broken, jammed, or otherwise unable to cool the Tegra X1 under worst-case conditions. If a thermal shutdown event is triggered, then a major fault in the Jetson Nano or system cooling solution has occurred. Thermal shutdown can be initiated by any of the sensors listed in Table 2-1. Using multiple sensors enables operation closer to the temperature limit without compromising reliability by reducing the uncertainty associated with the hotspot location.

The following thermal shutdown mechanism has been implemented:

- Internal sensor-based shutdown. Failsafe thermal shutdown is guaranteed by using the SHUTDOWN signal directly from Tegra to the PMIC. After the failsafe shutdown the user will have to manually turn the system on by pressing the power button or equivalent input.

The Tegra X1 shutdown settings cannot be altered. These settings are implemented by NVIDIA to meet safety and reliability standards.

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