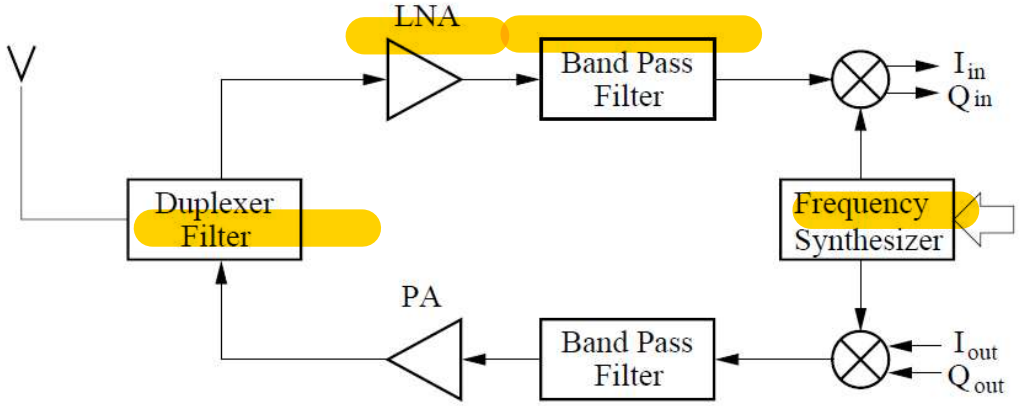
Frequency Synthesizers

Topics Relevant to Frequency Synthesizers

- Phase-locked loops (PLL)
- Synthesizer architecture (integer-N, fractional-N topologies)
- Direct synthesis
- Frequency division circuits

Performance parameters



· Accuracy, Frequency, Frequency Spacing : in AMPS the frequency spacing is 30 KHz. Typically 100 Hz accuracy is required.

· Side band spurs at: $\omega_S = \omega_{LO} \pm \omega_{Ref}$

– spurs can downconvert interferers: $\omega_{IF} = |\omega_{RF} - \omega_{LO}| = |\omega_{interf} - \omega_S|$

– spurs should be typically at 60 dBc.

· lock time:

– time required to establish new frequency.

– 10 ms to 10 μs (fast frequency hopping spread spectrum).

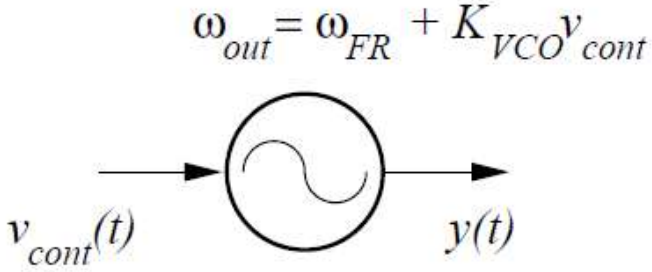
·Tracking – The max value of $\Delta\omega$ that the PLL can tolerate.

·Acquisition Time – Time taken for the loop to go from unlocked to locked state.

Phase Locked Loops

VCO dynamics:

$$\omega_{\text{out}} = \frac{d\varphi_{out}}{dt} = \omega_{RF} + K_{VCO} v_{cont}$$



The excess phase φ'_{out} is then :

$$\varphi'_{out}(t) = K_{VCO} \int_{-\infty}^{t} v_{cont}(t)\, dt$$

The oscillator output is then:

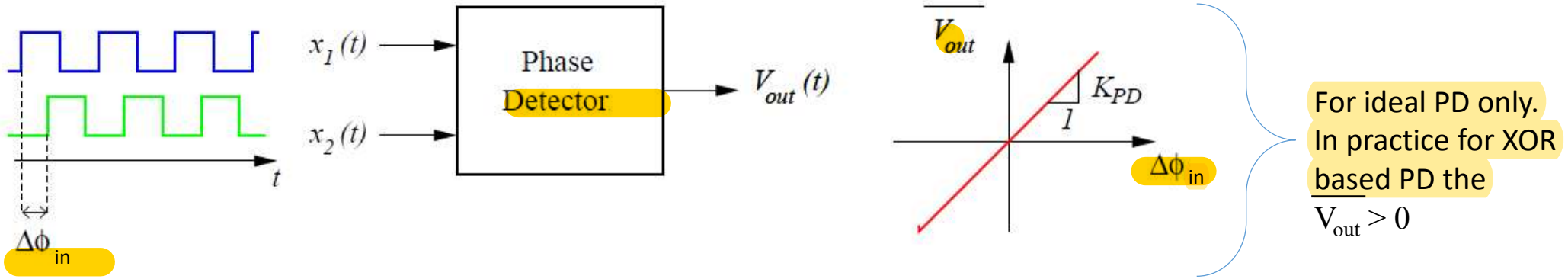
$$\text{y(t)} = \text{A}_\text{C} \cos\left[\omega_{RF} t + \varphi'_{\text{out}}\right] = \text{A}_\text{C} \cos\left[\omega_{RF} t + K_{VCO} \int_{-\infty}^{t} v_{cont}(t)\, dt\right]$$

The input-output transfer function of the VCO is then:

$$\frac{\varphi'_{out}(s)}{v_{cont}(s)} = \frac{K_{VCO}}{s}$$

- To change the output phase of the VCO we must first change the frequency.
- The output phase of the VCO depends on the history of v_{cont}.

Phase Detector (Ideal Charateristics)

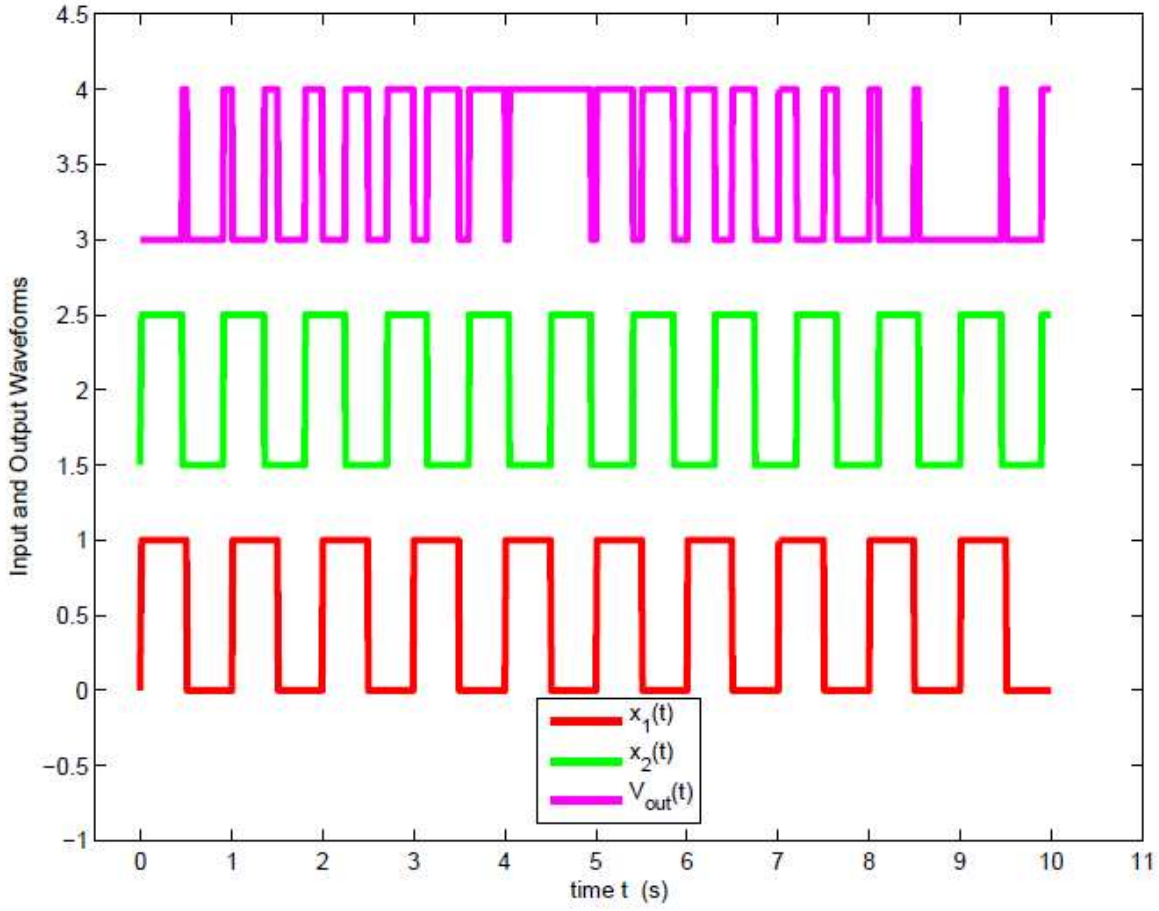


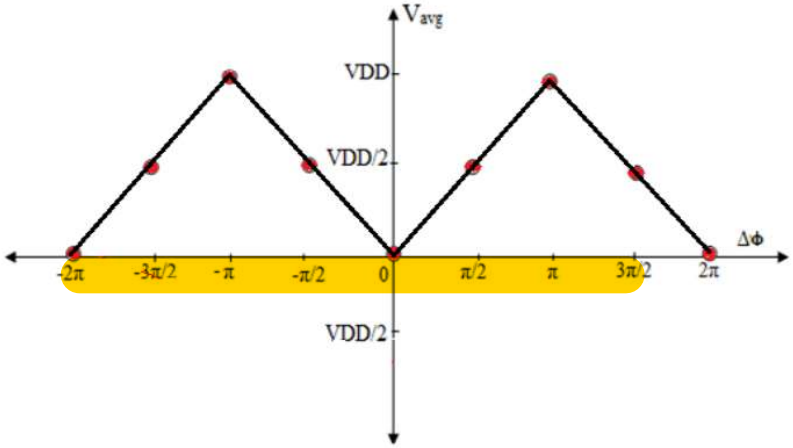
An ideal phase detector (PD) produces a DC output which is proportional to the phase difference between two periodic signals.

$$\overline{v_{out}} = K_{PD}\,\Delta\phi_{in}$$

In practice the characteristic is non linear for large $\Delta\phi$ and may depend on the amplitude or duty cycle

Digital Implementation of Phase Detector using XOR (see CMOS based XOR ckt in Razavi)

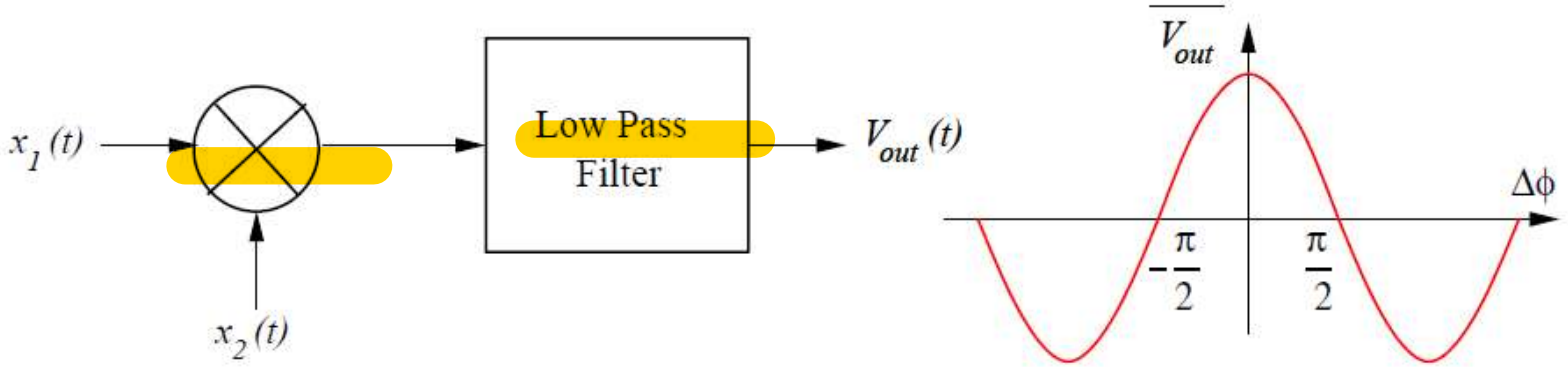




Actual Transfer Characteristics of XOR based PD

"DESIGN, IMPLEMENTATION AND CHARACTERIZATION OF XOR PHASE DETECTOR FOR DPLL IN 45 NM CMOS TECHNOLOGY", Delvadiya Harikrushna, Prof. Mukesh Tiwari, Prof. Jay Karan Singh, Dr. Anubhuti Khare,Advanced Computing: An International Journal (ACIJ), Vol.2, No.6, November 2011

Analog Phase Detector



A multiplier (mixer) can be used to implement an analog phase detector:

$$y(t) = \alpha\ A_1 \cos\left(\omega_1 t\right) \times A_1 \cos\left(\omega_2 t + \Delta\varphi\right)$$

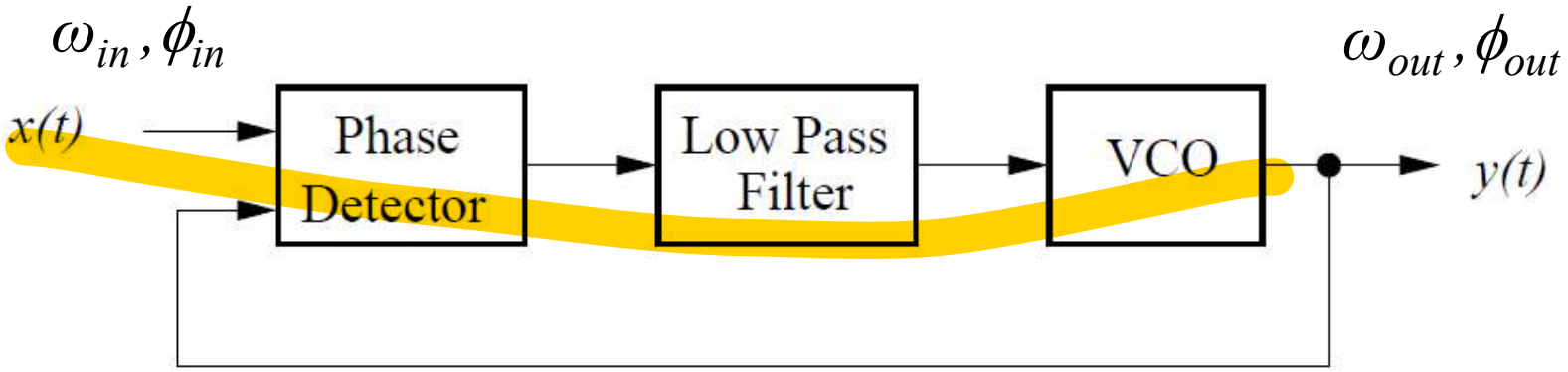
$$= \underbrace{\alpha \frac{A_1 A_2}{2} \cos\left[\left(\omega_1 + \omega_2\right)\ t + \Delta\varphi\right]}_{\text{Filtered out}} + \alpha \frac{A_1 A_2}{2} \cos\left[\left(\omega_1 - \omega_2\right)\ t - \Delta\varphi\right]$$

For $\omega_1 = \omega_2$ the phase/voltage characteristic is:

$$\overline{y(t)} = \alpha \frac{A_1 A_2}{2} \cos\Delta\varphi \approx \alpha \frac{A_1 A_2}{2}\left[\frac{\pi}{2} - \Delta\varphi\right] \quad \text{in the vicinity of } \pi/2.$$

For $\Delta\varphi$ departing strongly from $\pi/2$ the phase detector is non-linear.

Basic Phase Locked Loop (Type I)

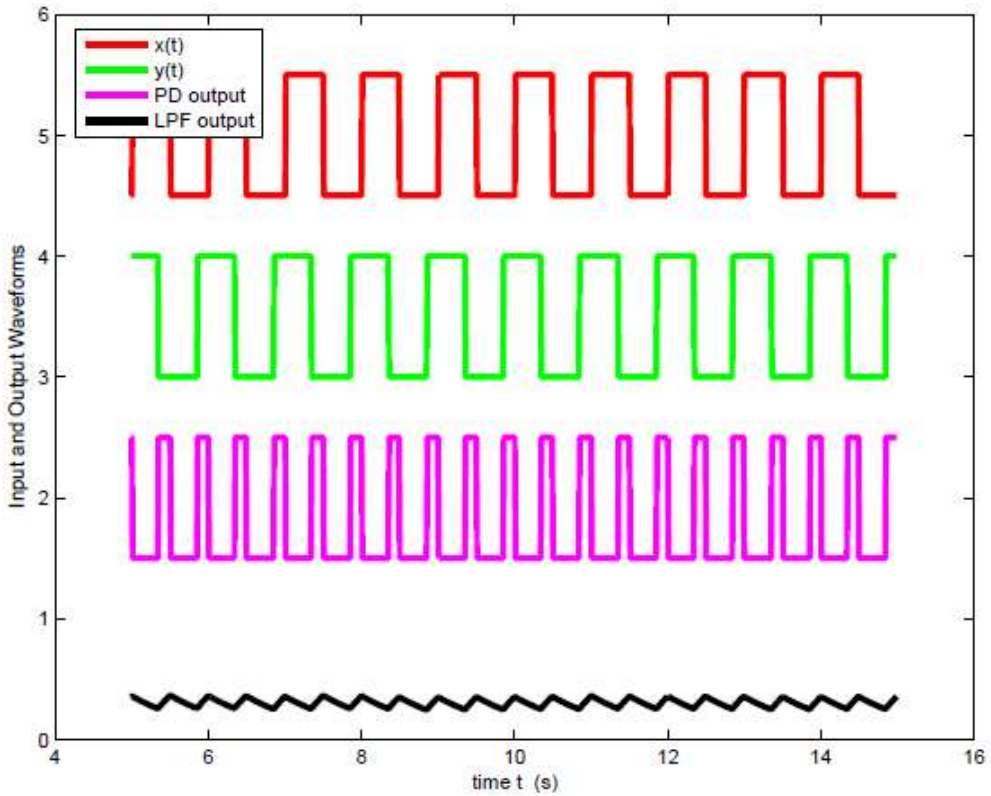


The phase detector provides the error signal which is minimized by feedback loop

The signal is locked when we have both :

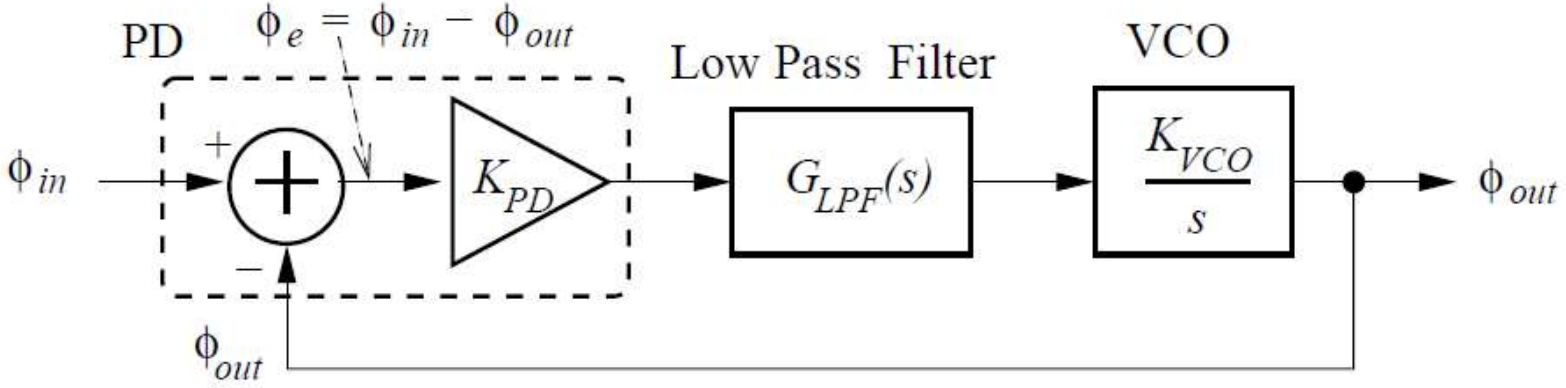
- $\omega_{in} = \omega_{out}$ (frequency acquisition)
- $\phi_{out} - \phi_{in} = \Delta\phi$ (phase acquisition)

Locked (Steady State) Condition



- The phase detector produces an output whose DC value is proportional to $\Delta\phi$.
- The low pass filter extracts the DC component.
- The VCO oscillates at the same frequency but with a phase difference $\Delta\phi$.

Linearized PLL



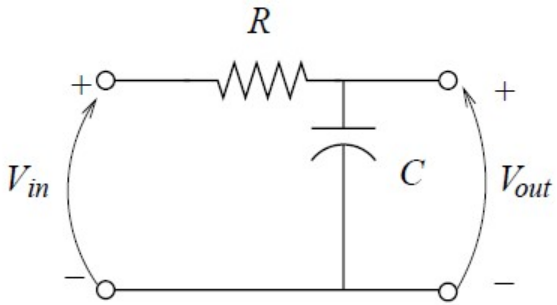
The open loop transfer function is:

$$H_0(s) = \frac{\Delta\phi_{out}}{\Delta\phi_{in}} = K_{PD}\ G_{LPF}(s)\frac{K_{VCO}}{s}$$

The closed loop transfer function is:

$$H(s) = \frac{\Delta\phi_{out}}{\Delta\phi_{in}} = \frac{K_{PD}\ G_{LPF}(s)\ K_{VCO}}{s + K_{PD}\ G_{LPF}(s)\ K_{VCO}}$$

1st Order Low Pass Filter (2nd Order PLL)



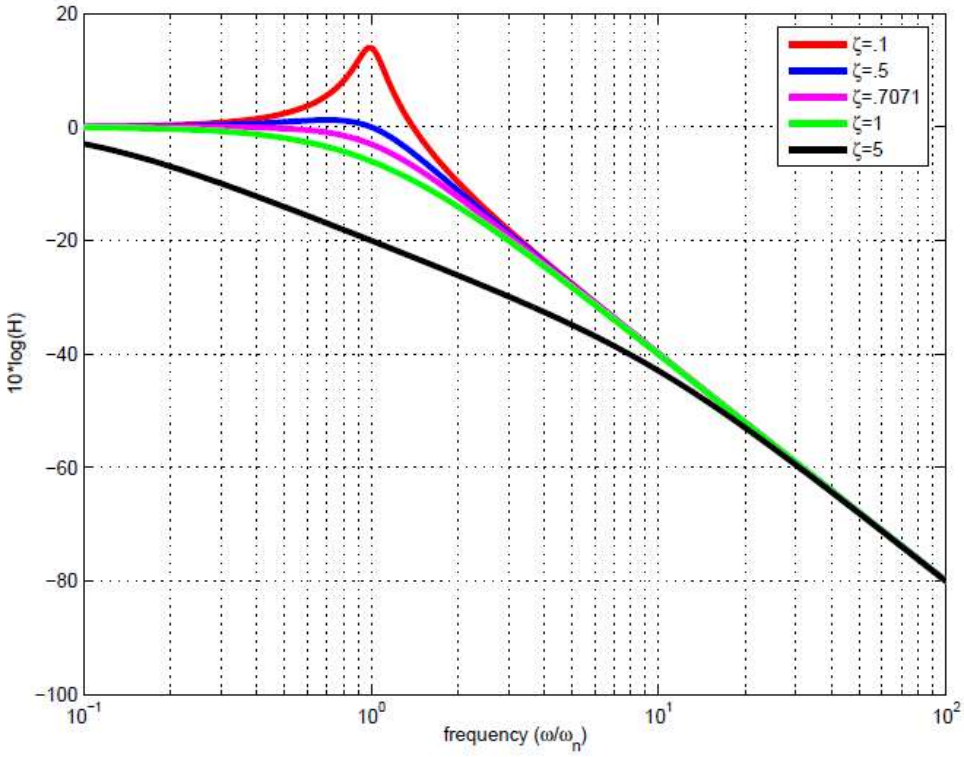
$$G_{LPF} = \frac{V_{out}}{V_{in}} = \underbrace{\frac{1}{1+\frac{s}{\omega_{LPF}}}}_{\text{first order}} \quad \text{with} \quad \omega_{LPF} = \frac{1}{RC}$$

The closed loop transfer function is then :

$$H(s) = \frac{\Delta\phi_{out}(s)}{\Delta\phi_{in}(s)} = \frac{K_{PD}G_{LPF}(s)K_{VCO}}{s + K_{PD}G_{LPF}(s)K_{VCO}} = \underbrace{\frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}}_{\text{second order}}$$

$$= \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{with} \quad \omega_n = \sqrt{\omega_{LPF}K} \quad \text{and} \quad \zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}}$$

where we introduce $K = K_{PD}K_{VCO}$ the loop gain.

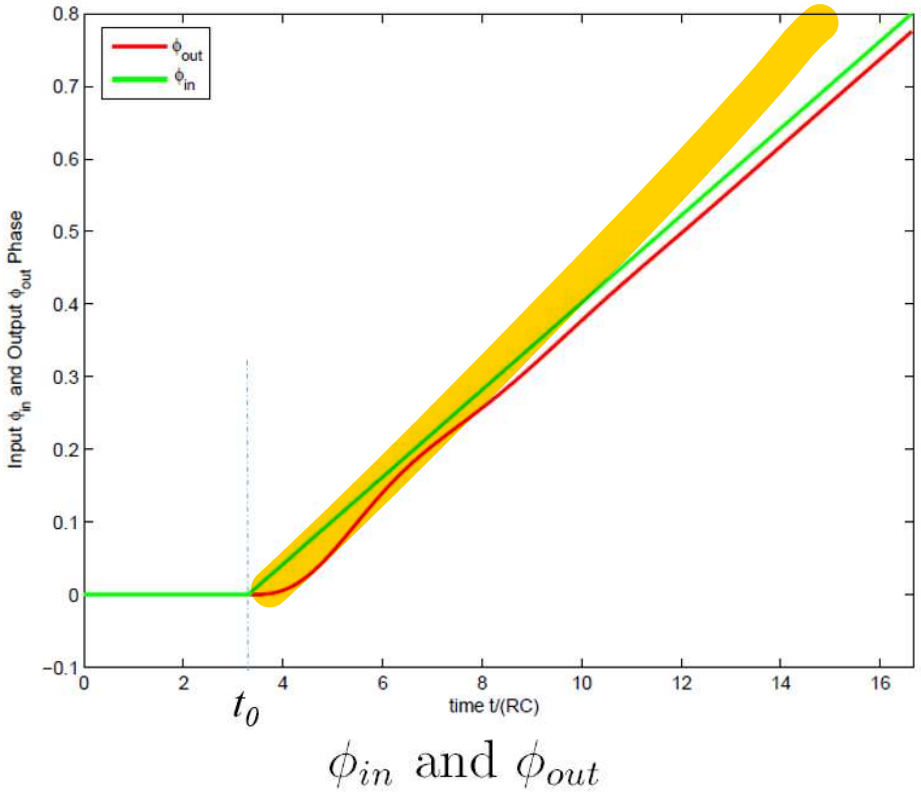


An optimum flat frequency response is obtained for

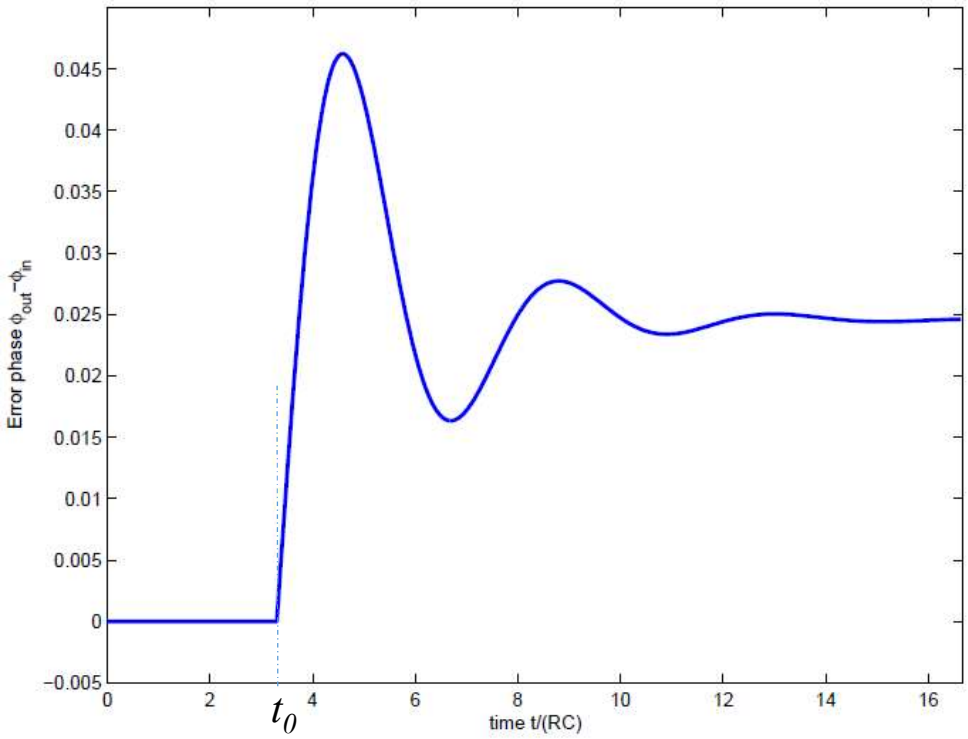
$\zeta \approx 1/\sqrt{2}$ (slightly underdamped)

$\Rightarrow K \approx \omega_{LPF}/2$

Response to a Frequency Shift $\Delta\omega$



ϕ_{in} and ϕ_{out}



Frequency jump at t_0: $\Delta\phi_{in} = \Delta\omega\,(t - t_0)\;u\;(t - t_0)$

Convergence of $\Delta\phi_{out}$ toward $\Delta\phi_e$

Evaluation of the Error Phase

To a frequency jump $\Delta\omega$ corresponds a phase ramp (assuming $t_0 = 0$) :

$$\Delta\phi_{in}(t) = \Delta\omega\ t\ u(t) \Rightarrow \Delta\phi_{in}(s) = \frac{\Delta\omega}{s^2}$$

The phase error transfer function is

$$H_e = \frac{\phi_e}{\Delta\phi_{in}} = \frac{\Delta\phi_{in} - \Delta\phi_{out}}{\Delta\phi_{in}} = 1 - H(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

The phase error for the phase ramp is then :

$$\phi_e(s) = H_e\ \Delta\phi_{in}(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \times \frac{\Delta\omega}{s^2}$$

The final steady state value is then :

$$\Delta\phi_e = \phi_e(t \to \infty) = \lim_{s\to 0}\ s\phi_e(s) = \frac{2\zeta\ \Delta\omega}{\omega_n} = \frac{\Delta\omega}{K} \rightarrow$$ direct relation between phase error and VCO frequency shift.

This is to be expected since for the VCO frequency to change by $\Delta\omega$ the phase error at PD must be $\Delta\omega/K$ with K the loop gain.

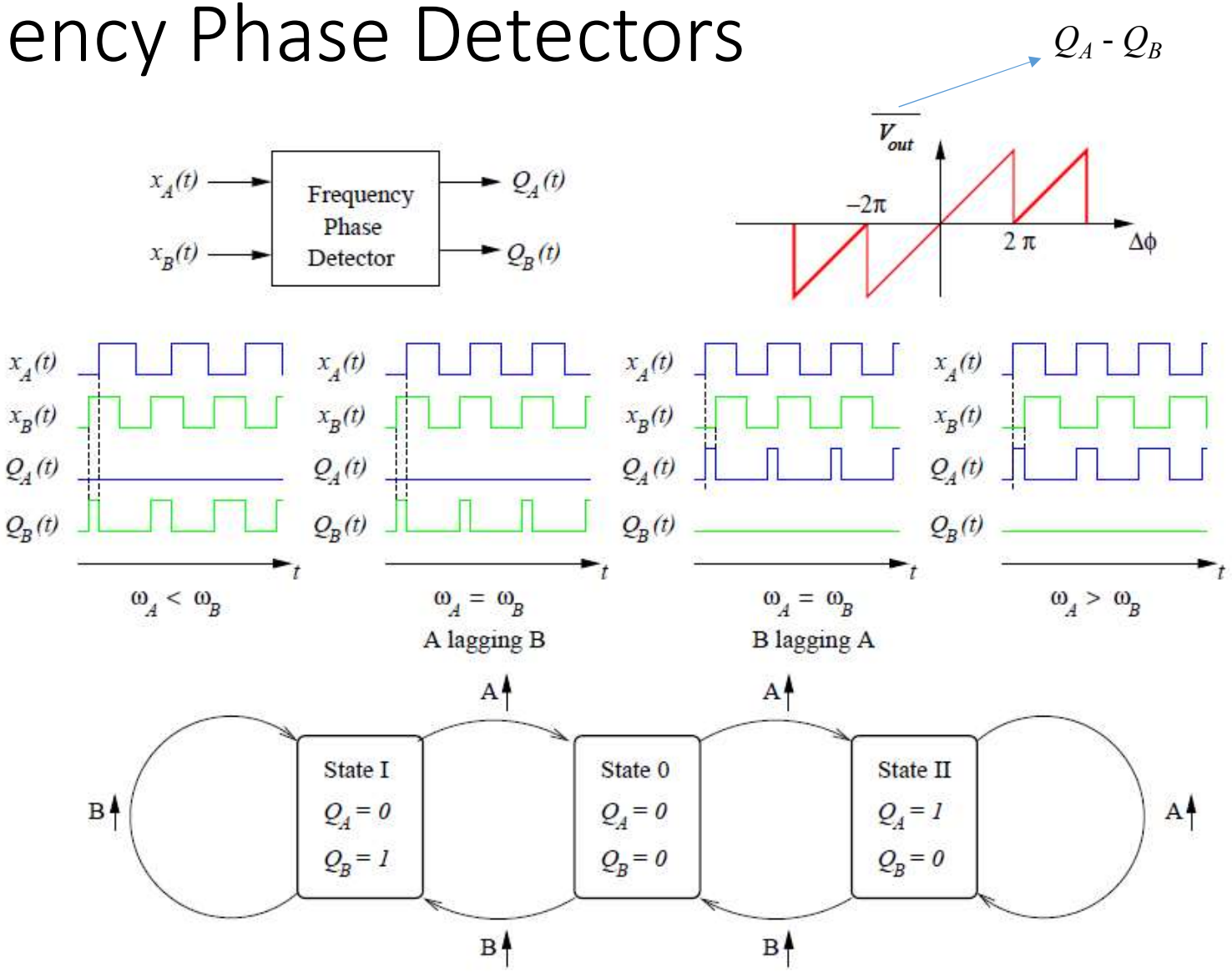
Issues with type I PLL

- Conflict between gain and BW - To reduce the phase error $\Delta\phi_e = \Delta\omega / K$, we must increase K the loop gain.
- But increasing the loop gain K increases the loop bandwidth since we have $K = \omega_{LPF} / 2 \ (\text{for } \zeta = 1/\sqrt{2})$.
- Conflict between stability and BW - If more stability is required then ζ must be high, but high ζ also means high ω_{LPF} (keeping K constant). High ω_{LPF} causes higher frequencies to be present in v_{cont} which in turn introduces spurious changes in o/p frequency.
- The acquisition time is on the order of $4\Delta f^2 / \omega_{LPF}^3$. For narrow loop bandwidth B the acquisition time is too long (hours). A frequency detector is required to assist the frequency acquisition before the phase acquisition can take over.
- Finite static phase error also can be undesirable for some applications.

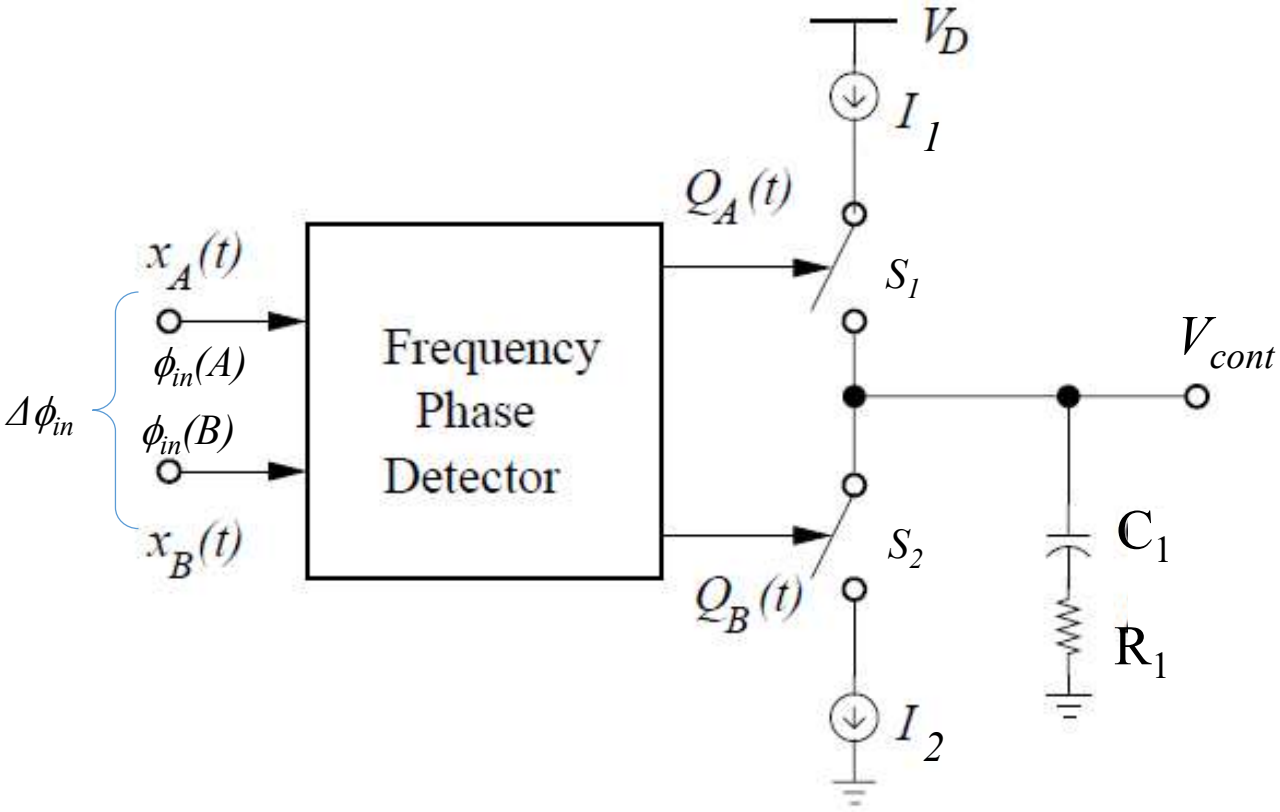
Type- II PLL

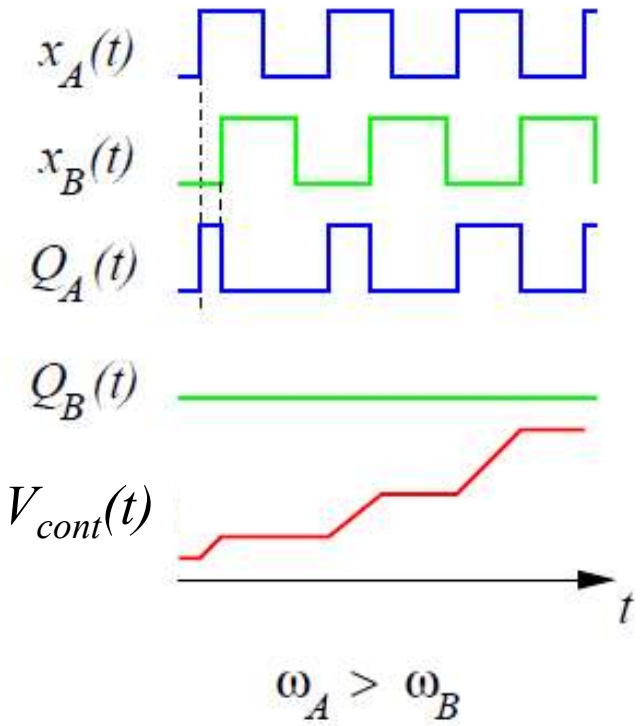
We can set the bandwidth and gain separately This will be achieved by having an infinite gain at DC using an integrator.

Frequency Phase Detectors



Phase Frequency Detector with Charge Pump





$Gain = V_{cont}/\Delta\phi_{in} \rightarrow$ can be infinite

$I_p = I_1 = I_2$

Charge Pump PLL (Type 2 PLL)

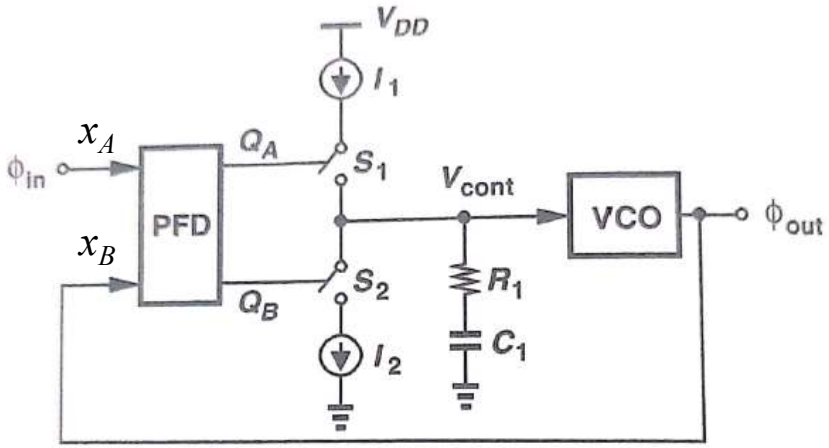


Figure 9.30 *Charge-pump PLL.*

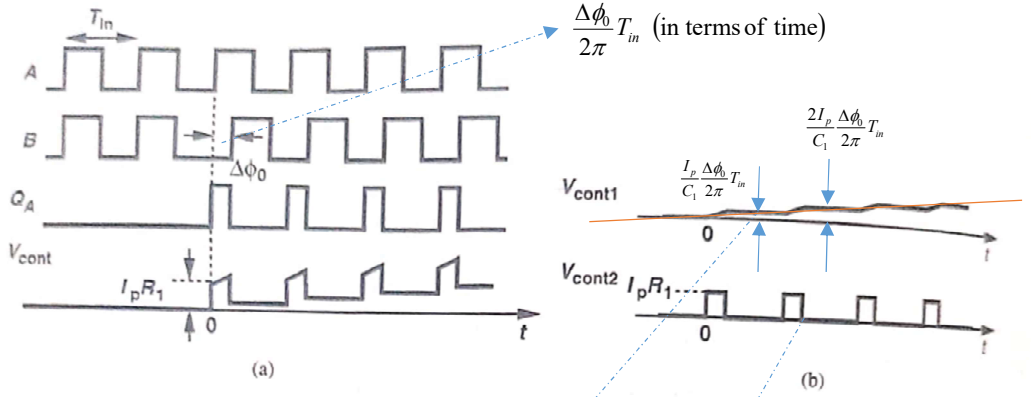


Figure 9.31 *(a) Phase step response of PFD/CP/LPF, (b) decomposition of output waveform into two.*

$$\frac{\Delta\phi_{out}(s)}{V_{cont}(s)} = \frac{K_{VCO}}{s}$$

$$\frac{V_{cont}(s)}{\Delta\phi_{in}(s)} = \frac{I_p}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right) \left[\because \Delta\phi_{in} = \Delta\phi_0\ \right]$$

Open loop H(s),

$$\frac{\Delta\phi_{out}}{\Delta\phi_{in}} = \frac{K_{VCO} I_p}{2\pi s}\left(R_1 + \frac{1}{C_1 s}\right)$$

Linearized *Average value*

$$V_{cont}(t) = \underbrace{\frac{\Delta\phi_0}{2\pi}\frac{I_p}{C_1} t\ u(t)}_{V_{cont1}} + \underbrace{\frac{\Delta\phi_0}{2\pi} I_p R_1 u(t)}_{V_{cont2}}$$

$$\Rightarrow \frac{V_{cont}(t)}{\Delta\phi_0(t)} = \frac{I_p}{2\pi C_1} t\ u(t) + \frac{I_p R_1 u(t)}{2\pi}$$

$$\Rightarrow \frac{V_{cont}(s)}{\Delta\phi_0(s)} = \frac{I_p}{2\pi C_1 s^2} + \frac{I_p R_1}{2\pi s} = \frac{I_p}{2\pi s}\left(R_1 + \frac{1}{C_1 s}\right)$$

Charge Pump PLL(Type 2 PLL)

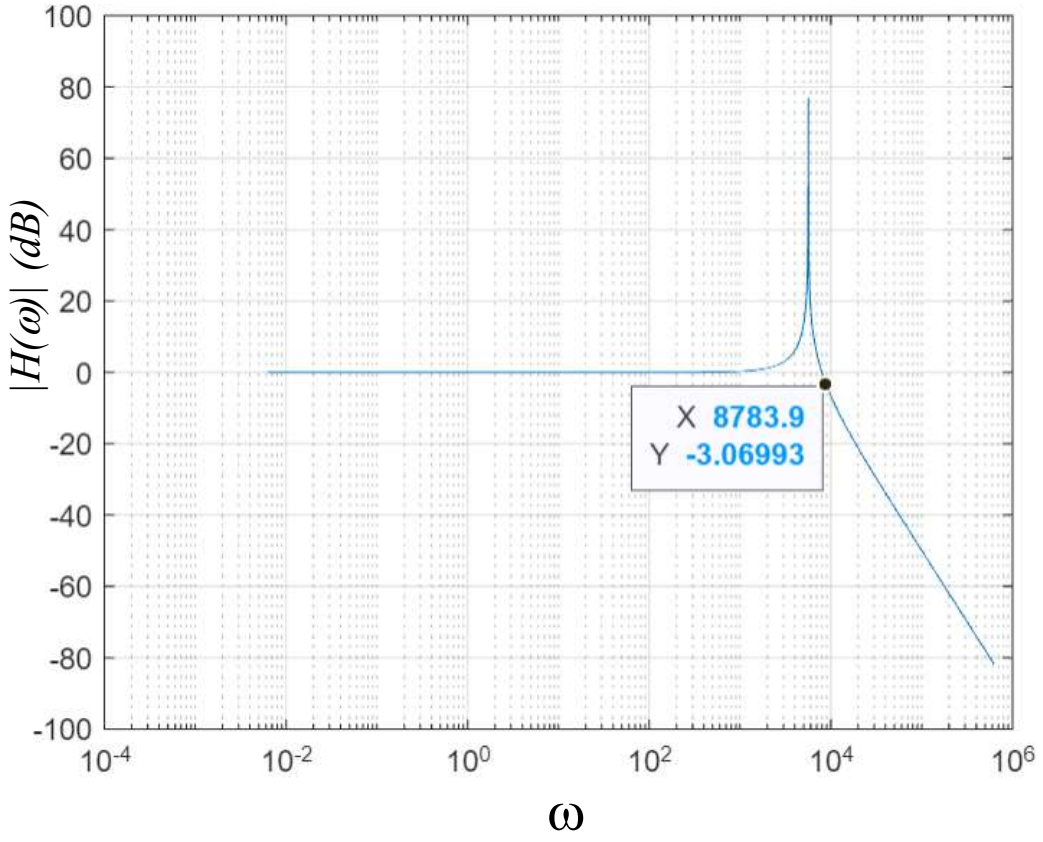
$$\text{Closed Loop, } H(s) = \frac{\Delta\phi_{out}}{\Delta\phi_{in}} = \frac{\frac{I_p K_{VCO}}{2\pi\ C_1}\left(R_1 C_1 s + 1\right)}{s^2 + \frac{I_p}{2\pi} K_{VCO} R_1 s + \frac{I_p}{2\pi\ C_1} K_{VCO}} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}},\quad \omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi\ C_1}},\ \text{3 dB frequency } \omega_{\text{LPF}} = \omega_n\sqrt{1 - 2\zeta^2 + \sqrt{1 + \left(1 - 2\zeta^2\right)^2}}$$

If $R_1 = 0$ then $\zeta = 0 \Rightarrow$ instability. Thus R_1 is necessary for stability

Increase in C_1 decreases ω_{LPF} but that also increases ζ(stability).

Hence the problem of stability conflicting low ω_{LPF} has been solved.



Closed Loop, $H(s) = \dfrac{\Delta\phi_{out}}{\Delta\phi_{in}}$

$$= \frac{\frac{I_p K_{VCO}}{2\pi\ C_1}\left(R_1 C_1 s + 1\right)}{s^2 + \frac{I_p}{2\pi} K_{VCO} R_1 s + \frac{I_p}{2\pi\ C_1} K_{VCO}}$$

$$= \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Taking, $C_1 = 1$ pF, $R_1 = 1$ Kohms , $I_p = 1$mA,

$K_{VCO} = 0.2$ GHz/V

$\zeta = 2.8209 \times 10^{-6}$, $\omega_n = 5.6419 \times 10^3$,

3 dB frequency $\omega_{LPF} = 8.7662 \times 10^3$

$$H_e = \frac{\phi_e}{\Delta\phi_{in}} = \frac{\Delta\phi_{in} - \Delta\phi_{out}}{\Delta\phi_{in}} = 1 - H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

The phase error for the phase ramp is then:

$$\phi_e(s) = H_e\ \Delta\phi_{in}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \times \frac{\Delta\omega}{s^2}$$

The final steady state value is then:

$$\Delta\phi_e = \phi_e\left(t \to \infty\right) = \lim_{s \to 0}\ s\phi_e(s) = 0$$

·Hence it is possible to obtain zero phase error. Loop bandwidth can be adjusted independent of steady state phase error.

·VCO frequency range has no relation to error phase. Hence it is only limited by VCO circuit.

Phase Noise(Effect of VCO Phase Noise)

Open loop, $\dfrac{\Delta\phi_{out}}{\Delta\phi_{in}} = \dfrac{I_p}{2\pi}\left(R_1 + \dfrac{1}{C_1 s}\right)\dfrac{K_{VCO}}{s}$

$$\Rightarrow \Delta\phi_{out} = \frac{I_p}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}\Delta\phi_{in}$$

With VCO phase variation added.

$$\Delta\phi_{out} = \frac{I_p}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}\Delta\phi_{in} + \Delta\phi_{VCO}$$

Let $\phi_{\text{out}}(\text{initial}) = \phi_{in}(\text{A}) = 0$

Hence,

$$\phi_{\text{out}}(\text{final}) - \phi_{\text{out}}(\text{initial}) = \frac{I_p}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}\left(\phi_{\text{in}}(\text{A}) - \phi_{\text{in}}(\text{B})\right) + \Delta\phi_{VCO}$$

Given, $\phi_{\text{out}}(\text{final}) = \phi_{\text{in}}(\text{B}) = \Delta\phi_{\text{out}}$

$$\Rightarrow \Delta\phi_{\text{out}} = -\left(\frac{I_p}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}\right)\Delta\phi_{\text{out}} + \Delta\phi_{VCO}$$

$$\Rightarrow \frac{\Delta\phi_{\text{out}}}{\Delta\phi_{VCO}} = \frac{1}{1 + \dfrac{I_p}{2\pi}\left(R_1 + \dfrac{1}{C_1 s}\right)\dfrac{K_{VCO}}{s}} = \underbrace{\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}}_{\text{HP Filtering}}, \ \zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}}, \ \omega_{\text{n}} = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}}$$

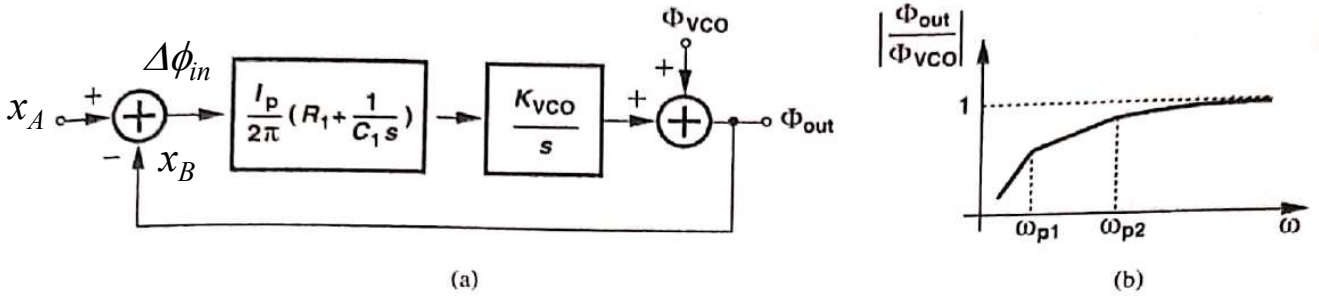


Figure 9.55 *(a) Phase-domain model for studying the effect of VCO phase noise, (b) resulting high-pass response.*

Phase Noise(Effect of VCO Phase Noise)

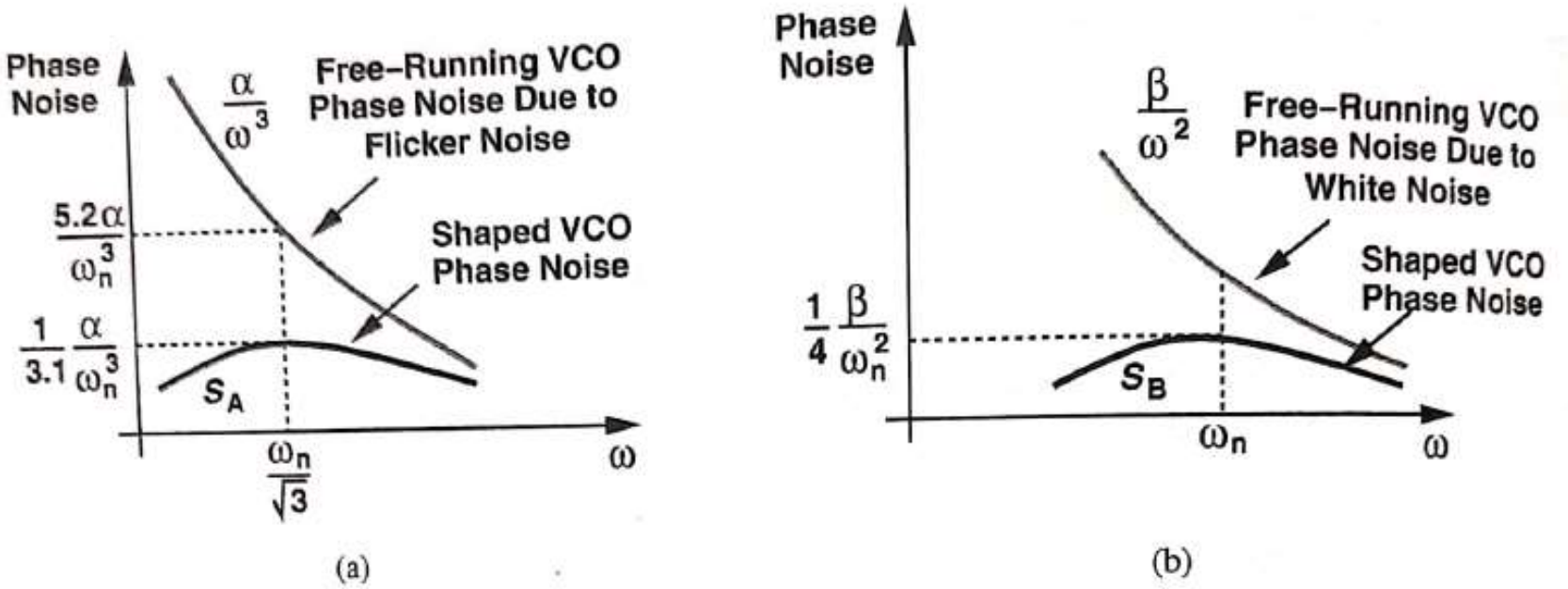


Figure 9.60 *Effect of PLL on VCO phase noise due to (a) flicker noise, (b) white noise.*

Phase Noise(Effect of Reference Phase Noise)

Follows directly from closed loop Transfer Function,

$$\text{Closed Loop, } H(s) = \frac{\Delta\phi_{out}}{\Delta\phi_{in}} == \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}},\ \omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}}$$

$$S_{out} = \frac{4\zeta^2\omega_n^2\omega^2 + \omega_n^4}{\left(\omega^2 - \omega_n^2\right)^2 + 4\zeta^2\omega_n^2\omega^2} S_{REF}$$

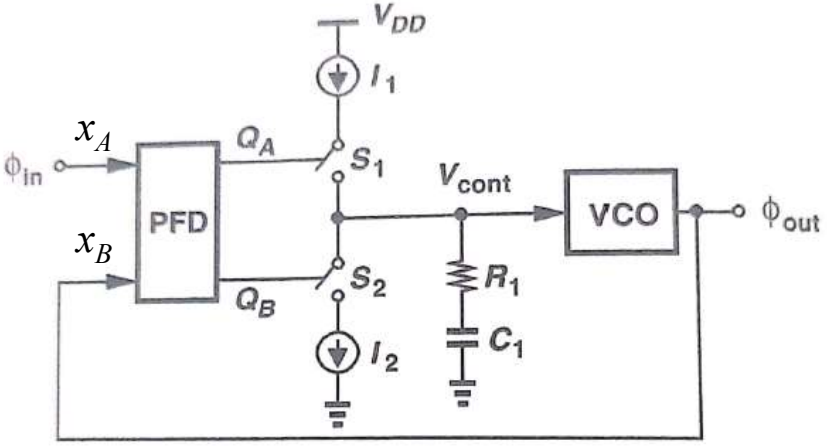


Figure 9.30 *Charge-pump PLL.*

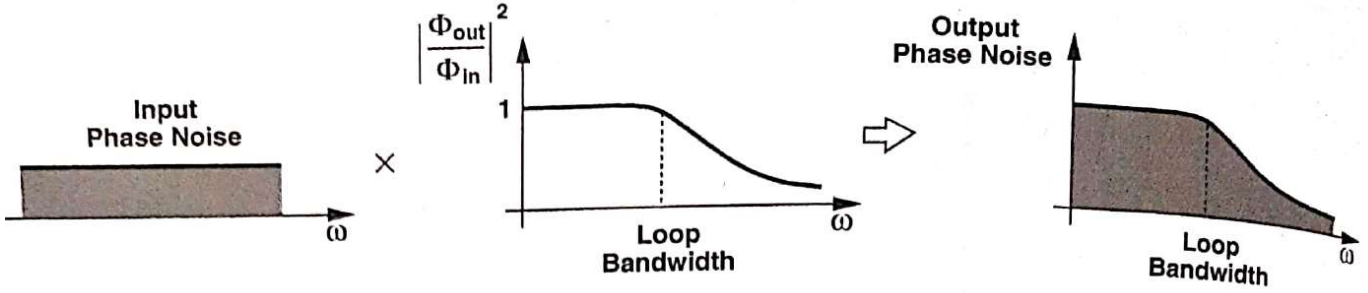


Figure 9.63 *Effect of reference phase noise in a PLL.*

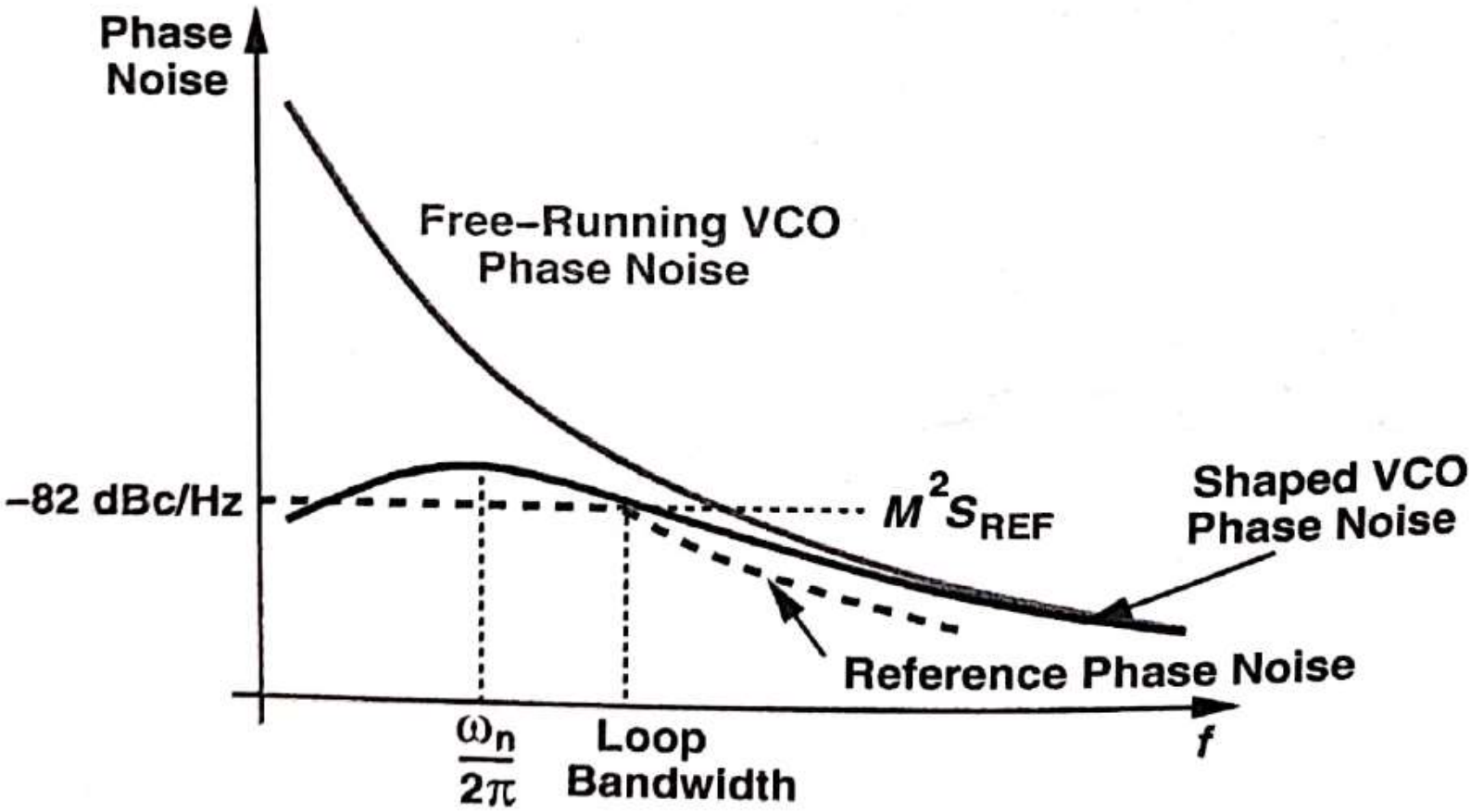
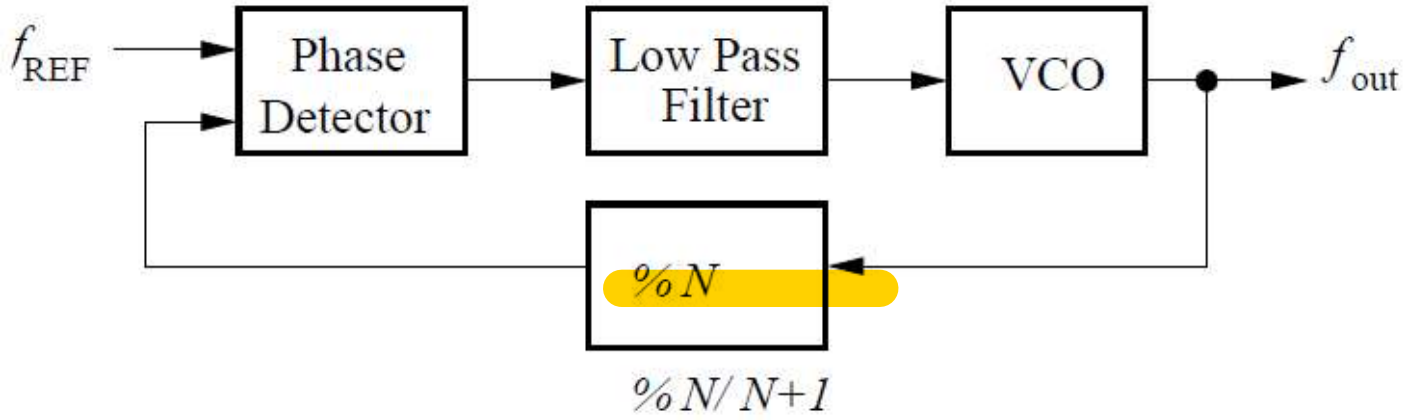


Figure 9.64 *Example of reference and shaped VCO phase noise in a PLL.*

Higher Order PLLs

- UP and DOWN signals may have a small skew between them.
- To mitigate this additional circuitry may be needed.

PLL Architecture



Integer-N Synthesizer:

· $f_{out} = N \times f_{REF}$

·Phase noise of f_{REF} is amplified by N within the loop bandwidth.

·Spurs at $f_{out} \pm f_{REF}$ appears due to imbalance/mismatch in the PD.

Fractional-N Synthesizer

·A pulses divided by N and B pulses divided by N+1 leads to an average division of $\frac{\mathrm{A}}{\mathrm{A+B}} N + \frac{\mathrm{B}}{\mathrm{A+B}}(N+1) = N + \alpha$ with $\alpha = \frac{B}{A+B}$.

· If the VCO is set to be $(\mathrm{N}+\alpha)\,\mathrm{f_{ref}}$, with fractional spurs at $\underbrace{f_{out}}_{N \times f_{ref}} \pm n\ \alpha\ f_{ref}$ appear.