RISC-V Processor Circui
Ti $k{\bf Z}$ Library

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1 Components

1.1 Instruction Memory

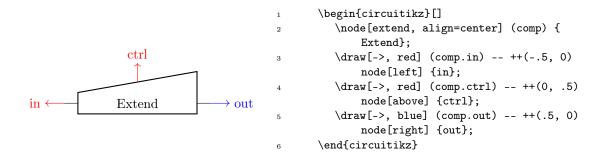
1.2 Data Memory

```
clk
                               \begin{circuitikz}[]
                                  \verb|\node[datamem, align=center]| (comp) {\tt Data} \\ \\
                                       Memory);
                                  \draw[->, red] (comp.a) -- ++(-.5, 0) node[
                                      left] {a};
                                  \draw[->, red] (comp.wd) -- ++(-.5, 0) node[
        RD
                                       left] {wd};
                                  \draw[->, red] (comp.clk) -- ++(0, .5) node[
  Data
                                       above] {clk};
 Memory
                                  \draw[->, red] (comp.we) -- ++(0, .5) node[
                                       above] {we};
                                  \draw[->, blue] (comp.rd) -- ++(.5, 0) node[
                                       right] {rd};
                                \end{circuitikz}
```

1.3 Register File

```
\begin{circuitikz}[]
                                                      \node[regfile, align=center] (comp) {
                                            2
                                                          Register\\File};
                                                      \draw[->, red] (comp.a1) -- ++(-.5, 0)
              clk we3
                                                           node[left] {a1};
                                                      \draw[->, red] (comp.a2) -- ++(-.5, 0)
                                                           node[left] {a2};
                  WE3
                                                      \draw[->, red] (comp.a3) -- ++(-.5, 0)
                                                           node[left] {a3};
                         RD1
 a1 ←
           A1
                                   \rightarrow rd1
                                                      \draw[->, red] (comp.wd3) -- ++(-.5,
                                                          0) node[left] {wd3};
 a2 ←
           A2
                         RD2
                                   \rightarrow rd2
                Register
                                                      \draw[->, red] (comp.clk) -- ++(0, .5)
                  File
                                                           node[above] {clk};
 a3 ←
           A3
                                                      \draw[->, red] (comp.we3) -- ++(0, .5)
                                            9
                                                           node[above] {we3};
wd3 \leftarrow
           WD3
                                                      \draw[->, blue] (comp.rd1) -- ++(.5,
                                           10
                                                          0) node[right] {rd1};
                                                      \draw[->, blue] (comp.rd2) -- ++(.5,
                                           11
                                                          0) node[right] {rd2};
                                           12
                                                   \end{circuitikz}
```

1.4 Extend Unit



1.5 Arithmetic Logic Unit

```
\begin{circuitikz}[]
                               \node[alu, align=center] (comp) {ALU};
\operatorname{ctrl}
                               \del{draw}[->, red] (comp.a) -- ++(-.5, 0) node[left] {
                                   a};
                               \draw[->, red] (comp.b) -- ++(-.5, 0) node[left] {
                                   b};
           → zero
                               \draw[->, red] (comp.ctrl) -- ++(0, .5) node[above
                                   ] {ctrl};
ALU
           \rightarrow out
                               \draw[->, blue] (comp.out) -- ++(.5, 0) node[right
                                   ] {out};
                               \draw[->, blue] (comp.zero) -- ++(.5, 0) node[
                                   right] {zero};
                            \end{circuitikz}
```

1.6 Register

```
begin{circuitikz}[]

node[reg, align=center] (comp) {};

draw[->, red] (comp.in) -- ++(-.5, 0) node[left] {in};

draw[->, red] (comp.clk) -- ++(0, .5) node[above] {clk

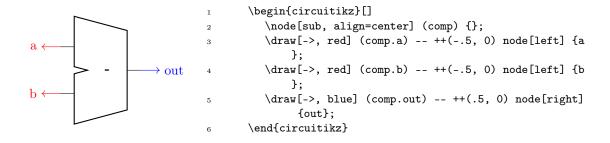
};

draw[->, blue] (comp.out) -- ++(.5, 0) node[right] {out
};

end{circuitikz}
```

1.7 Adder

1.8 Subtractor



1.9 Multiplexer

```
\begin{circuitikz}[]
                            1
                            2
                                       \node[mux, align=center] (comp) {};
                                       \draw[->, red] (comp.in1) -- ++(-.5, 0) node[left] {in
                           3
          sel
                                      \draw[->, red] (comp.in2) -- ++(-.5, 0) node[left] {in}
                                           2};
in1 \leftrightarrow
           0
                                      \draw[->, red] (comp.sel) -- ++(0, .5) node[above] {sel}
                   → out
in2 \leftrightarrow
                                       \draw[->, blue] (comp.out) -- ++(.5, 0) node[right] {
                            6
                                           out};
                                   \end{circuitikz}
```

1.10 Single-Cycle Control Unit

```
\begin{circuitikz}[]
                                                         \node[ctrlunitsc, align=center] (comp)
                                                               {Control\\Unit};
                                                         \draw[->, red] (comp.op) -- ++(-.5, 0)
                                                              node[left] {op};
                                                         \draw[->, red] (comp.funct3) --
                                                             ++(-.5, 0) node[left] {funct3};
                                                         \draw[->, red] (comp.funct7) --
                              → pcsrc
                                                             ++(-.5, 0) node[left] {funct7};
                                                        \draw[->, red] (comp.zero) -- ++(-.5,
               Control
                              \rightarrow resultsrc
                                                             0) node[left] {zero};
                 Unit
                              → memwrite
                                                        \draw[->, blue] (comp.pcsrc) -- ++(.5,
                                                               0) node[right] {pcsrc};
             op
   op \leftarrow
                              \rightarrow alucontrol
                                                         \draw[->, blue] (comp.resultsrc) --
                                                             ++(.5, 0) node[right] {resultsrc};
funct3 \leftarrow
             funct3
                              \rightarrow alusrc
                                                         \draw[->, blue] (comp.memwrite) --
                                                             ++(.5, 0) node[right] {memwrite};
funct7 \leftarrow
             funct7_5
                              \rightarrow \text{immsrc}
                                                         \draw[->, blue] (comp.alucontrol) --
                                             11
                              → regwrite
  zero \leftarrow
             zero
                                                             ++(.5, 0) node[right] {alucontrol
                                                             };
                                                        \draw[->, blue] (comp.alusrc) --
                                             12
                                                             ++(.5, 0) node[right] {alusrc};
                                                        \draw[->, blue] (comp.immsrc) --
                                             13
                                                             ++(.5, 0) node[right] {immsrc};
                                                         \draw[->, blue] (comp.regwrite) --
                                             14
                                                             ++(.5, 0) node[right] {regwrite};
                                                      \end{circuitikz}
```

2 Single-Cycle RISC-V Processor

