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FIELD EFFECT TRANSISTOR (FET)

INTRODUCTION

FET is a semiconductor device which can perform many of the functions of a bipolar junction transistor (BJT) but operates in a fundamentally different way.

A BJT is a current controlled device. i.e output characteristics of the device are controlled by base current and not by base voltage. However FET is a semiconductor device that depends for its operation on the control of current by an electric field (i.e. the output characteristics are controlled by input voltage (i.e. electric field) and not by input current. In other words FET is one voltage-controlled rather than current-controlled devices.

FET can replace bipolar transistors in many applications, can be designed to handle large currents, and are almost exclusively the devices used in large-scale integration etc. such as microprocessors and memory devices. FET is also known as a "Unipolar" transistor since current is transported by carriers of one polarity (majority carriers). In the BJT, both majority and minority carriers are involved.

The BJT has a low input impedance because of forward biased emitter junction. BJT also has considerable noise level. The FET has large input impedance which may be more than $100M\Omega$ and FET is generally much less noisy than BJT.

TYPE OF FET

There are two types of FET.

- (i) Junction field effect transistor (JFET)
- (ii) Insulated field effect transistor (IFET) also known as Metal Oxide Semiconductor FET (MOSFET).

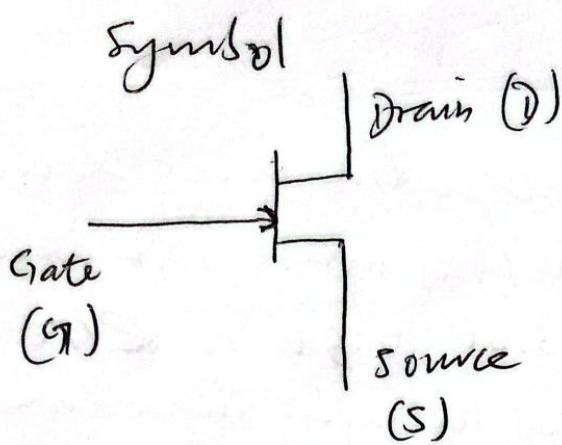
MOSFET further divided into two

- enhancement type
- depletion type.

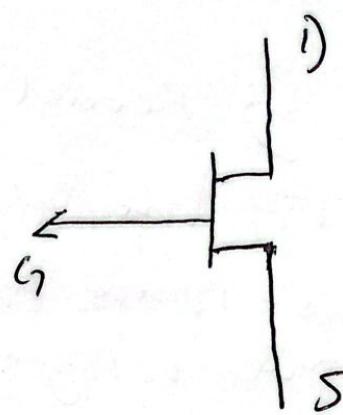
All FETs can be obtained in either n-channel or p-channel.

- The JFET consists of a piece of high-resistivity silicon that ~~conducts~~ provides a channel for the flow of majority carriers. The gate-source junction is operated in the reverse bias region, and thus the gate current is practically zero.

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n - channel MOSFET



p - channel MOSFET

→ The MOSFET depends for its operation on the fact that it is not necessary to form a semiconductor junction on the channel of an FET in order to achieve gate control of the channel current. Instead, the gate electrode is a metallic region separated from the conducting channel by a thin silicon dioxide layer. Because the gate is electrically insulated from the source-drain cut, its voltage polarity may go either positive or negative without gate current flowing. This allows for the existence of two types of MOSFET. These are

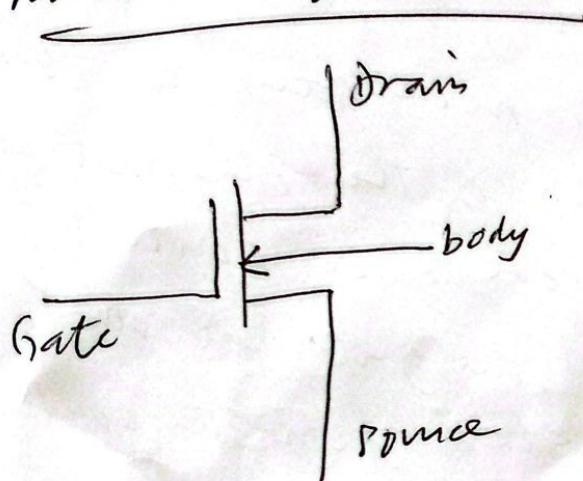
(a) - Enhancement type : This conducts only when forward biased and is cut off at zero volts between gate and source.

(b) Depletion type : This conducts in both forward and reverse directions and is cut off only when the gate-source is reversed.

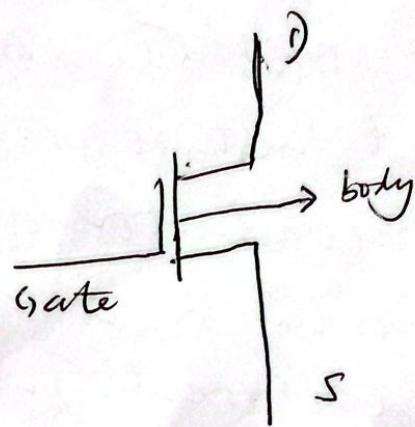
biased by several volts.

Note: JFETs are always depletion mode devices. The gate-source forward bias must not exceed a positive voltage of about 0.5V or else the junction will conduct and the input impedance will thus be drastically reduced.

MOSFET Symbol



n-channel MOSFET



p-channel MOSFET

JFET

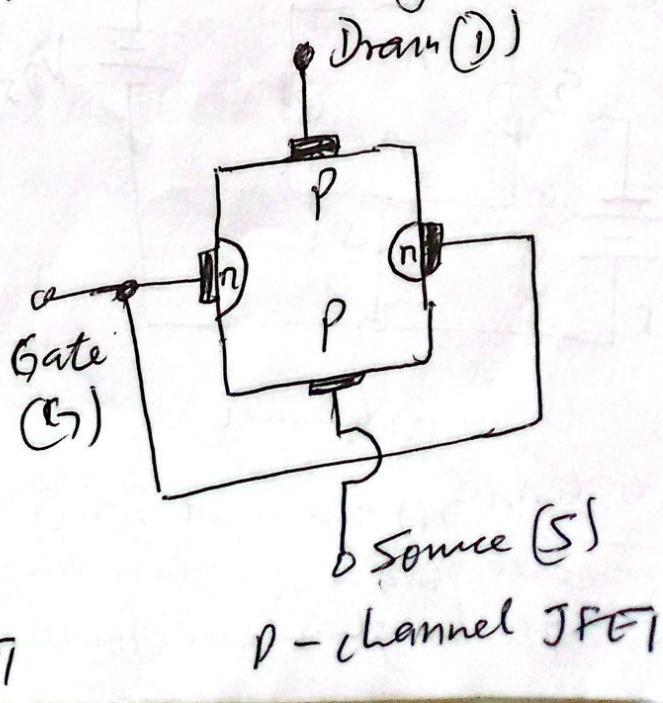
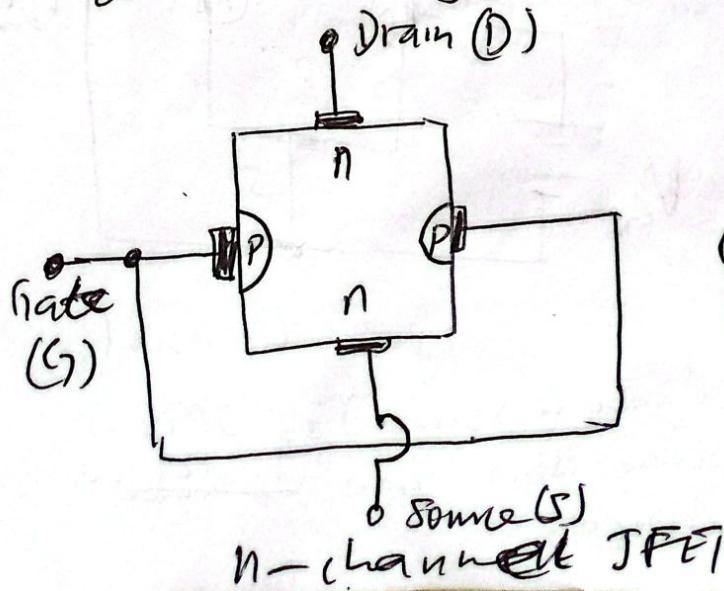
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A junction field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier (electrons or holes) and is controlled by means of an electric field between the gate electrode and the conducting channel of the device.

i.e It is a voltage control device (input Voltage, V_{GS} , controls the output current).

PHYSICAL STRUCTURE OF JFET

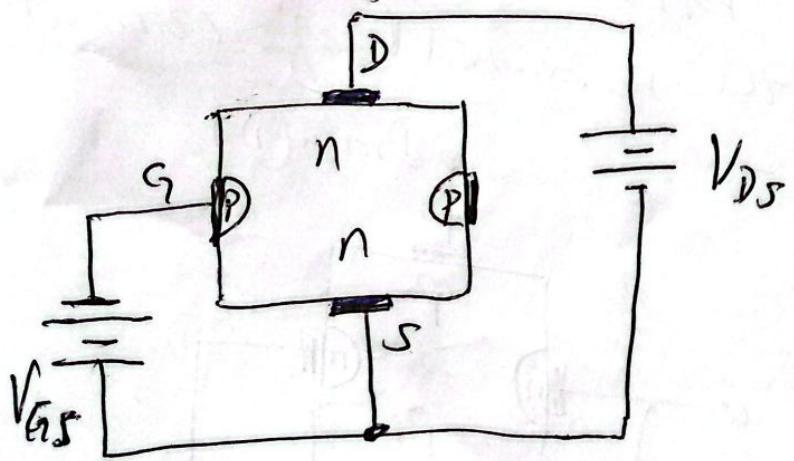
There are two fundamental varieties of JFETs, each of which is available in two polarities i.e n-channel which is like n-p-n and p-channel which is like p-n-p. Both work in a similar manner except for the reversal of current and voltage.



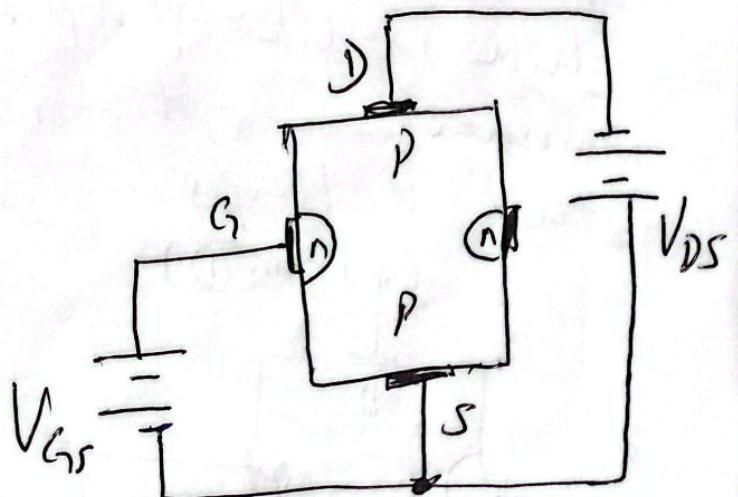
From the figure above, the drain D, the gate G and the source are analogous to collector, base and emitter in BJT respectively.

An n-channel JFET is normally operated with its drain more positive than the source. However unlike the npn transistor, current will flow from drain to source with the gate grounded. A gate junction must be reverse biased (at few voltages) to cut off the drain current.

JFET is never operated with the gate forward biased, so no current except leakage current flows in the circuit.



n-channel



p-channel

Points to Note (i) the input circuit (i.e. gate to source) of JFET is reverse biased. This implies that the ~~source~~ device has high input impedance.

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(ii) The drain is so biased w.r.t source that drain current I_D flows from the source to drain.

(iii) In all JFETs, source current I_S is equal to the drain current i.e $I_S = I_D$.

BASIC TERMS

(a) Channel: Is a region between the two gates through which the majority carriers move from the source to drain. The more negative the gate potential is the less the drain current due to the increased depletion region and the decreased channel width.

(b) Source: terminal through which the majority carriers enter the bar.

(c) Drain: Terminal through which the majority carriers leave the bar. The drain-to-source voltage is called V_{DS} and if it is +ve V_D is more the Ban S. V_{DD} is drain supply voltage.

(d) Gate: Gate G is the heavily doped materials on both sides of the bar. If the channel is n-type, the gate is the heavily doped p-type material forming

a p-n junction. If on the other hand, the channel is p-type material, then a heavily doped n-type material is used forming the gate. Between the gate and the source, a voltage V_{GS} is applied in the direction of reverse bias.

$$V_{GS} = -V_{GA} \text{ for n-type material.}$$

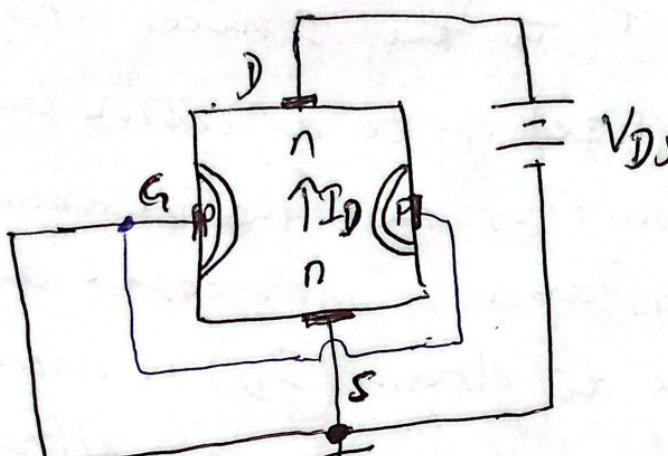
PRINCIPLE OF OPERATION OF JFET

Note: In each case (n-channel and p-channel), the voltage between the gate and source (V_{GS}) is such that the gate is reverse biased. This is the normal way of JFET function. Also note that drain and source terminals are interchangeable.

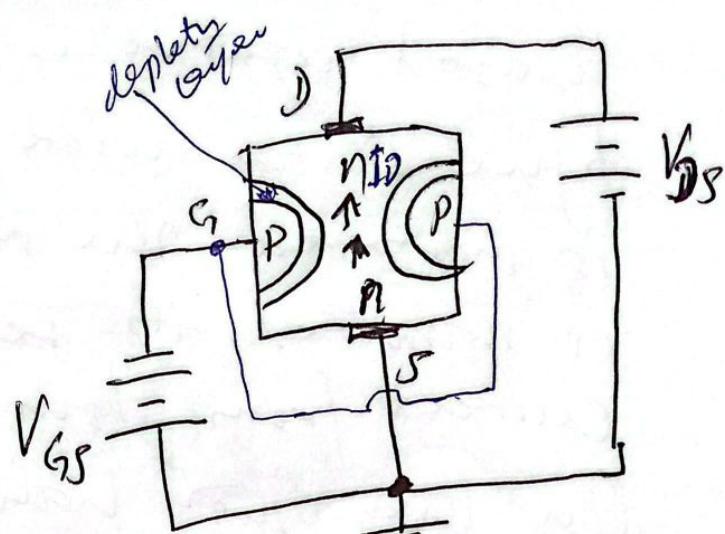
JFET operates on the principle that width and hence resistance of the conduction channel can be varied by changing the reverse voltage V_{GS} . That is drain current I_D can be changed by altering (varying) V_{GS} .

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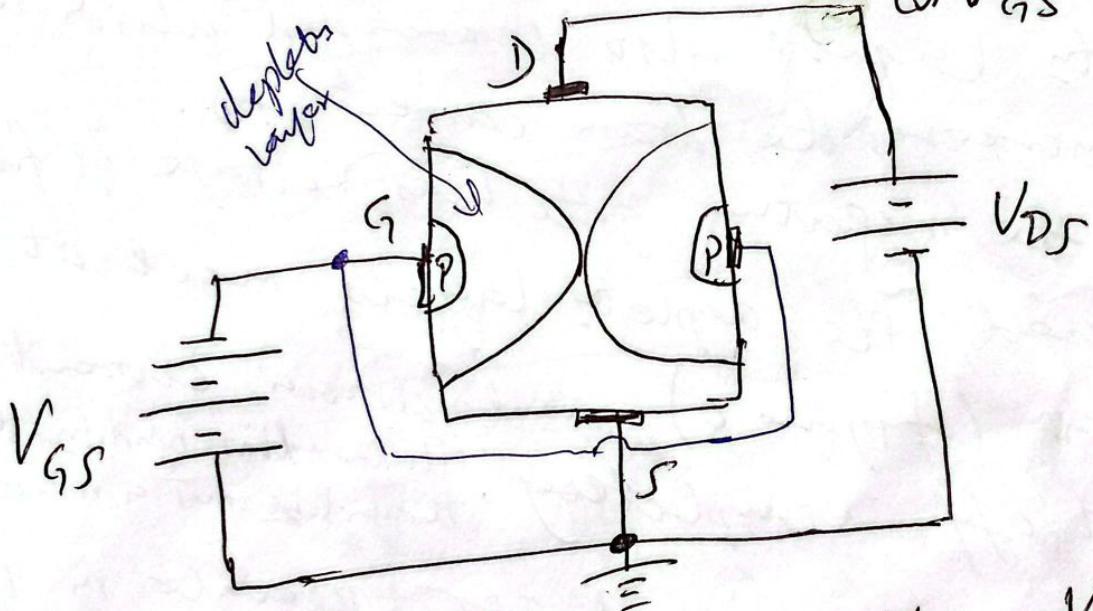
Consider the n-channel JFET



$$(a) \quad V_{GS} = 0$$



$$(b) \quad V_{GS} \neq 0$$



(c) more reverse voltage V_{GS} .

With the gate terminal not connected (figure), i.e. $V_{GS} = 0$, and a potential applied (+ve at drain and -ve at source), a drain current (I_D) flows as shown in figure above. The size of the depletion layers determines the width of the channel and hence the current conductivity through the bar.

When the reverse voltage V_{GS} i.e. Gate is biased negative w.r.t to the source as in figure 'b' the width (size) of the depletion layer is increased. The result is that the channel is narrowed, its resistance is increased and current from Source to drain (I_D) is decreased. On the other hand if the reverse voltage V_{GS} is decreased, the width of the depletion layers also decreased which in turn increases the drain current I_D .

When the negative gate bias voltage is further increased, the depletion layers meet at the center (figure c), and drain current I_D is cut off completely. Under this condition the channel becomes a non-conductor. Note that a p-channel JFET operates in the same manner as an n-channel except that channel current carriers will be holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

The value of the Gate - source Voltage (V_{GS}) at which the drain current approaches zero is called the Gate-cut off voltage or Pinch-off Voltage and is typically

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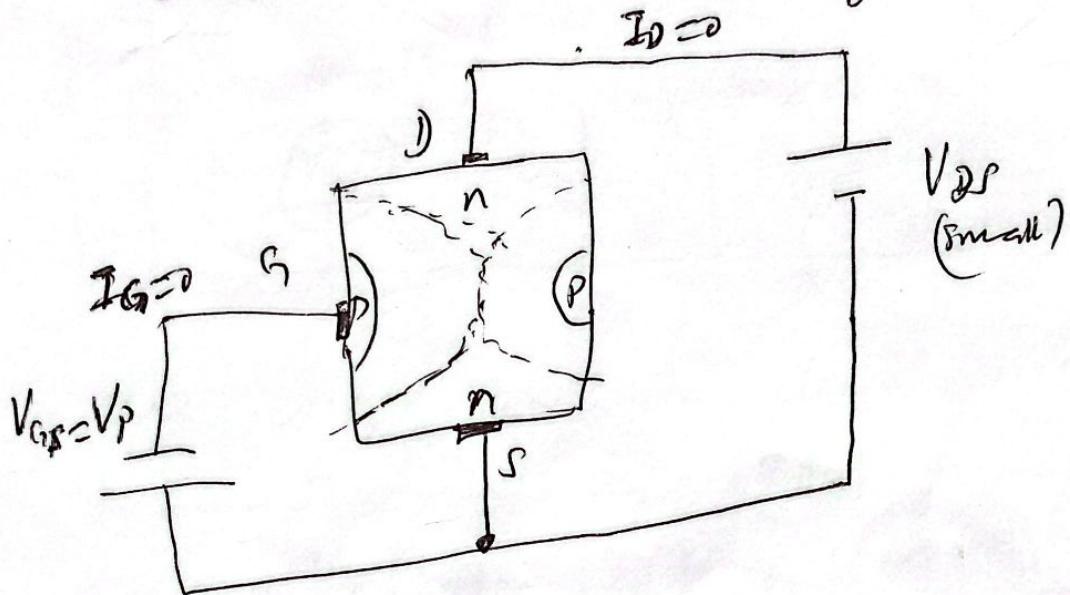
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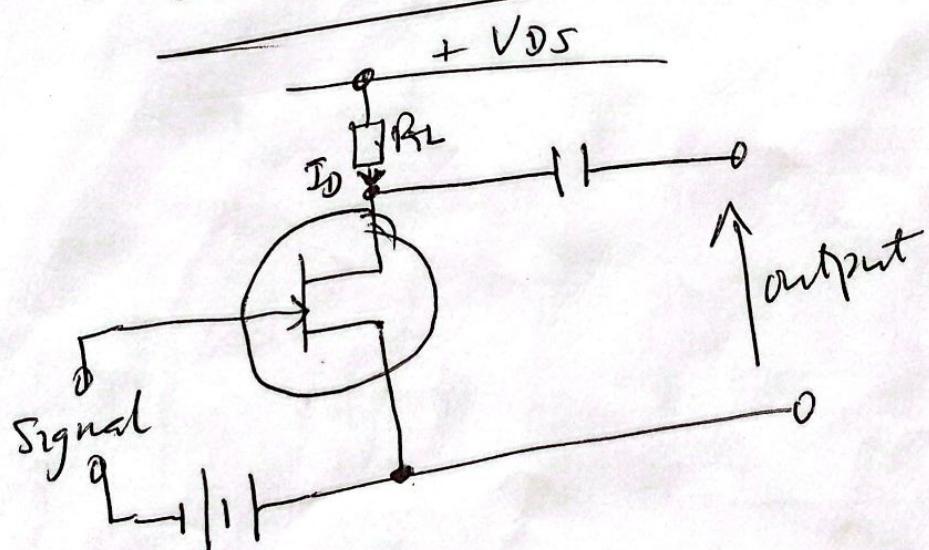
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is in the range of $-3V$ to $-10V$. ~~at which~~
 therefore, the Voltage V_{GS} at which pinch-off
 occurs is called Pinch-off Voltage V_P .

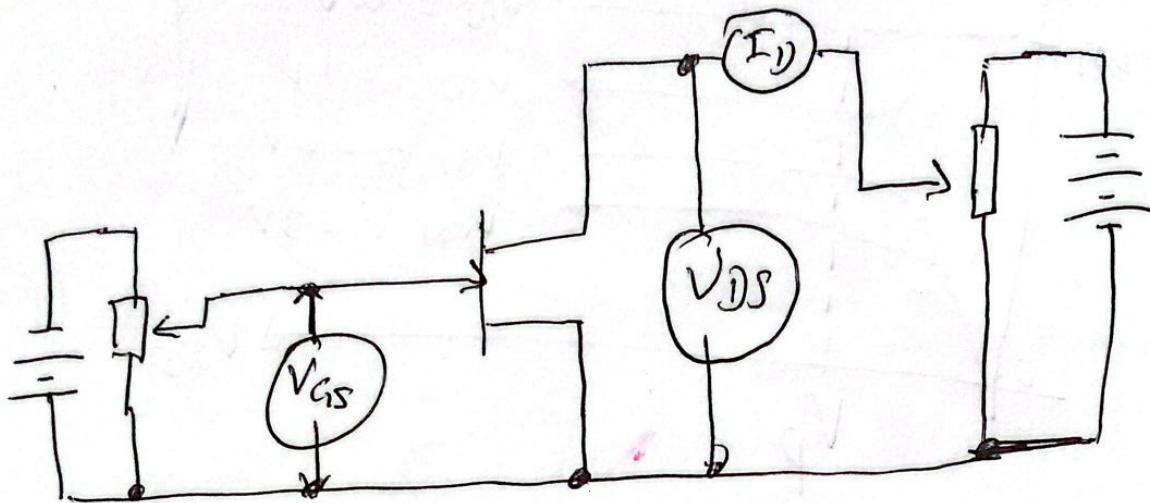


JFET AS AND AMPLIFIER

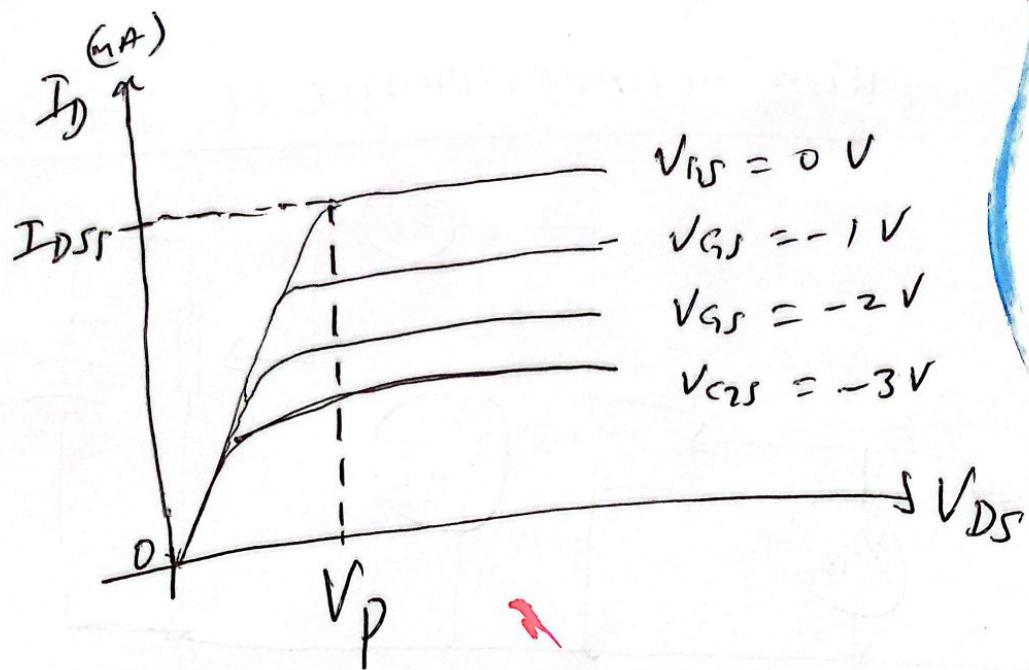


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OUTPUT CHARACTERISTICS OF JFET



The curve between drain current (I_D) and drain-source voltage (V_{DS}) at constant gate-source voltage (V_{GS}) is known as the output characteristics of JFET. The figure above shows the ~~circuit~~ diagram for determining the output characteristics of JFET. Keeping V_{GS} fixed at some values, then the drain source voltage is changed in steps. Note the corresponding values of drain current to each value of V_{DS} . A plot of I_D current against V_{DS} gives the output characteristics as shown in the figure below.



From this figure

- At first, the drain current I_D rises rapidly with V_{DS} but then becomes constant.
- the drain source voltage above which drain current I_D becomes constant is known as pinch off voltage V_p or V_p is the minimum drain-source voltage at which the drain current essentially becomes constant.
- I_{DSS} is the drain saturation current with the gate voltage V_{GS} at zero.

The dependency of the drain current I_D on both V_{DS} and V_{GS} is shown by the family of curves above.

Note that V_{DS} has little effect and V_{GS} essentially controls I_D . For proper functioning of JFET, it is always operated for $V_{DS} > V_p$. However V_{DS} should not exceed $V_{DS(\text{max})}$ otherwise JFET may breakdown.

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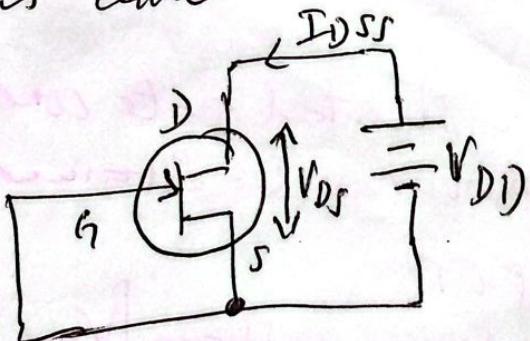
IMPORTANT TERMS :

The following important terms are often used in the analysis of JFET.

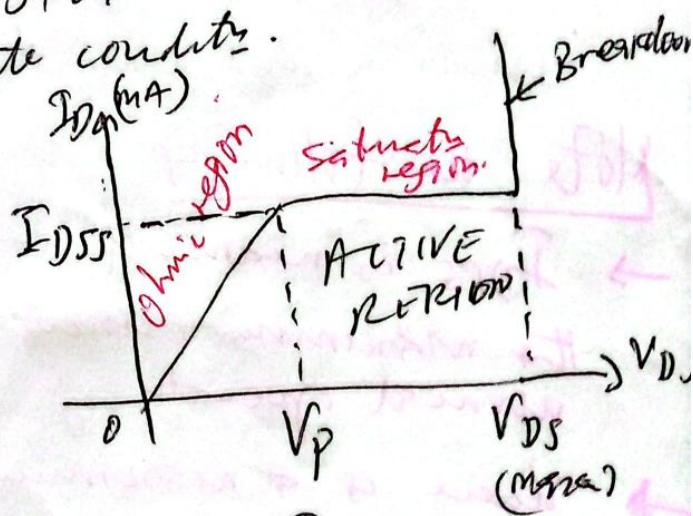
(1) Shorted-gate drain current (I_{DSS}) .

I_{DSS} is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage (V_p). It is sometimes called zero-bias current. It is the maximum drain current I_D with normal operation of JFET.

The cut below shows JFET with $V_{GS} = 0$. This cut is called shorted-gate condition.



(a)



(b)

From figure (b) when V_{DS} is greater than V_p , the drain current is almost constant. This is because when V_{DS} equals V_p , the channel is effectively closed and does not allow further increase in drain current I_D .

(7)

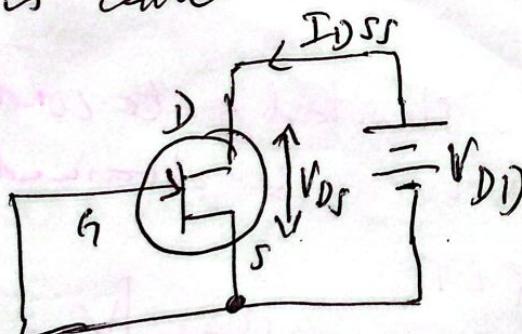
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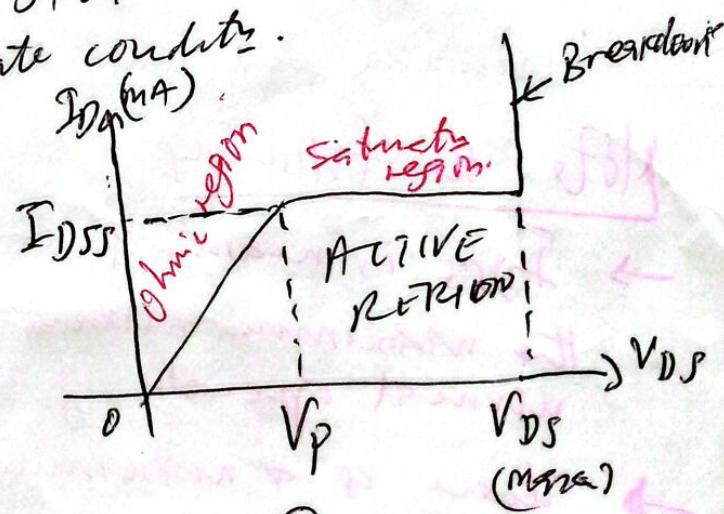
(1) Shorted-gate drain current (I_{DSS}).

I_{DSS} is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain circuit to ground. It is sometimes called zero-bias current. It is the maximum drain current I_D with normal operation of JFET.

The circuit below shows JFET with $V_{GS} = 0$. This circuit is called shorted-gate condition.



(a)



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From figure (b) when V_{DS} is greater than V_p , the drain current is almost constant. This is because when V_{DS} equals V_p , the channel is effectively closed and does not allow further increase in drain current I_D .

~~(2) Pinch off Voltage (V_p):~~ is the minimum drain source voltage at which the drain current essentially becomes constant.

With $V_{DS} = 0$ is cut 'a' above. Figure 6 shows

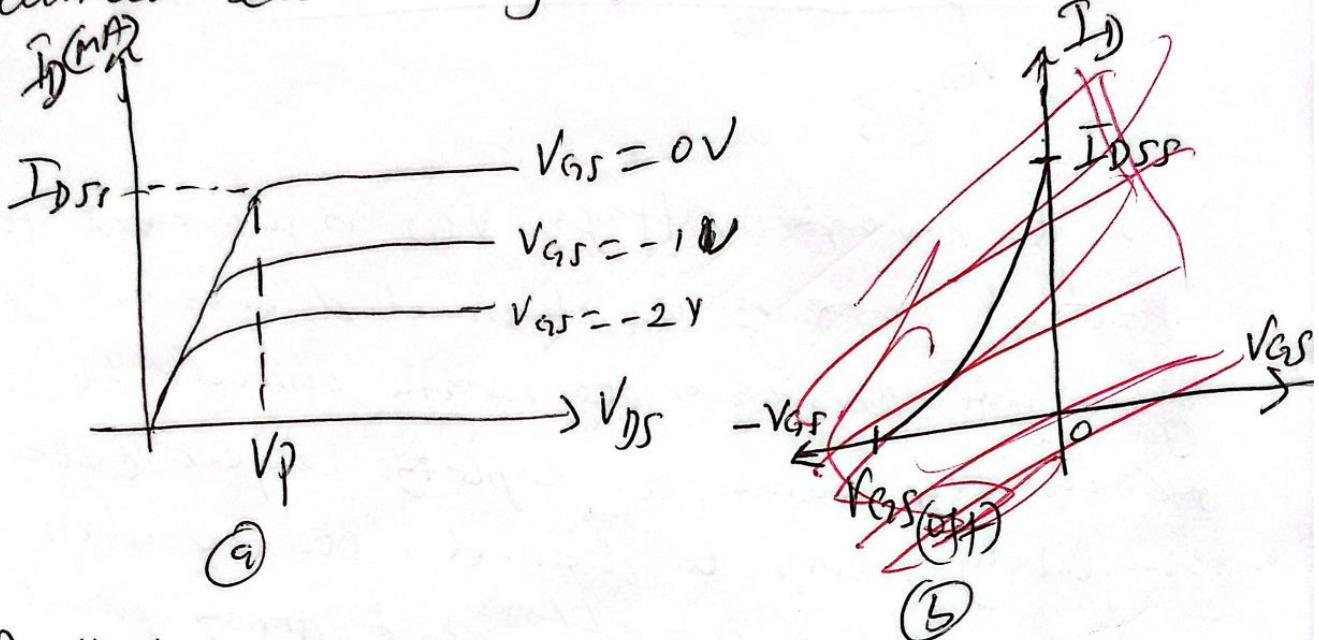
the relationship between drain current (I_D) and drain source voltage (V_{DS}) for $V_{GS} = 0$. The drain current increases rapidly at first and then remains constant at pinch off voltage V_p . At this point I_D reaches its maximum I_{DSS} . When V_{DS} is increased beyond V_p , the depletion layers expand at the top of the channel. At this point the channel acts as a current limiter and holds drain current constant at I_{DSS} .

Note the following

- I_{DSS} is measured under shorted gate condition, it is the maximum current that can be obtained with normal operating of JFET
- There is a maximum drain voltage [$V_{DS(max)}$] that can be applied to a JFET. If $V_{DS} > V_{DS(max)}$ then JFET would breakdown. See figure above
- The region between V_p and $V_{DS(max)}$ is called "constant-current region" or "active region". JFET behaves like a constant-current device. JFET works properly in this active region.

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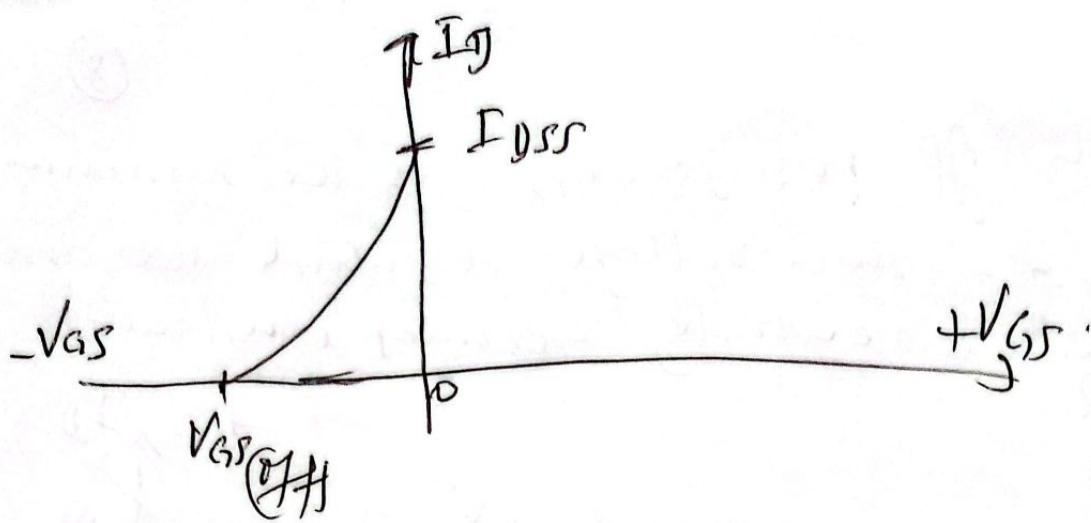
- ② Pinch off voltage (V_p): is the minimum drain-source voltage at which the drain current essentially becomes constant.



Note that in figure above that for values of $V_{DS} > V_p$, the drain current is almost constant. This is because when V_{DS} equals V_p , the channel is effectively closed and does not allow further increase in I_D . For proper functioning of JFET, $V_{DS} > V_p$. However V_{DS} should not exceed $V_{DS(\text{max})}$ otherwise JFET may breakdown.

- ③ Gate-source cut-off voltage $V_{GS(\text{off})}$: this is the gate-source voltage when the channel is completely cut off and $I_D = 0$. This is easily understood using transfer characteristic of JFET as shown in the figure below.

$$Q = 2\pi \cdot \frac{1}{2} \cdot qV \cdot \frac{1}{2} = 0.5qV^2$$



As the reverse voltage V_{DS} is increased, the cross-sectional area of the channel decreases. This results in which decreases the drain current. At some reverse V_{DS} value, the depletion layer extends completely across the channel. Under this condition, the channel is cut off and drain current $I_D = 0$. The gate voltage at which the channel is cut off is called gate-source cut off voltage $V_{GS(off)}$.

Note: V_{GS} will always have the same magnitude as V_p .
 $\text{eg if } V_p = 5V, \text{ then } V_{GS} = -5V.$

Note also that V_p is the value of V_{DS} that causes JFET to become a constant current device. It is measured at $V_{GS} = 0V$ and will have a constant drain current I_{DSR} . However, $V_{GS(off)}$ is the value of V_{GS} that cause I_D to drop to nearly zero.

$$\text{i.e } V_{GS(off)} = V_p \text{ for } V_{GS} = 0 \\ \text{or } V_p = |V_{GS(off)}|.$$

ADVANTAGES OF FETs OVER BJT

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FETs enjoys certain inherent advantages over BJTs.

- (i) Very high input impedance at low frequencies
(in practice the input impedance is limited by the shunt gate bias resistor). The high input impedance permits high degree of isolation between input and output.
- (ii) Low noise because they are voltage controlled
- (iii) Absence of thermal runaway, due to negative temperature coefficient.
- (iv) JFET has a very high power gain. This eliminates the necessity of using driver stages.
- (v) JFET has smaller size, longer life and high efficiency
- (vi) Junction capacitance is independent of device current (i.e. inherent stability allowing the design of stable frequency oscillations).

Differences between JFET and BJT

- (i) Operation of JFET depends on the flow of majority carriers (electrons or holes) making it a unipolar transistor. However BJT operation depends on both holes and electrons making it a bipolar transistor.
- (ii) The input circuit (i.e. gate-source) is reverse biased giving rise to high input impedance. However, the input circuit of BJT is forward biased and hence low input impedance.
- (iii) A very small (or no current) enters the gate of JFET ($i.e. I_g = 0A$). However, typical BJT base current might be a few μA .
- (iv) JFET is voltage-controlled device (i.e. it uses voltage at gate terminal to control the current between drain and source, while BJT uses current at its base to control a large current between collector and emitter). Thus a BJT is characterised by current gain, while JFET is characterised as a transconductance (i.e. ratio of change in output current (I_o) to input (gate) voltage).
- (v) There are no junctions as in BJT. Conduction is through n-type or p-type semiconductor material. This gives rise to low noise level.