Zecheng Li

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Education

ShanghaiTech University Sept. 2019 - Jun. 2023
Undergraduate, Major in Computer Science. GPA: 3.6/4.0. Shanghai, China
- A+ Courses: Operating Systems, Computer Architecture, Computer Networks, Compilers and more.

University of California, Berkeley Jan. 2022 - May. 2022
GLOBE Program, College of Engineering. Major in Computer Science. GPA: 4.0/4.0. Berkeley, CA, USA
- Main Courses: Artificial Intelligence, Computer Security, Nonlinear and Discrete Optimization.

Experience

GeekPie_HPC association July. 2021 - Present
Member Shanghai, China
- Participating Student Cluster Competition with a team of 6 members. Analyzed and tuned Fortran/C/C++ scientific applications with MPI/OpenMP/Charm++ on 2-20 nodes in supercomputers and trained new members who were interested in HPC systems. Related applications: Quantum Espresso, NWChem and NAMD.
- Awards: Ranked 2, SC21-SCC; Ranked 4, ISC22; Overall Winner, IndySCC in SC22.
- Publication: G. Li et al., "Critique of "A Parallel Framework for Constraint-Based Bayesian Network Learning via Markov Blanket Discovery by SCC Team from ShanghaiTech University," in IEEE Transactions on Parallel and Distributed Systems, 2022.

Sixie Capital July. 2022 - Present
C++ Software Engineer Intern Shanghai, China
- Optimized several computational intensive routines to improve performance to 70%-90% peak FP performance on dual-socket AMD EPYC servers with AVX2 and OpenMP, and by 2-3x on GPUs using multi-stream CUDA.
- Tuned kernel compile configurations and cmdline settings for low-latency real-time trading systems, and diagnosed and fixed periodic interrupts generated by certain graphics cards.
- Optimized kernel bypass network, lowering medium time of NIC to CPU transmission time by 30%.

Research on SSD Cache Management June. 2022 - Present
With Prof. Ruan from Cal State East Bay Remote
- Investigated the write cache contention when multiple I/O operations were running concurrently on an SSD simulator called MQSim, and proposed and implemented a dynamic cache partitioning algorithm that achieved a 10% improvement in bandwidth on synthetic workloads.
- Working on paper: Dynamic On-Board Write Cache Partitioning in Solid State Drives.

Personal Projects

Athernet Fall 2021
Computer Networks Athernet
- A network using sound to transmit data in C++ from physical layer, making the sound card an NIC.
- Implemented PSK and OFDM to encode data to acoustic signals, built a CSMA/CA state machine in MAC layer and a gateway for Athernet to support various protocols in the Internet.

COOL Compiler Spring 2021
Compilers COOL Compiler
- The Classroom Object-Oriented Language to MIPS assembly compiler originally from Stanford CS143.
- Implemented the front-end Lexer and Parser in Flex and Bison, the back-end Semantic Analysis and Code Generation in C++.

PintOS Fall 2021
Operating Systems PintOS
- A simple operating system for 80x86 architecture with a similar design to early Unix.
- Implemented Thread Scheduler, User Program loading, Syscalls, Virtual Memory and File System, providing fundamental hardware abstractions to user programs.

Miscellaneous

Teaching Assitant: Operating Systems, Fall 2022 at ShanghaiTech University. Instructor: Prof. Shu Yin.
Programming Languages: C, C++, Python, Java, Assembly (including SIMD intrinsics).
Tools and Frameworks: OpenMP, OpenMPI, CUDA, CMake, perf, gdb.
Interests: Computer Architecture, Parallel Computing, Program Profiling & Optimizing.