Lab 2 Report

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An Aggie does not lie, cheat or steal.
Nor does an Aggie tolerate those who do.

Problem 1

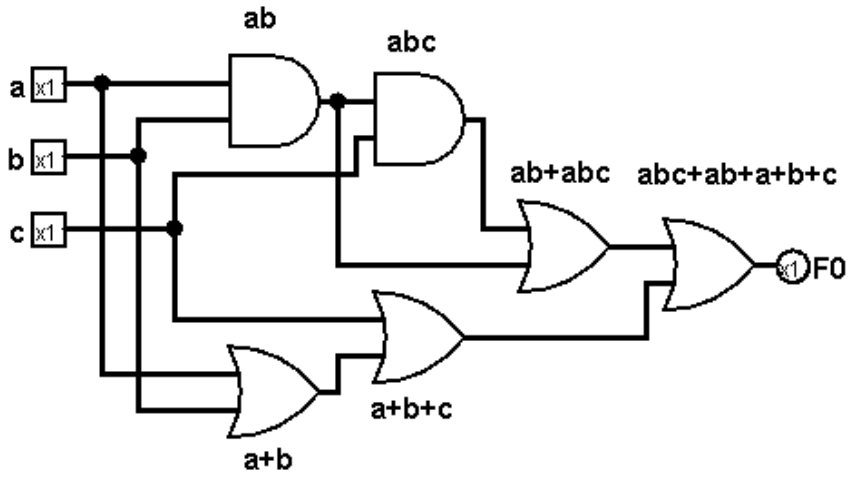

Figure 1: $F = abc + ab + a + b + c$

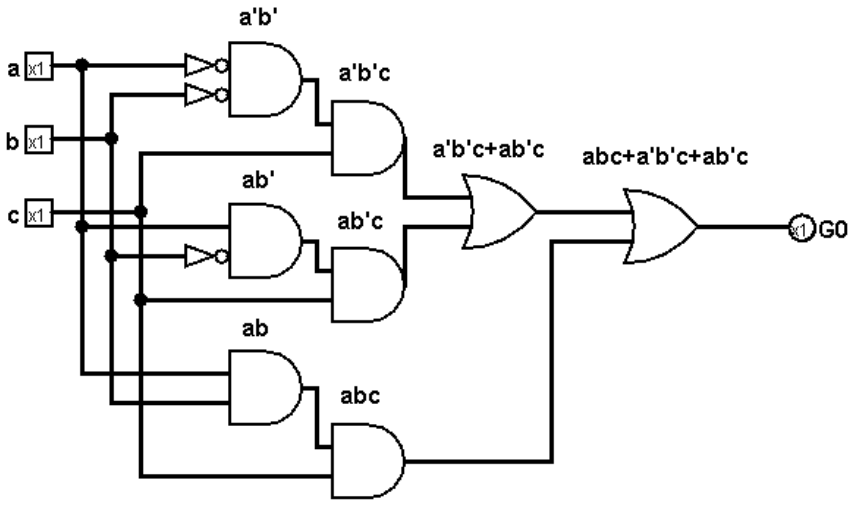

Figure 2: $G = a'b'c + ab'c + abc$

Chips used: 74LS04 hex inverter gate, 74LS08 quad 2-input AND gate, and 74LS32 quad 2-input OR gate.
To physically wire circuit F, a minimum of one 74LS08 chip and one 74LS32 chip are needed. After connecting both chips to power and ground through pin 14 and 7, wiring can begin. Using a wire, we can route input a into pin 13 on both chips. Next we wire input b into pin 12 on both chips. Then we wire the output, pin 11, to pin 10. This process is done for both chips. Next we wire input c into pin 9 on both chips. Branching from pin 11 of the 74LS08 chip, we add another wire from this pin to pin 1 of the 74LS32 chip. Next we wire pin 8 of the 74LS08 chip into pin 2 of the 74LS32 chip. Next, we connect pin 3 and pin 8 of the 74LS32 chip to pin 4 and pin 5 respectively. As a final result, pin 6 on the 74LS32 chip will be the output F.

To physically wire circuit G, a minimum of one 74LS04 chip, two 74LS08 chips, and one 74LS32 chip are needed. After connected all four chips to power and ground through 14 and 7, wiring can begin.

Parameters:
$V_{cc} = 5V, T_A = 25°C, C_L = 15pF, R_L = 2k\Omega$
Maximum delay, for F would be $2t_{OR} + 2t_{AND}$. This is equivalent to $2(11) + 2(13) = 48ns$. Likewise for G, its time delay would be $t_{NOT} + 2t_{AND} + 2t_{OR}$. This is equivalent to $10 + 2(13) + 2(11) = 58ns$.

The maximum delay under the indicated parameters would be 48 nanoseconds for Circuit F and 58 nanoseconds for Circuit G.

Problem 2

Click here to view a video of the circuit running.
Below are images of the circuits developed.

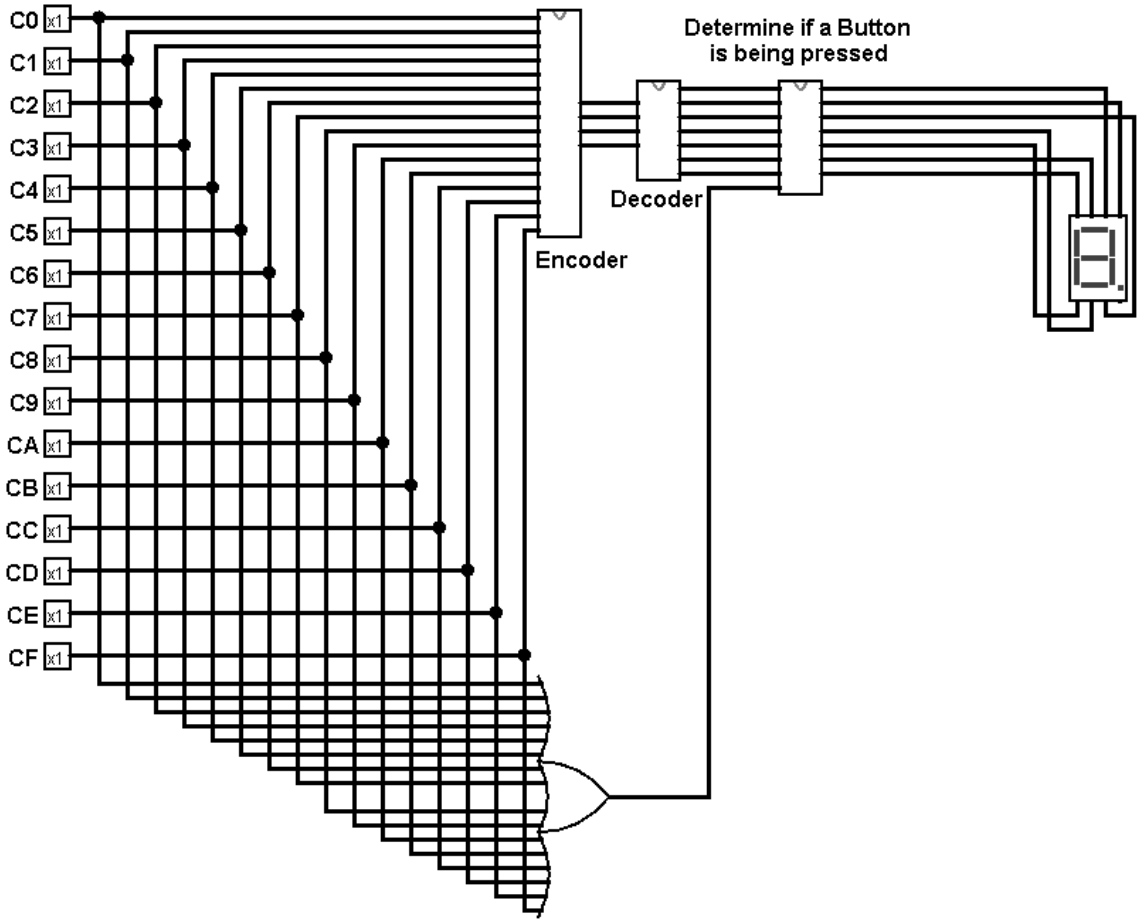

Figure 3: Main Circuit

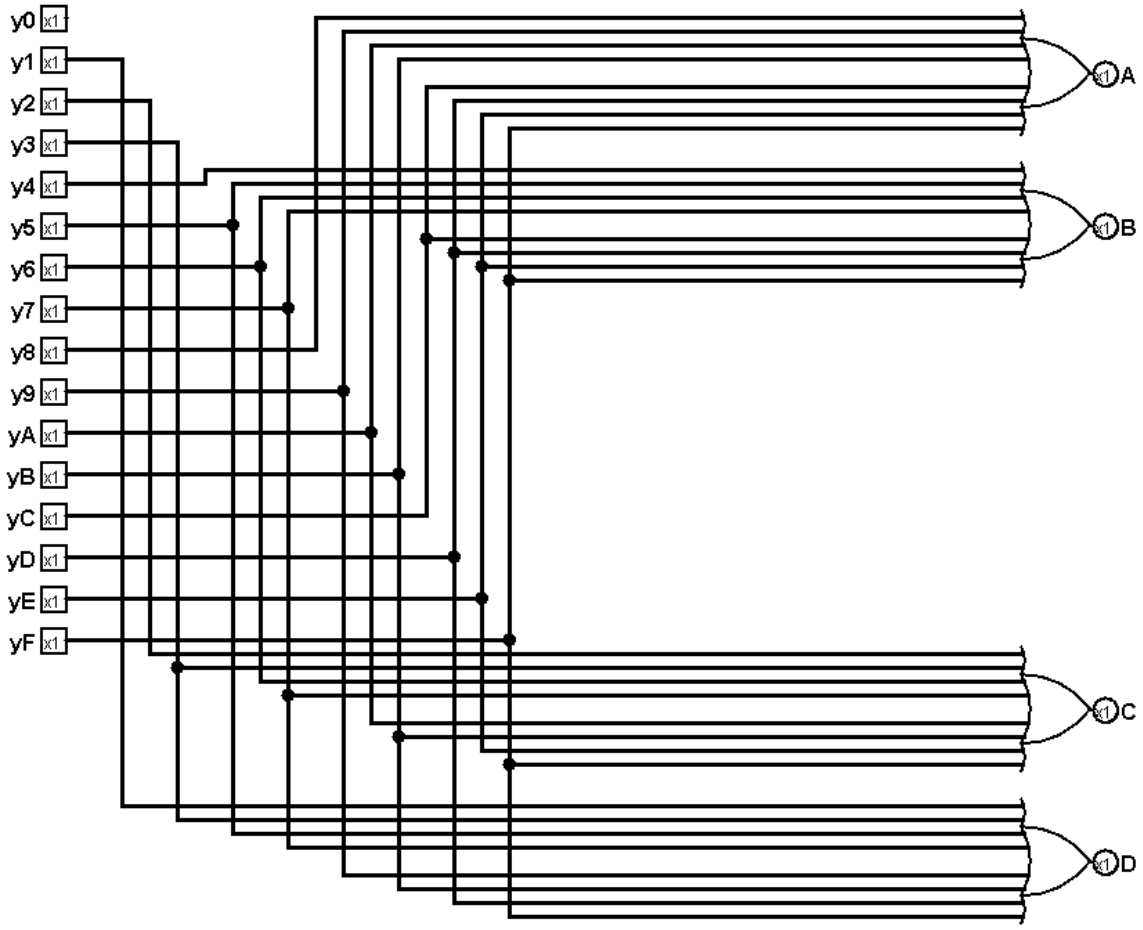

Figure 4: 16:4 Encoder

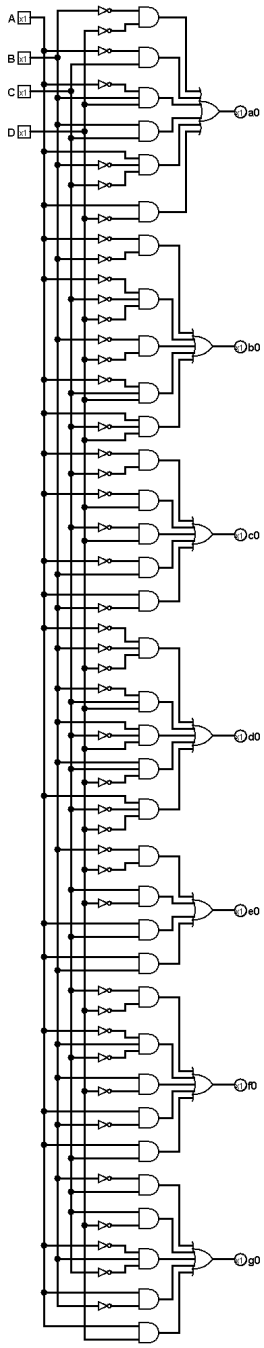

Figure 5: Decoder

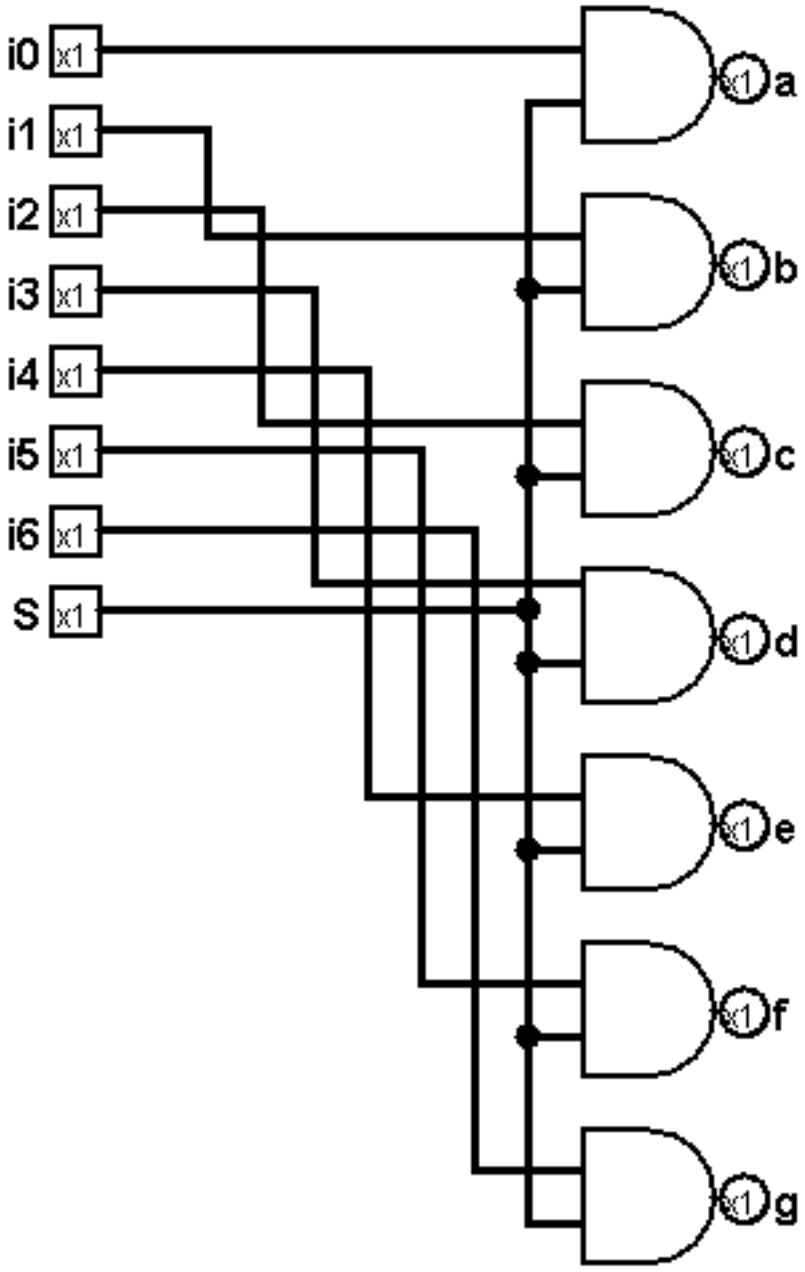

Figure 6: Filter Circuit