# Homework 2

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An Aggie does not lie, cheat or steal.
Nor does an Aggie tolerate those who do.

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## Chapter 4

### 4.2

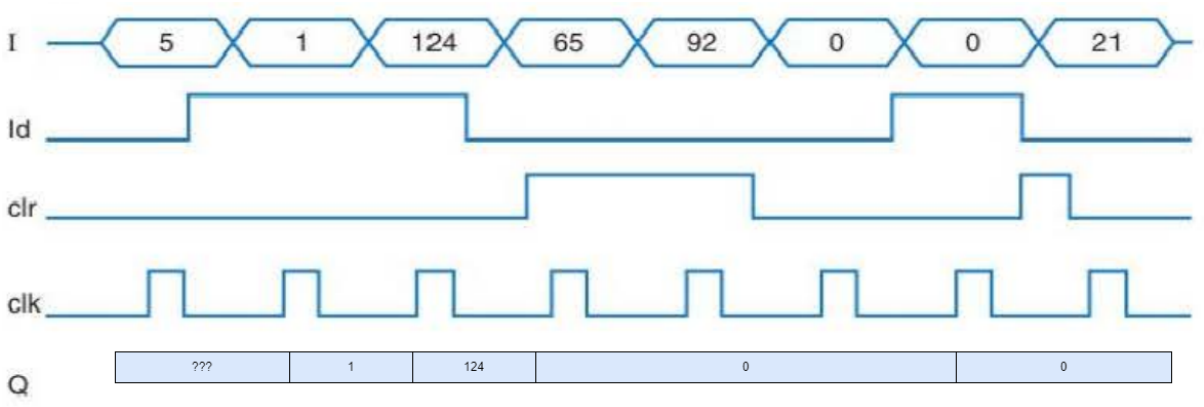


Figure 1: Timing Diagram

## 4.3

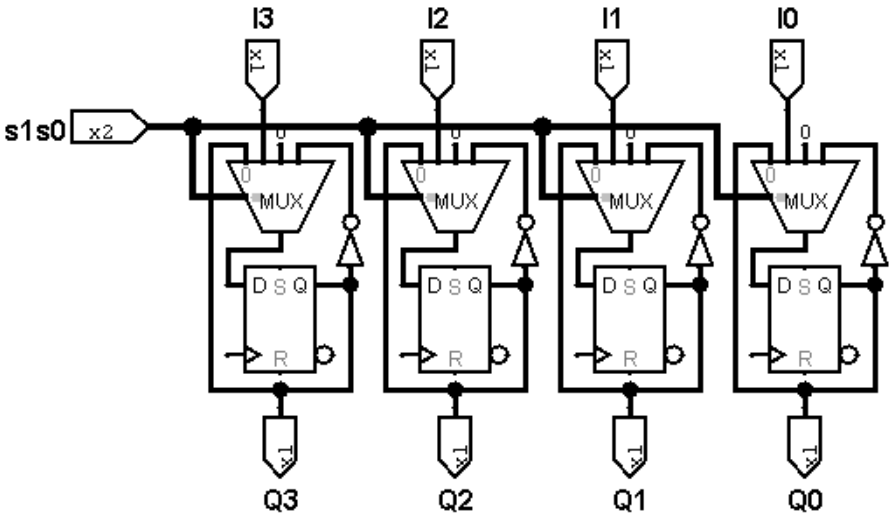


Figure 2: 4-bit Register

## 4.10

The maximum time delay for both the full adder and the half adder is 3 ns. Therefore, eight adders will have a total delay of 24 ns. However, the carry out of a half-adder will be correct after 2ns instead of 3ns. Since a half adder can be used to add the least significant bit of the numbers, the 8-bit sum will be correct by 23 ns.

## 4.13

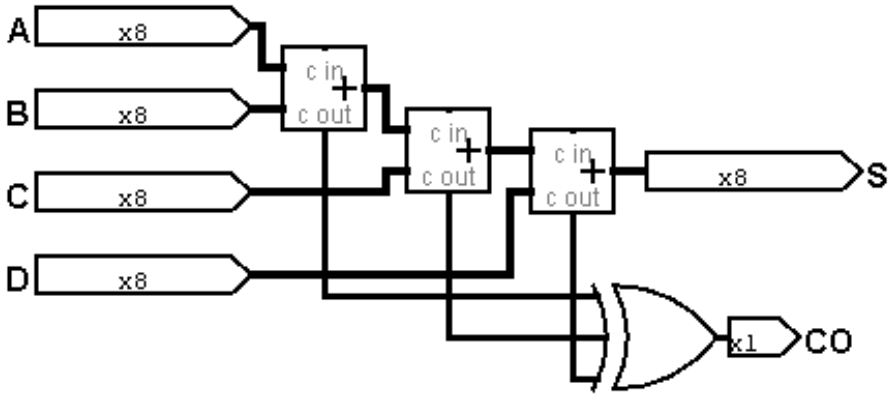


Figure 3: Quad 8-bit adder

## 4.21

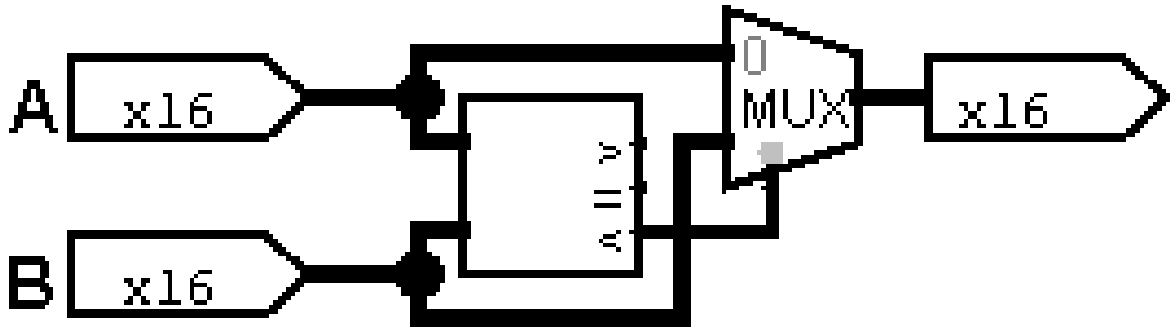


Figure 4: 16-bit Magnitude Comparator

## 4.30

(a) $11100000_2 = 32_{10}$

(b) $01111111_2 = 127_{10}$

(c) $11110000_2 = -16_{10}$

(d) $11000000_2 = -64_{10}$

(e) $11100000_2 = -32_{10}$

## 4.33

(a) $29_{10} = 00011101_2$

(b) $100_{10} = 01100100_2$

(c) $125_{10} = 01111101_2$

(d) $-29_{10} = 11100011_2$

(e) $-100_{10} = 10011100_2$

(f) $-125_{10} = 10000011_2$

(g) $-2_{10} = 11111110_2$

## 4.40

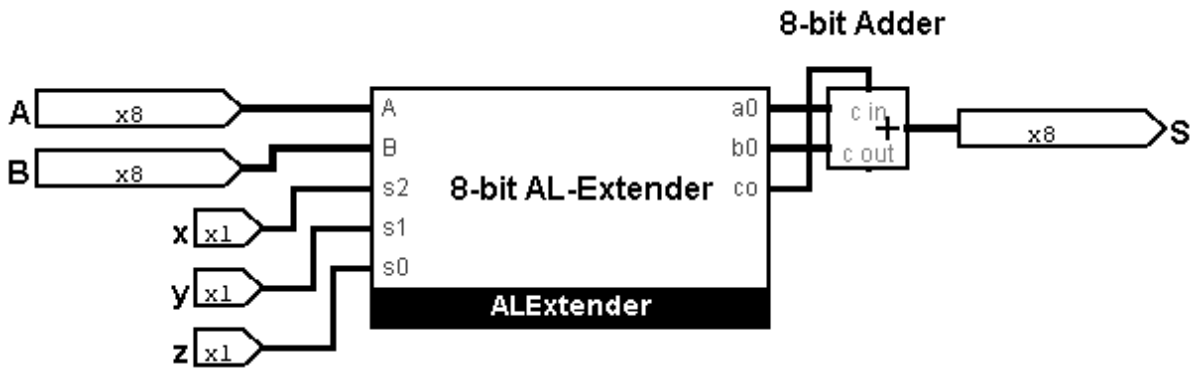


Figure 5: Arithmetic Logic Unit

Operation of the AL-Extender is as follows.

| $x$ | $y$ | $z$ | S | $a_o$ | $b_o$ | $c_o$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | $A - B$ | $a$ | $b'$ | 1 |
| 0 | 0 | 1 | $A + B$ | $a$ | $b$ | 0 |
| 0 | 1 | 0 | $A * 8$ | $a << 3$ | 0 | 0 |
| 0 | 1 | 0 | $A/8$ | $a >> 3$ | 0 | 0 |
| 1 | 0 | 0 | $A$ NAND $B$ | $a$ NAND $b$ | 0 | 0 |
| 1 | 0 | 1 | $A$ XOR $B$ | $a$ XOR $b$ | 0 | 0 |
| 1 | 1 | 0 | Reverse $A$ | $a$ reversed | 0 | 0 |
| 1 | 1 | 1 | NOT $A$ | NOT $a$ | 0 | 0 |

Table 1: AL Extender Functionality

## 4.62

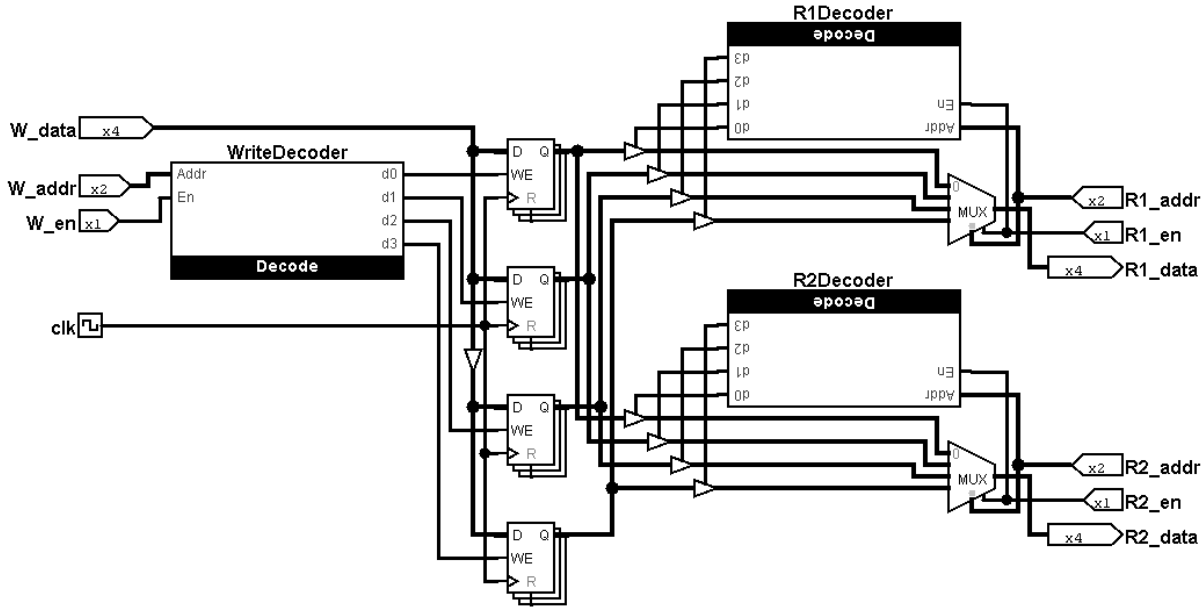


Figure 6: $4 \times 4$ Register File

## 4.64

(a) $W_{data} = 1110, W_{addr} = 11, W_{en} = 1, R_{addr} = 11, R_{en} = 1$

(b) Before rising edge.
$R_0 = 0101$
$R_1 = 0101$
$R_2 = 0101$
$R_3 = 0101$
$R_{data} = 0101$

After rising edge.
$R_0 = 0101$
$R_1 = 0101$
$R_2 = 0101$
$R_3 = 1110$
$R_{data} = 1110$