Lab 2 Report

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An Aggie does not lie, cheat or steal.
Nor does an Aggie tolerate those who do.

Problem 1

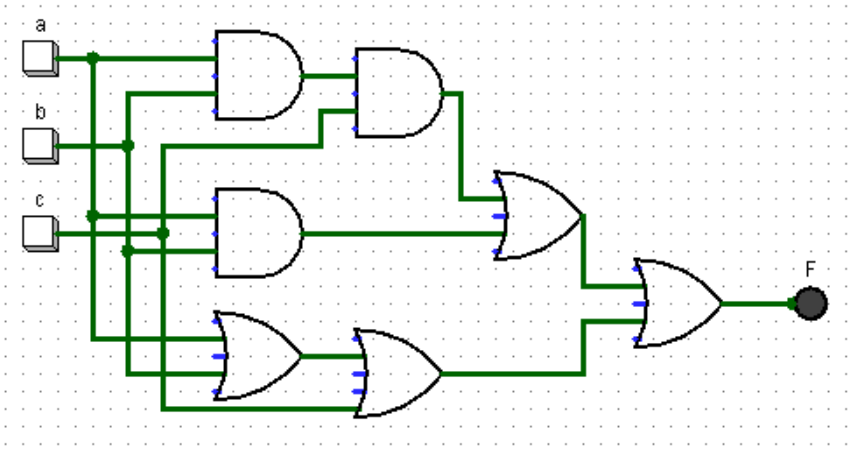

Figure 1: $F = abc + ab + a + b + c$

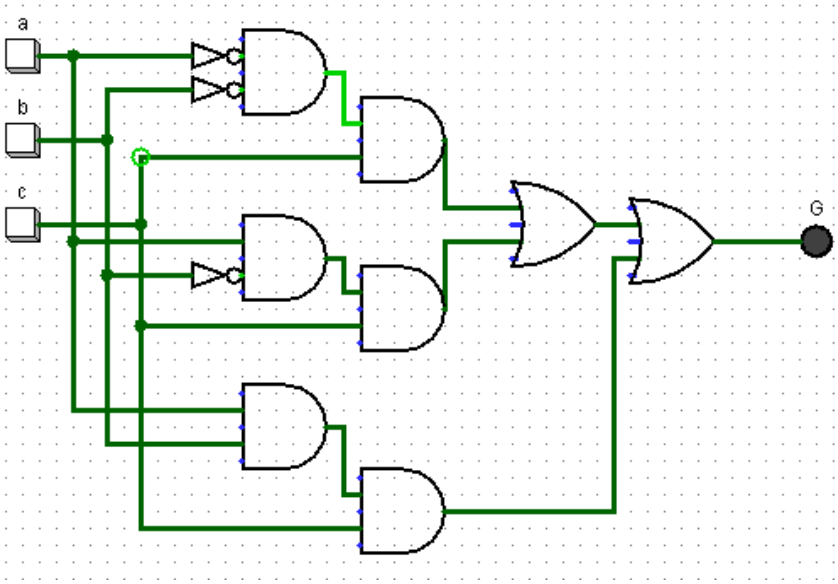

Figure 2: $G = a'b'c + ab'c + abc$

Chips used: 74LS04 inverter gate, 74LS08 quad 2-input AND gate, and 74LS32 quad 2-input OR gate.
To physically wire circuit F

Parameters:
$V_{cc} = 5V, T_A = 25°C, C_L = 15pF, R_L = 2k\Omega$
Maximum delay, for F would be $2t_{OR} + 2t_{AND}$. This is equivalent to $2(11) + 2(13) = 48ns$. Likewise for G, its time delay would be $t_{NOT} + 2t_{AND} + 2_{OR}$. This is equivalent to $10 + 2(13) + 2(11) = 58ns$.

The maximum delay under the indicated parameters would be 48 nanoseconds for Circuit F and 58 nanoseconds for Circuit G.

Problem 2