Lab 4 Report

Huy Lai — 132000359
Kyle Crusius — 428003578
Arjun Kurkal — 631004597
Vishnu Naidu — 630004567

Texas A&M University
20 October 2022

An Aggie does not lie, cheat or steal.
Nor does an Aggie tolerate those who do.

Problem 1

Our eternal thanks to Kevin Weston for enlightening our mortal brains with how the I/O Controller works

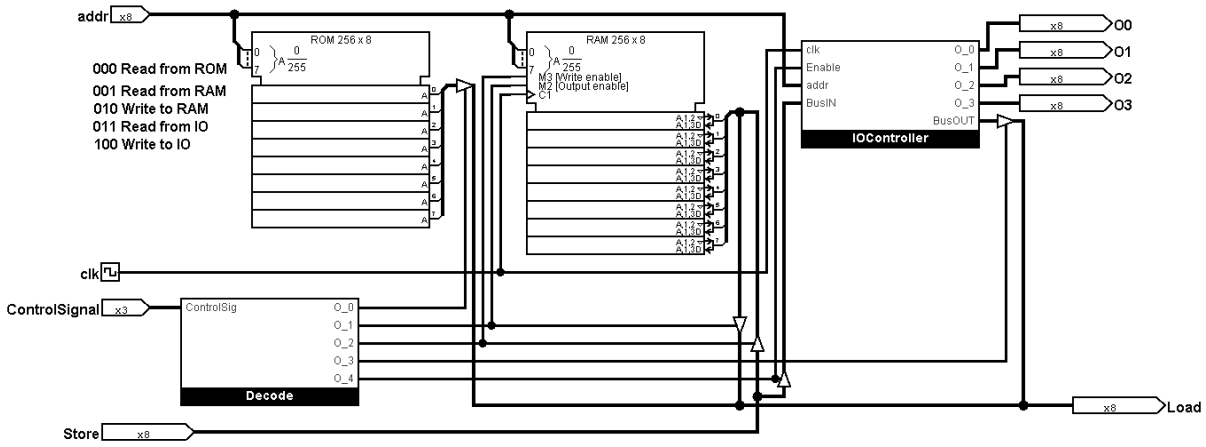


Figure 1: Microprocessor

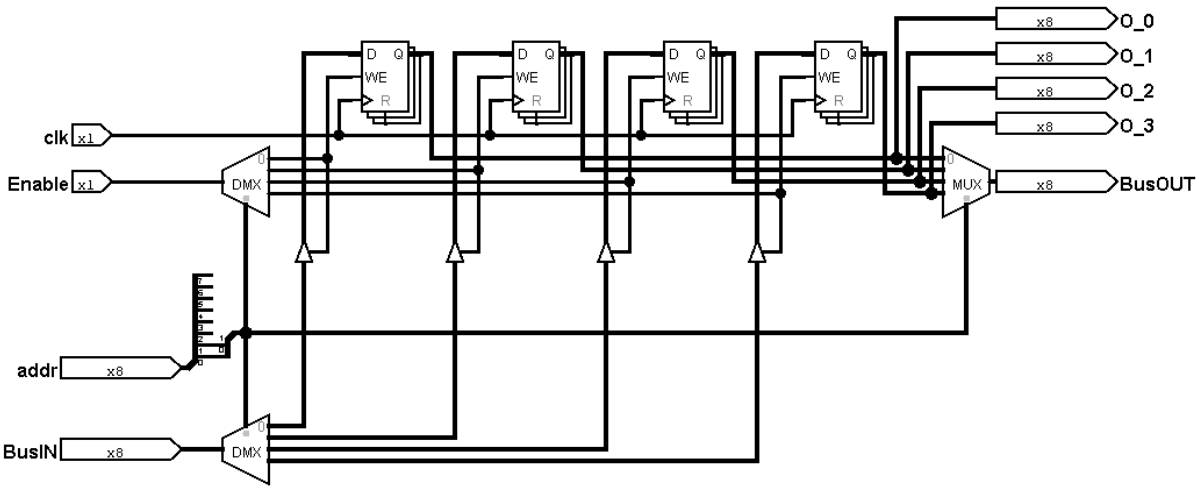


Figure 2: I/O Controller

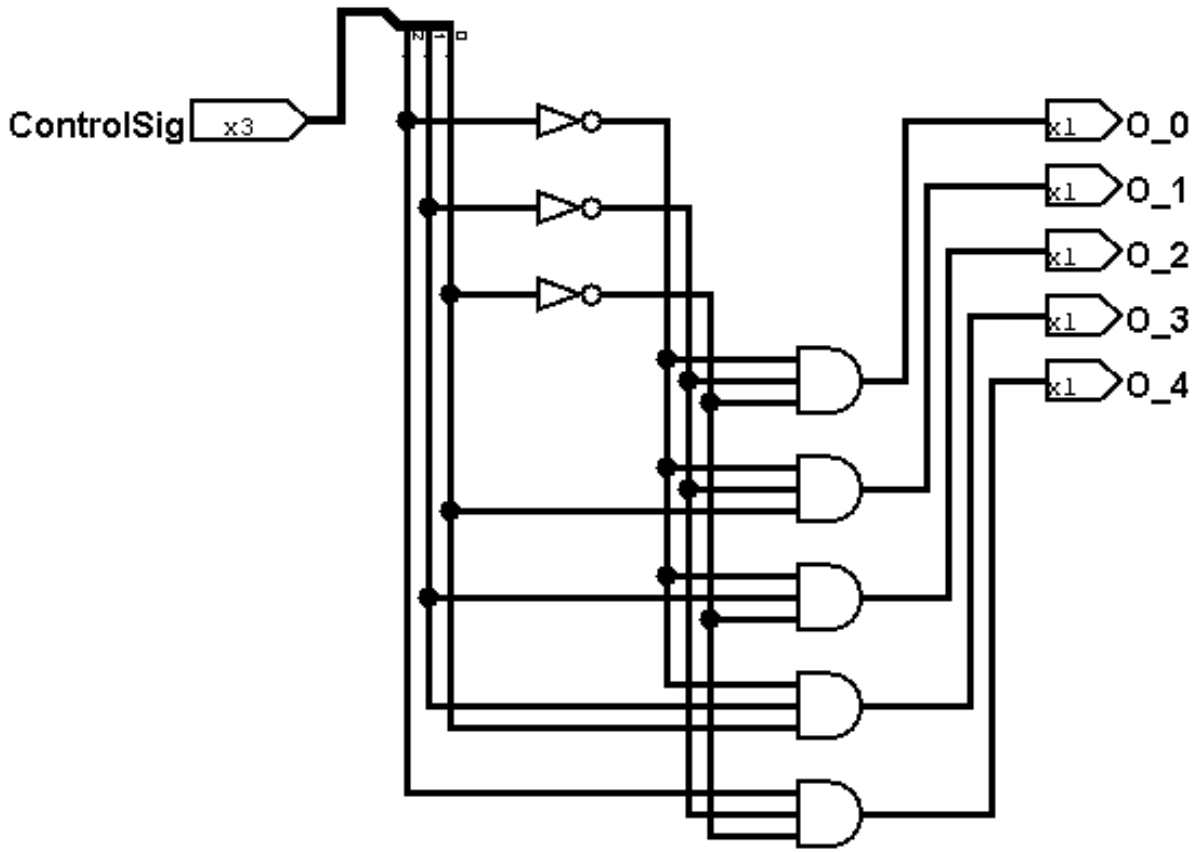


Figure 3: Decoder

Problem 2

Eight-bit Adder

The full 8-bit adder is implemented using eight 1-bit adders (arranged as ripple-carry).

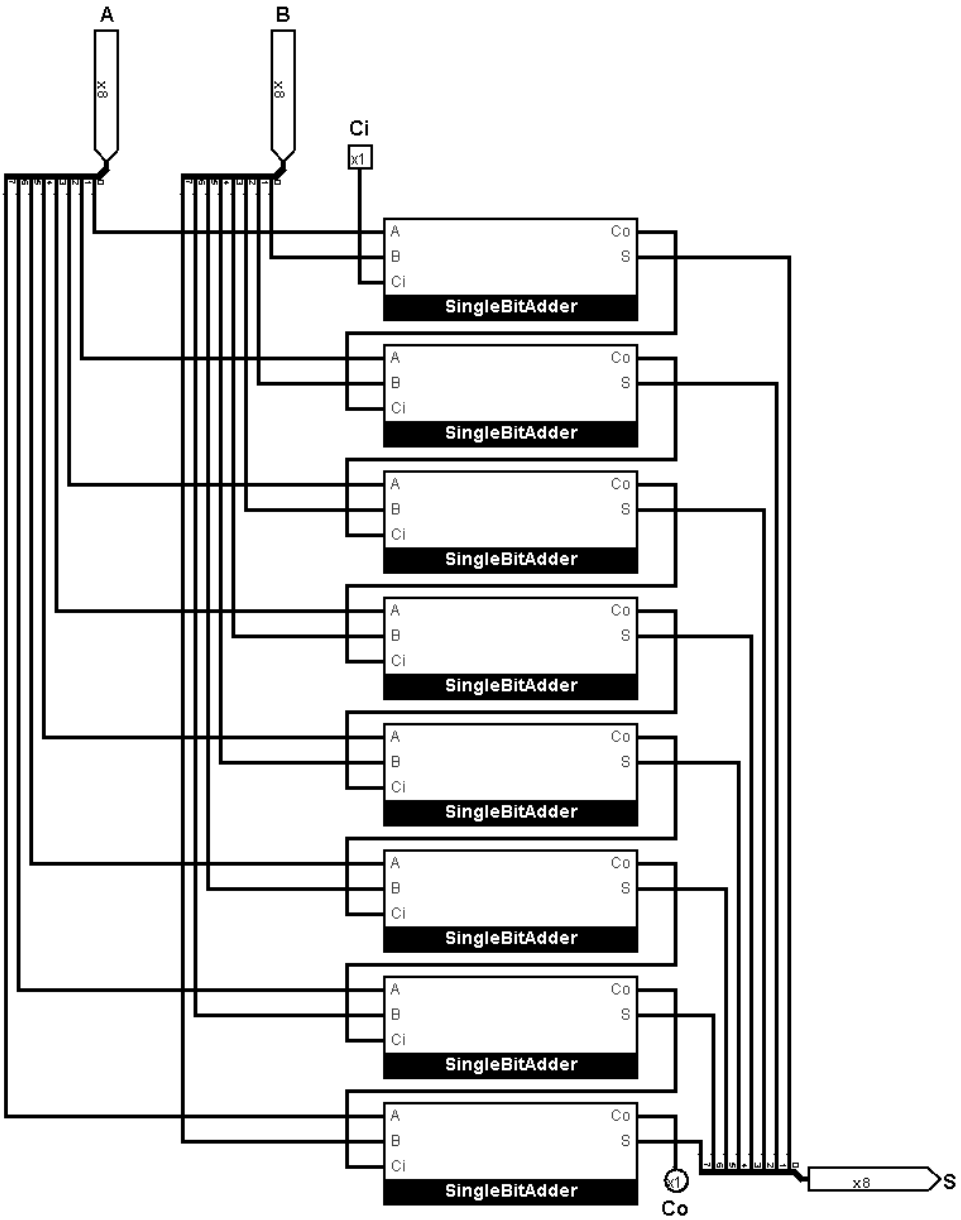


Figure 4: 8-bit Adder

Each single bit adder receives three inputs (A, B, C_i), and returns:
$S = A \oplus B \oplus C_i$
$C_o = AB + AC_i + BC_i$

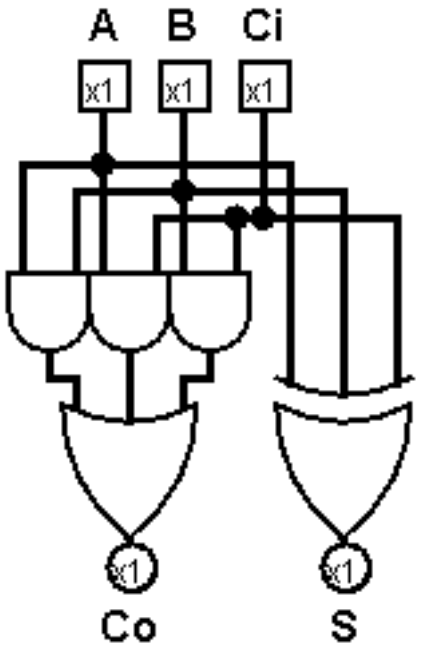


Figure 5: 1-bit Full Adder

Eight-bit Subtractor

The 8-bit subtractor is implemented using two's complement. Input B is inverted, and a constant value of `0x1` is supplied to the Carry-In input of the adder. The Carry-Out bit is not utilized.

Figure 6: 8-bit Subtractor

Eight-bit Magnitude Comparitor

The Magnitude comparator is implemented using eight 1-bit comparators connected from most significant bit to least significant.
A value of `010` is initially loaded into the first comparitor.

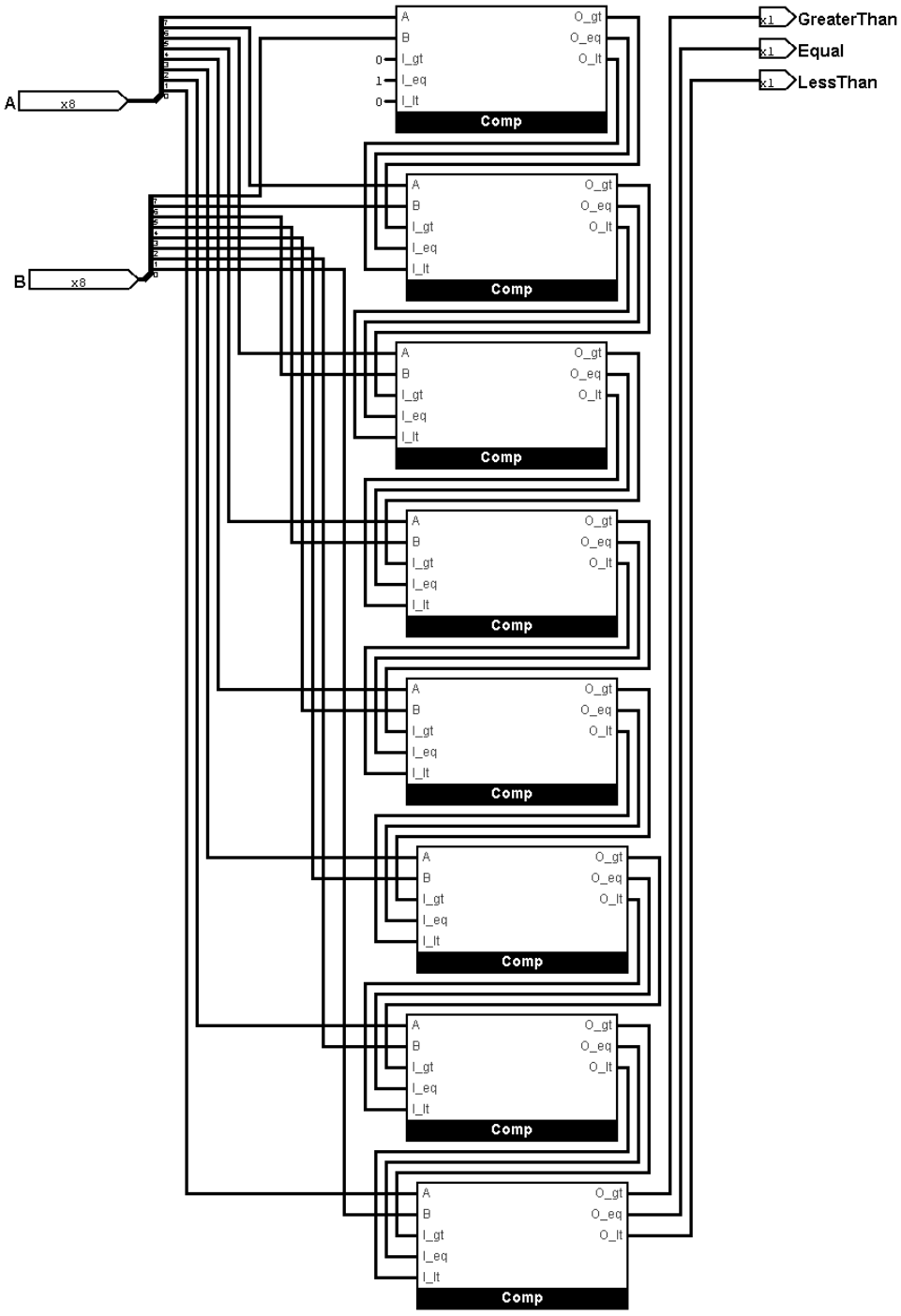


Figure 7: 8-bit Comparitor

Each single-bit comparitor received five inputs ($A, B, I_{gt}, I_{eq}, I_{lt}$), and returns:
$O_{gt} = I_{gt} + I_{eq}AB'$
$O_{eq} = I_{eq} \cdot (A \oplus B)'$
$O_{lt} = I_{lt} + I_{eq}A'B$

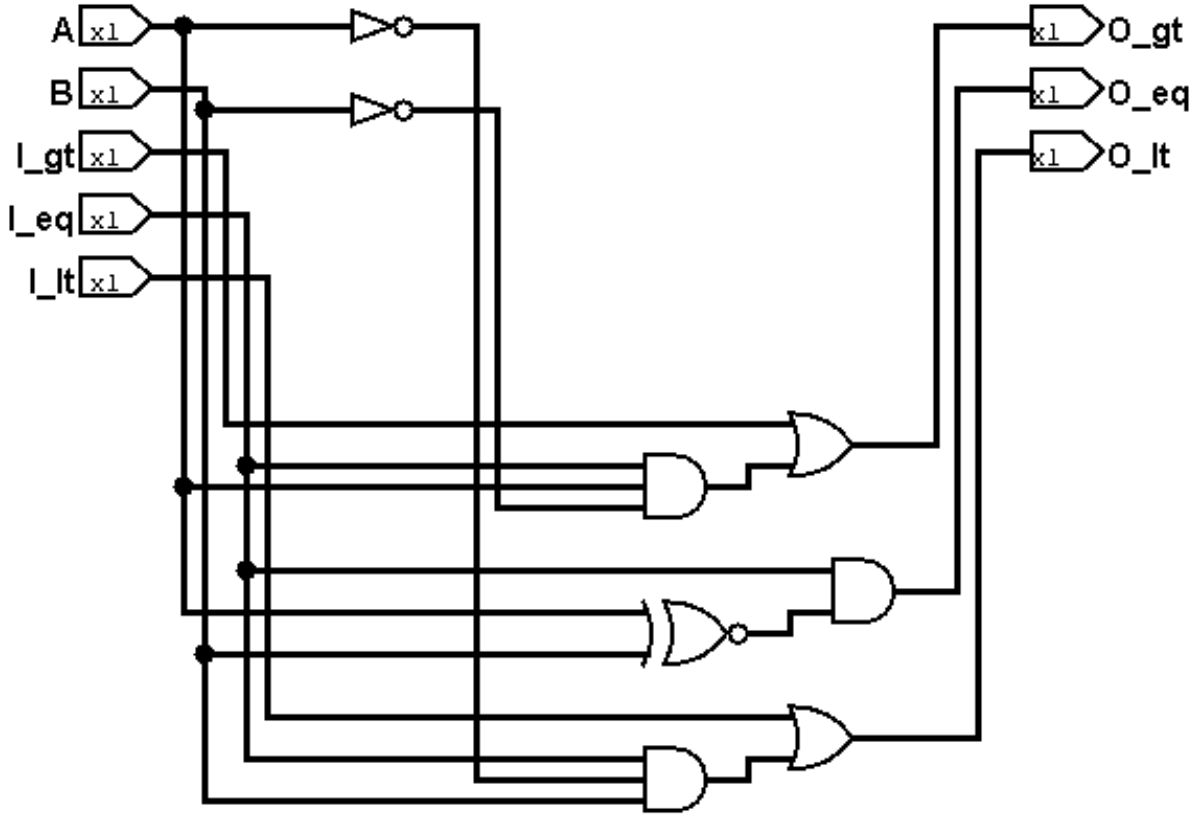


Figure 8: 1-bit Comparitor

The Eight-bit left shifter is composed of seven one-bit shifters.
Additionally, a 3×8 Decoder in order to shift more than one bit.

Eight-bit Left Shifter

Figure 9: 8-bit Left Shifter

The one-bit shifter will shift the input value by one bit. When Shift is set high, the inputed value will be shifted.

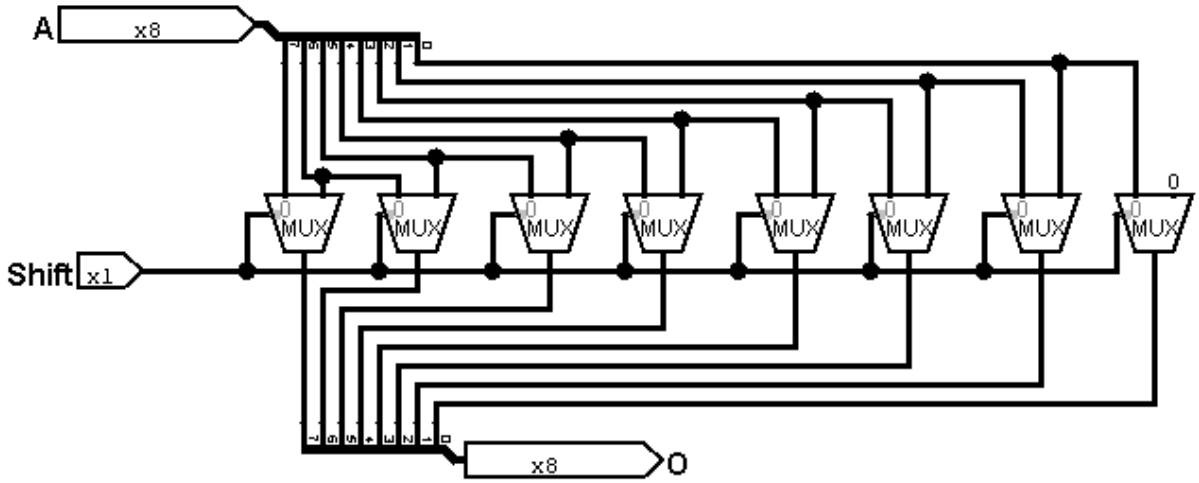


Figure 10: 1-bit Left Shifter

The decoder will allow more than one shifter to be active at once. When O_n are set high all outputs from O_1 to O_n are also set high.

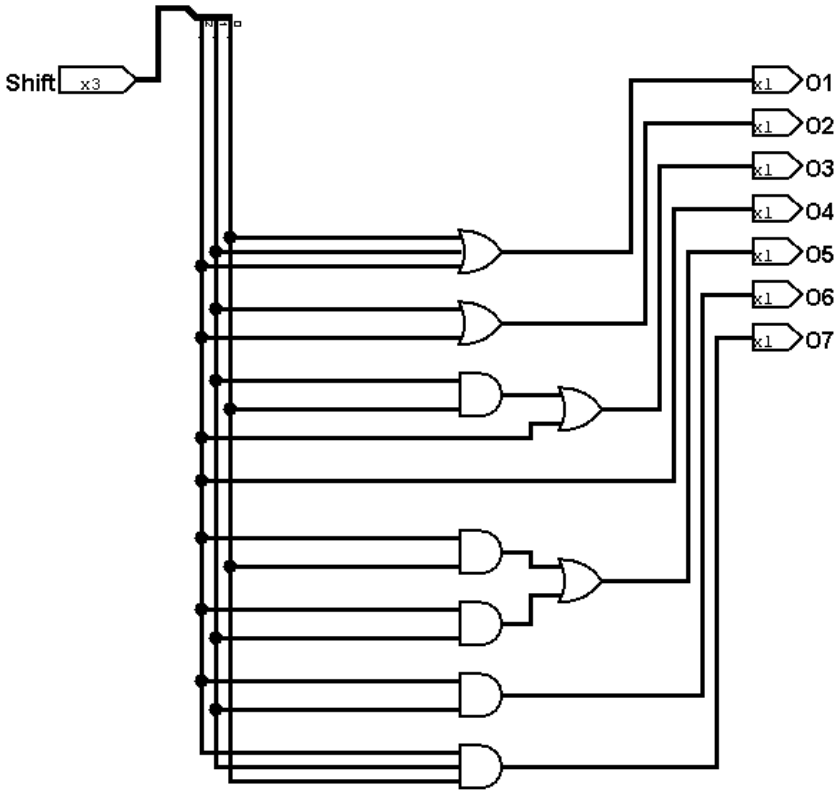


Figure 11: 3×7 Decoder

The eight-bit right shifter works similar to the left shifter. However, it has an extra mode for arithmetic or logical shifting. When the Arithmetic pin is set high, the right shifter will be set to arithmetic mode. When this pin is low, logical shifting will be active.

Eight-bit Right Shifter

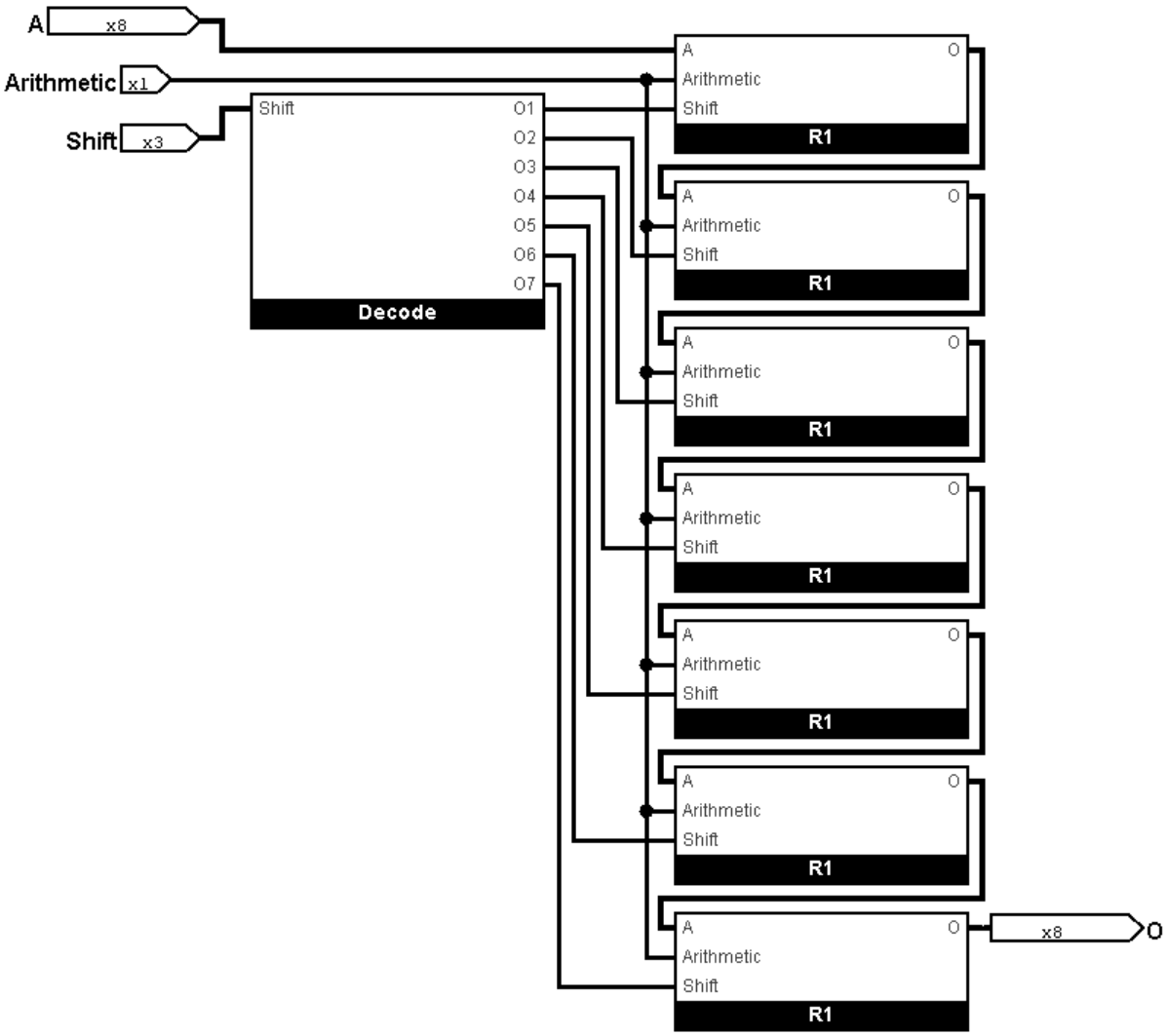


Figure 12: 8-bit Right Shifter with Arithmetic/Logical Switch

The one-bit right shifter will shift the input value by one bit. There is also an additional arithmetic mode where the shifter will arithmetically shift instead of logically shifting.

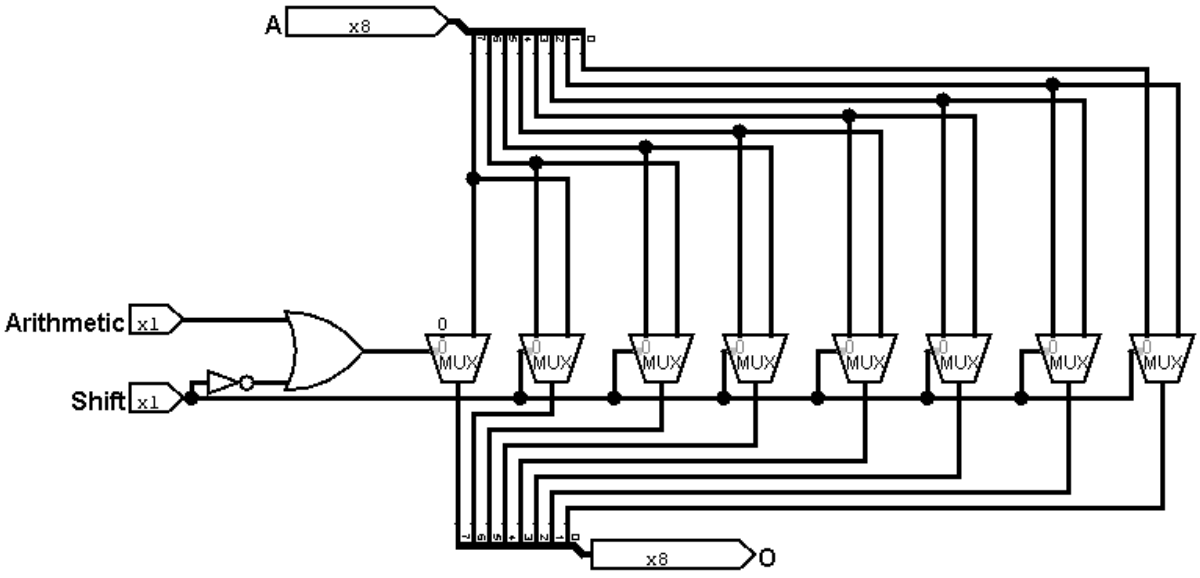
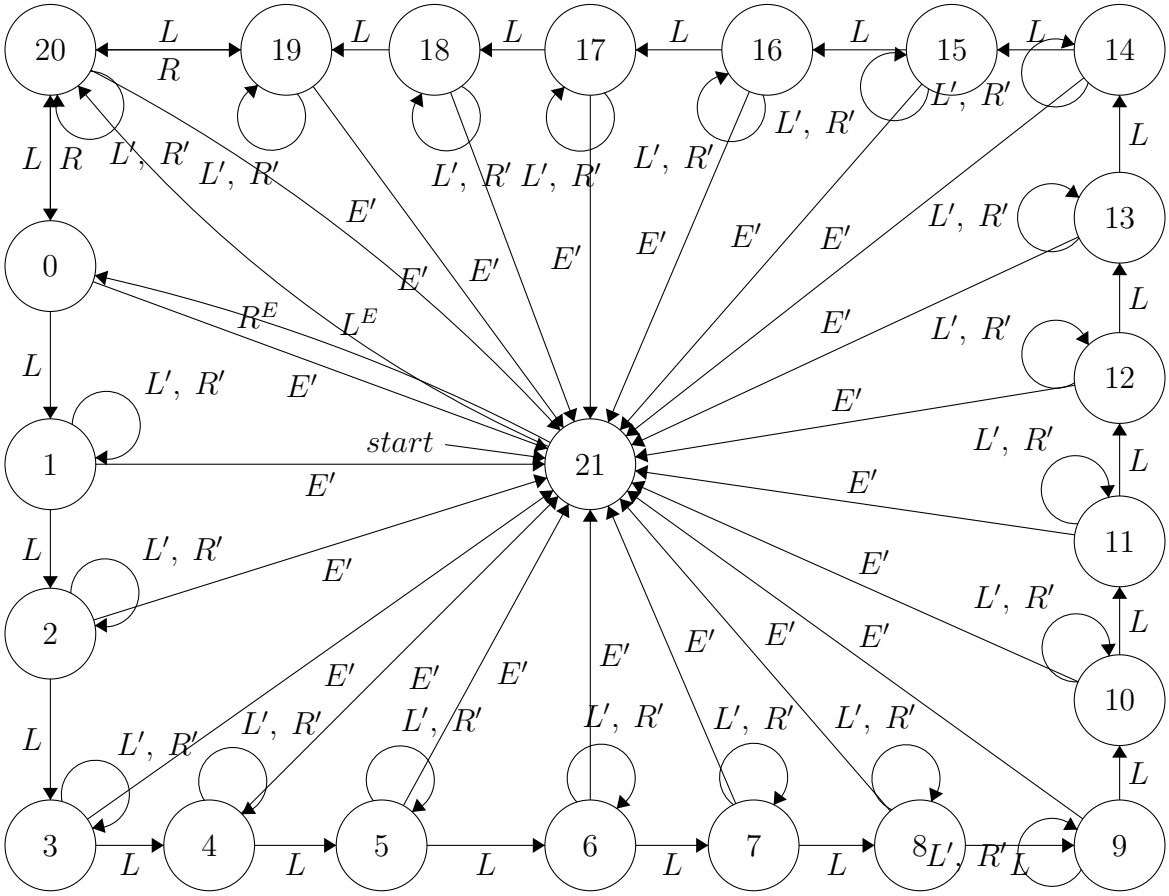


Figure 13: 1-bit Right Shifter

Problem 3



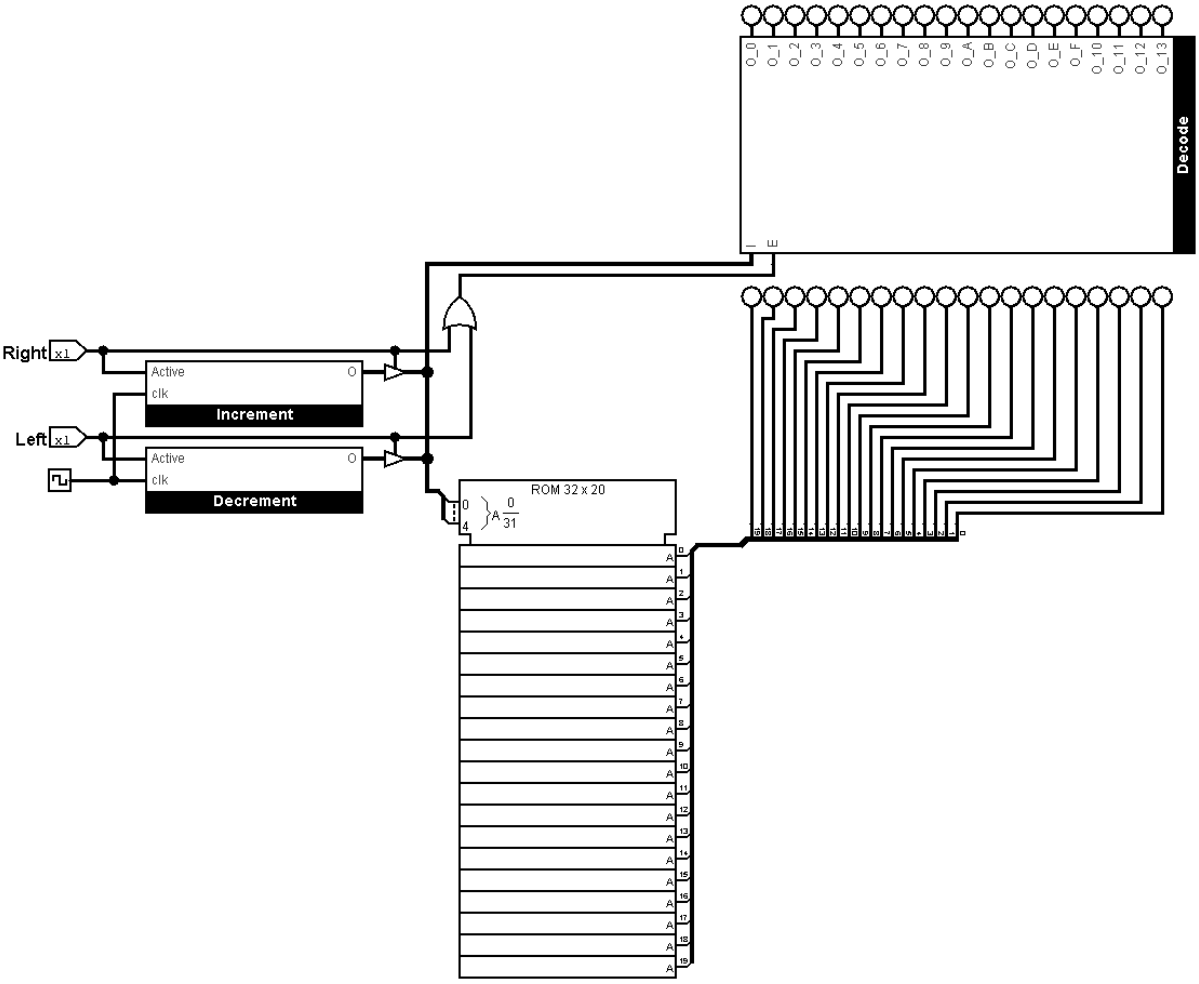


Figure 14: Blinker

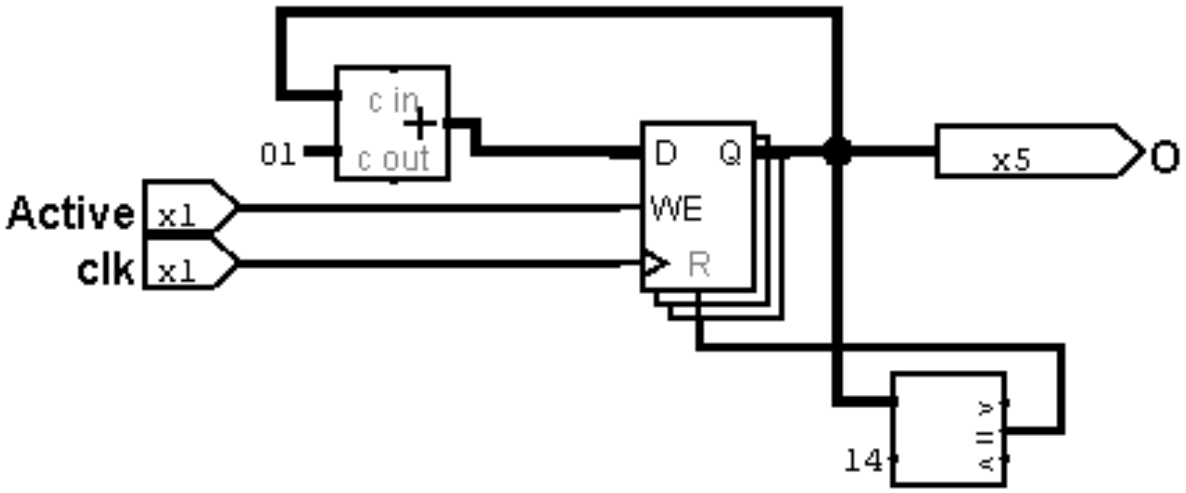


Figure 15: Incrementer

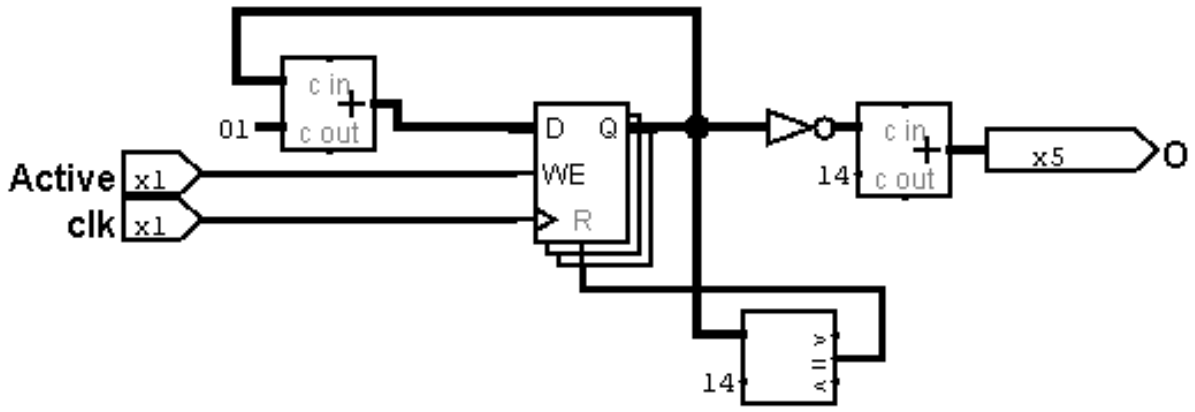


Figure 16: Decrementer

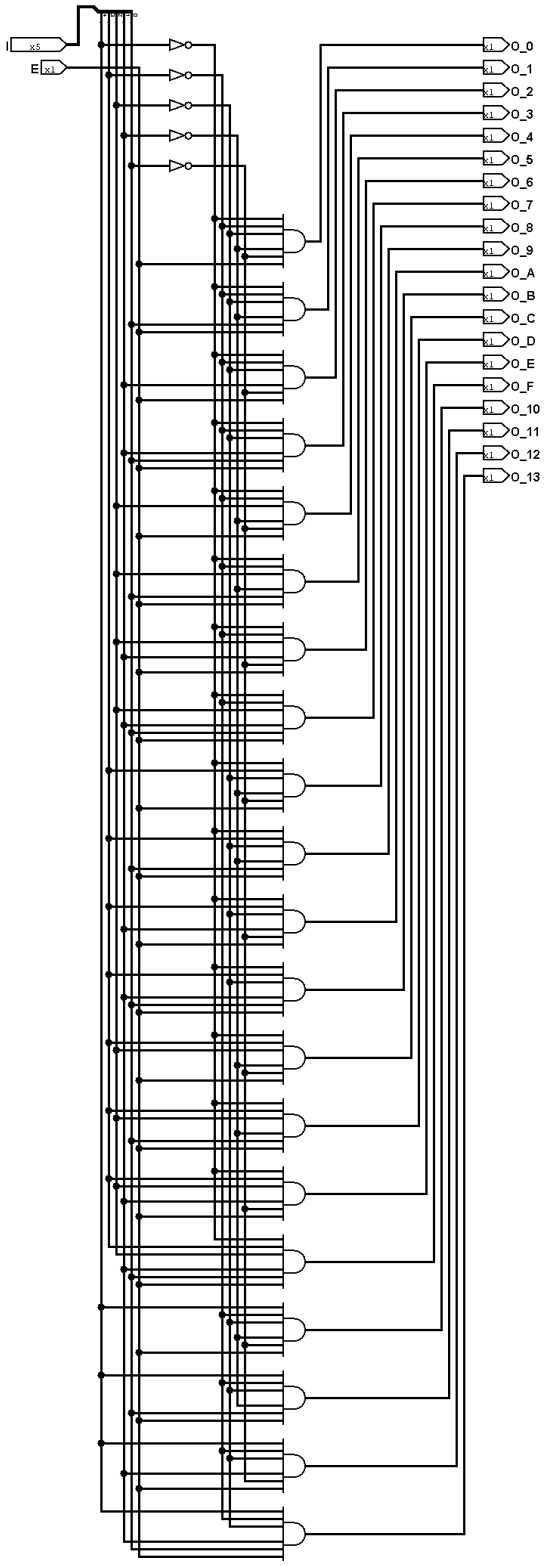


Figure 17: 5×20 Decoder