



Datasheet

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Version 1.1

2016/03



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1 GENERAL DESCRIPTION

The ST7701, a 16.7M-color System-on-Chip (SOC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 480RGBX864 in resolution which can transmit graphic data without RAM. The 480-channel source driver has true 8-bit resolution, which generates 256 Gamma-corrected values by an internal D/A converter.

The ST7701 is able to operate with low IO interface power supply and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver. The built-in timing controller in ST7701 can support several interfaces for the diverse request of medium or small size portable display.ST7701 provides several system interfaces ,which include MIPI/RGB/SPI/I2C.For further power control ,the dynamic backlight control function basing on displaying image content is also supported.



2 FEATURES

- Single chip WVGA a-Si TFT-LCD Controller/Driver without Display RAM
- Display Resolution
 - 480*RGB (H) *1024(V)
 - 480*RGB (H) *864(V) (WVGA)
 - 480*RGB (H) *854(V)
 - 480*RGB (H) *800(V)
 - 480*RGB (H) *720(V)
 - 480*RGB (H) *640(V) (VGA)
 - 480*RGB (H) *360(V)
- LCD Driver Output Circuits
 - Source Outputs: 480 RGB Channels
 - Support gate control signals to gate driver in the panel
 - Common Electrode Output
- Display Colors (Color Mode)
 - Full Color mode: 16.7M-colors, RGB=(888) max., Idle Mode Off
 - Reduce color mode: 262K colors
 - Reduce color mode: 65K colors
 - Idle Mode: 8-color, RGB=(111)
- Programmable Pixel Color Format (Color Depth) for Various Display Data input Format
 - 24-bit/pixel: RGB=(888)
 - 18-bit/pixel: RGB=(666)
 - 16-bit/pixel: RGB=(565)
- Display Interface
 - 8 bit,9bit and 16 bit serial peripheral interface
 - 16/18/24 RGB Interface(VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0], Sync and DE mode)
 - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)

Supports one data lane / maximum speed 800Mbps

- Supports two data lanes / maximum speed 550Mbps
- I2C Interface
- Display Features
 - Programmable Partial Display Duty
 - CABC for saving current consumption
 - Color enhancement
- On Chip Build-In Circuits
 - DC/DC Converter
 - Adjustable VCOM Generation



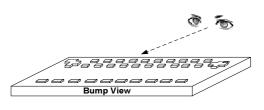
- Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
- Timing Controller
- 4 preset Gamma curve with separated RGB Gamma setting
- Build-In NV Memory for LCD Initial Register Setting
 - OTP to store VCOM and ID1~ID3
- Driving Algorithm Support
 - 1-dot/2-dot/3-dot/4-dot Inversion
 - Column Inversion
 - Zigzag Inversion
- Wide Supply Voltage Range
 - I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V (VDDI≤VDD)
 - Analog Voltage (VDDA to AGND): 2.5V ~ 3.6V
 - MIPI Voltage (VDDAM to VSSAM): 2.5V ~ 3.6V
- On-Chip Power System
 - Source Voltage (VAP (GVDD) to VAN (GVCL)): +3.64~6.5V,-1.05~-5V
 - VCOM level: GND
 - Gate driver HIGH level (VGH to AGND): +11.5V ~ +18 V
 - Gate driver LOW level (VGL to AGND): -12V ~ -7.6V
- Optimized layout for COG Assembly
- Operate temperature range: -30°C to +85°C
- Lower Power Consumption

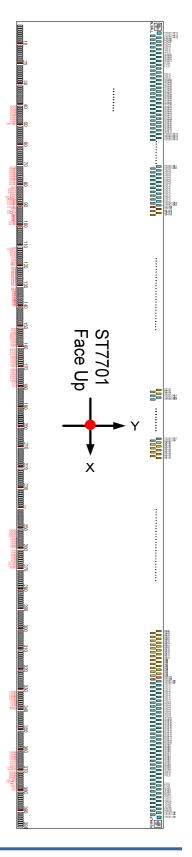


3 PAD ARRANGEMENT

3.1 Output Bump Dimension

Au bump height	9μm		
	14μmx95μm		
	Gate: GO1~GO32		
Au bump size	Source : S1~S1440		
	40μmx84μm		
	Input Pads: Pad 1 to Pad 398		

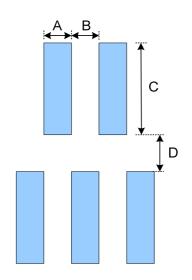






3.2 Input Bump Dimension

Output Pads



P400~P2076

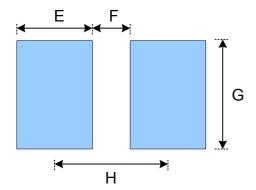
Symbol	Item	Size		
A	Bump Width	14 um		
В	Bump Gap 1 (Horizontal)	14 um		
С	Bump Height	95 um		
D	Bump Gap 2 (Vertical)	28 um		

P399 · P2077

Symbol	Item	Size
A	Bump Width	42 um
В	Bump Gap 1 (Horizontal)	14 um
С	Bump Height	95 um
D	Bump Gap 2 (Vertical)	28 um

Input Pads

No.1~398

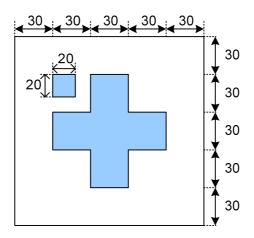


Symbol	Item	Size			
Е	Bump Width	40 um			
F	Bump Gap	20um			
G	Bump Height	84 um			
Н	Bump Pitch	60 um			

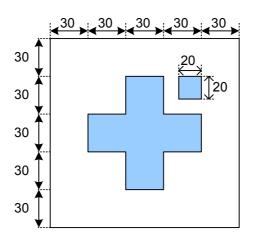


3.3 Alignment Mark Dimension

● Alignment Mark ALIGN_L : (X,Y)=(-11870,302)



Alignment Mark ALIGN_R: (X,Y)=(+11870,302)



3.4 Chip Information

Chip size	24000µm х800µm		
Chip thickness	250µm		
Pad Location	Pad center		
Coordinate Origin	Chip center		

Chip size included scribe line.

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4 PAD CENTER COORDINATES (AFTER HEAT CORRECTION)

PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y
1	VSSIDUM0	-11910	-315	33	DMY	-9990	-315	65	DGND	-8070	-315
2	VSSIDUM0	-11850	-315	34	VSSB	-9930	-315	66	VCC	-8010	-315
3	VSSIDUM1	-11790	-315	35	VSSB	-9870	-315	67	VCC	-7950	-315
4	PADA1	-11730	-315	36	VSSB	-9810	-315	68	VCC	-7890	-315
5	PADB1	-11670	-315	37	VSSB	-9750	-315	69	VDDB	-7830	-315
6	VCOM	-11610	-315	38	VDDB	-9690	-315	70	VDDB	-7770	-315
7	VCOM	-11550	-315	39	VDDB	-9630	-315	71	VDDB	-7710	-315
8	VCOM	-11490	-315	40	VDDB	-9570	-315	72	VSSB2	-7650	-315
9	VCOM	-11430	-315	41	VDDB	-9510	-315	73	VSSB2	-7590	-315
10	VCOM	-11370	-315	42	VDDB	-9450	-315	74	VSSB2	-7530	-315
11	CNTACT1	-11310	-315	43	VDDB	-9390	-315	75	VSSB2	-7470	-315
12	CNTACT1	-11250	-315	44	VDDB	-9330	-315	76	VSSB2	-7410	-315
13	VPP	-11190	-315	45	VDDB	-9270	-315	77	VSSB2	-7350	-315
14	VPP	-11130	-315	46	VSSB	-9210	-315	78	AGND	-7290	-315
15	VPP	-11070	-315	47	VSSB	-9150	-315	79	AGND	-7230	-315
16	VPP	-11010	-315	48	VSSB	-9090	-315	80	AGND	-7170	-315
17	VPP	-10950	-315	49	VSSB	-9030	-315	81	VDDI	-7110	-315
18	VGL	-10890	-315	50	TESTO[0]	-8970	-315	82	LANSEL	-7050	-315
19	VGL	-10830	-315	51	TESTO[1]	-8910	-315	83	DSWAP	-6990	-315
20	VGLO	-10770	-315	52	TESTO[2]	-8850	-315	84	PSWAP	-6930	-315
21	VGLO	-10710	-315	53	TESTO[3]	-8790	-315	85	DGND	-6870	-315
22	VGL_REG	-10650	-315	54	DMY	-8730	-315	86	DSTB_SEL	-6810	-315
23	VGL_REG	-10590	-315	55	DMY	-8670	-315	87	NBWSEL	-6750	-315
24	VGHEQ2	-10530	-315	56	DMY	-8610	-315	88	VGSW[3]	-6690	-315
25	VGHEQ2	-10470	-315	57	DMY	-8550	-315	89	VGSW[2]	-6630	-315
26	VSSB2	-10410	-315	58	DMY	-8490	-315	90	VGSW[1]	-6570	-315
27	VSSB2	-10350	-315	59	DMY	-8430	-315	91	VGSW[0]	-6510	-315
28	VSSB2	-10290	-315	60	DMY	-8370	-315	92	VDDI	-6450	-315
29	VSSB2	-10230	-315	61	DMY	-8310	-315	93	I2C_SA1	-6390	-315
30	DMY	-10170	-315	62	DMY	-8250	-315	94	I2C_SA0	-6330	-315
31	DMY	-10110	-315	63	DGND	-8190	-315	95	IM[3]	-6270	-315
32	DMY	-10050	-315	64	DGND	-8130	-315	96	IM[2]	-6210	-315

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98 IM(0) -6090 -315 132 D[10] -4050 -315 166 VSSB -2010 -315 99 GPO[3] -6030 -315 133 D[9] -3990 -315 167 VSSB -1950 -315 100 GPO[2] -5970 -315 134 D[8] -3930 -315 168 VSSB -1830 -315 101 GPO[1] -5910 -315 136 D[7] -3870 -315 169 VSSB -1830 -315 102 GPO[0] -5850 -315 136 D[6] -3810 -315 170 VDDA -1770 -315 103 EXBIT -5790 -315 138 D[6] -3810 -315 171 VDDA -1710 -315 104 TE_L -5730 -315 138 D[4] -3690 -315 172 VDDA -1650 -315 105 DMY -5670 -315 138 D[4] -3690 -315 172 VDDA -1650 -315 106 SDO -5610 -315 140 D[2] -3570 -315 174 DGND -1530 -315 107 SDA -5550 -315 141 D[1] -3510 -315 175 DGND -1470 -315 108 DCX -5490 -315 142 D[0] -3450 -315 176 DGND -1410 -315 109 SCL -5430 -315 144 DEL -3390 -315 178 VCC -1290 -315 110 RDX -5370 -315 146 VS -3210 -315 179 VCC -1230 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -11170 -315 114 DGND -5190 -315 148 LEDON -3090 -315 180 VCC -11170 -315 116 VDDI -4950 -315 150 ERR -2970 -315 180 VSM -990 -315 116 VDDI -4950 -315 150 ERR -2970 -315 180 VSM -930 -315 118 VDDI -4950 -315 150 ERR -2970 -315 180 VSM -930 -315 118 VDDI -4950 -315 150 DGND -2670 -315 180 DP1 -570 -315 122 D[2] -4770 -315 156 DGND -2670 -315 180 DP1 -570 -315 122 D[2] -4770 -315 156 DGND -2670 -315 180 DP1 -570 -315 122 D[2] -4770 -315 156 DGND -2670 -315 180 DP1 -570 -315 122 D[2] -4450 -315 156 DGND -2670 -315 180 DP1 -570 -315 122 D[2] -4450 -315 156 DGND -2670 -315 181 DNI -510 -315 122 D[2] -4450 -315 156 DGND -2670 -31												
98 IM(0]		PIN Name	х	Y		PIN Name	х	Y		PIN Name	х	Y
99 GPO[3] -6030 -315 133 D[9] -3990 -315 167 VSSB -1950 -315 100 GPO[2] -5970 -315 134 D[8] -3930 -315 168 VSSB -1890 -315 101 GPO[1] -5910 -315 136 D[7] -3870 -315 168 VSSB -1830 -315 102 GPO[0] -5850 -315 136 D[6] -3810 -315 170 VDDA -1770 -315 103 EXB1T -5790 -315 137 D[6] -3750 -315 171 VDDA -1710 -315 103 EXB1T -5790 -315 138 D[4] -3890 -315 172 VDDA -1660 -315 105 DMY -5670 -315 138 D[4] -3890 -315 172 VDDA -1660 -315 106 SDO -5610 -315 140 D[2] -3870 -315 174 DGND -1590 -315 107 SDA -5550 -315 141 D[1] -3510 -315 175 DGND -14470 -315 108 DCX -5490 -315 142 D[0] -3450 -315 177 DGND -1410 -315 110 RDX -5370 -315 144 PCLK -3330 -315 177 DGND -1410 -315 110 RDX -5370 -315 144 PCLK -3330 -315 179 VCC -1290 -315 111 CSX -5310 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5190 -315 146 VS -3210 -315 180 VCC -1170 -315 114 DGND -5190 -315 115 DGND -5190 -315 146 VS -3210 -315 180 VCC -1170 -315 117 DGND -5190 -315 147 DGND -5190 -315 148 LEDON -3090 -315 180 VCC -1170 -315 117 DGND -5190 -315 147 LEDPWM -3150 -315 180 VCC -1170 -315 117 DGND -5190 -315 149 DMY -3030 -315 182 VSSM -990 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 180 VSSM -990 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 180 VSSM -990 -315 118 VDDI -4950 -315 152 VDDI -2850 -315 187 DP1 -750 -315 119 D[2] -4770 -315 155 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4770 -315 155 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4770 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4770 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4760 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122 D[2] -4650 -315 156 DGND -2670 -315 189 DP1 -690 -315 122	97	IM[1]	-6150	-315	131	D[11]	-4110	-315	165	VSSB	-2070	-315
100 GPO[2] -5970 -315 134 D[8] -3930 -315 168 VSSB -1890 -315 101 GPO[1] -5910 -315 135 D[7] -3870 -315 169 VSSB -1830 -315 102 GPO[0] -5850 -315 138 D[6] -3810 -315 170 VDDA -1770 -315 103 EXBIT -5790 -315 137 D[5] -3750 -315 171 VDDA -1710 -315 104 TE_L -5730 -315 138 D[4] -38690 -315 172 VDDA -1650 -315 105 DMY -5670 -315 138 D[4] -38690 -315 173 VDDA -1590 -315 108 SDO -5610 -315 140 D[2] -3570 -315 174 DGND -1530 -315 107 SDA -5550 -315 141 D[1] -3510 -315 175 DGND -1470 -315 108 DCX -5490 -315 142 D[0] -3450 -315 176 DGND -1410 -315 109 SCL -5430 -315 143 DE -3390 -315 177 DGND -1350 -315 110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 145 HS -3270 -315 179 VCC -1230 -315 112 RESETX -5250 -315 148 LEDON -3090 -315 180 VCC -1170 -315 114 DGND -5190 -315 148 LEDON -3090 -315 181 VCC -1110 -315 115 DGND -5190 -315 150 ERR -2970 -315 184 VSSM -990 -315 117 VDDI -4950 -315 150 ERR -2970 -315 186 VSSM -870 -315 119 D[2] -4770 -315 154 DGND -2790 -315 188 DP1 -690 -315 120 D[22] -4770 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 155 DGND -2670 -315 190 DP1 -570 -315 122 D[20] -4650 -315 156 DGND -2650 -315 191 DN1 -510 -315 122 D[20] -4650 -315 155 DGND -2650 -315 191 DN1 -510 -315 122 D[20] -4650 -315 155 DGND -2650 -315 191 DN1 -510 -315 135 DN1 -570 -315 -	98	IM[0]	-6090	-315	132	D[10]	-4050	-315	166	VSSB	-2010	-315
101	99	GPO[3]	-6030	-315	133	D[9]	-3990	-315	167	VSSB	-1950	-315
102 GPO[0] -5850 -315 136 D[6] -3810 -315 170 VDDA -1770 -315 103 EXBIT -5790 -315 137 D[5] -3750 -315 171 VDDA -1710 -315 104 TE_L -5730 -315 138 D[4] -3690 -315 172 VDDA -1650 -315 105 DMY -5670 -315 139 D[3] -3630 -315 173 VDDA -1650 -315 106 SDO -5610 -315 140 D[2] -3570 -315 174 DGND -1530 -315 107 SDA -5550 -315 141 D[1] -3510 -315 175 DGND -1470 -315 108 DCX -5490 -315 142 D[0] -3450 -315 176 DGND -1410 -315 109 SCL -5430 -315 143 DE -3390 -315 177 DGND -1350 -315 110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 145 HS -3270 -315 180 VCC -11230 -315 113 DGND -5130 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 116 VDDI -5070 -315 150 ERR -2970 -315 184 VSSM -990 -315 118 VDDI -4890 -315 153 VDDI -22910 -315 186 VSSM -870 -315 120 D[22] -4770 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 157 VDDB -22550 -315 191 DN1 -510 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 191 DN1 -510 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 191 DN1 -510 -315 152 DGND -2670 -315 191 DN1 -570 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 191 DN1 -510 -315 150 DGND -22550 -315 191 DN1 -510 -315 152 DGND -22550 -315 191 DN1 -510	100	GPO[2]	-5970	-315	134	D[8]	-3930	-315	168	VSSB	-1890	-315
103	101	GPO[1]	-5910	-315	135	D[7]	-3870	-315	169	VSSB	-1830	-315
104 TE_L .5730 .315 138 D[4] .3690 .315 172 VDDA .1650 .315 105 DMY .5670 .315 139 D[3] .3630 .315 173 VDDA .1590 .315 106 SDO .5610 .315 140 D[2] .3570 .315 174 DGND .1530 .315 107 SDA .5550 .315 141 D[1] .3510 .315 175 DGND .1470 .315 108 DCX .5490 .315 142 D[0] .3450 .315 176 DGND .1410 .315 109 SCL .5430 .315 143 DE .3390 .315 177 DGND .1350 .315 110 RDX .5370 .315 144 PCLK .3330 .315 178 VCC .1290 .315 111 CSX .5310 .315 145 HS .3270 .315 179 VCC .1230 .315 112 RESETX .5250 .315 146 VS .3210 .315 180 VCC .1110 .315 114 DGND .5130 .315 148 LEDON .3090 .315 181 VCC .1110 .315 115 DGND .5070 .315 149 DMY .3030 .315 183 VSSM .990 .315 116 VDDI .5010 .315 151 VDDI .2910 .315 186 VSSM .870 .315 118 VDDI .4890 .315 153 VDDI .2850 .315 188 DP1 .630 .315 122 D[20] .4650 .315 156 DGND .2670 .315 190 DP1 .570 .315 123 D[19] .4590 .315 157 VDDB .2250 .315 190 DP1 .570 .315 123 D[19] .4590 .315 157 VDDB .2250 .315 191 DN1 .510 .315 .	102	GPO[0]	-5850	-315	136	D[6]	-3810	-315	170	VDDA	-1770	-315
105 DMY -5670 -315 139 D[3] -3630 -315 173 VDDA -1590 -315 106 SDO -5610 -315 140 D[2] -3570 -315 174 DGND -1530 -315 107 SDA -5550 -315 141 D[1] -3510 -315 175 DGND -1470 -315 108 DCX -5490 -315 142 D[0] -3450 -315 176 DGND -1410 -315 109 SCL -5430 -315 143 DE -3390 -315 177 DGND -1350 -315 110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 145 HS -3270 -315 179 VCC -1230 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5130 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 115 DGND -5070 -315 149 DMY -3030 -315 182 VSSM -990 -315 116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -930 -315 118 VDDI -4950 -315 151 VDDI -2850 -315 186 VSSM -870 -315 118 VDDI -4890 -315 153 VDDI -22850 -315 188 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -22610 -315 189 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 191 DN1 -510 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 190 DP1 -570 -315 133 D[19] -4590 -315 157 VDDB -22550 -315 191 DN1 -510 -315 150 DN1 -570 -315 150 DN1 -2250 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -22550 -315 191 DN1 -510 -315 150 DN1 -570	103	EXB1T	-5790	-315	137	D[5]	-3750	-315	171	VDDA	-1710	-315
106 SDO -5610 -315 140 D[2] -3570 -315 174 DGND -1530 -315 107 SDA -5550 -315 141 D[1] -3510 -315 175 DGND -1470 -315 108 DCX -5490 -315 142 D[0] -3450 -315 176 DGND -1410 -315 109 SCL -5430 -315 143 DE -3390 -315 177 DGND -1350 -315 110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 146 VS -3270 -315 180 VCC -11290 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5190 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 116 VDDI -5070 -315 149 DMY -3030 -315 183 VSSM -990 -315 116 VDDI -4950 -315 151 VDDI -2910 -315 186 VSSM -870 -315 118 VDDI -4890 -315 152 VDDI -2850 -315 186 VSSM -810 -315 120 D[22] -4770 -315 154 DGND -2670 -315 189 DP1 -690 -315 121 D[21] -4710 -315 156 DGND -2670 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315 133 DI19 DN1 -510 -315 DN1 DN1 -510	104	TE_L	-5730	-315	138	D[4]	-3690	-315	172	VDDA	-1650	-315
107 SDA -5550 -315 141 D[1] -3510 -315 175 DGND -1470 -315 108 DCX -5490 -315 142 D[0] -3450 -315 176 DGND -1410 -315 109 SCL -5430 -315 143 DE -3390 -315 177 DGND -1350 -315 110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 145 HS -3270 -315 179 VCC -1230 -315 111 CSX -5310 -315 146 VS -3210 -315 180 VCC -1170 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1110 -315 113 DGND -5190	105	DMY	-5670	-315	139	D[3]	-3630	-315	173	VDDA	-1590	-315
108 DCX -5490 -315 142 D[0] -3450 -315 176 DGND -1410 -315 109 SCL -5430 -315 143 DE -3390 -315 177 DGND -1350 -315 110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 145 HS -3270 -315 179 VCC -1230 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5190 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 115 DGND -5070 <td>106</td> <td>SDO</td> <td>-5610</td> <td>-315</td> <td>140</td> <td>D[2]</td> <td>-3570</td> <td>-315</td> <td>174</td> <td>DGND</td> <td>-1530</td> <td>-315</td>	106	SDO	-5610	-315	140	D[2]	-3570	-315	174	DGND	-1530	-315
109 SCL -5430 -315 143 DE -3390 -315 177 DGND -1350 -315 110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 145 HS -3270 -315 179 VCC -1230 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5190 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 115 DGND -5070 -315 149 DMY -3030 -315 183 VSSM -990 -315 116 VDDI -5010 <td>107</td> <td>SDA</td> <td>-5550</td> <td>-315</td> <td>141</td> <td>D[1]</td> <td>-3510</td> <td>-315</td> <td>175</td> <td>DGND</td> <td>-1470</td> <td>-315</td>	107	SDA	-5550	-315	141	D[1]	-3510	-315	175	DGND	-1470	-315
110 RDX -5370 -315 144 PCLK -3330 -315 178 VCC -1290 -315 111 CSX -5310 -315 145 HS -3270 -315 179 VCC -1230 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5190 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 115 DGND -5070 -315 149 DMY -3030 -315 182 VSSM -1050 -315 116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -930 -315 117 VDDI -4950 </td <td>108</td> <td>DCX</td> <td>-5490</td> <td>-315</td> <td>142</td> <td>D[0]</td> <td>-3450</td> <td>-315</td> <td>176</td> <td>DGND</td> <td>-1410</td> <td>-315</td>	108	DCX	-5490	-315	142	D[0]	-3450	-315	176	DGND	-1410	-315
111 CSX -5310 -315 145 HS -3270 -315 179 VCC -1230 -315 112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5190 -315 147 LEDPWM -3150 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 115 DGND -5070 -315 149 DMY -3030 -315 182 VSSM -990 -315 116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -990 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 185 VSSM -870 -315 118 VDDI -4890 -315 </td <td>109</td> <td>SCL</td> <td>-5430</td> <td>-315</td> <td>143</td> <td>DE</td> <td>-3390</td> <td>-315</td> <td>177</td> <td>DGND</td> <td>-1350</td> <td>-315</td>	109	SCL	-5430	-315	143	DE	-3390	-315	177	DGND	-1350	-315
112 RESETX -5250 -315 146 VS -3210 -315 180 VCC -1170 -315 113 DGND -5190 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 115 DGND -5070 -315 149 DMY -3030 -315 183 VSSM -990 -315 116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -930 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 185 VSSM -870 -315 118 VDDI -4890 -315 152 VDDI -2850 -315 186 VSSM -810 -315 119 D[23] -48	110	RDX	-5370	-315	144	PCLK	-3330	-315	178	VCC	-1290	-315
113 DGND -5190 -315 147 LEDPWM -3150 -315 181 VCC -1110 -315 114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 115 DGND -5070 -315 149 DMY -3030 -315 183 VSSM -990 -315 116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -930 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 185 VSSM -870 -315 118 VDDI -4950 -315 152 VDDI -2850 -315 186 VSSM -870 -315 118 VDDI -4890 -315 153 VDDI -2850 -315 186 VSSM -810 -315 120 D[22] -47	111	CSX	-5310	-315	145	HS	-3270	-315	179	VCC	-1230	-315
114 DGND -5130 -315 148 LEDON -3090 -315 182 VSSM -1050 -315 115 DGND -5070 -315 149 DMY -3030 -315 183 VSSM -990 -315 116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -930 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 185 VSSM -870 -315 118 VDDI -4890 -315 152 VDDI -2850 -315 186 VSSM -810 -315 119 D[23] -4830 -315 153 VDDI -2790 -315 187 DP1 -750 -315 120 D[22] -4770 -315 154 DGND -2730 -315 188 DP1 -690 -315 121 D[21] -4710	112	RESETX	-5250	-315	146	VS	-3210	-315	180	VCC	-1170	-315
115 DGND -5070 -315 149 DMY -3030 -315 183 VSSM -990 -315 116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -930 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 185 VSSM -870 -315 118 VDDI -4890 -315 152 VDDI -2850 -315 186 VSSM -810 -315 119 D[23] -4830 -315 153 VDDI -2790 -315 187 DP1 -750 -315 120 D[22] -4770 -315 154 DGND -2730 -315 188 DP1 -690 -315 121 D[21] -4710 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 </td <td>113</td> <td>DGND</td> <td>-5190</td> <td>-315</td> <td>147</td> <td>LEDPWM</td> <td>-3150</td> <td>-315</td> <td>181</td> <td>VCC</td> <td>-1110</td> <td>-315</td>	113	DGND	-5190	-315	147	LEDPWM	-3150	-315	181	VCC	-1110	-315
116 VDDI -5010 -315 150 ERR -2970 -315 184 VSSM -930 -315 117 VDDI -4950 -315 151 VDDI -2910 -315 185 VSSM -870 -315 118 VDDI -4890 -315 152 VDDI -2850 -315 186 VSSM -810 -315 119 D[23] -4830 -315 153 VDDI -2790 -315 187 DP1 -750 -315 120 D[22] -4770 -315 154 DGND -2730 -315 188 DP1 -690 -315 121 D[21] -4710 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -2610 -315 190 DP1 -570 -315 123 D[19] -4590<	114	DGND	-5130	-315	148	LEDON	-3090	-315	182	VSSM	-1050	-315
117 VDDI -4950 -315 151 VDDI -2910 -315 185 VSSM -870 -315 118 VDDI -4890 -315 152 VDDI -2850 -315 186 VSSM -810 -315 119 D[23] -4830 -315 153 VDDI -2790 -315 187 DP1 -750 -315 120 D[22] -4770 -315 154 DGND -2730 -315 188 DP1 -690 -315 121 D[21] -4710 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -2610 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315	115	DGND	-5070	-315	149	DMY	-3030	-315	183	VSSM	-990	-315
118 VDDI -4890 -315 152 VDDI -2850 -315 186 VSSM -810 -315 119 D[23] -4830 -315 153 VDDI -2790 -315 187 DP1 -750 -315 120 D[22] -4770 -315 154 DGND -2730 -315 188 DP1 -690 -315 121 D[21] -4710 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -2610 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315	116	VDDI	-5010	-315	150	ERR	-2970	-315	184	VSSM	-930	-315
119 D[23] -4830 -315 153 VDDI -2790 -315 187 DP1 -750 -315 120 D[22] -4770 -315 154 DGND -2730 -315 188 DP1 -690 -315 121 D[21] -4710 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -2610 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315	117	VDDI	-4950	-315	151	VDDI	-2910	-315	185	VSSM	-870	-315
120 D[22] -4770 -315 154 DGND -2730 -315 188 DP1 -690 -315 121 D[21] -4710 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -2610 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315	118	VDDI	-4890	-315	152	VDDI	-2850	-315	186	VSSM	-810	-315
121 D[21] -4710 -315 155 DGND -2670 -315 189 DP1 -630 -315 122 D[20] -4650 -315 156 DGND -2610 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315	119	D[23]	-4830	-315	153	VDDI	-2790	-315	187	DP1	-750	-315
122 D[20] -4650 -315 156 DGND -2610 -315 190 DP1 -570 -315 123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315	120	D[22]	-4770	-315	154	DGND	-2730	-315	188	DP1	-690	-315
123 D[19] -4590 -315 157 VDDB -2550 -315 191 DN1 -510 -315	121	D[21]	-4710	-315	155	DGND	-2670	-315	189	DP1	-630	-315
	122	D[20]	-4650	-315	156	DGND	-2610	-315	190	DP1	-570	-315
124 D[18] -4530 -315 158 VDDB -2490 -315 192 DN1 -450 -315	123	D[19]	-4590	-315	157	VDDB	-2550	-315	191	DN1	-510	-315
	124	D[18]	-4530	-315	158	VDDB	-2490	-315	192	DN1	-450	-315
125 D[17] -4470 -315 159 VDDB -2430 -315 193 DN1 -390 -315	125	D[17]	-4470	-315	159	VDDB	-2430	-315	193	DN1	-390	-315
126 D[16] -4410 -315 160 VDDB -2370 -315 194 DN1 -330 -315	126	D[16]	-4410	-315	160	VDDB	-2370	-315	194	DN1	-330	-315
127 D[15] -4350 -315 161 AGND -2310 -315 195 VSSM -270 -315	127	D[15]	-4350	-315	161	AGND	-2310	-315	195	VSSM	-270	-315
128 D[14] -4290 -315 162 AGND -2250 -315 196 VSSM -210 -315	128	D[14]	-4290	-315	162	AGND	-2250	-315	196	VSSM	-210	-315
129 D[13] -4230 -315 163 AGND -2190 -315 197 CP -150 -315	129	D[13]	-4230	-315	163	AGND	-2190	-315	197	СР	-150	-315
130 D[12] -4170 -315 164 AGND -2130 -315 198 CP -90 -315	130	D[12]	-4170	-315	164	AGND	-2130	-315	198	СР	-90	-315

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PAD No. PIN Name X. Y. PAD No. PIN Name X. PIN Name X. Y. PAD No. PIN Name X. Y. 1990 CPA -3-00 -3-16 233 VSSAA 2070 -315 286 VCCMD 410 -315 -315 -315 -316 -315 236 VSSAA 2100 -315 280 VCCMD 4170 -315 -315 230 VSSAA 2100 -315 280 VCCMD 4170 -315 231 -315 230 -315 210 -315 231 -315 220 -315 220 -315 220 -315 220 -315 220 -315 221 -1172 -410 -315 -316												
200 CP 30 -315 234 VSSA 2070 -315 288 VCCMD 4110 -315 201 CN 90 -315 235 VSSA 2130 -315 269 VCCMD 4170 -315 202 CN 1560 -315 236 VSSA 2190 -315 270 V12TX 4230 -315 203 CN 210 -315 238 V20 2250 -315 271 V12TX 4290 -315 204 CN 270 -315 238 V20 2310 -315 272 V12TX 4390 -315 205 VSSM 330 -315 240 DMY 2430 -315 274 AVCD 4410 -315 207 DP0 450 -315 241 DMY 2430 -315 276 AVCL 44690 -315 208 DP0 570 -315		PIN Name	x	Y		PIN Name	х	Y		PIN Name	х	Y
201	199	СР	-30	-315	233	VSSA	2010	-315	267	VCCMD	4050	-315
202 CN 150 315 236 VSSA 2190 -315 270 V12TX 4230 -315 203 CN 210 -315 237 V20 2250 -315 271 V12TX 4290 -315 204 CN 270 -315 238 V20 2310 -315 272 V12TX 4350 -315 208 VSSM 330 -315 239 DMY 2370 -315 274 AVDD 4410 -315 206 VSSM 380 -315 240 DMY 2430 -315 274 AVDD 4470 -315 207 DP0 450 -315 241 MAP 2490 -315 274 AVDD 4470 -315 208 DP0 570 -315 242 VAP 2550 -315 276 AVCL 4590 -315 210 DP0 570 -315 <	200	СР	30	-315	234	VSSA	2070	-315	268	VCCMD	4110	-315
203 CN 210 -315 237 V20 2250 -315 271 V12TX 4290 -315 204 CN 270 -315 238 V20 2310 -315 272 V12TX 4350 -315 206 VSSM 330 -315 239 DMY 2370 -315 273 AVDD 4410 -315 206 VSSM 330 -315 240 DMY 2430 -315 274 AVDD 4470 -315 207 DP0 450 -315 241 VAP 2490 -315 274 AVDD 4530 -315 208 DP0 510 -315 242 VAP 2550 -315 276 AVCL 4590 -315 210 DP0 630 -315 244 DMY 2610 -315 277 AVCL 4590 -315 211 DN0 690 -315 <	201	CN	90	-315	235	VSSA	2130	-315	269	VCCMD	4170	-315
204 CN 270 -315 238 V20 2310 -315 272 V12TX 4350 -315 206 VSSM 330 -315 239 DMY 2370 -315 273 AVDD 4410 -315 206 VSSM 390 -315 240 DMY 2430 -315 274 AVDD 4470 -315 207 DPO 450 -315 241 VAP 2490 -315 276 AVCL 4590 -315 208 DPO 510 -315 242 VAP 2550 -315 276 AVCL 4590 -315 209 DPO 570 -315 242 VAP 2550 -315 276 AVCL 4590 -315 210 DPO 630 -315 243 DMY 2670 -315 278 AVCL 4710 -315 211 DNO 690 -315 <	202	CN	150	-315	236	VSSA	2190	-315	270	V12TX	4230	-315
205 VSSM 330 -315 239 DMY 2370 -315 273 AVDD 4410 -315 206 VSSM 390 -315 240 DMY 2430 -315 274 AVDD 4470 -315 207 DPO 450 -315 241 VAP 2490 -315 275 AVDD 4530 -315 208 DPO 510 -315 242 VAP 2550 -315 276 AVCL 4590 -315 209 DPO 570 -315 242 VAP 2550 -315 276 AVCL 4590 -315 210 DPO 630 -315 244 DMY 2670 -315 278 AVCL 4710 -315 211 DNO 690 -315 246 DMY 2970 -315 280 DMY 4890 -315 212 DNO 750 -315 <t< td=""><td>203</td><td>CN</td><td>210</td><td>-315</td><td>237</td><td>V20</td><td>2250</td><td>-315</td><td>271</td><td>V12TX</td><td>4290</td><td>-315</td></t<>	203	CN	210	-315	237	V20	2250	-315	271	V12TX	4290	-315
206 VSSM 390 .315 240 DMY 2430 .315 274 AVDD .4470 .315 207 DPO 450 .315 241 VAP 2490 .315 275 AVDD .4530 .315 208 DPO .510 .315 242 VAP .2550 .315 .276 AVCL .4590 .315 209 DPO .570 .315 .242 DMY .2610 .315 .277 AVCL .4660 .315 210 DPO .630 .315 .244 DMY .2670 .315 .278 AVCL .4710 .315 211 DNO .660 .315 .244 DMY .2670 .315 .278 AVCL .4710 .315 211 DNO .660 .315 .245 VAN .2790 .315 .280 DMY .4830 .315 212 DNO .815	204	CN	270	-315	238	V20	2310	-315	272	V12TX	4350	-315
2077 DPO 450 -315 241 VAP 2490 -315 275 AVDD 4530 -315 208 DPO 510 -315 242 VAP 2550 -315 276 AVCL 4590 -315 209 DPO 570 -315 243 DMY 2610 -315 277 AVCL 4650 -315 210 DPO 630 -315 244 DMY 2670 -315 278 AVCL 4710 -315 211 DNO 690 -315 245 VAN 2730 -315 279 DMY 4770 -315 212 DNO 750 -315 246 VAN 2790 -315 280 DMY 4890 -315 213 DNO 810 -315 248 DMY 2910 -315 281 DMY 4890 -315 213 DNO 870 -315 2	205	VSSM	330	-315	239	DMY	2370	-315	273	AVDD	4410	-315
208 DPO 510 -316 242 VAP 2550 -315 276 AVCL 4590 -315 209 DPO 570 -316 243 DMY 2610 -315 277 AVCL 4650 -315 210 DPO 630 -315 244 DMY 2670 -315 278 AVCL 4710 -315 211 DNO 690 -315 245 VAN 2730 -315 279 DMY 4770 -315 212 DNO 750 -315 246 VAN 2790 -315 280 DMY 4830 -315 213 DNO 810 -315 248 DMY 2910 -315 281 DMY 4890 -315 214 DNO 870 -315 248 DMY 2910 -315 281 DMY 4950 -315 215 VSSM 990 -315 25	206	VSSM	390	-315	240	DMY	2430	-315	274	AVDD	4470	-315
209 DPO 570 -315 243 DMY 2610 -315 277 AVCL 4650 -315 210 DPO 630 -315 244 DMY 2670 -315 278 AVCL 4710 -315 211 DNO 690 -315 246 VAN 2730 -315 279 DMY 4770 -315 212 DNO 750 -315 246 VAN 2790 -315 280 DMY 4830 -315 213 DNO 810 -315 247 DMY 2850 -315 281 DMY 4830 -315 214 DNO 870 -315 248 DMY 2910 -315 281 DMY 4850 -315 215 VSSM 990 -315 249 VDDR1 2970 -315 283 DMY 5010 -315 216 VSSM 990 -315	207	DP0	450	-315	241	VAP	2490	-315	275	AVDD	4530	-315
210 DPO 630 .315 244 DMY 2670 .315 278 AVCL 4710 .315 211 DNO 690 .315 245 VAN 2730 .315 279 DMY 4770 .315 212 DNO 750 .315 246 VAN 2790 .315 280 DMY 4830 .315 213 DNO 810 .315 247 DMY 2850 .315 281 DMY 4890 .315 214 DNO 870 .315 248 DMY 2910 .315 282 DMY 4960 .315 215 VSSM 930 .315 249 VDDR1 2970 .315 282 DMY 5010 .315 216 VSSM 990 .315 250 VDDR1 3030 .315 284 DMY 5070 .315 218 VCCMA 1110 .315	208	DP0	510	-315	242	VAP	2550	-315	276	AVCL	4590	-315
211 DN0 690 -315 245 VAN 2730 -315 279 DMY 4770 -315 212 DN0 750 -315 246 VAN 2790 -315 280 DMY 4830 -315 213 DN0 810 -315 247 DMY 2850 -315 281 DMY 4890 -315 214 DN0 870 -315 248 DMY 2910 -315 282 DMY 4950 -315 215 VSSM 930 -315 249 VDDR1 2970 -315 283 DMY 5010 -315 216 VSSM 990 -315 250 VDDR1 3030 -315 284 DMY 5070 -315 217 VCCMA 1100 -315 251 VDDR1 3090 -315 286 VDDB 5130 -315 218 VCCMA 1170 -315	209	DP0	570	-315	243	DMY	2610	-315	277	AVCL	4650	-315
212 DNO 750 -315 246 VAN 2790 -315 280 DMY 4830 -315 213 DNO 810 -315 247 DMY 2850 -315 281 DMY 4890 -315 214 DNO 870 -315 248 DMY 2910 -315 282 DMY 4950 -315 215 VSSM 930 -315 249 VDDR1 2970 -315 283 DMY 5010 -315 216 VSSM 990 -315 250 VDDR1 3030 -315 284 DMY 5070 -315 217 VCCMA 1050 -315 251 VDDR1 3090 -315 285 VDDB 5130 -315 218 VCCMA 1110 -315 252 VDDR1 3210 -315 286 VDDB 5190 -315 220 DMY 1230 -315	210	DP0	630	-315	244	DMY	2670	-315	278	AVCL	4710	-315
213 DN0 810 -315 247 DMY 2850 -315 281 DMY 4890 -315 214 DN0 870 -315 248 DMY 2910 -315 282 DMY 4950 -315 215 VSSM 930 -315 249 VDDR1 2970 -315 283 DMY 5010 -315 216 VSSM 990 -315 250 VDDR1 3030 -315 284 DMY 5070 -315 217 VCCMA 1050 -315 251 VDDR1 3090 -315 285 VDDB 5130 -315 218 VCCMA 1110 -315 252 VDDR1 3150 -315 286 VDDB 5130 -315 219 VCCMA 1170 -315 253 VDDR1 3210 -315 287 VDDB 5250 -315 220 DMY 1290 -31	211	DN0	690	-315	245	VAN	2730	-315	279	DMY	4770	-315
214 DNO 870 -315 248 DMY 2910 -315 282 DMY 4950 -315 215 VSSM 930 -315 249 VDR1 2970 -315 283 DMY 5010 -315 216 VSSM 990 -315 250 VDR1 3030 -315 284 DMY 5070 -315 217 VCCMA 1050 -315 251 VDDR1 3090 -315 285 VDDB 5130 -315 218 VCCMA 1110 -315 252 VDDR1 3150 -315 286 VDDB 5130 -315 219 VCCMA 1170 -315 253 VDDR1 3210 -315 286 VDDB 5250 -315 220 DMY 1230 -315 254 VDDR1 3270 -315 288 VDDB 5310 -315 221 DMY 1350 -	212	DN0	750	-315	246	VAN	2790	-315	280	DMY	4830	-315
215 VSSM 930 -315 249 VDDR1 2970 -315 283 DMY 5010 -315 216 VSSM 990 -315 250 VDDR1 3030 -315 284 DMY 5070 -315 217 VCCMA 1050 -315 251 VDDR1 3090 -315 285 VDDB 5130 -315 218 VCCMA 1110 -315 252 VDDR1 3150 -315 286 VDDB 5190 -315 219 VCCMA 1170 -315 253 VDDR1 3210 -315 286 VDDB 5290 -315 220 DMY 1230 -315 254 VDDR1 3270 -315 288 VDDB 5310 -315 221 DMY 1350 -315 255 VSSR 3330 -315 289 AGND 5370 -315 222 DMY 1350	213	DN0	810	-315	247	DMY	2850	-315	281	DMY	4890	-315
216 VSSM 990 -315 250 VDDR1 3030 -315 284 DMY 5070 -315 217 VCCMA 1050 -315 251 VDDR1 3090 -315 285 VDDB 5130 -315 218 VCCMA 1110 -315 252 VDDR1 3150 -315 286 VDDB 5190 -315 219 VCCMA 1170 -315 253 VDDR1 3210 -315 286 VDDB 5250 -315 220 DMY 1230 -315 254 VDDR1 3270 -315 288 VDDB 5310 -315 221 DMY 1290 -315 255 VSSR 3330 -315 289 AGND 5370 -315 222 DMY 1350 -315 256 VSSR 3390 -315 290 AGND 5430 -315 223 VDDM 1470	214	DN0	870	-315	248	DMY	2910	-315	282	DMY	4950	-315
217 VCCMA 1050 -315 251 VDDR1 3090 -315 285 VDDB 5130 -315 218 VCCMA 1110 -315 252 VDDR1 3150 -315 286 VDDB 5190 -315 219 VCCMA 1170 -315 253 VDDR1 3210 -315 287 VDDB 5250 -315 220 DMY 1230 -315 254 VDDR1 3270 -315 288 VDDB 5310 -315 221 DMY 1290 -315 255 VSSR 3330 -315 289 AGND 5370 -315 222 DMY 1350 -315 256 VSSR 3390 -315 290 AGND 5430 -315 223 VDDM 1410 -315 257 VSSR 3450 -315 291 AGND 5490 -315 224 VDDM 1470	215	VSSM	930	-315	249	VDDR1	2970	-315	283	DMY	5010	-315
218 VCCMA 1110 -315 252 VDDR1 3150 -315 286 VDDB 5190 -315 219 VCCMA 1170 -315 253 VDDR1 3210 -315 287 VDDB 5250 -315 220 DMY 1230 -315 254 VDDR1 3270 -315 288 VDDB 5310 -315 221 DMY 1290 -315 255 VSSR 3330 -315 289 AGND 5370 -315 222 DMY 1350 -315 256 VSSR 3390 -315 290 AGND 5430 -315 223 VDDM 1410 -315 257 VSSR 3450 -315 291 AGND 5490 -315 224 VDDM 1470 -315 258 VSSR 3510 -315 291 AGND 5500 -315 225 VDDM 1530	216	VSSM	990	-315	250	VDDR1	3030	-315	284	DMY	5070	-315
219 VCCMA 1170 -315 253 VDDR1 3210 -315 287 VDDB 5250 -315 220 DMY 1230 -315 254 VDDR1 3270 -315 288 VDDB 5310 -315 221 DMY 1290 -315 255 VSSR 3330 -315 289 AGND 5370 -315 222 DMY 1350 -315 256 VSSR 3390 -315 290 AGND 5430 -315 223 VDDM 1410 -315 257 VSSR 3450 -315 291 AGND 5490 -315 224 VDDM 1470 -315 258 VSSR 3510 -315 292 AGND 5550 -315 225 VDDM 1530 -315 259 VSSR 3570 -315 293 AGND 5610 -315 226 VDDM 1590 <t< td=""><td>217</td><td>VCCMA</td><td>1050</td><td>-315</td><td>251</td><td>VDDR1</td><td>3090</td><td>-315</td><td>285</td><td>VDDB</td><td>5130</td><td>-315</td></t<>	217	VCCMA	1050	-315	251	VDDR1	3090	-315	285	VDDB	5130	-315
220 DMY 1230 -315 254 VDDR1 3270 -315 288 VDDB 5310 -315 221 DMY 1290 -315 255 VSSR 3330 -315 289 AGND 5370 -315 222 DMY 1350 -315 256 VSSR 3390 -315 290 AGND 5430 -315 223 VDDM 1410 -315 257 VSSR 3450 -315 291 AGND 5490 -315 224 VDDM 1470 -315 258 VSSR 3510 -315 292 AGND 5550 -315 225 VDDM 1530 -315 259 VSSR 3570 -315 293 AGND 5610 -315 226 VDDM 1590 -315 260 VSSR 3630 -315 294 VSSB 5670 -315 227 VDDM 1650	218	VCCMA	1110	-315	252	VDDR1	3150	-315	286	VDDB	5190	-315
221 DMY 1290 -315 255 VSSR 3330 -315 289 AGND 5370 -315 222 DMY 1350 -315 256 VSSR 3390 -315 290 AGND 5430 -315 223 VDDM 1410 -315 257 VSSR 3450 -315 291 AGND 5490 -315 224 VDDM 1470 -315 258 VSSR 3510 -315 292 AGND 5550 -315 225 VDDM 1530 -315 259 VSSR 3570 -315 293 AGND 5610 -315 226 VDDM 1590 -315 260 VSSR 3630 -315 294 VSSB 5670 -315 227 VDDM 1650 -315 261 VPS1 3690 -315 295 VSSB 5730 -315 228 VDDR 1710	219	VCCMA	1170	-315	253	VDDR1	3210	-315	287	VDDB	5250	-315
222 DMY 1350 -315 256 VSSR 3390 -315 290 AGND 5430 -315 223 VDDM 1410 -315 257 VSSR 3450 -315 291 AGND 5490 -315 224 VDDM 1470 -315 258 VSSR 3510 -315 292 AGND 5550 -315 225 VDDM 1530 -315 259 VSSR 3570 -315 293 AGND 5610 -315 226 VDDM 1590 -315 260 VSSR 3630 -315 294 VSSB 5670 -315 227 VDDM 1650 -315 261 VPS1 3690 -315 295 VSSB 5730 -315 228 VDDR 1710 -315 262 VPS1 3750 -315 296 VSSB 5790 -315 229 VDDR 1770 <td< td=""><td>220</td><td>DMY</td><td>1230</td><td>-315</td><td>254</td><td>VDDR1</td><td>3270</td><td>-315</td><td>288</td><td>VDDB</td><td>5310</td><td>-315</td></td<>	220	DMY	1230	-315	254	VDDR1	3270	-315	288	VDDB	5310	-315
223 VDDM 1410 -315 257 VSSR 3450 -315 291 AGND 5490 -315 224 VDDM 1470 -315 258 VSSR 3510 -315 292 AGND 5550 -315 225 VDDM 1530 -315 259 VSSR 3570 -315 293 AGND 5610 -315 226 VDDM 1590 -315 260 VSSR 3630 -315 294 VSSB 5670 -315 227 VDDM 1650 -315 261 VPS1 3690 -315 295 VSSB 5730 -315 228 VDDR 1710 -315 262 VPS1 3750 -315 296 VSSB 5790 -315 229 VDDR 1770 -315 263 VPS1 3810 -315 298 VSSB 5910 -315 230 VDDR 1830 <t< td=""><td>221</td><td>DMY</td><td>1290</td><td>-315</td><td>255</td><td>VSSR</td><td>3330</td><td>-315</td><td>289</td><td>AGND</td><td>5370</td><td>-315</td></t<>	221	DMY	1290	-315	255	VSSR	3330	-315	289	AGND	5370	-315
224 VDDM 1470 -315 258 VSSR 3510 -315 292 AGND 5550 -315 225 VDDM 1530 -315 259 VSSR 3570 -315 293 AGND 5610 -315 226 VDDM 1590 -315 260 VSSR 3630 -315 294 VSSB 5670 -315 227 VDDM 1650 -315 261 VPS1 3690 -315 295 VSSB 5730 -315 228 VDDR 1710 -315 262 VPS1 3750 -315 296 VSSB 5790 -315 229 VDDR 1770 -315 263 VPS1 3810 -315 297 VSSB 5850 -315 230 VDDR 1830 -315 264 VPS2 3870 -315 298 VSSB 5970 -315 231 DMY 1890 <td< td=""><td>222</td><td>DMY</td><td>1350</td><td>-315</td><td>256</td><td>VSSR</td><td>3390</td><td>-315</td><td>290</td><td>AGND</td><td>5430</td><td>-315</td></td<>	222	DMY	1350	-315	256	VSSR	3390	-315	290	AGND	5430	-315
225 VDDM 1530 -315 259 VSSR 3570 -315 293 AGND 5610 -315 226 VDDM 1590 -315 260 VSSR 3630 -315 294 VSSB 5670 -315 227 VDDM 1650 -315 261 VPS1 3690 -315 295 VSSB 5730 -315 228 VDDR 1710 -315 262 VPS1 3750 -315 296 VSSB 5790 -315 229 VDDR 1770 -315 263 VPS1 3810 -315 297 VSSB 5850 -315 230 VDDR 1830 -315 264 VPS2 3870 -315 298 VSSB 5910 -315 231 DMY 1890 -315 265 VPS2 3930 -315 299 VSSB 5970 -315	223	VDDM	1410	-315	257	VSSR	3450	-315	291	AGND	5490	-315
226 VDDM 1590 -315 260 VSSR 3630 -315 294 VSSB 5670 -315 227 VDDM 1650 -315 261 VPS1 3690 -315 295 VSSB 5730 -315 228 VDDR 1710 -315 262 VPS1 3750 -315 296 VSSB 5790 -315 229 VDDR 1770 -315 263 VPS1 3810 -315 297 VSSB 5850 -315 230 VDDR 1830 -315 264 VPS2 3870 -315 298 VSSB 5910 -315 231 DMY 1890 -315 265 VPS2 3930 -315 299 VSSB 5970 -315	224	VDDM	1470	-315	258	VSSR	3510	-315	292	AGND	5550	-315
227 VDDM 1650 -315 261 VPS1 3690 -315 295 VSSB 5730 -315 228 VDDR 1710 -315 262 VPS1 3750 -315 296 VSSB 5790 -315 229 VDDR 1770 -315 263 VPS1 3810 -315 297 VSSB 5850 -315 230 VDDR 1830 -315 264 VPS2 3870 -315 298 VSSB 5910 -315 231 DMY 1890 -315 265 VPS2 3930 -315 299 VSSB 5970 -315	225	VDDM	1530	-315	259	VSSR	3570	-315	293	AGND	5610	-315
228 VDDR 1710 -315 262 VPS1 3750 -315 296 VSSB 5790 -315 229 VDDR 1770 -315 263 VPS1 3810 -315 297 VSSB 5850 -315 230 VDDR 1830 -315 264 VPS2 3870 -315 298 VSSB 5910 -315 231 DMY 1890 -315 265 VPS2 3930 -315 299 VSSB 5970 -315	226	VDDM	1590	-315	260	VSSR	3630	-315	294	VSSB	5670	-315
229 VDDR 1770 -315 263 VPS1 3810 -315 297 VSSB 5850 -315 230 VDDR 1830 -315 264 VPS2 3870 -315 298 VSSB 5910 -315 231 DMY 1890 -315 265 VPS2 3930 -315 299 VSSB 5970 -315	227	VDDM	1650	-315	261	VPS1	3690	-315	295	VSSB	5730	-315
230 VDDR 1830 -315 264 VPS2 3870 -315 298 VSSB 5910 -315 231 DMY 1890 -315 265 VPS2 3930 -315 299 VSSB 5970 -315	228	VDDR	1710	-315	262	VPS1	3750	-315	296	VSSB	5790	-315
231 DMY 1890 -315 265 VPS2 3930 -315 299 VSSB 5970 -315	229	VDDR	1770	-315	263	VPS1	3810	-315	297	VSSB	5850	-315
	230	VDDR	1830	-315	264	VPS2	3870	-315	298	VSSB	5910	-315
232 DMY 1950 -315 266 VPS2 3990 -315 300 DMY 6030 -315	231	DMY	1890	-315	265	VPS2	3930	-315	299	VSSB	5970	-315
	232	DMY	1950	-315	266	VPS2	3990	-315	300	DMY	6030	-315

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PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y
301	DMY	6090	-315	335	VSSB2	8130	-315	369	VGHEQ2	10170	-315
302	DMY	6150	-315	336	VSSB	8190	-315	370	VGHEQ2	10230	-315
303	DMY	6210	-315	337	VSSB	8250	-315	371	VDDB2	10290	-315
304	DMY	6270	-315	338	VSSB	8310	-315	372	VDDB2	10350	-315
305	DMY	6330	-315	339	AGND	8370	-315	373	VDDB2	10410	-315
306	DMY	6390	-315	340	AGND	8430	-315	374	VDDB2	10470	-315
307	DMY	6450	-315	341	AGND	8490	-315	375	VGL_REG	10530	-315
308	DMY	6510	-315	342	AGND	8550	-315	376	VGL_REG	10590	-315
309	DMY	6570	-315	343	DMY	8610	-315	377	VGLO	10650	-315
310	DMY	6630	-315	344	DMY	8670	-315	378	VGLO	10710	-315
311	DMY	6690	-315	345	DMY	8730	-315	379	VGL	10770	-315
312	DMY	6750	-315	346	DMY	8790	-315	380	VGL	10830	-315
313	DMY	6810	-315	347	DMY	8850	-315	381	VGL	10890	-315
314	DMY	6870	-315	348	DMY	8910	-315	382	VGL	10950	-315
315	DMY	6930	-315	349	DMY	8970	-315	383	DMY	11010	-315
316	DMY	6990	-315	350	DMY	9030	-315	384	DMY	11070	-315
317	DMY	7050	-315	351	DMY	9090	-315	385	DMY	11130	-315
318	DMY	7110	-315	352	VGHP	9150	-315	386	DMY	11190	-315
319	DMY	7170	-315	353	VGHP	9210	-315	387	CNTACT2	11250	-315
320	DMY	7230	-315	354	VGHP	9270	-315	388	CNTACT2	11310	-315
321	DMY	7290	-315	355	VCC	9330	-315	389	VCOM	11370	-315
322	DMY	7350	-315	356	VCC	9390	-315	390	VCOM	11430	-315
323	DMY	7410	-315	357	VCC	9450	-315	391	VCOM	11490	-315
324	VDDB	7470	-315	358	DGND	9510	-315	392	VCOM	11550	-315
325	VDDB	7530	-315	359	DGND	9570	-315	393	VCOM	11610	-315
326	VDDB	7590	-315	360	DGND	9630	-315	394	PADA2	11670	-315
327	VDDB	7650	-315	361	VSSB2	9690	-315	395	PADB2	11730	-315
328	VDDB	7710	-315	362	VSSB2	9750	-315	396	VSSIDUM2	11790	-315
329	VSSB2	7770	-315	363	VSSB2	9810	-315	397	VSSIDUM3	11850	-315
330	VSSB2	7830	-315	364	VSSB2	9870	-315	398	VSSIDUM3	11910	-315
331	VSSB2	7890	-315	365	VGHS	9930	-315	399	DMY	11760	309.5
332	VSSB2	7950	-315	366	VGHS	9990	-315	400	DMY	11732	184.5
333	VSSB2	8010	-315	367	VGHO	10050	-315	401	DMY	11718	309.5
334	VSSB2	8070	-315	368	VGHO	10110	-315	402	PADA3	11704	184.5

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PAD	DIN Name	v	V	PAD	DIN Nome	v	V	PAD	DIN Nome	v	v
No.	PIN Name	Х	Y	No.	PIN Name	X	Y	No.	PIN Name	X	Y
403	PADB3	11690	309.5	437	GO[10]	11214	309.5	471	SDUM1	10738	309.5
404	VGHO	11676	184.5	438	GO[10]	11200	184.5	472	S[1]	10724	184.5
405	VGHO	11662	309.5	439	GO[11]	11186	309.5	473	S[2]	10710	309.5
406	VGHO	11648	184.5	440	GO[11]	11172	184.5	474	S[3]	10696	184.5
407	VGLO	11634	309.5	441	GO[12]	11158	309.5	475	S[4]	10682	309.5
408	VGLO	11620	184.5	442	GO[12]	11144	184.5	476	S[5]	10668	184.5
409	VGLO	11606	309.5	443	GO[13]	11130	309.5	477	S[6]	10654	309.5
410	GO[1]	11592	184.5	444	GO[13]	11116	184.5	478	S[7]	10640	184.5
411	GO[1]	11578	309.5	445	GO[14]	11102	309.5	479	S[8]	10626	309.5
412	GO[2]	11564	184.5	446	GO[14]	11088	184.5	480	S[9]	10612	184.5
413	GO[2]	11550	309.5	447	GO[15]	11074	309.5	481	S[10]	10598	309.5
414	VGL	11536	184.5	448	GO[15]	11060	184.5	482	S[11]	10584	184.5
415	VGL	11522	309.5	449	GO[16]	11046	309.5	483	S[12]	10570	309.5
416	VGL	11508	184.5	450	GO[16]	11032	184.5	484	S[13]	10556	184.5
417	DMY	11494	309.5	451	VGHO	11018	309.5	485	S[14]	10542	309.5
418	DMY	11480	184.5	452	VGHO	11004	184.5	486	S[15]	10528	184.5
419	DMY	11466	309.5	453	VGHO	10990	309.5	487	S[16]	10514	309.5
420	VGLO	11452	184.5	454	VGHO	10976	184.5	488	S[17]	10500	184.5
421	VGLO	11438	309.5	455	VGHO	10962	309.5	489	S[18]	10486	309.5
422	VGLO	11424	184.5	456	VGHO	10948	184.5	490	S[19]	10472	184.5
423	GO[3]	11410	309.5	457	VGHO	10934	309.5	491	S[20]	10458	309.5
424	GO[3]	11396	184.5	458	VGHO	10920	184.5	492	S[21]	10444	184.5
425	GO[4]	11382	309.5	459	VGLO	10906	309.5	493	S[22]	10430	309.5
426	GO[4]	11368	184.5	460	VGLO	10892	184.5	494	S[23]	10416	184.5
427	GO[5]	11354	309.5	461	VGLO	10878	309.5	495	S[24]	10402	309.5
428	GO[5]	11340	184.5	462	VGLO	10864	184.5	496	S[25]	10388	184.5
429	GO[6]	11326	309.5	463	VGLO	10850	309.5	497	S[26]	10374	309.5
430	GO[6]	11312	184.5	464	VGLO	10836	184.5	498	S[27]	10360	184.5
431	GO[7]	11298	309.5	465	VGLO	10822	309.5	499	S[28]	10346	309.5
432	GO[7]	11284	184.5	466	VGLO	10808	184.5	500	S[29]	10332	184.5
433	GO[8]	11270	309.5	467	VGLO	10794	309.5	501	S[30]	10318	309.5
434	GO[8]	11256	184.5	468	DMY	10780	184.5	502	S[31]	10304	184.5
435	GO[9]	11242	309.5	469	DMY	10766	309.5	503	S[32]	10290	309.5
436	GO[9]	11228	184.5	470	SDUM0	10752	184.5	504	S[33]	10276	184.5

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PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y
505	S[34]	10262	309.5	539	S[68]	9786	309.5	573	S[102]	9310	309.5
506	S[35]	10248	184.5	540	S[69]	9772	184.5	574	S[103]	9296	184.5
507	S[36]	10234	309.5	541	S[70]	9758	309.5	575	S[104]	9282	309.5
508	S[37]	10220	184.5	542	S[71]	9744	184.5	576	S[105]	9268	184.5
509	S[38]	10206	309.5	543	S[72]	9730	309.5	577	S[106]	9254	309.5
510	S[39]	10192	184.5	544	S[73]	9716	184.5	578	S[107]	9240	184.5
511	S[40]	10178	309.5	545	S[74]	9702	309.5	579	S[108]	9226	309.5
512	S[41]	10164	184.5	546	S[75]	9688	184.5	580	S[109]	9212	184.5
513	S[42]	10150	309.5	547	S[76]	9674	309.5	581	S[110]	9198	309.5
514	S[43]	10136	184.5	548	S[77]	9660	184.5	582	S[111]	9184	184.5
515	S[44]	10122	309.5	549	S[78]	9646	309.5	583	S[112]	9170	309.5
516	S[45]	10108	184.5	550	S[79]	9632	184.5	584	S[113]	9156	184.5
517	S[46]	10094	309.5	551	S[80]	9618	309.5	585	S[114]	9142	309.5
518	S[47]	10080	184.5	552	S[81]	9604	184.5	586	S[115]	9128	184.5
519	S[48]	10066	309.5	553	S[82]	9590	309.5	587	S[116]	9114	309.5
520	S[49]	10052	184.5	554	S[83]	9576	184.5	588	S[117]	9100	184.5
521	S[50]	10038	309.5	555	S[84]	9562	309.5	589	S[118]	9086	309.5
522	S[51]	10024	184.5	556	S[85]	9548	184.5	590	S[119]	9072	184.5
523	S[52]	10010	309.5	557	S[86]	9534	309.5	591	S[120]	9058	309.5
524	S[53]	9996	184.5	558	S[87]	9520	184.5	592	S[121]	9044	184.5
525	S[54]	9982	309.5	559	S[88]	9506	309.5	593	S[122]	9030	309.5
526	S[55]	9968	184.5	560	S[89]	9492	184.5	594	S[123]	9016	184.5
527	S[56]	9954	309.5	561	S[90]	9478	309.5	595	S[124]	9002	309.5
528	S[57]	9940	184.5	562	S[91]	9464	184.5	596	S[125]	8988	184.5
529	S[58]	9926	309.5	563	S[92]	9450	309.5	597	S[126]	8974	309.5
530	S[59]	9912	184.5	564	S[93]	9436	184.5	598	S[127]	8960	184.5
531	S[60]	9898	309.5	565	S[94]	9422	309.5	599	S[128]	8946	309.5
532	S[61]	9884	184.5	566	S[95]	9408	184.5	600	S[129]	8932	184.5
533	S[62]	9870	309.5	567	S[96]	9394	309.5	601	S[130]	8918	309.5
534	S[63]	9856	184.5	568	S[97]	9380	184.5	602	S[131]	8904	184.5
535	S[64]	9842	309.5	569	S[98]	9366	309.5	603	S[132]	8890	309.5
536	S[65]	9828	184.5	570	S[99]	9352	184.5	604	S[133]	8876	184.5
537	S[66]	9814	309.5	571	S[100]	9338	309.5	605	S[134]	8862	309.5
538	S[67]	9800	184.5	572	S[101]	9324	184.5	606	S[135]	8848	184.5

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PAD PIN Name X Y PAD No. PIN Name X Y PAD PIN Name X Y PAD No. PIN Name X Y PAD PIN Name X PIN Name X PIN Name X Y PAD PIN Name X PIN Name X PIN Name X PIN Name X Y PAD PIN Name X												
608 S[137] 8820 184.5 642 S[171] 8344 184.5 676 S[205] 7668 184.5 609 S[138] 8806 309.5 643 S[172] 8330 309.5 677 S[206] 7654 309.5 610 S[138] 8792 184.5 644 S[173] 8316 184.5 678 S[207] 7840 184.5 611 S[140] 8778 309.5 645 S[174] 8302 309.5 679 S[208] 7626 309.5 612 S[141] 8764 184.5 646 S[175] 8288 184.5 680 S[209] 7912 194.5 613 S[142] 8760 309.5 647 S[176] 8274 309.5 681 S[210] 7798 309.5 614 S[143] 8736 184.5 648 S[177] 8260 184.5 682 S[211] 7774 184.5 615 S[144] 8722 309.5 649 S[178] 8246 309.5 683 S[212] 7770 184.5 616 S[145] 8708 184.5 660 S[179] 8232 184.5 688 S[213] 7756 184.5 617 S[146] 8694 309.5 6651 S[160] 8218 309.5 688 S[214] 7772 309.5 649 S[178] 8246 309.5 688 S[214] 7774 309.5 649 S[147] 8680 184.5 6652 S[181] 8204 184.5 688 S[215] 7728 184.5 618 S[147] 8680 184.5 6652 S[181] 8204 184.5 688 S[215] 7778 184.5 620 S[149] 8662 309.5 653 S[182] 8190 309.5 687 S[216] 7774 309.5 620 S[149] 8662 184.5 664 S[183] 8176 184.5 688 S[217] 7700 184.5 622 S[151] 8624 184.5 666 S[185] 8148 184.5 690 S[221] 7668 309.5 622 S[151] 8624 184.5 666 S[185] 8148 184.5 690 S[221] 7668 309.5 622 S[151] 8624 184.5 666 S[185] 8148 184.5 690 S[221] 7694 184.5 625 S[157] 8540 184.5 668 S[187] 8120 184.5 693 S[221] 7694 184.5 625 S[156] 8584 309.5 669 S[188] 8106 309.5 693 S[222] 7630 309.5 622 S[156] 8484 184.5 666 S[189] 8002 184.5 694 S[223] 7616 184.5 622 S[151] 8404 8445 668 S[197] 8008 184.5 698 S[224] 7602 309.5 623 S[156] 8488 309.5 665 S[194] 8002 309.5 699 S[228] 7532 309.5 63		PIN Name	х	Y		PIN Name	х	Y		PIN Name	х	Y
609 \$[138] 8806 309.5 643 \$[172] 8330 309.5 677 \$[266] 7864 309.5 610 \$[139] 8792 184.5 644 \$[173] 8316 184.5 678 \$[207] 7840 184.5 611 \$[140] 8778 309.5 645 \$[174] 8302 309.5 679 \$[208] 7826 309.5 612 \$[141] 8764 184.5 646 \$[176] 8288 184.5 680 \$[209] 7812 184.5 613 \$[142] 8750 309.5 647 \$[176] 8274 309.5 681 \$[210] 7798 309.5 614 \$[143] 8736 184.5 648 \$[177] 820 184.5 682 \$[211] 7778 309.5 616 \$[144] 8722 309.5 653 \$[179] 8232 184.5 684 \$[213] 7776 184.5 6	607	S[136]	8834	309.5	641	S[170]	8358	309.5	675	S[204]	7882	309.5
610 S[139] 8792 184.5 644 S[173] 8316 184.5 678 S[207] 7640 184.5 611 S[140] 8778 309.5 645 S[174] 8302 309.5 679 S[208] 7826 309.5 612 S[141] 8764 184.5 646 S[175] 8288 184.5 680 S[209] 7812 184.5 613 S[142] 8750 309.5 647 S[176] 8274 309.5 681 S[210] 7798 309.5 614 S[143] 8736 184.5 648 S[177] 8280 184.5 682 S[211] 77784 184.5 615 S[144] 8722 309.5 649 S[178] 8246 309.5 683 S[212] 7770 309.5 616 S[145] 8708 184.5 660 S[179] 8232 184.5 684 S[213] 7756 184.5 617 S[146] 86894 309.5 6651 S[180] 8218 309.5 685 S[214] 7742 309.5 618 S[147] 8680 184.5 6652 S[181] 8204 184.5 686 S[215] 7728 184.5 619 S[148] 8666 309.5 6653 S[182] 8190 309.5 687 S[216] 7774 309.5 620 S[149] 86852 184.5 664 S[183] 8176 184.5 688 S[217] 7700 184.5 621 S[150] 8638 309.5 6655 S[184] 8162 309.5 689 S[218] 7686 309.5 622 S[151] 8624 184.5 666 S[165] 8148 184.5 669 S[219] 7672 184.5 623 S[152] 8610 309.5 6657 S[186] 8148 184.5 669 S[221] 7764 184.5 624 S[153] 8596 184.5 668 S[187] 8120 184.5 669 S[221] 7668 309.5 626 S[156] 8588 309.5 669 S[188] 8062 184.5 669 S[222] 7630 309.5 628 S[157] 8540 184.5 666 S[199] 8092 184.5 669 S[222] 7588 184.5 629 S[156] 8548 309.5 663 S[191] 8094 184.5 669 S[222] 7588 184.5 629 S[156] 8488 309.5 666 S[199] 8002 184.5 669 S[222] 7560 184.5 623 S[156] 8484 184.5 666 S[193] 8008 184.5 669 S[222] 7560 184.5 623 S[156] 8486 8486 309.5 666 S[189] 8092 184.5 669 S[222] 7630 309.5 626 S[156] 8486 8485 666 S[193] 8008 184.5 669 S[222] 7560 184.5 623	608	S[137]	8820	184.5	642	S[171]	8344	184.5	676	S[205]	7868	184.5
611 S[140] 8778 309.5 645 S[174] 8302 309.5 679 S[208] 7826 309.5 612 S[141] 8764 184.5 646 S[175] 8288 184.5 680 S[209] 7612 184.5 613 S[142] 8750 309.5 647 S[176] 8274 309.5 681 S[210] 7798 309.5 614 S[143] 8736 184.5 648 S[177] 8260 184.5 662 S[211] 7770 309.5 616 S[144] 8722 309.5 649 S[178] 8246 309.5 683 S[212] 7770 309.5 616 S[146] 8694 309.5 651 S[180] 8232 184.5 684 S[213] 7752 309.5 618 S[147] 8680 184.5 662 S[181] 8204 184.5 686 S[215] 7728 184.5	609	S[138]	8806	309.5	643	S[172]	8330	309.5	677	S[206]	7854	309.5
612 S[141] 8764 184.5 646 S[175] 8288 184.5 680 S[209] 7812 184.5 613 S[142] 8750 309.5 647 S[176] 8274 309.5 681 S[210] 7798 309.5 614 S[143] 8736 184.5 648 S[177] 8260 184.5 662 S[211] 7770 309.5 616 S[144] 8722 309.5 649 S[178] 8246 309.5 683 S[212] 7770 309.5 616 S[146] 8694 309.5 651 S[180] 8218 309.5 685 S[214] 7742 309.5 618 S[147] 8680 184.5 662 S[181] 8204 184.5 686 S[215] 7728 184.5 619 S[148] 8666 309.5 653 S[162] 8190 309.5 687 S[216] 7714 309.5	610	S[139]	8792	184.5	644	S[173]	8316	184.5	678	S[207]	7840	184.5
613 S[142] 8750 309.5 647 S[176] 8274 309.5 681 S[210] 7798 309.5 614 S[143] 8736 184.5 648 S[177] 8260 184.5 682 S[211] 7776 184.5 615 S[144] 8722 309.5 649 S[178] 8246 309.5 683 S[212] 7770 309.5 616 S[145] 8708 184.5 650 S[179] 8232 184.5 684 S[213] 7756 184.5 617 S[146] 8684 309.5 661 S[180] 8218 309.5 685 S[214] 7742 309.5 618 S[147] 8680 184.5 652 S[181] 8204 184.5 686 S[215] 7728 184.5 619 S[149] 8652 184.5 654 S[183] 8176 184.5 688 S[217] 7700 184.5	611	S[140]	8778	309.5	645	S[174]	8302	309.5	679	S[208]	7826	309.5
6144 S[143] 8736 184.5 648 S[177] 8260 184.5 682 S[211] 7784 184.5 615 S[144] 8722 309.5 649 S[178] 3246 309.5 683 S[212] 7770 309.5 616 S[145] 8708 184.5 660 S[179] 8232 184.5 684 S[213] 7756 184.5 617 S[146] 8684 309.5 661 S[180] 8218 309.5 685 S[214] 7742 309.5 618 S[147] 8680 184.5 662 S[181] 8204 184.5 668 S[215] 7728 184.5 619 S[148] 8666 309.5 663 S[182] 8190 309.5 687 S[216] 7714 309.5 620 S[149] 8652 184.5 664 S[183] 8176 184.5 668 S[217] 7700 184.5 663 </td <td>612</td> <td>S[141]</td> <td>8764</td> <td>184.5</td> <td>646</td> <td>S[175]</td> <td>8288</td> <td>184.5</td> <td>680</td> <td>S[209]</td> <td>7812</td> <td>184.5</td>	612	S[141]	8764	184.5	646	S[175]	8288	184.5	680	S[209]	7812	184.5
615 S[144] 8722 309.5 649 S[178] 8246 309.5 683 S[212] 7770 309.5 616 S[145] 8708 184.5 660 S[179] 8232 184.5 684 S[213] 7756 184.5 617 S[146] 8694 309.5 6651 S[180] 8218 309.5 685 S[214] 7742 309.5 618 S[147] 8680 184.5 6652 S[181] 8204 184.5 686 S[216] 7772 184.5 619 S[148] 8666 309.5 6653 S[182] 8190 309.5 687 S[216] 7774 309.5 620 S[149] 8652 184.5 655 S[184] 8162 309.5 688 S[217] 7700 184.5 621 S[150] 8638 309.5 655 S[184] 8162 309.5 689 S[218] 7668 309.5 <	613	S[142]	8750	309.5	647	S[176]	8274	309.5	681	S[210]	7798	309.5
616 S[145] 8708 184.5 650 S[179] 8232 184.5 684 S[213] 7756 184.5 617 S[146] 8694 309.5 651 S[180] 8218 309.5 685 S[214] 7742 309.5 618 S[147] 8680 184.5 652 S[181] 8204 184.5 686 S[215] 7728 184.5 619 S[148] 8666 309.5 653 S[182] 8190 309.5 687 S[216] 7714 309.5 620 S[149] 8652 184.5 654 S[183] 8176 184.5 688 S[217] 7700 184.5 621 S[150] 8638 309.5 655 S[184] 8162 309.5 689 S[218] 7686 309.5 622 S[151] 8624 184.5 656 S[185] 8148 184.5 690 S[219] 7672 184.5	614	S[143]	8736	184.5	648	S[177]	8260	184.5	682	S[211]	7784	184.5
617 S[146] 8694 309.5 661 S[180] 8218 309.5 685 S[214] 7742 309.5 618 S[147] 8680 184.5 652 S[181] 8204 184.5 686 S[215] 7728 184.5 619 S[148] 8666 309.5 653 S[182] 8190 309.5 687 S[216] 7714 309.5 620 S[149] 8652 184.5 654 S[183] 8176 184.5 688 S[217] 7700 184.5 621 S[150] 8638 309.5 655 S[184] 8162 309.5 689 S[218] 7686 309.5 622 S[151] 8624 184.5 656 S[185] 8148 184.5 690 S[219] 7672 184.5 623 S[152] 8610 309.5 657 S[186] 8134 309.5 691 S[220] 7658 309.5	615	S[144]	8722	309.5	649	S[178]	8246	309.5	683	S[212]	7770	309.5
618 S[147] 8680 184.5 662 S[181] 8204 184.5 686 S[215] 7728 184.5 619 S[148] 8666 309.5 653 S[182] 8190 309.5 687 S[216] 7714 309.5 620 S[149] 8652 184.5 654 S[183] 8176 184.5 688 S[217] 7700 184.5 621 S[150] 8638 309.5 655 S[184] 8162 309.5 689 S[218] 7686 309.5 622 S[151] 8624 184.5 656 S[185] 8148 184.5 690 S[219] 7672 184.5 623 S[152] 8610 309.5 657 S[186] 8134 309.5 691 S[220] 7658 309.5 624 S[153] 8596 184.5 658 S[187] 8120 184.5 692 S[221] 7644 184.5	616	S[145]	8708	184.5	650	S[179]	8232	184.5	684	S[213]	7756	184.5
619 S[148] 8666 309.5 653 S[182] 8190 309.5 687 S[216] 7714 309.5 620 S[149] 8652 184.5 654 S[183] 8176 184.5 688 S[217] 7700 184.5 621 S[150] 8638 309.5 655 S[184] 8162 309.5 689 S[218] 7686 309.5 622 S[151] 8624 184.5 656 S[185] 8148 184.5 690 S[219] 7672 184.5 623 S[152] 8610 309.5 657 S[186] 8134 309.5 691 S[220] 7658 309.5 624 S[153] 8596 184.5 658 S[187] 8120 184.5 692 S[221] 7644 184.5 625 S[154] 8582 309.5 659 S[188] 8106 309.5 693 S[222] 7630 309.5	617	S[146]	8694	309.5	651	S[180]	8218	309.5	685	S[214]	7742	309.5
620 S[149] 8652 184.5 664 S[183] 8176 184.5 668 S[217] 7700 184.5 621 S[150] 8638 309.5 655 S[184] 8162 309.5 689 S[218] 7686 309.5 622 S[151] 8624 184.5 656 S[185] 8148 184.5 690 S[219] 7672 184.5 623 S[152] 8610 309.5 657 S[186] 8134 309.5 691 S[220] 7658 309.5 624 S[153] 8596 184.5 658 S[187] 8120 184.5 692 S[221] 7644 184.5 625 S[154] 8582 309.5 669 S[188] 8106 309.5 693 S[222] 7630 309.5 626 S[155] 8568 184.5 660 S[189] 8092 184.5 694 S[223] 7616 184.5	618	S[147]	8680	184.5	652	S[181]	8204	184.5	686	S[215]	7728	184.5
621 S[150] 8638 309.5 655 S[184] 8162 309.5 689 S[218] 7686 309.5 622 S[151] 8624 184.5 656 S[185] 8148 184.5 690 S[219] 7672 184.5 623 S[152] 8610 309.5 657 S[186] 8134 309.5 691 S[220] 7658 309.5 624 S[153] 8596 184.5 658 S[187] 8120 184.5 692 S[221] 7644 184.5 625 S[154] 8582 309.5 659 S[188] 8106 309.5 693 S[222] 7630 309.5 626 S[155] 8568 184.5 660 S[189] 8092 184.5 694 S[223] 7616 184.5 627 S[156] 8554 309.5 661 S[190] 8078 309.5 695 S[224] 7602 309.5	619	S[148]	8666	309.5	653	S[182]	8190	309.5	687	S[216]	7714	309.5
622 S[151] 8624 184.5 656 S[185] 8148 184.5 690 S[219] 7672 184.5 623 S[152] 8610 309.5 657 S[186] 8134 309.5 691 S[220] 7658 309.5 624 S[153] 8596 184.5 668 S[187] 8120 184.5 692 S[221] 7644 184.5 625 S[154] 8582 309.5 659 S[188] 8106 309.5 693 S[222] 7630 309.5 626 S[155] 8568 184.5 660 S[189] 8092 184.5 694 S[223] 7616 184.5 627 S[156] 8554 309.5 661 S[190] 8078 309.5 695 S[224] 7602 309.5 628 S[157] 8540 184.5 662 S[191] 8064 184.5 696 S[225] 7588 184.5	620	S[149]	8652	184.5	654	S[183]	8176	184.5	688	S[217]	7700	184.5
623 S[152] 8610 309.5 657 S[186] 8134 309.5 691 S[220] 7658 309.5 624 S[153] 8596 184.5 658 S[187] 8120 184.5 692 S[221] 7644 184.5 625 S[154] 8582 309.5 659 S[188] 8106 309.5 693 S[222] 7630 309.5 626 S[155] 8568 184.5 660 S[189] 8092 184.5 694 S[223] 7616 184.5 627 S[156] 8554 309.5 661 S[190] 8078 309.5 695 S[224] 7602 309.5 628 S[157] 8540 184.5 662 S[191] 8064 184.5 696 S[225] 7588 184.5 629 S[158] 8526 309.5 663 S[192] 8050 309.5 697 S[226] 7574 309.5	621	S[150]	8638	309.5	655	S[184]	8162	309.5	689	S[218]	7686	309.5
624 S[153] 8596 184.5 658 S[187] 8120 184.5 692 S[221] 7644 184.5 625 S[154] 8582 309.5 659 S[188] 8106 309.5 693 S[222] 7630 309.5 626 S[155] 8568 184.5 660 S[189] 8092 184.5 694 S[223] 7616 184.5 627 S[156] 8554 309.5 661 S[190] 8078 309.5 695 S[224] 7602 309.5 628 S[157] 8540 184.5 662 S[191] 8064 184.5 696 S[225] 7588 184.5 629 S[158] 8526 309.5 663 S[192] 8050 309.5 697 S[226] 7574 309.5 630 S[159] 8512 184.5 664 S[193] 8036 184.5 698 S[227] 7560 184.5	622	S[151]	8624	184.5	656	S[185]	8148	184.5	690	S[219]	7672	184.5
625 S[154] 8582 309.5 659 S[188] 8106 309.5 693 S[222] 7630 309.5 626 S[155] 8568 184.5 660 S[189] 8092 184.5 694 S[223] 7616 184.5 627 S[156] 8554 309.5 661 S[190] 8078 309.5 695 S[224] 7602 309.5 628 S[157] 8540 184.5 662 S[191] 8064 184.5 696 S[225] 7588 184.5 629 S[158] 8526 309.5 663 S[192] 8050 309.5 697 S[226] 7574 309.5 630 S[159] 8512 184.5 664 S[193] 8036 184.5 698 S[227] 7560 184.5 631 S[160] 8498 309.5 665 S[194] 8022 309.5 699 S[228] 7546 309.5	623	S[152]	8610	309.5	657	S[186]	8134	309.5	691	S[220]	7658	309.5
626 S[155] 8568 184.5 660 S[189] 8092 184.5 694 S[223] 7616 184.5 627 S[156] 8554 309.5 661 S[190] 8078 309.5 695 S[224] 7602 309.5 628 S[157] 8540 184.5 662 S[191] 8064 184.5 696 S[225] 7588 184.5 629 S[158] 8526 309.5 663 S[192] 8050 309.5 697 S[226] 7574 309.5 630 S[159] 8512 184.5 664 S[193] 8036 184.5 698 S[227] 7560 184.5 631 S[160] 8498 309.5 665 S[194] 8022 309.5 699 S[228] 7546 309.5 632 S[161] 8484 184.5 666 S[195] 8008 184.5 700 S[229] 7532 184.5	624	S[153]	8596	184.5	658	S[187]	8120	184.5	692	S[221]	7644	184.5
627 S[156] 8554 309.5 661 S[190] 8078 309.5 695 S[224] 7602 309.5 628 S[157] 8540 184.5 662 S[191] 8064 184.5 696 S[225] 7588 184.5 629 S[158] 8526 309.5 663 S[192] 8050 309.5 697 S[226] 7574 309.5 630 S[159] 8512 184.5 664 S[193] 8036 184.5 698 S[227] 7560 184.5 631 S[160] 8498 309.5 665 S[194] 8022 309.5 699 S[228] 7546 309.5 632 S[161] 8484 184.5 666 S[195] 8008 184.5 700 S[229] 7532 184.5 633 S[162] 8470 309.5 667 S[196] 7994 309.5 701 S[230] 7518 309.5	625	S[154]	8582	309.5	659	S[188]	8106	309.5	693	S[222]	7630	309.5
628 S[157] 8540 184.5 662 S[191] 8064 184.5 696 S[225] 7588 184.5 629 S[158] 8526 309.5 663 S[192] 8050 309.5 697 S[226] 7574 309.5 630 S[159] 8512 184.5 664 S[193] 8036 184.5 698 S[227] 7560 184.5 631 S[160] 8498 309.5 665 S[194] 8022 309.5 699 S[228] 7546 309.5 632 S[161] 8484 184.5 666 S[195] 8008 184.5 700 S[229] 7532 184.5 633 S[162] 8470 309.5 667 S[196] 7994 309.5 701 S[230] 7518 309.5 634 S[163] 8456 184.5 668 S[197] 7980 184.5 702 S[231] 7504 184.5	626	S[155]	8568	184.5	660	S[189]	8092	184.5	694	S[223]	7616	184.5
629 S[158] 8526 309.5 663 S[192] 8050 309.5 697 S[226] 7574 309.5 630 S[159] 8512 184.5 664 S[193] 8036 184.5 698 S[227] 7560 184.5 631 S[160] 8498 309.5 665 S[194] 8022 309.5 699 S[228] 7546 309.5 632 S[161] 8484 184.5 666 S[195] 8008 184.5 700 S[229] 7532 184.5 633 S[162] 8470 309.5 667 S[196] 7994 309.5 701 S[230] 7518 309.5 634 S[163] 8456 184.5 668 S[197] 7980 184.5 702 S[231] 7504 184.5 635 S[164] 8442 309.5 669 S[198] 7966 309.5 703 S[232] 7490 309.5	627	S[156]	8554	309.5	661	S[190]	8078	309.5	695	S[224]	7602	309.5
630 S[159] 8512 184.5 664 S[193] 8036 184.5 698 S[227] 7560 184.5 631 S[160] 8498 309.5 665 S[194] 8022 309.5 699 S[228] 7546 309.5 632 S[161] 8484 184.5 666 S[195] 8008 184.5 700 S[229] 7532 184.5 633 S[162] 8470 309.5 667 S[196] 7994 309.5 701 S[230] 7518 309.5 634 S[163] 8456 184.5 668 S[197] 7980 184.5 702 S[231] 7504 184.5 635 S[164] 8442 309.5 669 S[198] 7966 309.5 703 S[232] 7490 309.5 636 S[165] 8428 184.5 670 S[199] 7952 184.5 704 S[233] 7476 184.5	628	S[157]	8540	184.5	662	S[191]	8064	184.5	696	S[225]	7588	184.5
631 S[160] 8498 309.5 665 S[194] 8022 309.5 699 S[228] 7546 309.5 632 S[161] 8484 184.5 666 S[195] 8008 184.5 700 S[229] 7532 184.5 633 S[162] 8470 309.5 667 S[196] 7994 309.5 701 S[230] 7518 309.5 634 S[163] 8456 184.5 668 S[197] 7980 184.5 702 S[231] 7504 184.5 635 S[164] 8442 309.5 669 S[198] 7966 309.5 703 S[232] 7490 309.5 636 S[165] 8428 184.5 670 S[199] 7952 184.5 704 S[233] 7476 184.5 637 S[166] 8414 309.5 671 S[200] 7938 309.5 705 S[234] 7462 309.5	629	S[158]	8526	309.5	663	S[192]	8050	309.5	697	S[226]	7574	309.5
632 S[161] 8484 184.5 666 S[195] 8008 184.5 700 S[229] 7532 184.5 633 S[162] 8470 309.5 667 S[196] 7994 309.5 701 S[230] 7518 309.5 634 S[163] 8456 184.5 668 S[197] 7980 184.5 702 S[231] 7504 184.5 635 S[164] 8442 309.5 669 S[198] 7966 309.5 703 S[232] 7490 309.5 636 S[165] 8428 184.5 670 S[199] 7952 184.5 704 S[233] 7476 184.5 637 S[166] 8414 309.5 671 S[200] 7938 309.5 705 S[234] 7462 309.5 638 S[167] 8400 184.5 672 S[201] 7924 184.5 706 S[235] 7448 184.5	630	S[159]	8512	184.5	664	S[193]	8036	184.5	698	S[227]	7560	184.5
633 S[162] 8470 309.5 667 S[196] 7994 309.5 701 S[230] 7518 309.5 634 S[163] 8456 184.5 668 S[197] 7980 184.5 702 S[231] 7504 184.5 635 S[164] 8442 309.5 669 S[198] 7966 309.5 703 S[232] 7490 309.5 636 S[165] 8428 184.5 670 S[199] 7952 184.5 704 S[233] 7476 184.5 637 S[166] 8414 309.5 671 S[200] 7938 309.5 705 S[234] 7462 309.5 638 S[167] 8400 184.5 672 S[201] 7924 184.5 706 S[235] 7448 184.5	631	S[160]	8498	309.5	665	S[194]	8022	309.5	699	S[228]	7546	309.5
634 S[163] 8456 184.5 668 S[197] 7980 184.5 702 S[231] 7504 184.5 635 S[164] 8442 309.5 669 S[198] 7966 309.5 703 S[232] 7490 309.5 636 S[165] 8428 184.5 670 S[199] 7952 184.5 704 S[233] 7476 184.5 637 S[166] 8414 309.5 671 S[200] 7938 309.5 705 S[234] 7462 309.5 638 S[167] 8400 184.5 672 S[201] 7924 184.5 706 S[235] 7448 184.5	632	S[161]	8484	184.5	666	S[195]	8008	184.5	700	S[229]	7532	184.5
635 S[164] 8442 309.5 669 S[198] 7966 309.5 703 S[232] 7490 309.5 636 S[165] 8428 184.5 670 S[199] 7952 184.5 704 S[233] 7476 184.5 637 S[166] 8414 309.5 671 S[200] 7938 309.5 705 S[234] 7462 309.5 638 S[167] 8400 184.5 672 S[201] 7924 184.5 706 S[235] 7448 184.5	633	S[162]	8470	309.5	667	S[196]	7994	309.5	701	S[230]	7518	309.5
636 S[165] 8428 184.5 670 S[199] 7952 184.5 704 S[233] 7476 184.5 637 S[166] 8414 309.5 671 S[200] 7938 309.5 705 S[234] 7462 309.5 638 S[167] 8400 184.5 672 S[201] 7924 184.5 706 S[235] 7448 184.5	634	S[163]	8456	184.5	668	S[197]	7980	184.5	702	S[231]	7504	184.5
637 S[166] 8414 309.5 671 S[200] 7938 309.5 705 S[234] 7462 309.5 638 S[167] 8400 184.5 672 S[201] 7924 184.5 706 S[235] 7448 184.5	635	S[164]	8442	309.5	669	S[198]	7966	309.5	703	S[232]	7490	309.5
638 S[167] 8400 184.5 672 S[201] 7924 184.5 706 S[235] 7448 184.5	636	S[165]	8428	184.5	670	S[199]	7952	184.5	704	S[233]	7476	184.5
	637	S[166]	8414	309.5	671	S[200]	7938	309.5	705	S[234]	7462	309.5
630 \$[168] 8386 309.5 673 \$[202] 7910 309.5 707 \$[236] 7434 309.5	638	S[167]	8400	184.5	672	S[201]	7924	184.5	706	S[235]	7448	184.5
000 0[100] 0000 000.0 070 0[202] 7010 000.0 707 0[200] 7404 000.0	639	S[168]	8386	309.5	673	S[202]	7910	309.5	707	S[236]	7434	309.5
640 S[169] 8372 184.5 674 S[203] 7896 184.5 708 S[237] 7420 184.5	640	S[169]	8372	184.5	674	S[203]	7896	184.5	708	S[237]	7420	184.5

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PAD No. PIN Name X Y PAD No. PIN Name No. X PIN Name No. X PY 709 Sig2301 7406 3084 743 Sig271 6830 757 Sig3061 6454 309.5 711 Sig2401 7378 309.5 745 Sig271 6860 184.5 770 Sig3001 6460 309.5 712 Sig241 7360 309.5 747 Sig271 6860 184.5 760 Sig301 6461 184.5 713 Sig241 7360 309.5 747 Sig271 6860 184.5 780 Sig301 6364 309.5 781 Sig301 6874 309.5 781 Sig301 6874 309.5 781 Sig401 7304 184.5 782 Sig401 7334 184.5 782 Sig41 6864 309.5 783 Sig141 6334 309.5 781 Sig2801 6894 309.5 782 Sig4												
710 S[239] 7392 184.5 744 S[273] 6916 184.5 778 S[307] 6440 184.5 711 S[240] 7378 309.5 745 S[274] 6802 309.5 779 S[308] 6426 309.5 712 S[241] 7364 184.5 746 S[276] 6888 184.5 780 S[309] 6412 184.5 713 S[242] 7390 309.5 747 S[276] 6860 184.5 780 S[381] 684.1 184.5 780 S[371] 6860 184.5 782 S[311] 6384 184.5 780 S[279] 6852 184.5 784 S[313] 6366 184.5 784 S[313] 6366 184.5 780 381.4 184.5 780 3820 6882 184.5 784 S[313] 6368 184.5 771 S[248] 7224 380.5 753 S[280] 6812 309.5 785		PIN Name	х	Y		PIN Name	х	Y		PIN Name	х	Y
T11 S[240] 7378 300.5 746 S[274] 6902 300.5 779 S[308] 6426 309.5 712 S[241] 7364 184.5 746 S[275] 6888 184.5 780 S[309] 6412 184.5 713 S[242] 7350 309.5 747 S[276] 6874 309.5 781 S[310] 6388 309.5 714 S[243] 7336 184.5 748 S[277] 6860 184.5 782 S[311] 6384 184.5 716 S[244] 7322 309.5 750 S[279] 6632 184.5 764 S[313] 6356 184.5 716 S[246] 7294 309.5 751 S[280] 6816 309.5 787 S[314] 6932 194.5 719 S[248] 7266 309.5 753 S[280] 6816 309.5 787 S[316] 6328 309.5	709	S[238]	7406	309.5	743	S[272]	6930	309.5	777	S[306]	6454	309.5
712 S[241] 7364 184.5 746 S[275] 6888 184.5 780 S[309] 6412 184.5 713 S[242] 7350 309.5 747 S[276] 6874 309.5 781 S[310] 6398 309.5 714 S[243] 7336 184.5 748 S[277] 6860 184.5 782 S[311] 6384 184.5 716 S[244] 7322 309.5 749 S[278] 6846 309.5 783 S[312] 6370 309.5 716 S[246] 7308 184.5 750 S[279] 6832 184.5 784 S[313] 6356 184.5 717 S[246] 7294 309.5 751 S[280] 6818 309.5 785 S[314] 6422 309.5 718 S[247] 7280 184.5 752 S[281] 6804 184.5 786 S[314] 6022 3125 7815 <t< td=""><td>710</td><td>S[239]</td><td>7392</td><td>184.5</td><td>744</td><td>S[273]</td><td>6916</td><td>184.5</td><td>778</td><td>S[307]</td><td>6440</td><td>184.5</td></t<>	710	S[239]	7392	184.5	744	S[273]	6916	184.5	778	S[307]	6440	184.5
713 S[242] 7350 309.5 747 S[276] 6874 309.5 781 S[310] 6398 309.5 714 S[243] 7336 184.5 748 S[277] 6860 184.5 762 S[311] 6384 184.5 715 S[244] 7322 309.5 749 S[278] 6846 309.5 783 S[312] 6370 309.5 716 S[245] 7308 184.5 750 S[278] 6832 184.5 784 S[313] 6366 184.5 717 S[246] 7294 309.5 751 S[280] 6818 309.5 785 S[314] 6342 309.5 718 S[247] 7260 184.5 752 S[281] 6804 184.5 786 S[314] 6342 309.5 753 S[282] 6790 309.5 787 S[316] 6342 309.5 753 S[282] 6790 309.5 783 S[317]	711	S[240]	7378	309.5	745	S[274]	6902	309.5	779	S[308]	6426	309.5
714 S[243] 7336 184.5 748 S[277] 6860 184.5 782 S[311] 6384 184.5 715 S[244] 7322 309.5 749 S[278] 6846 309.5 783 S[312] 6370 309.5 716 S[245] 7308 184.5 750 S[279] 6832 184.5 784 S[313] 6356 184.5 717 S[246] 7294 309.5 751 S[280] 6818 309.5 785 S[314] 6342 309.5 718 S[247] 7280 184.5 752 S[281] 6804 184.5 786 S[315] 6322 184.5 719 S[248] 7268 309.5 753 S[282] 6790 309.5 787 S[316] 6314 309.5 720 S[249] 7252 184.5 754 S[283] 6776 184.5 788 S[317] 6300 184.5	712	S[241]	7364	184.5	746	S[275]	6888	184.5	780	S[309]	6412	184.5
715 S[244] 7322 309.5 749 S[278] 6846 309.5 783 S[312] 6370 309.5 716 S[245] 7308 184.5 750 S[279] 6832 184.5 784 S[313] 6356 184.5 717 S[246] 7294 309.5 751 S[280] 6818 309.5 785 S[314] 6342 309.5 718 S[247] 7280 184.5 752 S[281] 6804 184.5 786 S[315] 6328 184.5 719 S[248] 7266 309.5 753 S[282] 6790 309.5 787 S[316] 6304 184.5 788 S[317] 6300 184.5 720 S[248] 7222 184.5 754 S[283] 6776 184.5 788 S[317] 6300 184.5 721 S[250] 7238 309.5 755 S[284] 6762 309.5 789 <t< td=""><td>713</td><td>S[242]</td><td>7350</td><td>309.5</td><td>747</td><td>S[276]</td><td>6874</td><td>309.5</td><td>781</td><td>S[310]</td><td>6398</td><td>309.5</td></t<>	713	S[242]	7350	309.5	747	S[276]	6874	309.5	781	S[310]	6398	309.5
716 S[245] 7308 184.5 750 S[279] 6832 184.5 764 S[313] 6356 184.5 717 S[246] 7294 309.5 751 S[280] 6818 309.5 765 S[314] 6342 309.5 718 S[247] 7280 184.5 752 S[281] 6804 184.5 766 S[315] 6328 184.5 719 S[248] 7266 309.5 753 S[282] 6790 309.5 787 S[316] 6314 309.5 720 S[249] 7252 184.5 754 S[283] 6776 184.5 768 S[317] 6300 184.5 721 S[250] 7238 309.5 755 S[284] 6762 309.5 789 S[318] 6286 309.5 722 S[251] 7210 309.5 757 S[286] 6748 184.5 790 S[319] 6272 184.5	714	S[243]	7336	184.5	748	S[277]	6860	184.5	782	S[311]	6384	184.5
717 S[246] 7294 309.5 751 S[280] 6818 309.5 785 S[314] 6342 309.5 718 S[247] 7280 184.5 752 S[281] 6804 184.5 786 S[315] 6328 184.5 719 S[248] 7266 309.5 753 S[282] 6790 309.5 787 S[316] 6314 309.5 720 S[249] 7252 184.5 754 S[283] 6776 184.5 788 S[317] 6300 184.5 721 S[250] 7238 309.5 755 S[284] 6762 309.5 789 S[318] 6266 309.5 722 S[251] 7224 184.5 756 S[285] 6748 184.5 790 S[319] 6272 184.5 723 S[252] 7210 309.5 757 S[286] 6720 184.5 792 S[321] 6244 184.5	715	S[244]	7322	309.5	749	S[278]	6846	309.5	783	S[312]	6370	309.5
778 S[247] 7280 184.5 752 S[281] 6804 184.5 786 S[315] 6328 184.5 779 S[248] 7266 309.5 753 S[282] 6790 309.5 787 S[316] 6314 309.5 720 S[249] 7252 184.5 754 S[283] 6776 184.5 788 S[317] 6300 184.5 721 S[250] 7238 309.5 755 S[284] 6762 309.5 789 S[318] 6226 309.5 722 S[251] 7224 184.5 756 S[286] 6734 309.5 791 S[320] 6228 309.5 723 S[252] 7210 309.5 757 S[286] 6734 309.5 791 S[320] 6228 309.5 724 S[253] 7196 184.5 758 S[287] 6720 184.5 792 S[321] 6244 184.5	716	S[245]	7308	184.5	750	S[279]	6832	184.5	784	S[313]	6356	184.5
719 S[248] 7266 309.5 753 S[282] 6790 309.5 787 S[316] 6314 309.5 720 S[249] 7252 184.5 754 S[283] 6776 184.5 788 S[317] 6300 184.5 721 S[250] 7238 309.5 755 S[284] 6762 309.5 789 S[318] 6226 309.5 722 S[251] 7224 184.5 756 S[285] 6748 184.5 790 S[319] 6272 184.5 723 S[252] 7210 309.5 757 S[286] 6734 309.5 791 S[320] 6258 309.5 724 S[253] 7196 184.5 758 S[287] 6720 184.5 792 S[321] 6244 184.5 725 S[254] 7182 309.5 759 S[288] 6706 309.5 793 S[322] 6230 309.5	717	S[246]	7294	309.5	751	S[280]	6818	309.5	785	S[314]	6342	309.5
720 S[249] 7252 184.5 754 S[283] 6776 184.5 768 S[317] 6300 184.5 721 S[250] 7238 309.5 755 S[284] 6762 309.5 789 S[318] 6286 309.5 722 S[251] 7224 184.5 756 S[285] 6748 184.5 790 S[319] 6272 184.5 723 S[252] 7210 309.5 757 S[286] 6734 309.5 791 S[320] 6258 309.5 724 S[253] 7196 184.5 758 S[287] 6720 184.5 792 S[3211] 6244 184.5 725 S[264] 7182 309.5 759 S[288] 6706 309.5 793 S[322] 6230 309.5 726 S[255] 7168 184.5 760 S[289] 6692 184.5 794 S[323] 6216 184.5 <td< td=""><td>718</td><td>S[247]</td><td>7280</td><td>184.5</td><td>752</td><td>S[281]</td><td>6804</td><td>184.5</td><td>786</td><td>S[315]</td><td>6328</td><td>184.5</td></td<>	718	S[247]	7280	184.5	752	S[281]	6804	184.5	786	S[315]	6328	184.5
721 S[250] 7238 309.5 755 S[284] 6762 309.5 789 S[318] 6286 309.5 722 S[251] 7224 184.5 756 S[285] 6748 184.5 790 S[319] 6272 184.5 723 S[252] 7210 309.5 757 S[286] 6734 309.5 791 S[320] 6258 309.5 724 S[253] 7196 184.5 758 S[287] 6720 184.5 792 S[321] 6244 184.5 725 S[254] 7182 309.5 759 S[288] 6706 309.5 793 S[322] 6230 309.5 726 S[255] 7168 184.5 760 S[288] 6692 184.5 794 S[323] 6216 184.5 727 S[256] 7154 309.5 761 S[290] 6678 309.5 795 S[324] 6202 309.5	719	S[248]	7266	309.5	753	S[282]	6790	309.5	787	S[316]	6314	309.5
722 S[251] 7224 184.5 756 S[285] 6748 184.5 790 S[319] 6272 184.5 723 S[252] 7210 309.5 757 S[286] 6734 309.5 791 S[320] 6258 309.5 724 S[253] 7196 184.5 758 S[287] 6720 184.5 792 S[321] 6244 184.5 725 S[254] 7182 309.5 759 S[288] 6706 309.5 793 S[322] 6230 309.5 726 S[255] 7168 184.5 760 S[289] 6692 184.5 794 S[323] 6216 184.5 727 S[256] 7154 309.5 761 S[290] 6678 309.5 795 S[324] 6202 309.5 728 S[257] 7140 184.5 762 S[291] 6664 184.5 796 S[325] 6188 184.5	720	S[249]	7252	184.5	754	S[283]	6776	184.5	788	S[317]	6300	184.5
723 S[252] 7210 309.5 757 S[286] 6734 309.5 791 S[320] 6258 309.5 724 S[253] 7196 184.5 758 S[287] 6720 184.5 792 S[321] 6244 184.5 725 S[254] 7182 309.5 759 S[288] 6706 309.5 793 S[322] 6230 309.5 726 S[255] 7168 184.5 760 S[289] 6692 184.5 794 S[323] 6216 184.5 727 S[256] 7154 309.5 761 S[290] 6678 309.5 795 S[324] 6202 309.5 728 S[257] 7140 184.5 762 S[291] 6664 184.5 796 S[325] 6188 184.5 729 S[258] 7126 309.5 763 S[292] 6650 309.5 797 S[326] 6174 309.5	721	S[250]	7238	309.5	755	S[284]	6762	309.5	789	S[318]	6286	309.5
724 S[253] 7196 184.5 758 S[287] 6720 184.5 792 S[321] 6244 184.5 725 S[254] 7182 309.5 759 S[288] 6706 309.5 793 S[322] 6230 309.5 726 S[255] 7168 184.5 760 S[289] 6692 184.5 794 S[323] 6216 184.5 727 S[256] 7154 309.5 761 S[290] 6678 309.5 795 S[324] 6202 309.5 728 S[257] 7140 184.5 762 S[291] 6664 184.5 796 S[325] 6188 184.5 729 S[258] 7112 184.5 762 S[291] 6660 309.5 797 S[326] 6174 309.5 730 S[259] 7112 184.5 764 S[293] 6636 184.5 798 S[327] 6160 184.5	722	S[251]	7224	184.5	756	S[285]	6748	184.5	790	S[319]	6272	184.5
725 S[254] 7182 309.5 759 S[288] 6706 309.5 793 S[322] 6230 309.5 726 S[255] 7168 184.5 760 S[289] 6692 184.5 794 S[323] 6216 184.5 727 S[256] 7154 309.5 761 S[290] 6678 309.5 795 S[324] 6202 309.5 728 S[257] 7140 184.5 762 S[291] 6664 184.5 796 S[325] 6188 184.5 729 S[258] 7126 309.5 763 S[292] 6650 309.5 797 S[326] 6174 309.5 730 S[259] 7112 184.5 764 S[293] 6636 184.5 798 S[327] 6160 184.5 731 S[260] 7098 309.5 765 S[294] 6622 309.5 799 S[328] 6146 309.5	723	S[252]	7210	309.5	757	S[286]	6734	309.5	791	S[320]	6258	309.5
726 S[255] 7168 184.5 760 S[289] 6692 184.5 794 S[323] 6216 184.5 727 S[256] 7154 309.5 761 S[290] 6678 309.5 795 S[324] 6202 309.5 728 S[257] 7140 184.5 762 S[291] 6664 184.5 796 S[325] 6188 184.5 729 S[258] 7126 309.5 763 S[292] 6650 309.5 797 S[326] 6174 309.5 730 S[259] 7112 184.5 764 S[293] 6636 184.5 798 S[327] 6160 184.5 731 S[260] 7098 309.5 765 S[294] 6622 309.5 799 S[328] 6146 309.5 732 S[261] 7084 184.5 766 S[295] 6608 184.5 800 S[329] 6132 184.5	724	S[253]	7196	184.5	758	S[287]	6720	184.5	792	S[321]	6244	184.5
727 S[256] 7154 309.5 761 S[290] 6678 309.5 795 S[324] 6202 309.5 728 S[257] 7140 184.5 762 S[291] 6664 184.5 796 S[325] 6188 184.5 729 S[258] 7126 309.5 763 S[292] 6650 309.5 797 S[326] 6174 309.5 730 S[259] 7112 184.5 764 S[293] 6636 184.5 798 S[327] 6160 184.5 731 S[260] 7098 309.5 765 S[294] 6622 309.5 799 S[328] 6146 309.5 732 S[261] 7084 184.5 766 S[295] 6608 184.5 800 S[329] 6132 184.5 733 S[262] 7070 309.5 767 S[296] 6594 309.5 801 S[330] 6118 309.5	725	S[254]	7182	309.5	759	S[288]	6706	309.5	793	S[322]	6230	309.5
728 S[257] 7140 184.5 762 S[291] 6664 184.5 796 S[325] 6188 184.5 729 S[258] 7126 309.5 763 S[292] 6650 309.5 797 S[326] 6174 309.5 730 S[259] 7112 184.5 764 S[293] 6636 184.5 798 S[327] 6160 184.5 731 S[260] 7098 309.5 765 S[294] 6622 309.5 799 S[328] 6146 309.5 732 S[261] 7084 184.5 766 S[295] 6608 184.5 800 S[329] 6132 184.5 733 S[262] 7070 309.5 767 S[296] 6594 309.5 801 S[330] 6118 309.5 734 S[263] 7056 184.5 768 S[297] 6580 184.5 802 S[331] 6104 184.5	726	S[255]	7168	184.5	760	S[289]	6692	184.5	794	S[323]	6216	184.5
729 S[258] 7126 309.5 763 S[292] 6650 309.5 797 S[326] 6174 309.5 730 S[259] 7112 184.5 764 S[293] 6636 184.5 798 S[327] 6160 184.5 731 S[260] 7098 309.5 765 S[294] 6622 309.5 799 S[328] 6146 309.5 732 S[261] 7084 184.5 766 S[295] 6608 184.5 800 S[329] 6132 184.5 733 S[262] 7070 309.5 767 S[296] 6594 309.5 801 S[330] 6118 309.5 734 S[263] 7056 184.5 768 S[297] 6580 184.5 802 S[331] 6104 184.5 735 S[264] 7042 309.5 769 S[298] 6566 309.5 803 S[332] 6090 309.5	727	S[256]	7154	309.5	761	S[290]	6678	309.5	795	S[324]	6202	309.5
730 S[259] 7112 184.5 764 S[293] 6636 184.5 798 S[327] 6160 184.5 731 S[260] 7098 309.5 765 S[294] 6622 309.5 799 S[328] 6146 309.5 732 S[261] 7084 184.5 766 S[295] 6608 184.5 800 S[329] 6132 184.5 733 S[262] 7070 309.5 767 S[296] 6594 309.5 801 S[330] 6118 309.5 734 S[263] 7056 184.5 768 S[297] 6580 184.5 802 S[331] 6104 184.5 735 S[264] 7042 309.5 769 S[298] 6566 309.5 803 S[332] 6090 309.5 736 S[265] 7028 184.5 770 S[299] 6552 184.5 804 S[333] 6076 184.5	728	S[257]	7140	184.5	762	S[291]	6664	184.5	796	S[325]	6188	184.5
731 S[260] 7098 309.5 765 S[294] 6622 309.5 799 S[328] 6146 309.5 732 S[261] 7084 184.5 766 S[295] 6608 184.5 800 S[329] 6132 184.5 733 S[262] 7070 309.5 767 S[296] 6594 309.5 801 S[330] 6118 309.5 734 S[263] 7056 184.5 768 S[297] 6580 184.5 802 S[331] 6104 184.5 735 S[264] 7042 309.5 769 S[298] 6566 309.5 803 S[332] 6090 309.5 736 S[265] 7028 184.5 770 S[299] 6552 184.5 804 S[333] 6076 184.5 737 S[266] 7014 309.5 771 S[300] 6538 309.5 805 S[334] 6062 309.5	729	S[258]	7126	309.5	763	S[292]	6650	309.5	797	S[326]	6174	309.5
732 S[261] 7084 184.5 766 S[295] 6608 184.5 800 S[329] 6132 184.5 733 S[262] 7070 309.5 767 S[296] 6594 309.5 801 S[330] 6118 309.5 734 S[263] 7056 184.5 768 S[297] 6580 184.5 802 S[331] 6104 184.5 735 S[264] 7042 309.5 769 S[298] 6566 309.5 803 S[332] 6090 309.5 736 S[265] 7028 184.5 770 S[299] 6552 184.5 804 S[333] 6076 184.5 737 S[266] 7014 309.5 771 S[300] 6538 309.5 805 S[334] 6062 309.5 738 S[267] 7000 184.5 772 S[301] 6524 184.5 806 S[335] 6048 184.5	730	S[259]	7112	184.5	764	S[293]	6636	184.5	798	S[327]	6160	184.5
733 S[262] 7070 309.5 767 S[296] 6594 309.5 801 S[330] 6118 309.5 734 S[263] 7056 184.5 768 S[297] 6580 184.5 802 S[331] 6104 184.5 735 S[264] 7042 309.5 769 S[298] 6566 309.5 803 S[332] 6090 309.5 736 S[265] 7028 184.5 770 S[299] 6552 184.5 804 S[333] 6076 184.5 737 S[266] 7014 309.5 771 S[300] 6538 309.5 805 S[334] 6062 309.5 738 S[267] 7000 184.5 772 S[301] 6524 184.5 806 S[335] 6048 184.5 739 S[268] 6986 309.5 773 S[302] 6510 309.5 807 S[336] 6034 309.5	731	S[260]	7098	309.5	765	S[294]	6622	309.5	799	S[328]	6146	309.5
734 S[263] 7056 184.5 768 S[297] 6580 184.5 802 S[331] 6104 184.5 735 S[264] 7042 309.5 769 S[298] 6566 309.5 803 S[332] 6090 309.5 736 S[265] 7028 184.5 770 S[299] 6552 184.5 804 S[333] 6076 184.5 737 S[266] 7014 309.5 771 S[300] 6538 309.5 805 S[334] 6062 309.5 738 S[267] 7000 184.5 772 S[301] 6524 184.5 806 S[335] 6048 184.5 739 S[268] 6986 309.5 773 S[302] 6510 309.5 807 S[336] 6034 309.5 740 S[269] 6972 184.5 774 S[303] 6496 184.5 808 S[337] 6020 184.5	732	S[261]	7084	184.5	766	S[295]	6608	184.5	800	S[329]	6132	184.5
735 S[264] 7042 309.5 769 S[298] 6566 309.5 803 S[332] 6090 309.5 736 S[265] 7028 184.5 770 S[299] 6552 184.5 804 S[333] 6076 184.5 737 S[266] 7014 309.5 771 S[300] 6538 309.5 805 S[334] 6062 309.5 738 S[267] 7000 184.5 772 S[301] 6524 184.5 806 S[335] 6048 184.5 739 S[268] 6986 309.5 773 S[302] 6510 309.5 807 S[336] 6034 309.5 740 S[269] 6972 184.5 774 S[303] 6496 184.5 808 S[337] 6020 184.5 741 S[270] 6958 309.5 775 S[304] 6482 309.5 809 S[338] 6006 309.5	733	S[262]	7070	309.5	767	S[296]	6594	309.5	801	S[330]	6118	309.5
736 S[265] 7028 184.5 770 S[299] 6552 184.5 804 S[333] 6076 184.5 737 S[266] 7014 309.5 771 S[300] 6538 309.5 805 S[334] 6062 309.5 738 S[267] 7000 184.5 772 S[301] 6524 184.5 806 S[335] 6048 184.5 739 S[268] 6986 309.5 773 S[302] 6510 309.5 807 S[336] 6034 309.5 740 S[269] 6972 184.5 774 S[303] 6496 184.5 808 S[337] 6020 184.5 741 S[270] 6958 309.5 775 S[304] 6482 309.5 809 S[338] 6006 309.5	734	S[263]	7056	184.5	768	S[297]	6580	184.5	802	S[331]	6104	184.5
737 S[266] 7014 309.5 771 S[300] 6538 309.5 805 S[334] 6062 309.5 738 S[267] 7000 184.5 772 S[301] 6524 184.5 806 S[335] 6048 184.5 739 S[268] 6986 309.5 773 S[302] 6510 309.5 807 S[336] 6034 309.5 740 S[269] 6972 184.5 774 S[303] 6496 184.5 808 S[337] 6020 184.5 741 S[270] 6958 309.5 775 S[304] 6482 309.5 809 S[338] 6006 309.5	735	S[264]	7042	309.5	769	S[298]	6566	309.5	803	S[332]	6090	309.5
738 S[267] 7000 184.5 772 S[301] 6524 184.5 806 S[335] 6048 184.5 739 S[268] 6986 309.5 773 S[302] 6510 309.5 807 S[336] 6034 309.5 740 S[269] 6972 184.5 774 S[303] 6496 184.5 808 S[337] 6020 184.5 741 S[270] 6958 309.5 775 S[304] 6482 309.5 809 S[338] 6006 309.5	736	S[265]	7028	184.5	770	S[299]	6552	184.5	804	S[333]	6076	184.5
739 S[268] 6986 309.5 773 S[302] 6510 309.5 807 S[336] 6034 309.5 740 S[269] 6972 184.5 774 S[303] 6496 184.5 808 S[337] 6020 184.5 741 S[270] 6958 309.5 775 S[304] 6482 309.5 809 S[338] 6006 309.5	737	S[266]	7014	309.5	771	S[300]	6538	309.5	805	S[334]	6062	309.5
740 S[269] 6972 184.5 774 S[303] 6496 184.5 808 S[337] 6020 184.5 741 S[270] 6958 309.5 775 S[304] 6482 309.5 809 S[338] 6006 309.5	738	S[267]	7000	184.5	772	S[301]	6524	184.5	806	S[335]	6048	184.5
741 S[270] 6958 309.5 775 S[304] 6482 309.5 809 S[338] 6006 309.5	739	S[268]	6986	309.5	773	S[302]	6510	309.5	807	S[336]	6034	309.5
	740	S[269]	6972	184.5	774	S[303]	6496	184.5	808	S[337]	6020	184.5
742 S[271] 6944 184.5 776 S[305] 6468 184.5 810 S[339] 5992 184.5	741	S[270]	6958	309.5	775	S[304]	6482	309.5	809	S[338]	6006	309.5
	742	S[271]	6944	184.5	776	S[305]	6468	184.5	810	S[339]	5992	184.5

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PAD No. PIN Name No. X PAD No. PRAD No. PIN Name No. X PIN Name No. X PY No. PRAD No. PIN Name No. X Y 8111 SISH01 5978 308 863 31931 5562 308.5 879 S[6108] 6026 308.5 8112 SISH11 5980 3198.5 848 833771 5480 380.5 5810 54110 4888 309.5 8114 58343 5836 184.5 848 583771 5480 308.5 58111 4980 498.6 815 583441 5820 308.5 889 583791 5448 300.5 581413 4960 184.5 8116 583471 5880 184.5 580 308.5 58131 5840 584113 4960 496.5 812 583481 5866 308.5 58331 53321 580 581413 490.0 184.5 812 583481												
812 S[S41] 5964 184.5 846 S[375] 5488 184.5 880 S[409] 5012 184.5 813 S[342] 5950 309.5 847 S[376] 5474 309.5 881 S[410] 4998 309.5 814 S[343] 5936 184.5 848 S[377] 5460 184.5 882 S[411] 4984 184.5 816 S[344] 5922 309.5 849 S[378] 5446 309.5 883 S[412] 4970 309.5 816 S[344] 5908 184.5 880 S[379] 5432 184.5 884 S[413] 4966 104.5 817 S[346] 5868 309.5 851 S[300] 5418 309.5 885 S[414] 4942 309.5 818 S[347] 5880 399.5 883 S[414] 4942 309.5 818 S[347] 5880 5334]		PIN Name	х	Y		PIN Name	х	Y		PIN Name	х	Y
813 S[342] 5950 309.5 847 S[376] 5474 309.5 881 S[410] 4998 309.5 814 S[343] 5936 184.5 848 S[377] 5460 184.5 882 S[411] 4984 184.5 815 S[344] 5922 309.5 849 S[378] 5446 309.5 883 S[412] 4970 309.5 816 S[345] 5908 184.5 850 S[379] 5432 184.5 884 S[413] 4966 184.5 817 S[346] 5994 309.5 851 S[380] 5418 309.5 885 S[414] 4942 309.5 818 S[347] 5860 184.5 862 S[381] 5404 184.5 886 S[416] 4914 309.5 819 S[348] 5680 309.5 885 S[417] 4900 481.5 819 S[340] 5932 184.5	811	S[340]	5978	309.5	845	S[374]	5502	309.5	879	S[408]	5026	309.5
814 S[343] 5936 184.5 84B S[377] 5460 184.5 882 S[41] 4984 184.5 815 S[344] 5922 309.5 849 S[378] 5446 309.5 883 S[412] 4970 309.5 816 S[346] 5908 184.5 850 S[379] 5432 184.5 884 S[413] 4956 184.5 817 S[346] 5894 309.5 851 S[380] 5418 309.5 885 S[414] 4942 309.5 818 S[347] 5880 184.5 882 S[381] 5404 184.5 886 S[415] 4928 184.5 819 S[348] 5686 309.5 853 S[382] 5300 309.5 867 S[416] 4928 184.5 822 S[331] 5822 184.5 854 S[383] 5376 184.5 888 S[417] 4900 184.5 8	812	S[341]	5964	184.5	846	S[375]	5488	184.5	880	S[409]	5012	184.5
815 S[344] 5922 309.5 849 S[378] 5446 309.5 883 S[412] 4970 309.5 816 S[345] 5908 184.5 850 S[379] 5432 184.5 884 S[413] 4956 184.5 817 S[346] 5894 309.5 851 S[380] 5418 309.5 885 S[414] 4942 309.5 818 S[347] 5880 184.5 882 S[381] 5404 184.5 886 S[415] 4928 184.5 819 S[348] 5686 309.5 853 S[382] 5390 309.5 867 S[416] 4914 309.5 820 S[349] 5652 184.5 854 S[383] 5576 184.5 888 S[417] 4900 184.5 821 S[350] 5838 309.5 857 S[386] 5348 184.5 890 S[419] 4872 184.5	813	S[342]	5950	309.5	847	S[376]	5474	309.5	881	S[410]	4998	309.5
816 S[345] 5908 184.5 850 S[379] 5432 184.5 884 S[413] 4956 184.5 817 S[346] 5894 309.5 851 S[380] 5418 309.5 885 S[414] 4942 309.5 818 S[347] 5880 184.5 852 S[381] 5404 184.5 886 S[415] 4928 184.5 819 S[348] 5866 309.5 853 S[382] 5390 309.5 887 S[416] 4914 309.5 820 S[349] 5862 184.5 854 S[383] 5376 184.5 888 S[417] 4900 184.5 821 S[350] 5838 309.5 855 S[384] 5362 309.5 889 S[418] 486 309.5 822 S[351] 5824 184.5 856 S[385] 5348 184.5 890 S[418] 4872 184.5 8	814	S[343]	5936	184.5	848	S[377]	5460	184.5	882	S[411]	4984	184.5
817 Si346i 5894 309.5 851 Si380i 5418 309.5 865 Si441 4942 309.5 818 Si347i 5880 184.5 852 Si381i 5404 184.5 886 Si415i 4928 184.5 819 Si348i 5866 309.5 853 Si382i 5390 309.5 887 Si416i 4914 309.5 820 Si349i 5852 184.5 864 Si383i 5376 184.5 888 Si417i 4900 184.5 821 Si350i 5838 309.5 855 Si384j 5362 309.5 889 Si418j 4866 309.5 822 Si351i 5824 184.5 866 Si386j 5344 308.5 891 Si419j 4872 184.5 823 Si351i 580 309.5 867 Si386j 5334 308.5 891 Si421j 484.5 822 Si3	815	S[344]	5922	309.5	849	S[378]	5446	309.5	883	S[412]	4970	309.5
818 S[347] 5880 184.5 852 S[381] 5404 184.5 886 S[415] 4928 184.5 819 S[348] 5866 309.5 853 S[382] 5390 309.5 887 S[416] 4914 309.5 820 S[349] 5852 184.5 864 S[383] 5376 184.5 888 S[417] 4900 184.5 821 S[350] 5838 309.5 855 S[384] 5962 309.5 889 S[418] 4866 309.5 822 S[351] 5824 184.5 866 S[385] 5348 184.5 890 S[419] 4872 184.5 823 S[352] 5810 309.5 857 S[386] 5334 309.5 891 S[420] 4858 309.5 826 S[353] 5762 309.5 859 S[388] 5206 309.5 893 S[422] 4816 184.5	816	S[345]	5908	184.5	850	S[379]	5432	184.5	884	S[413]	4956	184.5
Big Signar Sabe Sabe Signar Signar	817	S[346]	5894	309.5	851	S[380]	5418	309.5	885	S[414]	4942	309.5
820 S[349] 5852 184.5 854 S[383] 5376 184.5 888 S[417] 4900 184.5 821 S[350] 5838 309.5 855 S[384] 5362 309.5 889 S[418] 4886 309.5 822 S[351] 5824 184.5 856 S[386] 5334 309.5 891 S[420] 4868 309.5 824 S[353] 5796 184.5 858 S[387] 5320 184.5 892 S[421] 4844 184.5 825 S[354] 5782 309.5 859 S[388] 5306 309.5 893 S[422] 4830 309.5 826 S[355] 5768 184.5 860 S[389] 5292 184.5 894 S[423] 4816 184.5 827 S[366] 5754 309.5 861 S[390] 5292 184.5 896 S[423] 4816 184.5	818	S[347]	5880	184.5	852	S[381]	5404	184.5	886	S[415]	4928	184.5
821 S[350] 5838 309.5 855 S[384] 5362 309.5 889 S[418] 4886 309.5 822 S[351] 5824 184.5 856 S[385] 5348 184.5 890 S[419] 4872 184.5 823 S[352] 5810 309.5 857 S[386] 5334 309.5 891 S[420] 4868 309.5 824 S[353] 5796 184.5 858 S[387] 5320 184.5 892 S[421] 4844 184.5 825 S[354] 5782 309.5 859 S[388] 5306 309.5 893 S[422] 4830 309.5 826 S[355] 5768 184.5 860 S[389] 5292 184.5 894 S[423] 4816 184.5 827 S[356] 5754 309.5 861 S[390] 5278 309.5 895 S[424] 4802 309.5	819	S[348]	5866	309.5	853	S[382]	5390	309.5	887	S[416]	4914	309.5
822 S[351] 5824 184.5 856 S[385] 5348 184.5 890 S[419] 4872 184.5 823 S[352] 5810 309.5 857 S[386] 5334 309.5 891 S[420] 4858 309.5 824 S[353] 5796 184.5 858 S[387] 5320 184.5 892 S[421] 4844 184.5 825 S[354] 5782 309.5 859 S[388] 5306 309.5 893 S[422] 4830 309.5 826 S[355] 5768 184.5 860 S[389] 5292 184.5 894 S[423] 4816 184.5 827 S[356] 5754 309.5 861 S[390] 5278 309.5 895 S[424] 4802 309.5 828 S[357] 5740 184.5 862 S[391] 5264 184.5 896 S[425] 4788 184.5	820	S[349]	5852	184.5	854	S[383]	5376	184.5	888	S[417]	4900	184.5
823 \$\sqrt{352}\sigma\$ 5810 309.5 857 \$\sqrt{386}\sqrt{3}\$ 309.5 891 \$\sqrt{420}\sqrt{1}\$ 4858 309.5 824 \$\sqrt{353}\sqrt{3}\$ 5796 184.5 858 \$\sqrt{387}\sqrt{1}\$ 5320 184.5 892 \$\sqrt{421}\sqrt{1}\$ 4844 184.5 825 \$\sqrt{356}\sqrt{1}\$ 5782 309.5 859 \$\sqrt{388}\sqrt{1}\$ 5306 309.5 893 \$\sqrt{422}\sqrt{2}\$ 4830 309.5 826 \$\sqrt{356}\sqrt{1}\$ 5768 184.5 860 \$\sqrt{389}\sqrt{2}\$ 5292 184.5 894 \$\sqrt{423}\sqrt{2}\$ 4816 184.5 827 \$\sqrt{356}\sqrt{1}\$ 5754 309.5 861 \$\sqrt{390}\sqrt{2}\$ 5278 309.5 895 \$\sqrt{421}\sqrt{4}\$ 4802 309.5 828 \$\sqrt{357}\sqrt{1}\$ 5740 184.5 862 \$\sqrt{391}\sqrt{526} 309.5 897 \$\sqrt{426}\sqrt{1}\$ 4774 309.5 830 \$\sqrt{359}\sqrt{1}\$ 5712 1	821	S[350]	5838	309.5	855	S[384]	5362	309.5	889	S[418]	4886	309.5
824 S[353] 5796 184.5 858 S[387] 5320 184.5 892 S[421] 4844 184.5 825 S[354] 5782 309.5 859 S[388] 5306 309.5 893 S[422] 4830 309.5 826 S[355] 5768 184.5 860 S[389] 5292 184.5 894 S[423] 4816 184.5 827 S[356] 5754 309.5 861 S[390] 5278 309.5 895 S[424] 4802 309.5 828 S[357] 5740 184.5 862 S[391] 5264 184.5 896 S[425] 4788 184.5 829 S[358] 5726 309.5 863 S[392] 5250 309.5 897 S[426] 4774 309.5 830 S[359] 5712 184.5 864 S[393] 5236 184.5 898 S[427] 4760 184.5	822	S[351]	5824	184.5	856	S[385]	5348	184.5	890	S[419]	4872	184.5
825 S[354] 5782 309.5 859 S[388] 5306 309.5 893 S[422] 4830 309.5 826 S[355] 5768 184.5 860 S[389] 5292 184.5 894 S[423] 4816 184.5 827 S[356] 5754 309.5 861 S[390] 5278 309.5 895 S[424] 4802 309.5 828 S[357] 5740 184.5 862 S[391] 5264 184.5 896 S[425] 4788 184.5 829 S[358] 5726 309.5 863 S[392] 5250 309.5 897 S[426] 4774 309.5 830 S[359] 5712 184.5 864 S[393] 5236 184.5 898 S[427] 4760 184.5 831 S[360] 5698 309.5 865 S[394] 5222 309.5 899 S[428] 4746 309.5	823	S[352]	5810	309.5	857	S[386]	5334	309.5	891	S[420]	4858	309.5
826 S[355] 5768 184.5 860 S[389] 5292 184.5 894 S[423] 4816 184.5 827 S[356] 5754 309.5 861 S[390] 5278 309.5 895 S[424] 4802 309.5 828 S[357] 5740 184.5 862 S[391] 5264 184.5 896 S[425] 4788 184.5 829 S[358] 5726 309.5 863 S[392] 5250 309.5 897 S[426] 4774 309.5 830 S[359] 5712 184.5 864 S[393] 5236 184.5 898 S[427] 4760 184.5 831 S[360] 5698 309.5 865 S[394] 5222 309.5 899 S[428] 4746 309.5 832 S[361] 5684 184.5 866 S[395] 5208 184.5 900 S[429] 4732 184.5	824	S[353]	5796	184.5	858	S[387]	5320	184.5	892	S[421]	4844	184.5
827 S[356] 5754 309.5 861 S[390] 5278 309.5 895 S[424] 4802 309.5 828 S[357] 5740 184.5 862 S[391] 5264 184.5 896 S[425] 4788 184.5 829 S[358] 5726 309.5 863 S[392] 5250 309.5 897 S[426] 4774 309.5 830 S[359] 5712 184.5 864 S[393] 5236 184.5 898 S[427] 4760 184.5 831 S[360] 5698 309.5 865 S[394] 5222 309.5 899 S[428] 4746 309.5 832 S[361] 5684 184.5 866 S[395] 5208 184.5 900 S[429] 4732 184.5 833 S[362] 5670 309.5 867 S[396] 5194 309.5 901 S[430] 4718 309.5	825	S[354]	5782	309.5	859	S[388]	5306	309.5	893	S[422]	4830	309.5
828 S[357] 5740 184.5 862 S[391] 5264 184.5 896 S[425] 4788 184.5 829 S[358] 5726 309.5 863 S[392] 5250 309.5 897 S[426] 4774 309.5 830 S[359] 5712 184.5 864 S[393] 5236 184.5 898 S[427] 4760 184.5 831 S[360] 5698 309.5 865 S[394] 5222 309.5 899 S[428] 4746 309.5 832 S[361] 5684 184.5 866 S[395] 5208 184.5 900 S[429] 4732 184.5 833 S[362] 5670 309.5 867 S[396] 5194 309.5 901 S[430] 4718 309.5 834 S[363] 5656 184.5 868 S[397] 5180 184.5 902 S[431] 4704 184.5	826	S[355]	5768	184.5	860	S[389]	5292	184.5	894	S[423]	4816	184.5
829 S[358] 5726 309.5 863 S[392] 5250 309.5 897 S[426] 4774 309.5 830 S[359] 5712 184.5 864 S[393] 5236 184.5 898 S[427] 4760 184.5 831 S[360] 5698 309.5 865 S[394] 5222 309.5 899 S[428] 4746 309.5 832 S[361] 5684 184.5 866 S[395] 5208 184.5 900 S[429] 4732 184.5 833 S[362] 5670 309.5 867 S[396] 5194 309.5 901 S[430] 4718 309.5 834 S[363] 5656 184.5 868 S[397] 5180 184.5 902 S[431] 4704 184.5 835 S[364] 5642 309.5 869 S[398] 5166 309.5 903 S[432] 4690 309.5	827	S[356]	5754	309.5	861	S[390]	5278	309.5	895	S[424]	4802	309.5
830 S[359] 5712 184.5 864 S[393] 5236 184.5 898 S[427] 4760 184.5 831 S[360] 5698 309.5 865 S[394] 5222 309.5 899 S[428] 4746 309.5 832 S[361] 5684 184.5 866 S[395] 5208 184.5 900 S[429] 4732 184.5 833 S[362] 5670 309.5 867 S[396] 5194 309.5 901 S[430] 4718 309.5 834 S[363] 5656 184.5 868 S[397] 5180 184.5 902 S[431] 4704 184.5 835 S[364] 5642 309.5 869 S[398] 5166 309.5 903 S[432] 4690 309.5 836 S[365] 5628 184.5 870 S[399] 5152 184.5 904 S[433] 4676 184.5	828	S[357]	5740	184.5	862	S[391]	5264	184.5	896	S[425]	4788	184.5
831 S[360] 5698 309.5 865 S[394] 5222 309.5 899 S[428] 4746 309.5 832 S[361] 5684 184.5 866 S[395] 5208 184.5 900 S[429] 4732 184.5 833 S[362] 5670 309.5 867 S[396] 5194 309.5 901 S[430] 4718 309.5 834 S[363] 5656 184.5 868 S[397] 5180 184.5 902 S[431] 4704 184.5 835 S[364] 5642 309.5 869 S[398] 5166 309.5 903 S[432] 4690 309.5 836 S[365] 5628 184.5 870 S[399] 5152 184.5 904 S[433] 4676 184.5 837 S[366] 5614 309.5 871 S[400] 5138 309.5 905 S[434] 4662 309.5	829	S[358]	5726	309.5	863	S[392]	5250	309.5	897	S[426]	4774	309.5
832 S[361] 5684 184.5 866 S[395] 5208 184.5 900 S[429] 4732 184.5 833 S[362] 5670 309.5 867 S[396] 5194 309.5 901 S[430] 4718 309.5 834 S[363] 5656 184.5 868 S[397] 5180 184.5 902 S[431] 4704 184.5 835 S[364] 5642 309.5 869 S[398] 5166 309.5 903 S[432] 4690 309.5 836 S[365] 5628 184.5 870 S[399] 5152 184.5 904 S[433] 4676 184.5 837 S[366] 5614 309.5 871 S[400] 5138 309.5 905 S[434] 4662 309.5 838 S[367] 5600 184.5 872 S[401] 5124 184.5 906 S[435] 4648 184.5	830	S[359]	5712	184.5	864	S[393]	5236	184.5	898	S[427]	4760	184.5
833 S[362] 5670 309.5 867 S[396] 5194 309.5 901 S[430] 4718 309.5 834 S[363] 5656 184.5 868 S[397] 5180 184.5 902 S[431] 4704 184.5 835 S[364] 5642 309.5 869 S[398] 5166 309.5 903 S[432] 4690 309.5 836 S[365] 5628 184.5 870 S[399] 5152 184.5 904 S[433] 4676 184.5 837 S[366] 5614 309.5 871 S[400] 5138 309.5 905 S[434] 4662 309.5 838 S[367] 5600 184.5 872 S[401] 5124 184.5 906 S[435] 4648 184.5 839 S[368] 5586 309.5 873 S[402] 5110 309.5 907 S[436] 4634 309.5	831	S[360]	5698	309.5	865	S[394]	5222	309.5	899	S[428]	4746	309.5
834 S[363] 5656 184.5 868 S[397] 5180 184.5 902 S[431] 4704 184.5 835 S[364] 5642 309.5 869 S[398] 5166 309.5 903 S[432] 4690 309.5 836 S[365] 5628 184.5 870 S[399] 5152 184.5 904 S[433] 4676 184.5 837 S[366] 5614 309.5 871 S[400] 5138 309.5 905 S[434] 4662 309.5 838 S[367] 5600 184.5 872 S[401] 5124 184.5 906 S[435] 4648 184.5 839 S[368] 5586 309.5 873 S[402] 5110 309.5 907 S[436] 4634 309.5 840 S[369] 5572 184.5 874 S[403] 5096 184.5 908 S[437] 4620 184.5	832	S[361]	5684	184.5	866	S[395]	5208	184.5	900	S[429]	4732	184.5
835 S[364] 5642 309.5 869 S[398] 5166 309.5 903 S[432] 4690 309.5 836 S[365] 5628 184.5 870 S[399] 5152 184.5 904 S[433] 4676 184.5 837 S[366] 5614 309.5 871 S[400] 5138 309.5 905 S[434] 4662 309.5 838 S[367] 5600 184.5 872 S[401] 5124 184.5 906 S[435] 4648 184.5 839 S[368] 5586 309.5 873 S[402] 5110 309.5 907 S[436] 4634 309.5 840 S[369] 5572 184.5 874 S[403] 5096 184.5 908 S[437] 4620 184.5 841 S[370] 5558 309.5 875 S[404] 5082 309.5 909 S[438] 4606 309.5	833	S[362]	5670	309.5	867	S[396]	5194	309.5	901	S[430]	4718	309.5
836 S[365] 5628 184.5 870 S[399] 5152 184.5 904 S[433] 4676 184.5 837 S[366] 5614 309.5 871 S[400] 5138 309.5 905 S[434] 4662 309.5 838 S[367] 5600 184.5 872 S[401] 5124 184.5 906 S[435] 4648 184.5 839 S[368] 5586 309.5 873 S[402] 5110 309.5 907 S[436] 4634 309.5 840 S[369] 5572 184.5 874 S[403] 5096 184.5 908 S[437] 4620 184.5 841 S[370] 5558 309.5 875 S[404] 5082 309.5 909 S[438] 4606 309.5 842 S[371] 5544 184.5 876 S[405] 5068 184.5 910 S[439] 4592 184.5	834	S[363]	5656	184.5	868	S[397]	5180	184.5	902	S[431]	4704	184.5
837 S[366] 5614 309.5 871 S[400] 5138 309.5 905 S[434] 4662 309.5 838 S[367] 5600 184.5 872 S[401] 5124 184.5 906 S[435] 4648 184.5 839 S[368] 5586 309.5 873 S[402] 5110 309.5 907 S[436] 4634 309.5 840 S[369] 5572 184.5 874 S[403] 5096 184.5 908 S[437] 4620 184.5 841 S[370] 5558 309.5 875 S[404] 5082 309.5 909 S[438] 4606 309.5 842 S[371] 5544 184.5 876 S[405] 5068 184.5 910 S[439] 4592 184.5 843 S[372] 5530 309.5 877 S[406] 5054 309.5 911 S[440] 4578 309.5	835	S[364]	5642	309.5	869	S[398]	5166	309.5	903	S[432]	4690	309.5
838 S[367] 5600 184.5 872 S[401] 5124 184.5 906 S[435] 4648 184.5 839 S[368] 5586 309.5 873 S[402] 5110 309.5 907 S[436] 4634 309.5 840 S[369] 5572 184.5 874 S[403] 5096 184.5 908 S[437] 4620 184.5 841 S[370] 5558 309.5 875 S[404] 5082 309.5 909 S[438] 4606 309.5 842 S[371] 5544 184.5 876 S[405] 5068 184.5 910 S[439] 4592 184.5 843 S[372] 5530 309.5 877 S[406] 5054 309.5 911 S[440] 4578 309.5	836	S[365]	5628	184.5	870	S[399]	5152	184.5	904	S[433]	4676	184.5
839 S[368] 5586 309.5 873 S[402] 5110 309.5 907 S[436] 4634 309.5 840 S[369] 5572 184.5 874 S[403] 5096 184.5 908 S[437] 4620 184.5 841 S[370] 5558 309.5 875 S[404] 5082 309.5 909 S[438] 4606 309.5 842 S[371] 5544 184.5 876 S[405] 5068 184.5 910 S[439] 4592 184.5 843 S[372] 5530 309.5 877 S[406] 5054 309.5 911 S[440] 4578 309.5	837	S[366]	5614	309.5	871	S[400]	5138	309.5	905	S[434]	4662	309.5
840 S[369] 5572 184.5 874 S[403] 5096 184.5 908 S[437] 4620 184.5 841 S[370] 5558 309.5 875 S[404] 5082 309.5 909 S[438] 4606 309.5 842 S[371] 5544 184.5 876 S[405] 5068 184.5 910 S[439] 4592 184.5 843 S[372] 5530 309.5 877 S[406] 5054 309.5 911 S[440] 4578 309.5	838	S[367]	5600	184.5	872	S[401]	5124	184.5	906	S[435]	4648	184.5
841 S[370] 5558 309.5 875 S[404] 5082 309.5 909 S[438] 4606 309.5 842 S[371] 5544 184.5 876 S[405] 5068 184.5 910 S[439] 4592 184.5 843 S[372] 5530 309.5 877 S[406] 5054 309.5 911 S[440] 4578 309.5	839	S[368]	5586	309.5	873	S[402]	5110	309.5	907	S[436]	4634	309.5
842 S[371] 5544 184.5 876 S[405] 5068 184.5 910 S[439] 4592 184.5 843 S[372] 5530 309.5 877 S[406] 5054 309.5 911 S[440] 4578 309.5	840	S[369]	5572	184.5	874	S[403]	5096	184.5	908	S[437]	4620	184.5
843 S[372] 5530 309.5 877 S[406] 5054 309.5 911 S[440] 4578 309.5	841	S[370]	5558	309.5	875	S[404]	5082	309.5	909	S[438]	4606	309.5
	842	S[371]	5544	184.5	876	S[405]	5068	184.5	910	S[439]	4592	184.5
844 S[373] 5516 184.5 878 S[407] 5040 184.5 912 S[441] 4564 184.5	843	S[372]	5530	309.5	877	S[406]	5054	309.5	911	S[440]	4578	309.5
	844	S[373]	5516	184.5	878	S[407]	5040	184.5	912	S[441]	4564	184.5

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PAD No. PIN Name No. X Y PAD No. PIN Name No. Y PAD No. PIN Name No. X Y 913 SI6441 4556 305 947 SI4471 4040 4050 1815 1816 1814 1400 1814.5 1816 308.5 1816 308.5 1816 308.5 1816 309.5 1816 308.6 1816 309.5 1816 309.5 1816 309.5 1816 309.5 1816 309.5 1816 309.5 1816 309.5 1816 309.5												
914 S[443] 4536 184.5 948 S[477] 4060 184.5 982 S[511] 3584 184.5 915 S[444] 4522 309.5 949 S[478] 4046 309.5 983 S[512] 3570 309.5 916 S[445] 4508 184.5 950 S[478] 4046 309.5 983 S[512] 3570 309.5 917 S[446] 4494 309.5 951 S[480] 4018 309.5 985 S[514] 3522 309.5 918 S[447] 4490 184.5 962 S[481] 4004 184.5 986 S[516] 3514 309.5 919 S[448] 4466 309.5 963 S[483] 3976 184.5 988 S[517] 3500 184.5 922 S[451] 4428 184.5 965 S[484] 3962 39.5 989 S[518] 3472 184.5 9		PIN Name	x	Y		PIN Name	х	Y		PIN Name	х	Y
915 S[444] 4522 309.5 949 S[478] 4046 309.5 983 S[512] 3570 309.5 916 S[445] 4508 184.5 960 S[479] 4032 184.5 984 S[513] 3566 184.5 917 S[446] 4494 309.5 961 S[480] 4018 309.5 985 S[514] 3522 309.5 918 S[447] 4480 184.5 962 S[481] 4004 184.5 986 S[515] 3528 184.5 919 S[448] 4466 309.5 963 S[482] 3990 309.5 987 S[516] 3514 309.5 920 S[444] 4452 184.5 966 S[483] 3976 184.5 988 S[517] 3500 184.5 921 S[452] 4410 309.5 967 S[486] 3304 309.5 991 S[521] 3442 184.5	913	S[442]	4550	309.5	947	S[476]	4074	309.5	981	S[510]	3598	309.5
916 S[445] 4508 184.5 990 S[479] 4032 194.5 984 S[513] 3566 184.5 917 S[446] 4494 309.5 961 S[480] 4018 309.5 965 S[514] 3542 309.5 918 S[447] 4480 184.5 962 S[481] 4004 184.5 966 S[515] 3528 184.5 919 S[448] 4466 309.5 963 S[482] 3990 309.5 987 S[516] 3514 305.5 920 S[449] 4452 184.5 965 S[485] 3948 184.5 988 S[516] 3486 309.5 922 S[451] 4424 184.5 966 S[485] 3948 194.5 990 S[519] 3472 184.5 922 S[451] 4400 309.5 966 S[485] 3934 309.5 991 S[520] 3488 309.5	914	S[443]	4536	184.5	948	S[477]	4060	184.5	982	S[511]	3584	184.5
917 S[446] 4494 309.5 951 S[480] 4018 309.5 985 S[514] 3542 309.5 918 S[447] 4490 184.5 952 S[481] 4004 184.5 986 S[515] 3528 184.5 919 S[448] 4466 309.5 953 S[482] 3990 309.5 987 S[516] 3514 309.5 920 S[449] 4452 184.5 964 S[483] 3976 184.5 988 S[517] 3500 184.5 921 S[450] 4438 309.5 956 S[486] 309.5 989 S[518] 3486 309.5 922 S[451] 4424 184.5 966 S[486] 3394 309.5 991 S[520] 3486 309.5 922 S[453] 4396 184.5 966 S[487] 3220 184.5 992 S[521] 3444 184.5 922 S	915	S[444]	4522	309.5	949	S[478]	4046	309.5	983	S[512]	3570	309.5
918 S[447] 4480 184.5 952 S[481] 4004 184.5 986 S[515] 3528 184.5 919 S[448] 4466 309.5 953 S[482] 3990 309.5 987 S[516] 3514 309.5 920 S[449] 4452 184.5 954 S[483] 3976 184.5 988 S[517] 3500 184.5 921 S[450] 4438 309.5 955 S[484] 3962 309.5 989 S[518] 3486 309.5 922 S[451] 4424 184.5 956 S[486] 3934 309.5 991 S[519] 3472 184.5 923 S[452] 4410 309.5 958 S[488] 390.5 991 S[520] 3458 309.5 926 S[454] 4382 309.5 959 S[488] 390.6 290.5 952 3440 344.5 390.5 992 S[489]	916	S[445]	4508	184.5	950	S[479]	4032	184.5	984	S[513]	3556	184.5
919 S 448 4466 309.5 953 S 482 3990 309.5 987 S 516 3514 309.5 920 S 449 4452 184.5 954 S 483 3976 184.5 988 S 517 3500 184.5 921 S 450 4438 309.5 955 S 484 3962 309.5 989 S 518 3486 309.5 922 S 451 4424 184.5 956 S 486 3934 184.5 990 S 519 3472 184.5 923 S 452 4410 309.5 957 S 486 3934 309.5 991 S 520 3488 309.5 924 S 453 4336 184.5 968 S 487 3920 184.5 992 S 521 3440 184.5 926 S 456 4354 309.5 969 S 489 3892 184.5 994 S 523 3416 184.5	917	S[446]	4494	309.5	951	S[480]	4018	309.5	985	S[514]	3542	309.5
920 S[449] 4452 184.5 954 S[483] 3976 184.5 988 S[517] 3500 184.5 921 S[450] 4438 309.5 955 S[484] 3962 309.5 989 S[518] 3486 309.5 922 S[451] 4424 184.5 966 S[485] 3948 184.5 990 S[519] 3472 184.5 923 S[452] 4410 309.5 957 S[486] 3934 309.5 991 S[520] 3458 309.5 924 S[453] 4396 184.5 958 S[487] 3920 184.5 992 S[521] 3444 184.5 925 S[456] 4386 184.5 960 S[489] 3892 184.5 994 S[523] 3416 184.5 926 S[456] 4354 309.5 961 S[490] 3878 309.5 S[524] 3402 309.5 928	918	S[447]	4480	184.5	952	S[481]	4004	184.5	986	S[515]	3528	184.5
921 Si450 4438 309.5 955 Si484 3962 309.5 989 Si518 3486 309.5 922 Si451 4424 184.5 956 Si485 3948 184.5 990 Si519 3472 184.5 923 Si452 4410 309.5 957 Si486 3934 309.5 991 Si520 3488 309.5 924 Si453 4396 184.5 958 Si487 3920 184.5 992 Si521 3444 184.5 925 Si454 4382 309.5 959 Si489 3892 184.5 994 Si523 3416 184.5 926 Si456 4354 309.5 961 Si490 3878 309.5 995 Si524 3402 309.5 928 Si457 4340 184.5 962 Si491 3864 184.5 996 Si525 3388 184.5	919	S[448]	4466	309.5	953	S[482]	3990	309.5	987	S[516]	3514	309.5
922 S[451] 4424 184.5 956 S[486] 3948 184.5 990 S[519] 3472 184.5 923 S[452] 4410 309.5 957 S[486] 3934 309.5 991 S[520] 3458 309.5 924 S[453] 4396 184.5 958 S[487] 3920 184.5 992 S[521] 3444 184.5 925 S[454] 4382 309.5 959 S[488] 390.5 993 S[522] 3430 309.5 926 S[455] 4368 184.5 960 S[489] 3892 184.5 994 S[523] 3416 184.5 927 S[456] 4354 309.5 962 S[491] 3864 184.5 996 S[525] 3388 184.5 929 S[458] 4312 184.5 962 S[491] 382 395. 997 S[526] 3374 309.5 930 S[4	920	S[449]	4452	184.5	954	S[483]	3976	184.5	988	S[517]	3500	184.5
923 S[452] 4410 309.5 957 S[486] 3934 309.5 991 S[520] 3458 309.5 924 S[453] 4396 184.5 958 S[487] 3920 184.5 992 S[521] 3444 184.5 925 S[454] 4382 309.5 959 S[488] 3906 309.5 993 S[522] 3430 309.5 926 S[455] 4368 184.5 960 S[489] 3892 184.5 994 S[523] 3416 184.5 927 S[456] 4354 309.5 961 S[490] 3878 309.5 995 S[524] 3402 309.5 928 S[457] 4340 184.5 962 S[491] 3864 184.5 996 S[526] 3374 309.5 930 S[458] 4312 184.5 964 S[493] 3836 184.5 998 S[527] 3360 184.5	921	S[450]	4438	309.5	955	S[484]	3962	309.5	989	S[518]	3486	309.5
924 S[453] 4396 184.5 958 S[487] 3920 184.5 992 S[521] 3444 184.5 925 S[454] 4382 399.5 959 S[488] 3906 309.5 993 S[522] 3430 309.5 926 S[455] 4368 184.5 960 S[489] 3892 184.5 994 S[523] 3416 184.5 927 S[456] 4354 309.5 961 S[490] 3878 309.5 995 S[524] 3402 309.5 928 S[457] 4340 184.5 962 S[491] 3864 184.5 996 S[525] 3388 184.5 929 S[458] 4326 309.5 963 S[492] 3850 309.5 997 S[526] 3374 309.5 930 S[459] 4312 184.5 964 S[493] 3836 184.5 998 S[528] 3346 309.5	922	S[451]	4424	184.5	956	S[485]	3948	184.5	990	S[519]	3472	184.5
925 S[454] 4382 309.5 959 S[488] 3906 309.5 993 S[522] 3430 309.5 926 S[455] 4368 184.5 960 S[489] 3892 184.5 994 S[523] 3416 184.5 927 S[456] 4354 309.5 961 S[490] 3878 309.5 995 S[524] 3402 309.5 928 S[457] 4340 184.5 962 S[491] 3864 184.5 996 S[525] 3388 184.5 929 S[458] 4326 309.5 963 S[492] 3850 309.5 997 S[526] 3374 309.5 930 S[459] 4312 184.5 964 S[493] 3836 184.5 998 S[527] 3360 184.5 931 S[460] 4298 309.5 965 S[494] 3822 309.5 1999 S[528] 3346 309.5 <td< td=""><td>923</td><td>S[452]</td><td>4410</td><td>309.5</td><td>957</td><td>S[486]</td><td>3934</td><td>309.5</td><td>991</td><td>S[520]</td><td>3458</td><td>309.5</td></td<>	923	S[452]	4410	309.5	957	S[486]	3934	309.5	991	S[520]	3458	309.5
926 S[455] 4368 184.5 960 S[489] 3892 184.5 994 S[523] 3416 184.5 927 S[456] 4354 309.5 961 S[490] 3878 309.5 995 S[524] 3402 309.5 928 S[457] 4340 184.5 962 S[491] 3864 184.5 996 S[525] 3388 184.5 929 S[458] 4326 309.5 963 S[492] 3850 309.5 997 S[526] 3374 309.5 930 S[459] 4312 184.5 964 S[493] 3836 184.5 998 S[527] 3360 184.5 931 S[460] 4298 309.5 965 S[494] 3822 309.5 999 S[528] 3346 309.5 1932 S[461] 4284 184.5 966 S[495] 3808 184.5 1000 S[529] 3332 184.5 933	924	S[453]	4396	184.5	958	S[487]	3920	184.5	992	S[521]	3444	184.5
927 S[456] 4354 309.5 961 S[490] 3878 309.5 995 S[524] 3402 309.5 928 S[457] 4340 184.5 962 S[491] 3864 184.5 996 S[525] 3388 184.5 929 S[458] 4326 309.5 963 S[492] 3850 309.5 997 S[526] 3374 309.5 930 S[459] 4312 184.5 964 S[493] 3836 184.5 998 S[527] 3360 184.5 931 S[460] 4298 309.5 965 S[494] 3822 309.5 999 S[528] 3346 309.5 932 S[461] 4284 184.5 966 S[495] 3808 184.5 1000 S[529] 3332 184.5 933 S[462] 4270 309.5 967 S[496] 3794 309.5 1001 S[530] 3318 309.5 <t< td=""><td>925</td><td>S[454]</td><td>4382</td><td>309.5</td><td>959</td><td>S[488]</td><td>3906</td><td>309.5</td><td>993</td><td>S[522]</td><td>3430</td><td>309.5</td></t<>	925	S[454]	4382	309.5	959	S[488]	3906	309.5	993	S[522]	3430	309.5
928 S[457] 4340 184.5 962 S[491] 3864 184.5 996 S[525] 3388 184.5 929 S[458] 4326 309.5 963 S[492] 3850 309.5 997 S[526] 3374 309.5 930 S[459] 4312 184.5 964 S[493] 3836 184.5 998 S[527] 3360 184.5 931 S[460] 4298 309.5 965 S[494] 3822 309.5 999 S[528] 3346 309.5 932 S[461] 4284 184.5 966 S[495] 3808 184.5 1000 S[529] 3332 184.5 933 S[462] 4270 309.5 967 S[496] 3794 309.5 1001 S[530] 3318 309.5 934 S[463] 4256 184.5 968 S[497] 3780 184.5 1002 S[531] 3290 309.5 <	926	S[455]	4368	184.5	960	S[489]	3892	184.5	994	S[523]	3416	184.5
929 S[458] 4326 309.5 963 S[492] 3850 309.5 997 S[526] 3374 309.5 930 S[459] 4312 184.5 964 S[493] 3836 184.5 998 S[527] 3360 184.5 931 S[460] 4298 309.5 966 S[494] 3822 309.5 999 S[528] 3346 309.5 932 S[461] 4284 184.5 966 S[495] 3808 184.5 1000 S[529] 3332 184.5 933 S[462] 4270 309.5 967 S[496] 3794 309.5 1001 S[530] 3318 309.5 934 S[463] 4256 184.5 968 S[497] 3780 184.5 1002 S[531] 3304 184.5 935 S[464] 4242 309.5 969 S[498] 3766 309.5 1003 S[532] 3290 309.5	927	S[456]	4354	309.5	961	S[490]	3878	309.5	995	S[524]	3402	309.5
930 S[459] 4312 184.5 964 S[493] 3836 184.5 998 S[527] 3360 184.5 931 S[460] 4298 309.5 965 S[494] 3822 309.5 999 S[528] 3346 309.5 932 S[461] 4284 184.5 966 S[495] 3808 184.5 1000 S[529] 3332 184.5 933 S[462] 4270 309.5 967 S[496] 3794 309.5 1001 S[530] 3318 309.5 934 S[463] 4256 184.5 968 S[497] 3780 184.5 1002 S[531] 3304 184.5 935 S[464] 4242 309.5 969 S[498] 3766 309.5 1003 S[532] 3290 309.5 936 S[466] 4228 184.5 970 S[499] 3752 184.5 1004 S[533] 3276 184.5	928	S[457]	4340	184.5	962	S[491]	3864	184.5	996	S[525]	3388	184.5
931 S[460] 4298 309.5 965 S[494] 3822 309.5 999 S[528] 3346 309.5 932 S[461] 4284 184.5 966 S[495] 3808 184.5 1000 S[529] 3332 184.5 933 S[462] 4270 309.5 967 S[496] 3794 309.5 1001 S[530] 3318 309.5 934 S[463] 4256 184.5 968 S[497] 3780 184.5 1002 S[531] 3304 184.5 935 S[464] 4242 309.5 969 S[498] 3766 309.5 1003 S[532] 3290 309.5 936 S[465] 4228 184.5 970 S[499] 3752 184.5 1004 S[533] 3276 184.5 937 S[466] 4214 309.5 971 S[500] 3738 309.5 1005 S[534] 3262 309.5	929	S[458]	4326	309.5	963	S[492]	3850	309.5	997	S[526]	3374	309.5
932 S[461] 4284 184.5 966 S[495] 3808 184.5 1000 S[529] 3332 184.5 933 S[462] 4270 309.5 967 S[496] 3794 309.5 1001 S[530] 3318 309.5 934 S[463] 4256 184.5 968 S[497] 3780 184.5 1002 S[531] 3304 184.5 935 S[464] 4242 309.5 969 S[498] 3766 309.5 1003 S[532] 3290 309.5 936 S[465] 4228 184.5 970 S[499] 3752 184.5 1004 S[533] 3276 184.5 937 S[466] 4214 309.5 971 S[500] 3738 309.5 1005 S[534] 3262 309.5 938 S[467] 4200 184.5 972 S[501] 3724 184.5 1006 S[536] 3234 309.5	930	S[459]	4312	184.5	964	S[493]	3836	184.5	998	S[527]	3360	184.5
933 S[462] 4270 309.5 967 S[496] 3794 309.5 1001 S[530] 3318 309.5 934 S[463] 4256 184.5 968 S[497] 3780 184.5 1002 S[531] 3304 184.5 935 S[464] 4242 309.5 969 S[498] 3766 309.5 1003 S[532] 3290 309.5 936 S[465] 4228 184.5 970 S[499] 3752 184.5 1004 S[533] 3276 184.5 937 S[466] 4214 309.5 971 S[500] 3738 309.5 1005 S[534] 3262 309.5 938 S[467] 4200 184.5 972 S[501] 3724 184.5 1006 S[535] 3248 184.5 939 S[468] 4186 309.5 973 S[502] 3710 309.5 1007 S[536] 3234 309.5	931	S[460]	4298	309.5	965	S[494]	3822	309.5	999	S[528]	3346	309.5
934 S[463] 4256 184.5 968 S[497] 3780 184.5 1002 S[531] 3304 184.5 935 S[464] 4242 309.5 969 S[498] 3766 309.5 1003 S[532] 3290 309.5 936 S[465] 4228 184.5 970 S[499] 3752 184.5 1004 S[533] 3276 184.5 937 S[466] 4214 309.5 971 S[500] 3738 309.5 1005 S[534] 3262 309.5 938 S[467] 4200 184.5 972 S[501] 3724 184.5 1006 S[535] 3248 184.5 939 S[468] 4186 309.5 973 S[502] 3710 309.5 1007 S[536] 3234 309.5 940 S[469] 4172 184.5 974 S[503] 3696 184.5 1008 S[537] 3220 184.5	932	S[461]	4284	184.5	966	S[495]	3808	184.5	1000	S[529]	3332	184.5
935 S[464] 4242 309.5 969 S[498] 3766 309.5 1003 S[532] 3290 309.5 936 S[465] 4228 184.5 970 S[499] 3752 184.5 1004 S[533] 3276 184.5 937 S[466] 4214 309.5 971 S[500] 3738 309.5 1005 S[534] 3262 309.5 938 S[467] 4200 184.5 972 S[501] 3724 184.5 1006 S[535] 3248 184.5 939 S[468] 4186 309.5 973 S[502] 3710 309.5 1007 S[536] 3234 309.5 940 S[469] 4172 184.5 974 S[503] 3696 184.5 1008 S[537] 3220 184.5 941 S[470] 4158 309.5 975 S[504] 3682 309.5 1009 S[538] 3206 309.5	933	S[462]	4270	309.5	967	S[496]	3794	309.5	1001	S[530]	3318	309.5
936 S[465] 4228 184.5 970 S[499] 3752 184.5 1004 S[533] 3276 184.5 937 S[466] 4214 309.5 971 S[500] 3738 309.5 1005 S[534] 3262 309.5 938 S[467] 4200 184.5 972 S[501] 3724 184.5 1006 S[535] 3248 184.5 939 S[468] 4186 309.5 973 S[502] 3710 309.5 1007 S[536] 3234 309.5 940 S[469] 4172 184.5 974 S[503] 3696 184.5 1008 S[537] 3220 184.5 941 S[470] 4158 309.5 975 S[504] 3682 309.5 1009 S[538] 3206 309.5 942 S[471] 4144 184.5 976 S[505] 3668 184.5 1010 S[539] 3192 184.5	934	S[463]	4256	184.5	968	S[497]	3780	184.5	1002	S[531]	3304	184.5
937 S[466] 4214 309.5 971 S[500] 3738 309.5 1005 S[534] 3262 309.5 938 S[467] 4200 184.5 972 S[501] 3724 184.5 1006 S[535] 3248 184.5 939 S[468] 4186 309.5 973 S[502] 3710 309.5 1007 S[536] 3234 309.5 940 S[469] 4172 184.5 974 S[503] 3696 184.5 1008 S[537] 3220 184.5 941 S[470] 4158 309.5 975 S[504] 3682 309.5 1009 S[538] 3206 309.5 942 S[471] 4144 184.5 976 S[505] 3668 184.5 1010 S[539] 3192 184.5 943 S[472] 4130 309.5 977 S[506] 3654 309.5 1011 S[540] 3178 309.5	935	S[464]	4242	309.5	969	S[498]	3766	309.5	1003	S[532]	3290	309.5
938 S[467] 4200 184.5 972 S[501] 3724 184.5 1006 S[535] 3248 184.5 939 S[468] 4186 309.5 973 S[502] 3710 309.5 1007 S[536] 3234 309.5 940 S[469] 4172 184.5 974 S[503] 3696 184.5 1008 S[537] 3220 184.5 941 S[470] 4158 309.5 975 S[504] 3682 309.5 1009 S[538] 3206 309.5 942 S[471] 4144 184.5 976 S[505] 3668 184.5 1010 S[539] 3192 184.5 943 S[472] 4130 309.5 977 S[506] 3654 309.5 1011 S[540] 3178 309.5 944 S[473] 4116 184.5 978 S[507] 3640 184.5 1012 S[541] 3164 184.5	936	S[465]	4228	184.5	970	S[499]	3752	184.5	1004	S[533]	3276	184.5
939 S[468] 4186 309.5 973 S[502] 3710 309.5 1007 S[536] 3234 309.5 940 S[469] 4172 184.5 974 S[503] 3696 184.5 1008 S[537] 3220 184.5 941 S[470] 4158 309.5 975 S[504] 3682 309.5 1009 S[538] 3206 309.5 942 S[471] 4144 184.5 976 S[505] 3668 184.5 1010 S[539] 3192 184.5 943 S[472] 4130 309.5 977 S[506] 3654 309.5 1011 S[540] 3178 309.5 944 S[473] 4116 184.5 978 S[507] 3640 184.5 1012 S[541] 3164 184.5 945 S[474] 4102 309.5 979 S[508] 3626 309.5 1013 S[542] 3150 309.5	937	S[466]	4214	309.5	971	S[500]	3738	309.5	1005	S[534]	3262	309.5
940 S[469] 4172 184.5 974 S[503] 3696 184.5 1008 S[537] 3220 184.5 941 S[470] 4158 309.5 975 S[504] 3682 309.5 1009 S[538] 3206 309.5 942 S[471] 4144 184.5 976 S[505] 3668 184.5 1010 S[539] 3192 184.5 943 S[472] 4130 309.5 977 S[506] 3654 309.5 1011 S[540] 3178 309.5 944 S[473] 4116 184.5 978 S[507] 3640 184.5 1012 S[541] 3164 184.5 945 S[474] 4102 309.5 979 S[508] 3626 309.5 1013 S[542] 3150 309.5	938	S[467]	4200	184.5	972	S[501]	3724	184.5	1006	S[535]	3248	184.5
941 S[470] 4158 309.5 975 S[504] 3682 309.5 1009 S[538] 3206 309.5 942 S[471] 4144 184.5 976 S[505] 3668 184.5 1010 S[539] 3192 184.5 943 S[472] 4130 309.5 977 S[506] 3654 309.5 1011 S[540] 3178 309.5 944 S[473] 4116 184.5 978 S[507] 3640 184.5 1012 S[541] 3164 184.5 945 S[474] 4102 309.5 979 S[508] 3626 309.5 1013 S[542] 3150 309.5	939	S[468]	4186	309.5	973	S[502]	3710	309.5	1007	S[536]	3234	309.5
942 S[471] 4144 184.5 976 S[505] 3668 184.5 1010 S[539] 3192 184.5 943 S[472] 4130 309.5 977 S[506] 3654 309.5 1011 S[540] 3178 309.5 944 S[473] 4116 184.5 978 S[507] 3640 184.5 1012 S[541] 3164 184.5 945 S[474] 4102 309.5 979 S[508] 3626 309.5 1013 S[542] 3150 309.5	940	S[469]	4172	184.5	974	S[503]	3696	184.5	1008	S[537]	3220	184.5
943 S[472] 4130 309.5 977 S[506] 3654 309.5 1011 S[540] 3178 309.5 944 S[473] 4116 184.5 978 S[507] 3640 184.5 1012 S[541] 3164 184.5 945 S[474] 4102 309.5 979 S[508] 3626 309.5 1013 S[542] 3150 309.5	941	S[470]	4158	309.5	975	S[504]	3682	309.5	1009	S[538]	3206	309.5
944 S[473] 4116 184.5 978 S[507] 3640 184.5 1012 S[541] 3164 184.5 945 S[474] 4102 309.5 979 S[508] 3626 309.5 1013 S[542] 3150 309.5	942	S[471]	4144	184.5	976	S[505]	3668	184.5	1010	S[539]	3192	184.5
945 S[474] 4102 309.5 979 S[508] 3626 309.5 1013 S[542] 3150 309.5	943	S[472]	4130	309.5	977	S[506]	3654	309.5	1011	S[540]	3178	309.5
	944	S[473]	4116	184.5	978	S[507]	3640	184.5	1012	S[541]	3164	184.5
946 S[475] 4088 184.5 980 S[509] 3612 184.5 1014 S[543] 3136 184.5	945	S[474]	4102	309.5	979	S[508]	3626	309.5	1013	S[542]	3150	309.5
	946	S[475]	4088	184.5	980	S[509]	3612	184.5	1014	S[543]	3136	184.5

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PAD No. PIN Name X Y PAD No. PIN Name X Y PAD No. PIN Name X 1015 S[544] 3122 309.5 1049 S[578] 2646 309.5 1083 S[612] 2170 1016 S[545] 3108 184.5 1050 S[579] 2632 184.5 1084 S[613] 2156 1017 S[546] 3094 309.5 1051 S[580] 2618 309.5 1085 S[614] 2142 1018 S[547] 3080 184.5 1052 S[581] 2604 184.5 1086 S[615] 2128 1019 S[548] 3066 309.5 1053 S[582] 2590 309.5 1087 S[616] 2114 1020 S[549] 3052 184.5 1054 S[583] 2576 184.5 1088 S[617] 2100	Y 309.5 184.5 309.5 184.5 309.5
1016 S[545] 3108 184.5 1050 S[579] 2632 184.5 1084 S[613] 2156 1017 S[546] 3094 309.5 1051 S[580] 2618 309.5 1085 S[614] 2142 1018 S[547] 3080 184.5 1052 S[581] 2604 184.5 1086 S[615] 2128 1019 S[548] 3066 309.5 1053 S[582] 2590 309.5 1087 S[616] 2114	184.5 309.5 184.5
1017 S[546] 3094 309.5 1051 S[580] 2618 309.5 1085 S[614] 2142 1018 S[547] 3080 184.5 1052 S[581] 2604 184.5 1086 S[615] 2128 1019 S[548] 3066 309.5 1053 S[582] 2590 309.5 1087 S[616] 2114	309.5 184.5
1018 S[547] 3080 184.5 1052 S[581] 2604 184.5 1086 S[615] 2128 1019 S[548] 3066 309.5 1053 S[582] 2590 309.5 1087 S[616] 2114	184.5
1019 S[548] 3066 309.5 1053 S[582] 2590 309.5 1087 S[616] 2114	
	309.5
1020 S[549] 3052 184.5 1054 S[583] 2576 184.5 1088 S[617] 2100	
	184.5
1021 S[550] 3038 309.5 1055 S[584] 2562 309.5 1089 S[618] 2086	309.5
1022 S[551] 3024 184.5 1056 S[585] 2548 184.5 1090 S[619] 2072	184.5
1023 S[552] 3010 309.5 1057 S[586] 2534 309.5 1091 S[620] 2058	309.5
1024 S[553] 2996 184.5 1058 S[587] 2520 184.5 1092 S[621] 2044	184.5
1025 S[554] 2982 309.5 1059 S[588] 2506 309.5 1093 S[622] 2030	309.5
1026 S[555] 2968 184.5 1060 S[589] 2492 184.5 1094 S[623] 2016	184.5
1027 S[556] 2954 309.5 1061 S[590] 2478 309.5 1095 S[624] 2002	309.5
1028 S[557] 2940 184.5 1062 S[591] 2464 184.5 1096 S[625] 1988	184.5
1029 S[558] 2926 309.5 1063 S[592] 2450 309.5 1097 S[626] 1974	309.5
1030 S[559] 2912 184.5 1064 S[593] 2436 184.5 1098 S[627] 1960	184.5
1031 S[560] 2898 309.5 1065 S[594] 2422 309.5 1099 S[628] 1946	309.5
1032 S[561] 2884 184.5 1066 S[595] 2408 184.5 1100 S[629] 1932	184.5
1033 S[562] 2870 309.5 1067 S[596] 2394 309.5 1101 S[630] 1918	309.5
1034 S[563] 2856 184.5 1068 S[597] 2380 184.5 1102 S[631] 1904	184.5
1035 S[564] 2842 309.5 1069 S[598] 2366 309.5 1103 S[632] 1890	309.5
1036 S[565] 2828 184.5 1070 S[599] 2352 184.5 1104 S[633] 1876	184.5
1037 S[566] 2814 309.5 1071 S[600] 2338 309.5 1105 S[634] 1862	309.5
1038 S[567] 2800 184.5 1072 S[601] 2324 184.5 1106 S[635] 1848	184.5
1039 S[568] 2786 309.5 1073 S[602] 2310 309.5 1107 S[636] 1834	309.5
1040 S[569] 2772 184.5 1074 S[603] 2296 184.5 1108 S[637] 1820	184.5
1041 S[570] 2758 309.5 1075 S[604] 2282 309.5 1109 S[638] 1806	309.5
1042 S[571] 2744 184.5 1076 S[605] 2268 184.5 1110 S[639] 1792	184.5
1043 S[572] 2730 309.5 1077 S[606] 2254 309.5 1111 S[640] 1778	309.5
1044 S[573] 2716 184.5 1078 S[607] 2240 184.5 1112 S[641] 1764	184.5
1045 S[574] 2702 309.5 1079 S[608] 2226 309.5 1113 S[642] 1750	309.5
1046 S[575] 2688 184.5 1080 S[609] 2212 184.5 1114 S[643] 1736	184.5
1047 S[576] 2674 309.5 1081 S[610] 2198 309.5 1115 S[644] 1722	309.5
1048 S[577] 2660 184.5 1082 S[611] 2184 184.5 1116 S[645] 1708	184.5

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PAD No.	PIN Name	x	Y	PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y
1117	S[646]	1694	309.5	1151	S[680]	1218	309.5	1185	S[714]	742	309.5
1118	S[647]	1680	184.5	1152	S[681]	1204	184.5	1186	S[715]	728	184.5
1119	S[648]	1666	309.5	1153	S[682]	1190	309.5	1187	S[716]	714	309.5
1120	S[649]	1652	184.5	1154	S[683]	1176	184.5	1188	S[717]	700	184.5
1121	S[650]	1638	309.5	1155	S[684]	1162	309.5	1189	S[718]	686	309.5
1122	S[651]	1624	184.5	1156	S[685]	1148	184.5	1190	S[719]	672	184.5
1123	S[652]	1610	309.5	1157	S[686]	1134	309.5	1191	S[720]	658	309.5
1124	S[653]	1596	184.5	1158	S[687]	1120	184.5	1192	DMY	644	184.5
1125	S[654]	1582	309.5	1159	S[688]	1106	309.5	1193	DMY	630	309.5
1126	S[655]	1568	184.5	1160	S[689]	1092	184.5	1194	DMY	616	184.5
1127	S[656]	1554	309.5	1161	S[690]	1078	309.5	1195	DMY	602	309.5
1128	S[657]	1540	184.5	1162	S[691]	1064	184.5	1196	DMY	588	184.5
1129	S[658]	1526	309.5	1163	S[692]	1050	309.5	1197	DMY	574	309.5
1130	S[659]	1512	184.5	1164	S[693]	1036	184.5	1198	DMY	560	184.5
1131	S[660]	1498	309.5	1165	S[694]	1022	309.5	1199	DMY	546	309.5
1132	S[661]	1484	184.5	1166	S[695]	1008	184.5	1200	DMY	532	184.5
1133	S[662]	1470	309.5	1167	S[696]	994	309.5	1201	DMY	518	309.5
1134	S[663]	1456	184.5	1168	S[697]	980	184.5	1202	DMY	504	184.5
1135	S[664]	1442	309.5	1169	S[698]	966	309.5	1203	DMY	490	309.5
1136	S[665]	1428	184.5	1170	S[699]	952	184.5	1204	DMY	476	184.5
1137	S[666]	1414	309.5	1171	S[700]	938	309.5	1205	DMY	462	309.5
1138	S[667]	1400	184.5	1172	S[701]	924	184.5	1206	DMY	448	184.5
1139	S[668]	1386	309.5	1173	S[702]	910	309.5	1207	DMY	434	309.5
1140	S[669]	1372	184.5	1174	S[703]	896	184.5	1208	DMY	420	184.5
1141	S[670]	1358	309.5	1175	S[704]	882	309.5	1209	DMY	406	309.5
1142	S[671]	1344	184.5	1176	S[705]	868	184.5	1210	DMY	392	184.5
1143	S[672]	1330	309.5	1177	S[706]	854	309.5	1211	DMY	378	309.5
1144	S[673]	1316	184.5	1178	S[707]	840	184.5	1212	DMY	364	184.5
1145	S[674]	1302	309.5	1179	S[708]	826	309.5	1213	DMY	350	309.5
1146	S[675]	1288	184.5	1180	S[709]	812	184.5	1214	DMY	336	184.5
1147	S[676]	1274	309.5	1181	S[710]	798	309.5	1215	DMY	322	309.5
1148	S[677]	1260	184.5	1182	S[711]	784	184.5	1216	DMY	308	184.5
1149	S[678]	1246	309.5	1183	S[712]	770	309.5	1217	DMY	294	309.5
1150	S[679]	1232	184.5	1184	S[713]	756	184.5	1218	DMY	280	184.5

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PAD				PAD				PAD			
No.	PIN Name	Х	Y	No.	PIN Name	Х	Y	No.	PIN Name	Х	Y
1219	DMY	266	309.5	1253	S[733]	-210	309.5	1287	S[767]	-686	309.5
1220	DMY	252	184.5	1254	S[734]	-224	184.5	1288	S[768]	-700	184.5
1221	DMY	238	309.5	1255	S[735]	-238	309.5	1289	S[769]	-714	309.5
1222	DMY	224	184.5	1256	S[736]	-252	184.5	1290	S[770]	-728	184.5
1223	DMY	210	309.5	1257	S[737]	-266	309.5	1291	S[771]	-742	309.5
1224	DMY	196	184.5	1258	S[738]	-280	184.5	1292	S[772]	-756	184.5
1225	DMY	182	309.5	1259	S[739]	-294	309.5	1293	S[773]	-770	309.5
1226	DMY	168	184.5	1260	S[740]	-308	184.5	1294	S[774]	-784	184.5
1227	DMY	154	309.5	1261	S[741]	-322	309.5	1295	S[775]	-798	309.5
1228	DMY	140	184.5	1262	S[742]	-336	184.5	1296	S[776]	-812	184.5
1229	DMY	126	309.5	1263	S[743]	-350	309.5	1297	S[777]	-826	309.5
1230	DMY	112	184.5	1264	S[744]	-364	184.5	1298	S[778]	-840	184.5
1231	DMY	98	309.5	1265	S[745]	-378	309.5	1299	S[779]	-854	309.5
1232	DMY	84	184.5	1266	S[746]	-392	184.5	1300	S[780]	-868	184.5
1233	DMY	70	309.5	1267	S[747]	-406	309.5	1301	S[781]	-882	309.5
1234	DMY	56	184.5	1268	S[748]	-420	184.5	1302	S[782]	-896	184.5
1235	DMY	42	309.5	1269	S[749]	-434	309.5	1303	S[783]	-910	309.5
1236	DMY	28	184.5	1270	S[750]	-448	184.5	1304	S[784]	-924	184.5
1237	DMY	14	309.5	1271	S[751]	-462	309.5	1305	S[785]	-938	309.5
1238	DMY	0	184.5	1272	S[752]	-476	184.5	1306	S[786]	-952	184.5
1239	DMY	-14	309.5	1273	S[753]	-490	309.5	1307	S[787]	-966	309.5
1240	DMY	-28	184.5	1274	S[754]	-504	184.5	1308	S[788]	-980	184.5
1241	S[721]	-42	309.5	1275	S[755]	-518	309.5	1309	S[789]	-994	309.5
1242	S[722]	-56	184.5	1276	S[756]	-532	184.5	1310	S[790]	-1008	184.5
1243	S[723]	-70	309.5	1277	S[757]	-546	309.5	1311	S[791]	-1022	309.5
1244	S[724]	-84	184.5	1278	S[758]	-560	184.5	1312	S[792]	-1036	184.5
1245	S[725]	-98	309.5	1279	S[759]	-574	309.5	1313	S[793]	-1050	309.5
1246	S[726]	-112	184.5	1280	S[760]	-588	184.5	1314	S[794]	-1064	184.5
1247	S[727]	-126	309.5	1281	S[761]	-602	309.5	1315	S[795]	-1078	309.5
1248	S[728]	-140	184.5	1282	S[762]	-616	184.5	1316	S[796]	-1092	184.5
1249	S[729]	-154	309.5	1283	S[763]	-630	309.5	1317	S[797]	-1106	309.5
1250	S[730]	-168	184.5	1284	S[764]	-644	184.5	1318	S[798]	-1120	184.5
1251	S[731]	-182	309.5	1285	S[765]	-658	309.5	1319	S[799]	-1134	309.5
1252	S[732]	-196	184.5	1286	S[766]	-672	184.5	1320	S[800]	-1148	184.5

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PAD				PAD				PAD			
No.	PIN Name	Х	Y	No.	PIN Name	Х	Y	No.	PIN Name	Х	Y
1321	S[801]	-1162	309.5	1355	S[835]	-1638	309.5	1389	S[869]	-2114	309.5
1322	S[802]	-1176	184.5	1356	S[836]	-1652	184.5	1390	S[870]	-2128	184.5
1323	S[803]	-1190	309.5	1357	S[837]	-1666	309.5	1391	S[871]	-2142	309.5
1324	S[804]	-1204	184.5	1358	S[838]	-1680	184.5	1392	S[872]	-2156	184.5
1325	S[805]	-1218	309.5	1359	S[839]	-1694	309.5	1393	S[873]	-2170	309.5
1326	S[806]	-1232	184.5	1360	S[840]	-1708	184.5	1394	S[874]	-2184	184.5
1327	S[807]	-1246	309.5	1361	S[841]	-1722	309.5	1395	S[875]	-2198	309.5
1328	S[808]	-1260	184.5	1362	S[842]	-1736	184.5	1396	S[876]	-2212	184.5
1329	S[809]	-1274	309.5	1363	S[843]	-1750	309.5	1397	S[877]	-2226	309.5
1330	S[810]	-1288	184.5	1364	S[844]	-1764	184.5	1398	S[878]	-2240	184.5
1331	S[811]	-1302	309.5	1365	S[845]	-1778	309.5	1399	S[879]	-2254	309.5
1332	S[812]	-1316	184.5	1366	S[846]	-1792	184.5	1400	S[880]	-2268	184.5
1333	S[813]	-1330	309.5	1367	S[847]	-1806	309.5	1401	S[881]	-2282	309.5
1334	S[814]	-1344	184.5	1368	S[848]	-1820	184.5	1402	S[882]	-2296	184.5
1335	S[815]	-1358	309.5	1369	S[849]	-1834	309.5	1403	S[883]	-2310	309.5
1336	S[816]	-1372	184.5	1370	S[850]	-1848	184.5	1404	S[884]	-2324	184.5
1337	S[817]	-1386	309.5	1371	S[851]	-1862	309.5	1405	S[885]	-2338	309.5
1338	S[818]	-1400	184.5	1372	S[852]	-1876	184.5	1406	S[886]	-2352	184.5
1339	S[819]	-1414	309.5	1373	S[853]	-1890	309.5	1407	S[887]	-2366	309.5
1340	S[820]	-1428	184.5	1374	S[854]	-1904	184.5	1408	S[888]	-2380	184.5
1341	S[821]	-1442	309.5	1375	S[855]	-1918	309.5	1409	S[889]	-2394	309.5
1342	S[822]	-1456	184.5	1376	S[856]	-1932	184.5	1410	S[890]	-2408	184.5
1343	S[823]	-1470	309.5	1377	S[857]	-1946	309.5	1411	S[891]	-2422	309.5
1344	S[824]	-1484	184.5	1378	S[858]	-1960	184.5	1412	S[892]	-2436	184.5
1345	S[825]	-1498	309.5	1379	S[859]	-1974	309.5	1413	S[893]	-2450	309.5
1346	S[826]	-1512	184.5	1380	S[860]	-1988	184.5	1414	S[894]	-2464	184.5
1347	S[827]	-1526	309.5	1381	S[861]	-2002	309.5	1415	S[895]	-2478	309.5
1348	S[828]	-1540	184.5	1382	S[862]	-2016	184.5	1416	S[896]	-2492	184.5
1349	S[829]	-1554	309.5	1383	S[863]	-2030	309.5	1417	S[897]	-2506	309.5
1350	S[830]	-1568	184.5	1384	S[864]	-2044	184.5	1418	S[898]	-2520	184.5
1351	S[831]	-1582	309.5	1385	S[865]	-2058	309.5	1419	S[899]	-2534	309.5
1352	S[832]	-1596	184.5	1386	S[866]	-2072	184.5	1420	S[900]	-2548	184.5
1353	S[833]	-1610	309.5	1387	S[867]	-2086	309.5	1421	S[901]	-2562	309.5
1354	S[834]	-1624	184.5	1388	S[868]	-2100	184.5	1422	S[902]	-2576	184.5

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PAD No. PIN Name X. Lysional No. PAD No. PIN Name No. Year Pin Name No. X. PY Name No. X. Year Pin Name No. X. X. <t< th=""><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></t<>												
1424 S 904 -2604 184.5 1458 S 938 -3090 184.5 1492 S 972 -3556 184.5 1425 S 905 -2218 309.5 1459 S 939 -3094 309.5 1493 S 973 -3570 309.5 1428 S 906 -2632 184.5 1460 S 940 -3108 184.5 1494 S 974 -3584 184.5 1428 S 907 -2646 309.5 1461 S 941 -3122 309.5 1495 S 975 -3598 309.5 1428 S 908 -2660 184.5 1482 S 942 -3336 184.5 1496 S 977 -3668 309.5 1428 S 909 -2674 309.5 1463 S 944 -3164 184.5 1498 S 978 -3662 309.5 1431 S 911 -2702 309.5 1465 S 944 -3164 184.5 1498 S 978 -3664 309.5 1431 S 911 -2702 309.5 1466 S 946 -3312 184.5 1409 S 979 -3664 309.5 1433 S 913 -2730 309.5 1467 S 947 -3206 309.5 1501 S 981 -3682 309.5 1433 S 913 -2730 309.5 1467 S 949 -3224 309.5 1501 S 981 -3682 309.5 1434 S 914 -2744 184.5 1468 S 948 -3224 309.5 1501 S 981 -3682 309.5 1438 S 913 -2778 309.5 1471 S 961 -3224 309.5 1503 S 983 -3710 309.5 1438 S 913 -2772 184.5 1470 S 962 -3226 309.5 1505 S 986 -3724 184.5 1439 S 919 -2684 309.5 1471 S 961 -3282 309.5 1505 S 986 -3738 309.5 1438 S 919 -2684 309.5 1471 S 961 -3282 309.5 1505 S 986 -3738 309.5 1440 S 922 -2684 309.5 1477 S 967 -3346 309.5 1507 S 987 -3766 309.5 1444 S 922 -2688 184.5 1476 S 968 -3332 184.5 1510 S 981 -3802 309.5 1445 S 922 -2688 309.5 1477 S 967 -3346 309.5 1511 S 991 -3622 309.5 1445 S 922 -2688 309.5 1477 S 967 -3346 309.5 1511 S 991 -3622 309.5 1445 S 922 -2688 309.5 1477 S 969 -3374 309.5 1511 S 991 -3622 309.5 1445 S 922 -2688 309.5 1485 S 969 -3374 309.5 1515 S 991 -3692 309.5 1445 S 932 -2694 309.		PIN Name	x	Y		PIN Name	х	Y		PIN Name	х	Y
1425 Sigo5j -2616 309.5 1459 Sigo3j -3094 309.5 1493 Sigo7j -3564 184.5 148.6 Sigo7j -2632 184.5 1460 Sigo4j -3108 184.5 1484 Sigo7j -3684 184.5 1428 Sigo7j -2646 309.5 1461 Sigo4j -3108 184.5 1496 Sigo7j -3660 184.5 1462 Sigo4j -3136 184.5 1496 Sigo7j -3662 309.5 1493 Sigo7j -3660 184.5 1462 Sigo4j -3136 184.5 1496 Sigo7j -3626 309.5 1493 Sigo7j -3660 184.5 1462 Sigo4j -3164 184.5 1496 Sigo7j -3626 309.5 1430 Sigo1j -2768 184.5 1466 Sigo4j -3164 184.5 1498 Sigo7j -3660 184.5 1486 Sigo4j -3192 184.5 1498 Sigo7j -3660 184.5 1486 Sigo4j -3192 184.5 1499 Sigo7j -3664 309.5 1433 Sigo1j -2772 309.5 1465 Sigo4j -3192 184.5 1500 Sigo0j -3664 309.5 1433 Sigo1j -2723 309.5 1467 Sigo4j -3220 184.5 1500 Sigo0j -3666 184.5 1438 Sigo1j -2744 184.5 1468 Sigo4j -3220 184.5 1500 Sigo0j -3666 184.5 1438 Sigo1j -2772 184.5 1470 Sigo0j -3248 184.5 1504 Sigo4j -3724 184.5 1438 Sigo1j -2772 184.5 1470 Sigo0j -3248 184.5 1504 Sigo6j -3738 309.5 1438 Sigo1j -2800 184.5 1470 Sigo0j -3248 184.5 1504 Sigo6j -3738 309.5 1438 Sigo1j -2814 309.5 1471 Sigo0j -3248 184.5 1506 Sigo6j -3738 309.5 1446 Sigo2j -2868 184.5 1476 Sigo6j -3230 309.5 1507 Sigo7j -3766 309.5 1446 Sigo2j -2814 309.5 1473 Sigo0j -3234 309.5 1507 Sigo7j -3766 309.5 1446 Sigo2j -2826 184.5 1476 Sigo6j -3332 184.5 1504 Sigo9j -33794 309.5 1446 Sigo2j -2866 184.5 1476 Sigo6j -3332 184.5 1504 Sigo9j -3808 144.5 1444 Sigo2j -2826 184.5 1476 Sigo6j -3332 184.5 1510 Sigo9j -3866 184.5 1446 Sigo2j -2886 184.5 1476 Sigo6j -3332 184.5 1510 Sigo9j -3802 184.5 1446 Sigo0j -2826 30	1423	S[903]	-2590	309.5	1457	S[937]	-3066	309.5	1491	S[971]	-3542	309.5
1426 S 906 -2632 184.5 1460 S 940 -3108 184.5 1494 S 974 -3564 184.5 1427 S 907 -2646 309.5 1461 S 941 -3122 309.5 1495 S 975 -3598 309.5 1428 S 906 -2660 184.5 1462 S 942 -3136 184.5 1496 S 976 -3612 184.5 1428 S 909 -2674 309.5 1463 S 943 -3150 309.5 1497 S 977 -3628 309.5 1431 S 910 -2688 184.5 1464 S 944 -3164 184.5 1498 S 978 -3640 184.5 1431 S 911 -2702 309.5 1465 S 948 -3178 309.5 1499 S 979 -3654 309.5 1432 S 912 -2716 184.5 1466 S 948 -3192 184.5 1500 S 980 -3662 309.5 1433 S 913 -2730 309.5 1467 S 947 -3208 309.5 1501 S 981 -3682 309.5 1433 S 913 -2758 309.5 1469 S 948 -3220 184.5 1500 S 982 -3696 184.5 1435 S 915 -2758 309.5 1469 S 948 -3224 309.5 1501 S 983 -3710 309.5 1433 S 913 -2772 184.5 1470 S 951 -3262 309.5 1505 S 986 -3738 309.5 1438 S 919 -22814 309.5 1471 S 951 -3262 309.5 1505 S 986 -3738 309.5 1440 S 920 -2282 184.5 1472 S 952 -3276 184.5 1506 S 989 -3736 309.5 1444 S 921 -2842 309.5 1477 S 951 -3304 184.5 1506 S 989 -3770 184.5 1444 S 921 -2282 184.5 1476 S 955 -3318 309.5 1501 S 991 -3962 309.5 1445 319.	1424	S[904]	-2604	184.5	1458	S[938]	-3080	184.5	1492	S[972]	-3556	184.5
1427 S(907) -2646 309.5 1461 S(941) -3122 309.5 1496 S(975) -3698 309.5 1428 S(908) -2660 184.5 1462 S(942) -3136 184.5 1496 S(976) -3612 184.5 1429 S(909) -2674 309.5 1463 S(943) -3150 309.5 1497 S(977) -3626 309.5 1431 S(911) -2702 309.5 1465 S(944) -3164 184.5 1498 S(978) -3640 184.5 1431 S(911) -2702 309.5 1465 S(945) -3178 309.5 1499 S(979) -3654 309.5 1432 S(912) -2716 184.5 1466 S(946) -3172 184.5 1500 S(980) -3688 184.5 1433 S(913) -2730 309.5 1467 S(947) -3206 309.5 1501 S(981) -3682 309.5 1434 S(914) -2744 184.5 1468 S(948) -3220 184.5 1500 S(982) -3696 184.5 1435 S(916) -2772 184.5 1469 S(949) -3224 309.5 1503 S(983) -3710 309.5 1437 S(917) -2768 309.5 1471 S(951) -3262 309.5 1503 S(984) -3752 184.5 1439 S(918) -2284 309.5 1473 S(951) -3206 309.5 1500 S(986) -3752 184.5 1439 S(919) -2284 309.5 1473 S(951) -3202 309.5 1500 S(986) -3752 184.5 1439 S(919) -2284 309.5 1475 S(952) -3276 184.5 1506 S(986) -3752 184.5 1440 S(920) -2286 184.5 1476 S(956) -3318 309.5 1507 S(987) -3780 309.5 1446 S(922) -2286 184.5 1476 S(956) -3318 309.5 1507 S(989) -3794 309.5 1446 S(922) -2286 309.5 1477 S(957) -3346 309.5 1507 S(989) -3794 309.5 1444 S(921) -2284 309.5 1477 S(956) -3318 309.5 1507 S(989) -3794 309.5 1446 S(922) -2286 309.5 1477 S(956) -3338 309.5 1507 S(989) -3794 309.5 1444 S(922) -2286 309.5 1478 S(958) -3374 309.5 1511 S(991) -3808 184.5 1446 S(922) -2286 309.5 1478 S(968) -3332 184.5 1510 S(999) -3898 184.5 1446 S(922) -2286 309.5 1481 S(961) -3402 309.5 1517 S(997) -3864 184.5 1448 S(922) -2286 309.	1425	S[905]	-2618	309.5	1459	S[939]	-3094	309.5	1493	S[973]	-3570	309.5
1428 S[008] -2660 184.5 1462 S[942] -3136 184.5 1496 S[076] -3612 184.5 1429 S[909] -2674 309.5 1463 S[943] -3150 309.5 1497 S[977] -3626 309.5 1430 S[910] -2688 184.5 1464 S[944] -3164 184.5 1498 S[978] -3640 184.5 1431 S[911] -2702 309.5 1466 S[946] -3178 309.5 1499 S[979] -3654 309.5 1432 S[912] -2716 184.5 1466 S[946] -3192 184.5 1500 S[980] -3688 184.5 1433 S[913] -2770 309.5 1467 S[947] -3206 309.5 1501 S[981] -3682 309.5 1434 S[914] -2772 184.5 1468 S[948] -3220 184.5 1504 S[983] -3710	1426	S[906]	-2632	184.5	1460	S[940]	-3108	184.5	1494	S[974]	-3584	184.5
1429 S[809] .2674 309.5 1463 S[943] .3150 309.5 1497 S[877] .3626 309.5 1430 S[910] .2688 184.5 1464 S[944] .3164 184.5 1498 S[978] .3640 184.5 1431 S[911] .2702 309.5 1466 S[946] .3178 309.5 1499 S[979] .3664 309.5 1432 S[912] .2716 184.5 1466 S[946] .3192 184.5 1500 S[980] .3668 184.5 1433 S[913] .2730 309.5 1467 S[947] .3206 309.5 1501 S[981] .3682 309.5 1434 S[914] .2744 184.5 1468 S[948] .3220 184.5 1502 S[982] .3696 184.5 1435 S[916] .2778 309.5 1469 S[949] .3234 309.5 1503 S[983] .3710 309.5 1436 S[916] .2772 184.5 1470 S[950] .3248 184.5 1504 S[984] .3724 184.5 1437 S[917] .2786 309.5 1471 S[951] .3262 309.5 1505 S[88] .3738 309.5 1438 S[918] .2800 184.5 1472 S[952] .3276 184.5 1506 S[986] .3752 184.5 1439 S[919] .2814 309.5 1473 S[953] .3290 309.5 1507 S[987] .3766 309.5 1441 S[920] .2828 184.5 1474 S[954] .3304 184.5 1508 S[988] .3790 184.5 1441 S[921] .2842 309.5 1478 S[956] .3338 309.5 1511 S[991] .3822 309.5 1444 S[922] .2856 184.5 1476 S[956] .3332 184.5 1510 S[991] .3823 309.5 1444 S[922] .2856 184.5 1478 S[956] .3334 309.5 1511 S[991] .3822 309.5 1444 S[922] .2864 309.5 1478 S[956] .3334 309.5 1515 S[991] .3823 309.5 1448 S[928] .2940 184.5 1480 S[960] .3340 309.5 1515 S[991] .3820 309.5 1448 S[922] .2956 309.5 1478 S[956] .3334 309.5 1515 S[991] .3822 309.5 1448 S[922] .2968 309.5 1448 S[960] .3430 309.5 1515 S[991] .3822 309.5 1445 309.5	1427	S[907]	-2646	309.5	1461	S[941]	-3122	309.5	1495	S[975]	-3598	309.5
1430 S[910] -2688 184.5 1464 S[944] -3164 184.5 1498 S[978] -3640 184.5 1431 S[911] -2702 309.5 1465 S[945] -3178 309.5 1499 S[979] -3664 309.5 1432 S[912] -2716 184.5 1466 S[946] -3192 184.5 1500 S[980] -3668 184.5 1433 S[913] -2730 309.5 1467 S[947] -3206 309.5 1501 S[981] -3662 309.5 1434 S[914] -2744 184.5 1468 S[948] -3220 184.5 1502 S[982] -3666 184.5 1435 S[916] -2772 184.5 1470 S[950] -3248 184.5 1504 S[984] -3774 184.5 1437 S[917] -2786 309.5 1471 S[951] -3276 184.5 1506 S[986] -3732	1428	S[908]	-2660	184.5	1462	S[942]	-3136	184.5	1496	S[976]	-3612	184.5
1431 S[911] -2702 309.5 1465 S[945] -3178 309.5 1499 S[979] -3664 309.5 1432 S[912] -2716 184.5 1466 S[946] -3192 184.5 1500 S[980] -3668 184.5 1433 S[913] -2730 309.5 1467 S[947] -3206 309.5 1501 S[981] -3662 309.5 1434 S[914] -2744 184.5 1468 S[948] -3220 184.5 1502 S[982] -3666 184.5 1435 S[916] -2772 184.5 1470 S[950] -3248 184.5 1504 S[984] -3724 184.5 1437 S[917] -2786 309.5 1471 S[951] -3262 309.5 1505 S[986] -3732 184.5 1439 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3782	1429	S[909]	-2674	309.5	1463	S[943]	-3150	309.5	1497	S[977]	-3626	309.5
1432 S[912] -2716 184.5 1466 S[946] -3192 184.5 1500 S[980] -3668 184.5 1433 S[913] -2730 309.5 1467 S[947] -3206 309.5 1501 S[981] -3682 309.5 1434 S[914] -2744 184.5 1468 S[948] -3220 184.5 1502 S[982] -3696 184.5 1435 S[915] -2758 309.5 1469 S[949] -3234 309.5 1503 S[983] -3710 309.5 1435 S[916] -2772 184.5 1470 S[950] -3248 184.5 1504 S[984] -3724 184.5 1437 S[917] -2786 309.5 1471 S[951] -3262 309.5 1505 S[985] -3738 309.5 1438 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3752 184.5 1439 S[919] -2814 309.5 1473 S[953] -3290 309.5 1505 S[986] -3766 309.5 1440 S[920] -2828 184.5 1474 S[954] -3304 184.5 1508 S[988] -3780 184.5 1441 S[921] -2842 309.5 1475 S[955] -3318 309.5 1509 S[989] -3794 309.5 1442 S[922] -2866 184.5 1476 S[956] -3332 184.5 1510 S[990] -3808 184.5 1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1511 S[991] -3822 309.5 1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1511 S[991] -3823 309.5 1479 S[959] -3374 309.5 1513 S[992] -3836 184.5 1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[992] -3836 184.5 1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[996] -3892 184.5 1449 S[929] -2954 309.5 1483 S[963] -3402 309.5 1515 S[996] -3992 184.5 1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[996] -3934 309.5 1451 S[931] -2962 309.5 1485 S[966] -3468 309.5 1519 S[999] -3934 309.5 1451 S[931] -2962 309.5 1485 S[966] -3468 309.5 1519 S[999] -3934 309.5 1455 S[931] -2962 309.5 1485 S[966] -3468 309.5 1519 S[999] -3934 309.5 1454 S[932] -2966 184.5 1486 S[966] -3472 184.	1430	S[910]	-2688	184.5	1464	S[944]	-3164	184.5	1498	S[978]	-3640	184.5
1433 S[913] -2730 309.5 1467 S[947] -3206 309.5 1501 S[981] -3682 309.5 1434 S[914] -2744 184.5 1468 S[948] -3220 184.5 1502 S[982] -3696 184.5 1435 S[915] -2758 309.5 1469 S[949] -3234 309.5 1503 S[983] -3710 309.5 1436 S[916] -2772 184.5 1470 S[950] -3248 184.5 1504 S[984] -3724 184.5 1437 S[917] -2786 309.5 1471 S[951] -3262 309.5 1505 S[986] -3732 184.5 1438 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3732 184.5 1439 S[919] -2814 309.5 1473 S[953] -3300 184.5 1508 S[988] -3766	1431	S[911]	-2702	309.5	1465	S[945]	-3178	309.5	1499	S[979]	-3654	309.5
1434 S[914] -2744 184.5 1468 S[948] -3220 184.5 1502 S[982] -3696 184.5 1435 S[915] -2758 309.5 1469 S[949] -3234 309.5 1503 S[983] -3710 309.5 1436 S[916] -2772 184.5 1470 S[950] -3248 184.5 1504 S[984] -3724 184.5 1437 S[917] -2786 309.5 1471 S[951] -3262 309.5 1505 S[985] -3738 309.5 1438 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3752 184.5 1440 S[920] -2828 184.5 1474 S[953] -3304 184.5 1508 S[988] -3760 184.5 1441 S[921] -2842 309.5 1475 S[955] -3318 309.5 1509 S[989] -3794	1432	S[912]	-2716	184.5	1466	S[946]	-3192	184.5	1500	S[980]	-3668	184.5
1435 S[916] -2758 309.5 1469 S[949] -3234 309.5 1503 S[983] -3710 309.5 1436 S[916] -2772 184.5 1470 S[950] -3248 184.5 1504 S[984] -3724 184.5 1437 S[917] -2786 309.5 1471 S[951] -3262 309.5 1505 S[986] -3738 309.5 1438 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3752 184.5 1439 S[919] -2814 309.5 1473 S[953] -3290 309.5 1507 S[987] -3766 309.5 1440 S[920] -2828 184.5 1474 S[954] -3304 184.5 1508 S[988] -3780 184.5 1441 S[921] -2826 184.5 1476 S[956] -3332 184.5 1510 S[989] -3794	1433	S[913]	-2730	309.5	1467	S[947]	-3206	309.5	1501	S[981]	-3682	309.5
1436 S[916] -2772 184.5 1470 S[950] -3248 184.5 1504 S[984] -3724 184.5 1437 S[917] -2786 309.5 1471 S[951] -3262 309.5 1505 S[985] -3738 309.5 1438 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3752 184.5 1439 S[919] -2814 309.5 1473 S[953] -3290 309.5 1507 S[987] -3766 309.5 1440 S[920] -2828 184.5 1474 S[954] -3304 184.5 1508 S[988] -3780 184.5 1441 S[921] -2828 184.5 1476 S[955] -3318 309.5 1509 S[989] -3794 309.5 1442 S[922] -2856 184.5 1476 S[957] -3346 309.5 1510 S[990] -3808	1434	S[914]	-2744	184.5	1468	S[948]	-3220	184.5	1502	S[982]	-3696	184.5
1437 S[917] -2786 309.5 1471 S[951] -3262 309.5 1505 S[985] -3738 309.5 1438 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3752 184.5 1439 S[919] -2814 309.5 1473 S[953] -3290 309.5 1507 S[987] -3766 309.5 1440 S[920] -2828 184.5 1474 S[955] -3318 309.5 1508 S[988] -3780 184.5 1441 S[921] -2842 309.5 1475 S[955] -3318 309.5 1509 S[989] -3794 309.5 1442 S[922] -2866 184.5 1476 S[956] -3332 184.5 1510 S[990] -3808 184.5 1443 S[923] -2870 309.5 1477 S[957] -3346 309.5 1511 S[991] -3822	1435	S[915]	-2758	309.5	1469	S[949]	-3234	309.5	1503	S[983]	-3710	309.5
1438 S[918] -2800 184.5 1472 S[952] -3276 184.5 1506 S[986] -3752 184.5 1439 S[919] -2814 309.5 1473 S[953] -3290 309.5 1507 S[987] -3766 309.5 1440 S[920] -2828 184.5 1474 S[954] -3304 184.5 1508 S[988] -3780 184.5 1441 S[921] -2842 309.5 1475 S[956] -3318 309.5 1509 S[989] -3794 309.5 1442 S[922] -2866 184.5 1476 S[956] -3332 184.5 1510 S[990] -3808 184.5 1443 S[923] -2870 309.5 1477 S[957] -3346 309.5 1511 S[991] -3836 184.5 1444 S[924] -2884 184.5 1479 S[958] -3374 309.5 1513 S[993] -3850	1436	S[916]	-2772	184.5	1470	S[950]	-3248	184.5	1504	S[984]	-3724	184.5
1439 S[919] -2814 309.5 1473 S[953] -3290 309.5 1507 S[987] -3766 309.5 1440 S[920] -2828 184.5 1474 S[954] -3304 184.5 1508 S[988] -3780 184.5 1441 S[921] -2842 309.5 1475 S[955] -3318 309.5 1509 S[989] -3794 309.5 1442 S[922] -2856 184.5 1476 S[956] -3332 184.5 1510 S[990] -3808 184.5 1443 S[923] -2870 309.5 1477 S[957] -3346 309.5 1511 S[991] -3822 309.5 1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1512 S[992] -3836 184.5 1445 S[926] -2988 309.5 1479 S[959] -3374 309.5 1513 S[993] -3860	1437	S[917]	-2786	309.5	1471	S[951]	-3262	309.5	1505	S[985]	-3738	309.5
1440 S[920] -2828 184.5 1474 S[954] -3304 184.5 1508 S[988] -3780 184.5 1441 S[921] -2842 309.5 1475 S[955] -3318 309.5 1509 S[989] -3794 309.5 1442 S[922] -2856 184.5 1476 S[956] -3332 184.5 1510 S[990] -3808 184.5 1443 S[923] -2870 309.5 1477 S[957] -3346 309.5 1511 S[991] -3822 309.5 1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1512 S[992] -3836 184.5 1445 S[926] -2898 309.5 1479 S[959] -3374 309.5 1513 S[993] -3850 309.5 1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[994] -3864	1438	S[918]	-2800	184.5	1472	S[952]	-3276	184.5	1506	S[986]	-3752	184.5
1441 S[921] -2842 309.5 1475 S[956] -3318 309.5 1509 S[989] -3794 309.5 1442 S[922] -2856 184.5 1476 S[956] -3332 184.5 1510 S[990] -3808 184.5 1443 S[923] -2870 309.5 1477 S[957] -3346 309.5 1511 S[991] -3822 309.5 1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1512 S[992] -3836 184.5 1445 S[925] -2898 309.5 1479 S[959] -3374 309.5 1513 S[993] -3850 309.5 1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[994] -3864 184.5 1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[995] -3878	1439	S[919]	-2814	309.5	1473	S[953]	-3290	309.5	1507	S[987]	-3766	309.5
1442 S[922] -2856 184.5 1476 S[956] -3332 184.5 1510 S[990] -3808 184.5 1443 S[923] -2870 309.5 1477 S[957] -3346 309.5 1511 S[991] -3822 309.5 1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1512 S[992] -3836 184.5 1445 S[926] -2898 309.5 1479 S[959] -3374 309.5 1513 S[993] -3850 309.5 1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[994] -3864 184.5 1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[995] -3878 309.5 1448 S[928] -2940 184.5 1482 S[962] -3416 184.5 1516 S[996] -3892	1440	S[920]	-2828	184.5	1474	S[954]	-3304	184.5	1508	S[988]	-3780	184.5
1443 S[923] -2870 309.5 1477 S[957] -3346 309.5 1511 S[991] -3822 309.5 1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1512 S[992] -3836 184.5 1445 S[925] -2898 309.5 1479 S[959] -3374 309.5 1513 S[993] -3850 309.5 1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[994] -3864 184.5 1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[995] -3878 309.5 1448 S[928] -2940 184.5 1482 S[962] -3416 184.5 1516 S[996] -3892 184.5 1449 S[929] -2954 309.5 1483 S[963] -3430 309.5 1517 S[997] -3906	1441	S[921]	-2842	309.5	1475	S[955]	-3318	309.5	1509	S[989]	-3794	309.5
1444 S[924] -2884 184.5 1478 S[958] -3360 184.5 1512 S[992] -3836 184.5 1445 S[925] -2898 309.5 1479 S[959] -3374 309.5 1513 S[993] -3850 309.5 1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[994] -3864 184.5 1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[995] -3878 309.5 1448 S[928] -2940 184.5 1482 S[962] -3416 184.5 1516 S[996] -3892 184.5 1449 S[929] -2954 309.5 1483 S[963] -3430 309.5 1517 S[997] -3906 309.5 1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[998] -3920	1442	S[922]	-2856	184.5	1476	S[956]	-3332	184.5	1510	S[990]	-3808	184.5
1445 S[925] -2898 309.5 1479 S[959] -3374 309.5 1513 S[993] -3850 309.5 1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[994] -3864 184.5 1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[995] -3878 309.5 1448 S[928] -2940 184.5 1482 S[962] -3416 184.5 1516 S[996] -3892 184.5 1449 S[929] -2954 309.5 1483 S[963] -3430 309.5 1517 S[997] -3906 309.5 1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[998] -3920 184.5 1451 S[931] -2982 309.5 1485 S[965] -3458 309.5 1519 S[999] -3934	1443	S[923]	-2870	309.5	1477	S[957]	-3346	309.5	1511	S[991]	-3822	309.5
1446 S[926] -2912 184.5 1480 S[960] -3388 184.5 1514 S[994] -3864 184.5 1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[995] -3878 309.5 1448 S[928] -2940 184.5 1482 S[962] -3416 184.5 1516 S[996] -3892 184.5 1449 S[929] -2954 309.5 1483 S[963] -3430 309.5 1517 S[997] -3906 309.5 1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[998] -3920 184.5 1451 S[931] -2982 309.5 1485 S[965] -3458 309.5 1519 S[999] -3934 309.5 1452 S[932] -2996 184.5 1486 S[966] -3472 184.5 1520 S[1000] -3948 <td< td=""><td>1444</td><td>S[924]</td><td>-2884</td><td>184.5</td><td>1478</td><td>S[958]</td><td>-3360</td><td>184.5</td><td>1512</td><td>S[992]</td><td>-3836</td><td>184.5</td></td<>	1444	S[924]	-2884	184.5	1478	S[958]	-3360	184.5	1512	S[992]	-3836	184.5
1447 S[927] -2926 309.5 1481 S[961] -3402 309.5 1515 S[995] -3878 309.5 1448 S[928] -2940 184.5 1482 S[962] -3416 184.5 1516 S[996] -3892 184.5 1449 S[929] -2954 309.5 1483 S[963] -3430 309.5 1517 S[997] -3906 309.5 1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[998] -3920 184.5 1451 S[931] -2982 309.5 1485 S[965] -3458 309.5 1519 S[998] -3920 184.5 1452 S[932] -2996 184.5 1486 S[966] -3472 184.5 1520 S[1000] -3948 184.5 1453 S[933] -3010 309.5 1487 S[967] -3486 309.5 1521 S[1001] -3962 <t< td=""><td>1445</td><td>S[925]</td><td>-2898</td><td>309.5</td><td>1479</td><td>S[959]</td><td>-3374</td><td>309.5</td><td>1513</td><td>S[993]</td><td>-3850</td><td>309.5</td></t<>	1445	S[925]	-2898	309.5	1479	S[959]	-3374	309.5	1513	S[993]	-3850	309.5
1448 S[928] -2940 184.5 1482 S[962] -3416 184.5 1516 S[996] -3892 184.5 1449 S[929] -2954 309.5 1483 S[963] -3430 309.5 1517 S[997] -3906 309.5 1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[998] -3920 184.5 1451 S[931] -2982 309.5 1485 S[965] -3458 309.5 1519 S[999] -3934 309.5 1452 S[932] -2996 184.5 1486 S[966] -3472 184.5 1520 S[1000] -3948 184.5 1453 S[933] -3010 309.5 1487 S[967] -3486 309.5 1521 S[1001] -3962 309.5 1454 S[934] -3024 184.5 1488 S[968] -3500 184.5 1523 S[1003] -3976 <	1446	S[926]	-2912	184.5	1480	S[960]	-3388	184.5	1514	S[994]	-3864	184.5
1449 S[929] -2954 309.5 1483 S[963] -3430 309.5 1517 S[997] -3906 309.5 1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[998] -3920 184.5 1451 S[931] -2982 309.5 1485 S[965] -3458 309.5 1519 S[999] -3934 309.5 1452 S[932] -2996 184.5 1486 S[966] -3472 184.5 1520 S[1000] -3948 184.5 1453 S[933] -3010 309.5 1487 S[967] -3486 309.5 1521 S[1001] -3962 309.5 1454 S[934] -3024 184.5 1488 S[968] -3500 184.5 1522 S[1002] -3976 184.5 1455 S[935] -3038 309.5 1489 S[969] -3514 309.5 1523 S[1003] -3990	1447	S[927]	-2926	309.5	1481	S[961]	-3402	309.5	1515	S[995]	-3878	309.5
1450 S[930] -2968 184.5 1484 S[964] -3444 184.5 1518 S[998] -3920 184.5 1451 S[931] -2982 309.5 1485 S[965] -3458 309.5 1519 S[999] -3934 309.5 1452 S[932] -2996 184.5 1486 S[966] -3472 184.5 1520 S[1000] -3948 184.5 1453 S[933] -3010 309.5 1487 S[967] -3486 309.5 1521 S[1001] -3962 309.5 1454 S[934] -3024 184.5 1488 S[968] -3500 184.5 1522 S[1002] -3976 184.5 1455 S[935] -3038 309.5 1489 S[969] -3514 309.5 1523 S[1003] -3990 309.5	1448	S[928]	-2940	184.5	1482	S[962]	-3416	184.5	1516	S[996]	-3892	184.5
1451 S[931] -2982 309.5 1485 S[965] -3458 309.5 1519 S[999] -3934 309.5 1452 S[932] -2996 184.5 1486 S[966] -3472 184.5 1520 S[1000] -3948 184.5 1453 S[933] -3010 309.5 1487 S[967] -3486 309.5 1521 S[1001] -3962 309.5 1454 S[934] -3024 184.5 1488 S[968] -3500 184.5 1522 S[1002] -3976 184.5 1455 S[935] -3038 309.5 1489 S[969] -3514 309.5 1523 S[1003] -3990 309.5	1449	S[929]	-2954	309.5	1483	S[963]	-3430	309.5	1517	S[997]	-3906	309.5
1452 S[932] -2996 184.5 1486 S[966] -3472 184.5 1520 S[1000] -3948 184.5 1453 S[933] -3010 309.5 1487 S[967] -3486 309.5 1521 S[1001] -3962 309.5 1454 S[934] -3024 184.5 1488 S[968] -3500 184.5 1522 S[1002] -3976 184.5 1455 S[935] -3038 309.5 1489 S[969] -3514 309.5 1523 S[1003] -3990 309.5	1450	S[930]	-2968	184.5	1484	S[964]	-3444	184.5	1518	S[998]	-3920	184.5
1453 S[933] -3010 309.5 1487 S[967] -3486 309.5 1521 S[1001] -3962 309.5 1454 S[934] -3024 184.5 1488 S[968] -3500 184.5 1522 S[1002] -3976 184.5 1455 S[935] -3038 309.5 1489 S[969] -3514 309.5 1523 S[1003] -3990 309.5	1451	S[931]	-2982	309.5	1485	S[965]	-3458	309.5	1519	S[999]	-3934	309.5
1454 S[934] -3024 184.5 1488 S[968] -3500 184.5 1522 S[1002] -3976 184.5 1455 S[935] -3038 309.5 1489 S[969] -3514 309.5 1523 S[1003] -3990 309.5	1452	S[932]	-2996	184.5	1486	S[966]	-3472	184.5	1520	S[1000]	-3948	184.5
1455 S[935] -3038 309.5 1489 S[969] -3514 309.5 1523 S[1003] -3990 309.5	1453	S[933]	-3010	309.5	1487	S[967]	-3486	309.5	1521	S[1001]	-3962	309.5
	1454	S[934]	-3024	184.5	1488	S[968]	-3500	184.5	1522	S[1002]	-3976	184.5
1456 S[936] -3052 184.5 1490 S[970] -3528 184.5 1524 S[1004] -4004 184.5	1455	S[935]	-3038	309.5	1489	S[969]	-3514	309.5	1523	S[1003]	-3990	309.5
	1456	S[936]	-3052	184.5	1490	S[970]	-3528	184.5	1524	S[1004]	-4004	184.5

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PAD				PAD				PAD			
No.	PIN Name	Х	Y	No.	PIN Name	Х	Y	No.	PIN Name	Х	Y
1525	S[1005]	-4018	309.5	1559	S[1039]	-4494	309.5	1593	S[1073]	-4970	309.5
1526	S[1006]	-4032	184.5	1560	S[1040]	-4508	184.5	1594	S[1074]	-4984	184.5
1527	S[1007]	-4046	309.5	1561	S[1041]	-4522	309.5	1595	S[1075]	-4998	309.5
1528	S[1008]	-4060	184.5	1562	S[1042]	-4536	184.5	1596	S[1076]	-5012	184.5
1529	S[1009]	-4074	309.5	1563	S[1043]	-4550	309.5	1597	S[1077]	-5026	309.5
1530	S[1010]	-4088	184.5	1564	S[1044]	-4564	184.5	1598	S[1078]	-5040	184.5
1531	S[1011]	-4102	309.5	1565	S[1045]	-4578	309.5	1599	S[1079]	-5054	309.5
1532	S[1012]	-4116	184.5	1566	S[1046]	-4592	184.5	1600	S[1080]	-5068	184.5
1533	S[1013]	-4130	309.5	1567	S[1047]	-4606	309.5	1601	S[1081]	-5082	309.5
1534	S[1014]	-4144	184.5	1568	S[1048]	-4620	184.5	1602	S[1082]	-5096	184.5
1535	S[1015]	-4158	309.5	1569	S[1049]	-4634	309.5	1603	S[1083]	-5110	309.5
1536	S[1016]	-4172	184.5	1570	S[1050]	-4648	184.5	1604	S[1084]	-5124	184.5
1537	S[1017]	-4186	309.5	1571	S[1051]	-4662	309.5	1605	S[1085]	-5138	309.5
1538	S[1018]	-4200	184.5	1572	S[1052]	-4676	184.5	1606	S[1086]	-5152	184.5
1539	S[1019]	-4214	309.5	1573	S[1053]	-4690	309.5	1607	S[1087]	-5166	309.5
1540	S[1020]	-4228	184.5	1574	S[1054]	-4704	184.5	1608	S[1088]	-5180	184.5
1541	S[1021]	-4242	309.5	1575	S[1055]	-4718	309.5	1609	S[1089]	-5194	309.5
1542	S[1022]	-4256	184.5	1576	S[1056]	-4732	184.5	1610	S[1090]	-5208	184.5
1543	S[1023]	-4270	309.5	1577	S[1057]	-4746	309.5	1611	S[1091]	-5222	309.5
1544	S[1024]	-4284	184.5	1578	S[1058]	-4760	184.5	1612	S[1092]	-5236	184.5
1545	S[1025]	-4298	309.5	1579	S[1059]	-4774	309.5	1613	S[1093]	-5250	309.5
1546	S[1026]	-4312	184.5	1580	S[1060]	-4788	184.5	1614	S[1094]	-5264	184.5
1547	S[1027]	-4326	309.5	1581	S[1061]	-4802	309.5	1615	S[1095]	-5278	309.5
1548	S[1028]	-4340	184.5	1582	S[1062]	-4816	184.5	1616	S[1096]	-5292	184.5
1549	S[1029]	-4354	309.5	1583	S[1063]	-4830	309.5	1617	S[1097]	-5306	309.5
1550	S[1030]	-4368	184.5	1584	S[1064]	-4844	184.5	1618	S[1098]	-5320	184.5
1551	S[1031]	-4382	309.5	1585	S[1065]	-4858	309.5	1619	S[1099]	-5334	309.5
1552	S[1032]	-4396	184.5	1586	S[1066]	-4872	184.5	1620	S[1100]	-5348	184.5
1553	S[1033]	-4410	309.5	1587	S[1067]	-4886	309.5	1621	S[1101]	-5362	309.5
1554	S[1034]	-4424	184.5	1588	S[1068]	-4900	184.5	1622	S[1102]	-5376	184.5
1555	S[1035]	-4438	309.5	1589	S[1069]	-4914	309.5	1623	S[1103]	-5390	309.5
1556	S[1036]	-4452	184.5	1590	S[1070]	-4928	184.5	1624	S[1104]	-5404	184.5
1557	S[1037]	-4466	309.5	1591	S[1071]	-4942	309.5	1625	S[1105]	-5418	309.5
1558	S[1038]	-4480	184.5	1592	S[1072]	-4956	184.5	1626	S[1106]	-5432	184.5

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PAD			.,	PAD		.,	,,	PAD		.,	.,
No.	PIN Name	Х	Y	No.	PIN Name	Х	Y	No.	PIN Name	Х	Y
1627	S[1107]	-5446	309.5	1661	S[1141]	-5922	309.5	1695	S[1175]	-6398	309.5
1628	S[1108]	-5460	184.5	1662	S[1142]	-5936	184.5	1696	S[1176]	-6412	184.5
1629	S[1109]	-5474	309.5	1663	S[1143]	-5950	309.5	1697	S[1177]	-6426	309.5
1630	S[1110]	-5488	184.5	1664	S[1144]	-5964	184.5	1698	S[1178]	-6440	184.5
1631	S[1111]	-5502	309.5	1665	S[1145]	-5978	309.5	1699	S[1179]	-6454	309.5
1632	S[1112]	-5516	184.5	1666	S[1146]	-5992	184.5	1700	S[1180]	-6468	184.5
1633	S[1113]	-5530	309.5	1667	S[1147]	-6006	309.5	1701	S[1181]	-6482	309.5
1634	S[1114]	-5544	184.5	1668	S[1148]	-6020	184.5	1702	S[1182]	-6496	184.5
1635	S[1115]	-5558	309.5	1669	S[1149]	-6034	309.5	1703	S[1183]	-6510	309.5
1636	S[1116]	-5572	184.5	1670	S[1150]	-6048	184.5	1704	S[1184]	-6524	184.5
1637	S[1117]	-5586	309.5	1671	S[1151]	-6062	309.5	1705	S[1185]	-6538	309.5
1638	S[1118]	-5600	184.5	1672	S[1152]	-6076	184.5	1706	S[1186]	-6552	184.5
1639	S[1119]	-5614	309.5	1673	S[1153]	-6090	309.5	1707	S[1187]	-6566	309.5
1640	S[1120]	-5628	184.5	1674	S[1154]	-6104	184.5	1708	S[1188]	-6580	184.5
1641	S[1121]	-5642	309.5	1675	S[1155]	-6118	309.5	1709	S[1189]	-6594	309.5
1642	S[1122]	-5656	184.5	1676	S[1156]	-6132	184.5	1710	S[1190]	-6608	184.5
1643	S[1123]	-5670	309.5	1677	S[1157]	-6146	309.5	1711	S[1191]	-6622	309.5
1644	S[1124]	-5684	184.5	1678	S[1158]	-6160	184.5	1712	S[1192]	-6636	184.5
1645	S[1125]	-5698	309.5	1679	S[1159]	-6174	309.5	1713	S[1193]	-6650	309.5
1646	S[1126]	-5712	184.5	1680	S[1160]	-6188	184.5	1714	S[1194]	-6664	184.5
1647	S[1127]	-5726	309.5	1681	S[1161]	-6202	309.5	1715	S[1195]	-6678	309.5
1648	S[1128]	-5740	184.5	1682	S[1162]	-6216	184.5	1716	S[1196]	-6692	184.5
1649	S[1129]	-5754	309.5	1683	S[1163]	-6230	309.5	1717	S[1197]	-6706	309.5
1650	S[1130]	-5768	184.5	1684	S[1164]	-6244	184.5	1718	S[1198]	-6720	184.5
1651	S[1131]	-5782	309.5	1685	S[1165]	-6258	309.5	1719	S[1199]	-6734	309.5
1652	S[1132]	-5796	184.5	1686	S[1166]	-6272	184.5	1720	S[1200]	-6748	184.5
1653	S[1133]	-5810	309.5	1687	S[1167]	-6286	309.5	1721	S[1201]	-6762	309.5
1654	S[1134]	-5824	184.5	1688	S[1168]	-6300	184.5	1722	S[1202]	-6776	184.5
1655	S[1135]	-5838	309.5	1689	S[1169]	-6314	309.5	1723	S[1203]	-6790	309.5
1656	S[1136]	-5852	184.5	1690	S[1170]	-6328	184.5	1724	S[1204]	-6804	184.5
1657	S[1137]	-5866	309.5	1691	S[1171]	-6342	309.5	1725	S[1205]	-6818	309.5
1658	S[1138]	-5880	184.5	1692	S[1172]	-6356	184.5	1726	S[1206]	-6832	184.5
1659	S[1139]	-5894	309.5	1693	S[1173]	-6370	309.5	1727	S[1207]	-6846	309.5
1660	S[1140]	-5908	184.5	1694	S[1174]	-6384	184.5	1728	S[1208]	-6860	184.5

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PAD No.	PIN Name	x	Y	PAD No.	PIN Name	x	Y	PAD No.	PIN Name	x	Y
1729	S[1209]	-6874	309.5	1763	S[1243]	-7350	309.5	1797	S[1277]	-7826	309.5
1730	S[1210]	-6888	184.5	1764	S[1244]	-7364	184.5	1798	S[1278]	-7840	184.5
1731	S[1211]	-6902	309.5	1765	S[1245]	-7378	309.5	1799	S[1279]	-7854	309.5
1732	S[1212]	-6916	184.5	1766	S[1246]	-7392	184.5	1800	S[1280]	-7868	184.5
1733	S[1213]	-6930	309.5	1767	S[1247]	-7406	309.5	1801	S[1281]	-7882	309.5
1734	S[1214]	-6944	184.5	1768	S[1248]	-7420	184.5	1802	S[1282]	-7896	184.5
1735	S[1215]	-6958	309.5	1769	S[1249]	-7434	309.5	1803	S[1283]	-7910	309.5
1736	S[1216]	-6972	184.5	1770	S[1250]	-7448	184.5	1804	S[1284]	-7924	184.5
1737	S[1217]	-6986	309.5	1771	S[1251]	-7462	309.5	1805	S[1285]	-7938	309.5
1738	S[1218]	-7000	184.5	1772	S[1252]	-7476	184.5	1806	S[1286]	-7952	184.5
1739	S[1219]	-7014	309.5	1773	S[1253]	-7490	309.5	1807	S[1287]	-7966	309.5
1740	S[1220]	-7028	184.5	1774	S[1254]	-7504	184.5	1808	S[1288]	-7980	184.5
1741	S[1221]	-7042	309.5	1775	S[1255]	-7518	309.5	1809	S[1289]	-7994	309.5
1742	S[1222]	-7056	184.5	1776	S[1256]	-7532	184.5	1810	S[1290]	-8008	184.5
1743	S[1223]	-7070	309.5	1777	S[1257]	-7546	309.5	1811	S[1291]	-8022	309.5
1744	S[1224]	-7084	184.5	1778	S[1258]	-7560	184.5	1812	S[1292]	-8036	184.5
1745	S[1225]	-7098	309.5	1779	S[1259]	-7574	309.5	1813	S[1293]	-8050	309.5
1746	S[1226]	-7112	184.5	1780	S[1260]	-7588	184.5	1814	S[1294]	-8064	184.5
1747	S[1227]	-7126	309.5	1781	S[1261]	-7602	309.5	1815	S[1295]	-8078	309.5
1748	S[1228]	-7140	184.5	1782	S[1262]	-7616	184.5	1816	S[1296]	-8092	184.5
1749	S[1229]	-7154	309.5	1783	S[1263]	-7630	309.5	1817	S[1297]	-8106	309.5
1750	S[1230]	-7168	184.5	1784	S[1264]	-7644	184.5	1818	S[1298]	-8120	184.5
1751	S[1231]	-7182	309.5	1785	S[1265]	-7658	309.5	1819	S[1299]	-8134	309.5
1752	S[1232]	-7196	184.5	1786	S[1266]	-7672	184.5	1820	S[1300]	-8148	184.5
1753	S[1233]	-7210	309.5	1787	S[1267]	-7686	309.5	1821	S[1301]	-8162	309.5
1754	S[1234]	-7224	184.5	1788	S[1268]	-7700	184.5	1822	S[1302]	-8176	184.5
1755	S[1235]	-7238	309.5	1789	S[1269]	-7714	309.5	1823	S[1303]	-8190	309.5
1756	S[1236]	-7252	184.5	1790	S[1270]	-7728	184.5	1824	S[1304]	-8204	184.5
1757	S[1237]	-7266	309.5	1791	S[1271]	-7742	309.5	1825	S[1305]	-8218	309.5
1758	S[1238]	-7280	184.5	1792	S[1272]	-7756	184.5	1826	S[1306]	-8232	184.5
1759	S[1239]	-7294	309.5	1793	S[1273]	-7770	309.5	1827	S[1307]	-8246	309.5
1760	S[1240]	-7308	184.5	1794	S[1274]	-7784	184.5	1828	S[1308]	-8260	184.5
1761	S[1241]	-7322	309.5	1795	S[1275]	-7798	309.5	1829	S[1309]	-8274	309.5
1762	S[1242]	-7336	184.5	1796	S[1276]	-7812	184.5	1830	S[1310]	-8288	184.5

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No.	No. PIN Name X Y Y No. PIN Name X No. PIN Name X No. PIN Name X No. PIN Name X Y No. PIN Name X Y No. PIN Name X No. PIN												
1832 S[1312]	1832 S 1312 -8316		PIN Name	х	Y		PIN Name	х	Y		PIN Name	х	Y
1833 S 1313	1833 S 1313 -8.330 309.5 1867 S 1347 -8806 309.5 1901 S 1381 -9282 309.5 1834 S 1314 -8344 184.5 1868 S 1349 -8820 184.5 1902 S 1382 -9286 184.5 1835 S 1316 -8358 309.5 1869 S 1349 -8834 309.5 1903 S 1383 -9310 309.5 1836 S 1317 -8386 309.5 1871 S 1359 -8848 184.5 1904 S 1384 -9324 184.5 1837 S 1317 -8386 309.5 1871 S 1359 -8862 309.5 1905 S 1383 -9338 309.5 1833 S 1319 -8400 184.5 1872 S 1353 -8860 309.5 1906 S 1386 -9392 184.5 1838 S 1319 -8414 309.5 1873 S 1353 -8890 309.5 1907 S 1387 -9366 308.5 1840 S 1322 -8466 184.5 1876 S 1359 -8918 309.5 1907 S 1387 -9366 309.5 1841 S 1322 -8456 184.5 1876 S 1359 -8918 309.5 1910 S 1389 3934 309.5 1844 S 1323 -8470 309.5 1877 S 1359 -8946 309.5 1910 S 1389 -9422 309.5 1844 S 1322 -8468 309.5 1877 S 1359 -8946 309.5 1911 S 1391 -9422 309.5 1844 S 1322 -8488 309.5 1878 S 1359 -8974 309.5 1913 S 1333 -9450 309.5 1844 S 1322 -8566 309.5 1881 S 1369 -9002 309.5 1914 S 1339 -9478 309.5 1849 S 1332 -8566 309.5 1883 S 1369 -9002 309.5 1915 S 1399 -9478 309.5 1849 S 1332 -8660 184.5 1882 S 1369 -9002 309.5 1915 S 1399 -9478 309.5 1845 1849 S 1332 -8660 184.5 1883 S 1369 -9002 309.5 1919 S 1399 -9438 184.5 1868 S 1339 -8686 184.5 1888 S 1369 -9002 309.5 1919 S 1399 -9544 309.5 1845 S 1332 -8666 309.5 1883 S 1369 -9004 184.5 1919 S 1399 -9548 309.5 1845 S 1332 -8666 309.5 1883 S 1369 -9004 184.5 1919 S 1399 -9548 309.5 1845 S 1339 -8666 309.5 1889 S 1369 -9014 309.5 1919 S 1399 -9534 309.5 1855 S 1339 -8666 309.5 1889 S 1369 -9014	1831	S[1311]	-8302	309.5	1865	S[1345]	-8778	309.5	1899	S[1379]	-9254	309.5
1834 S[1314] -8344 184.5 1866 S[1348] -8820 184.5 1902 S[1382] -9266 184.5 1835 S[1315] -8358 309.5 1869 S[1349] -8834 309.5 1903 S[1383] -9310 300	1834 S[1314] -8344 184.5 1868 S[1348] -8820 184.5 1902 S[1383] -9296 184.5 1835 S[1315] -8358 309.5 1869 S[1349] -8834 309.5 1903 S[1383] -9310 309.5 1836 S[1316] -8372 184.5 1870 S[1350] -8848 184.5 1904 S[1384] -9324 184.5 1837 S[1317] -8386 309.5 1871 S[1352] -8876 184.5 1906 S[1386] -9362 184.5 1839 S[1319] -8414 309.5 1873 S[1352] -8876 184.5 1906 S[1386] -9362 184.5 1840 S[1320] -8428 184.5 1874 S[1352] -8904 184.5 1909 S[1387] -9366 309.5 1841 S[1322] -8426 184.5 1910 S[1380] -9300 184.5 1842 S[1322]<	1832	S[1312]	-8316	184.5	1866	S[1346]	-8792	184.5	1900	S[1380]	-9268	184.5
1835 S[1315]	1835 S 1315 -8358 309.5 1869 S 1319 -8334 309.5 1903 S 1333 -9310 309.5 1836 S 1316 -8372 184.5 1870 S 1350 -8848 184.5 1904 S 1384 -9324 184.5 1837 S 1317 -8366 309.5 1871 S 1351 -8862 309.5 1905 S 1386 -9332 309.5 1833 S 1318 -8400 184.5 1872 S 1352 -8876 184.5 1906 S 1386 -9352 184.5 1839 S 1319 -8414 309.5 1873 S 1353 -8890 309.5 1907 S 1387 -9366 309.5 1841 S 1321 -8422 309.5 1873 S 1353 -8890 309.5 1907 S 1387 -9366 309.5 1841 S 1321 -8442 309.5 1875 S 1355 -8918 309.5 1909 S 1388 -9380 184.5 1841 S 1322 -8456 184.5 1876 S 1356 -8932 184.5 1910 S 1390 -9408 184.5 1843 S 1323 -8470 309.5 1877 S 1357 -8946 309.5 1911 S 1391 -9422 309.5 1844 S 1324 -8444 184.5 1878 S 1358 -8960 184.5 1912 S 1392 -9436 184.5 1844 S 1322 -8468 309.5 1879 S 1359 -8974 309.5 1913 S 1393 -9460 309.5 1844 S 1326 -8952 309.5 1881 S 1360 -8988 184.5 1914 S 1324 -9464 184.5 1848 S 1328 -8540 184.5 1888 S 1360 -9002 309.5 1915 S 1396 -9478 309.5 1845 1848 S 1329 -8544 309.5 1883 S 1363 -9003 309.5 1917 S 1397 -9506 309.5 1850 S 1333 -8660 309.5 1887 S 1366 -9072 184.5 1918 S 1399 -9634 309.5 1855 S 13331 -8660 309.5 1887 S 1366 -9072 184.5 1919 S 1309 -9664 309.5 1845 31339 -9660 309.5 1917 S 1307 -9666 309.5 1855 S 13331 -8660 309.5 1887 S 1369 -9114 309.5 1917 S 1401 -9662 309.5 1855 S 13331 -8660 309.5 1887 S 1369 -9114 309.5 1917 S 1401 -9662 309.5 1855 S 13331 -8660 309.5 1887 S 1369 -9114 309.5 1917 S 1401 -9662 309.5 1855 S 1336 -9660 309.5 1917 S 1407 -9666 309.5 1855 S 1339 -9666	1833	S[1313]	-8330	309.5	1867	S[1347]	-8806	309.5	1901	S[1381]	-9282	309.5
1836 S[1316] -8372 184.5 1870 S[1350] -8948 184.5 1904 S[1344] -9324 184.5 1837 S[1317] -8386 309.5 1871 S[1311] -8982 309.5 1905 S[1385] -9338 309.5 1838 S[1318] -8400 184.5 1872 S[1352] -8876 184.5 1906 S[1386] -9352 184.5 1839 S[1319] -8414 309.5 1873 S[1353] -8890 309.5 1907 S[1387] -9366 309.5 1840 S[1320] -8428 184.5 1874 S[1354] -8904 184.5 1908 S[1388] -9380 184.5 1844 S[1321] -8442 309.5 1875 S[1355] -8918 309.5 1909 S[1389] -9394 309.5 1842 S[1322] -8456 184.5 1876 S[1356] -8932 184.5 1910 S[1390] -9408 184.5 1843 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1324] -8484 184.5 1878 S[1356] -8960 184.5 1912 S[1392] -9436 184.5 1845 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1849 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184.5 1849 S[1329] -8554 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 306 1852 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9520 184.5 1855 S[1333] -8610 309.5 1887 S[1366] -9072 184.5 1922 S[1402] -9576 184.5 1856 S[1336] -8652 184.5 1889 S[1369] -9114 309.5 1922 S[1402] -9576 184.5 1856 S[1336] -8666 309.5 1891 S[1371] -9142 300.5 1922 S[1404] -9604 184.5 1856 S[1336] -8668 184.5 1896 S[1371] -9142 300.5 1922 S[1402] -9576 184.5 1856 S[1336] -8666 309.5 1891 S[1371] -9142 300.5 1922 S[1402] -9576 184.5 1856 S[1336] -8664 309.5 1893 S[1377] -9166 184.5 1928 S[1406] -9632 184.5 1866 S[1340] -8708 184.5 1896 S[1377] -9166 184.5	1836 S 1316 .8372 184.5 1870 S 1350 .8848 184.5 1904 S 1384 .9324 184.5 1837 S 1317 .8386 309.5 1871 S 1351 .8862 309.5 1905 S 1385 .9338 309.5 1838 S 1318 .8400 184.5 1872 S 1352 .8876 184.5 1906 S 1386 .9352 184.5 1838 S 1318 .8414 309.5 1873 S 1353 .8890 309.5 1907 S 1387 .9366 309.5 184.5 1840 S 1320 .8428 184.5 1874 S 1354 .88904 309.5 1907 S 1387 .9366 309.5 1841 S 1321 .8442 309.5 1875 S 1355 .8918 309.5 1909 S 1389 .9394 309.5 1844 S 1322 .8456 184.5 1876 S 1356 .8932 184.5 1910 S 1389 .9340 184.5 1843 S 1323 .8470 309.5 1877 S 1357 .8946 309.5 1911 S 1391 .9422 309.5 1844 S 1324 .8484 184.5 1878 S 1359 .8960 184.5 1912 S 1392 .9436 184.5 1844 S 1326 .8488 309.5 1879 S 1359 .8974 309.5 1913 S 1389 .9450 309.5 1846 S 1326 .8612 .8612 .8612 .8882 .81366 .8932 .8950 .8948 .8454 .8	1834	S[1314]	-8344	184.5	1868	S[1348]	-8820	184.5	1902	S[1382]	-9296	184.5
1837 S 1317 -8366 309.5 1871 S 1351 -8662 309.5 1905 S 1365 -9338 309.5 1838 S 1318 -8400 184.5 1872 S 1352 -8876 184.5 1906 S 1366 -9352 184.5 1839 S 1319 -8414 309.5 1873 S 1353 -8890 309.5 1907 S 1367 -9366 300.5 1840 S 1320 -8428 184.5 1874 S 1354 -8904 184.5 1908 S 1368 -9380 184.5 1841 S 1321 -8442 309.5 1875 S 1355 -8918 309.5 1909 S 1369 -9394 300.5 1842 S 1322 -8456 184.5 1876 S 1356 -8932 184.5 1910 S 1390 -9408 184.5 1843 S 1323 -8470 309.5 1877 S 1357 -8946 309.5 1911 S 1391 -9422 305.5 1844 S 1324 -8484 184.5 1878 S 1358 -8960 184.5 1912 S 1392 -9436 184.5 S 1326 -8512 184.5 1860 S 1369 -8974 309.5 1913 S 1393 -9450 306.5 1844 S 1326 -8512 184.5 1880 S 1360 -8968 184.5 1914 S 1394 -9464 184.5 1848 S 1328 -8540 184.5 1882 S 1362 -9016 184.5 1916 S 1396 -9492 184.5 1849 S 1329 -8564 309.5 1883 S 1363 -9030 309.5 1917 S 1399 -9534 306.5 1853 S 1331 -8582 309.5 1885 S 1365 -9058 309.5 1919 S 1399 -9534 306.5 1855 S 1333 -8610 309.5 1887 S 1369 -9072 184.5 1922 S 1402 -9576 184.5 1856 S 1336 -8652 184.5 1888 S 1369 -9114 309.5 1922 S 1402 -9576 184.5 1856 S 1338 -8660 309.5 1891 S 1371 -9142 300.5 1925 S 1402 -9660 184.5 1856 S 1338 -8660 184.5 1896 S 1370 -9128 184.5 1928 S 1406 -9632 184.5 1856 S 1338 -8660 184.5 1896 S 1370 -9128 184.5 1928 S 1406 -9632 184.5 1856 S 1339 -8664 309.5 1893 S 1371 -9142 300.5 1925 S 1405 -9660 309.5 1856 S 1338 -8660 184.5 1896 S 1370 -9128 184.5 1928 S 1406 -9632 184.5 1856 S 1338 -8660 184.5 1896 S 1370 -9128 184.5 1928	1837 S[1317] -8386 309.5 1871 S[1361] -8662 309.5 1905 S[1365] -9338 309.5 1838 S[1318] -8400 184.5 1672 S[1362] -8876 184.5 1906 S[1366] -9352 184.5 1839 S[1319] -8414 309.5 1673 S[1363] -8890 309.5 1907 S[1367] -9366 309.5 1840 S[1320] -8428 184.5 1874 S[1355] -8918 309.5 1909 S[1369] -9394 309.5 1841 S[1322] -8456 184.5 1876 S[1356] -8922 184.5 1910 S[1369] -9394 309.5 1842 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1326] -8484 184.5 1876 S[1369] -8960 184.5 1912 S[1392] -9	1835	S[1315]	-8358	309.5	1869	S[1349]	-8834	309.5	1903	S[1383]	-9310	309.5
1838 S[1318]	1838 S[1318] .8400 184.5 1872 S[1362] -8876 184.5 1906 S[1386] -9352 184.5 1839 S[1319] .8414 309.5 1873 S[1353] -8890 309.5 1907 S[1387] -9366 309.5 1840 S[1320] .8428 184.5 1874 S[1356] -8918 309.5 1909 S[1388] -9394 309.5 1841 S[1322] .8456 184.5 1876 S[1356] -8932 184.5 1910 S[1390] -9408 184.5 1843 S[1322] .8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1326] -8484 184.5 1878 S[1356] -8960 184.5 1912 S[1392] -9436 184.5 1845 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9	1836	S[1316]	-8372	184.5	1870	S[1350]	-8848	184.5	1904	S[1384]	-9324	184.5
1839 S[1319]	1849 S[1329]	1837	S[1317]	-8386	309.5	1871	S[1351]	-8862	309.5	1905	S[1385]	-9338	309.5
1840 S[1320] -8428 184.5 1874 S[1354] -8904 184.5 1908 S[1388] -9380 184 1841 S[1321] -8442 309.5 1875 S[1355] -8918 309.5 1909 S[1389] -9394 309 30	1840 S 1320	1838	S[1318]	-8400	184.5	1872	S[1352]	-8876	184.5	1906	S[1386]	-9352	184.5
1841 S[1321] -8442 309.5 1875 S[1355] -8918 309.5 1909 S[1389] -9394 308 1842 S[1322] -8456 184.5 1876 S[1356] -8932 184.5 1910 S[1390] -9408 184 1843 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309 1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184 1845 S[1325] -8498 309.5 1879 S[1359] -8974 309.5 1913 S[1393] -9450 306 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1396] -9478	1841 S[1321] -8442 309.5 1875 S[1355] -8918 309.5 1909 S[1389] -9394 309.5 1842 S[1322] -8456 184.5 1876 S[1356] -8932 184.5 1910 S[1390] -9408 184.5 1843 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184.5 1845 S[1325] -8498 309.5 1879 S[1359] -9974 309.5 1913 S[1393] -9450 309.5 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1847 S[1322] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1397] -9	1839	S[1319]	-8414	309.5	1873	S[1353]	-8890	309.5	1907	S[1387]	-9366	309.5
1842 S[1322] -8456 184.5 1876 S[1356] -8932 184.5 1910 S[1390] -9408 184.8 184.8 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184.8 1845 S[1325] -8498 309.5 1879 S[1359] -8974 309.5 1913 S[1393] -9450 309.5 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.8 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1395] -9478 309.5 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184.8 1849 S[1329] -8554 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 309.5 1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9520 184.8 1851 S[1333] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309.5 1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548 184.5 1854 S[1334] -6624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9604 184.5 1855 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1926 S[1404] -9604 184.5 1859 S[1338] -8660 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1859 S[1338] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309.5 1860 S[1340] -8708 184.5 1894 S[1374] -9144 184.5 1928 S[1408] -9660 184.5 1862 S[1342] -8708 184.5 1896 S[1375] -9198 309.5 1927 S[1407] -9648 309.5 1862 S[1342] -8708 184.5 1896 S[1376] -9212 184.5 1920 S[1409] -9674 309.5 1862 S[1342] -8708 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9668 184.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5	1842 S[1322] -8456 184.5 1876 S[1366] -8932 184.5 1910 S[1390] -9408 184.5 1843 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184.5 1845 S[1325] -8498 309.5 1879 S[1359] -8974 309.5 1913 S[1393] -9450 309.5 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1396] -9478 309.5 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184.5 1849 S[1329] -8554 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 309.5 1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9520 184.5 1851 S[1331] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309.5 1853 S[1333] -8610 309.5 1887 S[1366] -9072 184.5 1920 S[1400] -9548 184.5 1855 S[1336] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1922 S[1402] -9576 184.5 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1922 S[1402] -9664 309.5 1858 S[1338] -8694 309.5 1893 S[1371] -9142 309.5 1922 S[1406] -9646 309.5 1858 S[1338] -8680 184.5 1890 S[1371] -9142 309.5 1922 S[1406] -9646 309.5 1858 S[1337] -8666 S[1336] -8660 184.5 1892 S[1371] -9142 309.5 1922 S[1406] -9664 309.5 1858 S[1338] -8694 309.5 1893 S[1371] -9142 309.5 1922 S[1406] -9646 309.5 1858 S[1338] -8680 184.5 1892 S[1371] -9142 309.5 1922 S[1406] -9660 184.5 1860 S[1341] -8722 309.5 1893 S[1371] -9148 184.5 1928 S[1406] -9660 184.5 1860 S[1341] -8722 309.5 1895 S[1376	1840	S[1320]	-8428	184.5	1874	S[1354]	-8904	184.5	1908	S[1388]	-9380	184.5
1843 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184.5 1845 S[1325] -8498 309.5 1879 S[1359] -8974 309.5 1913 S[1393] -9450 309.5 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1395] -9478 309.5 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184.5 1849 S[1329] -8554 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 309.5 1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9520 184.5 1851 S[1331] -8582 309.5 1885 S[1366] -9072 184.5 1920 S[1400] -9548 184.5 1853 S[1333] -8610 309.5 1887 S[1366] -9072 184.5 1922 S[1400] -9548 184.5 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9604 184.5 1855 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1406] -9632 184.5 1859 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1406] -9632 184.5 1859 S[1339] -8690 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1859 S[1339] -8694 309.5 1893 S[1371] -9142 309.5 1925 S[1406] -9632 184.5 1859 S[1374] -9184 184.5 1928 S[1408] -9660 184.5 1856 S[1340] -8728 309.5 1895 S[1375] -9184 309.5 1929 S[1409] -9674 309.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1920 S[1410] -9668 184.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1920 S[1410] -9668 184.5 1866 S[1341] -8722 309.5 1895 S[1376] -9212 184.5 1920 S[1410] -9668 184.5	1843 S[1323] -8470 309.5 1877 S[1357] -8946 309.5 1911 S[1391] -9422 309.5 1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184.5 1845 S[1325] -8498 309.5 1879 S[1359] -8974 309.5 1913 S[1393] -9450 309.5 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1396] -9478 309.5 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184.5 1849 S[1329] -8554 309.5 1883 S[1362] -9016 184.5 1918 S[1397] -9	1841	S[1321]	-8442	309.5	1875	S[1355]	-8918	309.5	1909	S[1389]	-9394	309.5
1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184 1845 S[1325] -8498 309.5 1879 S[1359] -8974 309.5 1913 S[1393] -9450 309.5 1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1396] -9478 309.5 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184 1849 S[1329] -8564 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 309.5 1850 S[1330] -8562 309.5 1885 S[1364] -9044 184.5 1918 S[1399] -9534<	1844 S[1324] -8484 184.5 1878 S[1358] -8960 184.5 1912 S[1392] -9436 184.5 1845 S[1325] -8498 309.5 1879 S[1359] -8974 309.5 1913 S[1393] -9450 309.5 1846 S[1326] -8512 184.5 1880 S[1360] -9988 184.5 1914 S[1394] -9464 184.5 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1396] -9478 309.5 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184.5 1849 S[1329] -8554 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 309.5 1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9	1842	S[1322]	-8456	184.5	1876	S[1356]	-8932	184.5	1910	S[1390]	-9408	184.5
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1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1395] -9478 309 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184 1849 S[1329] -8554 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 309 1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9520 184 1851 S[1331] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309 1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548	1846 S[1326] -8512 184.5 1880 S[1360] -8988 184.5 1914 S[1394] -9464 184.5 1847 S[1327] -8526 309.5 1881 S[1361] -9002 309.5 1915 S[1395] -9478 309.5 1848 S[1328] -8540 184.5 1882 S[1362] -9016 184.5 1916 S[1396] -9492 184.5 1849 S[1329] -8554 309.5 1883 S[1363] -9030 309.5 1917 S[1397] -9506 309.5 1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1399] -9520 184.5 1851 S[1331] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309.5 1852 S[1332] -8696 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9	1844	S[1324]	-8484	184.5	1878	S[1358]	-8960	184.5	1912	S[1392]	-9436	184.5
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1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9520 184 1851 S[1331] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309 1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548 184 1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604	1850 S[1330] -8568 184.5 1884 S[1364] -9044 184.5 1918 S[1398] -9520 184.5 1851 S[1331] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309.5 1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548 184.5 1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309.5 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309.5 1856 S[1336] -8652 184.5 1890 S[1377] -9128 184.5 1924 S[1404] -9	1848	S[1328]	-8540	184.5	1882	S[1362]	-9016	184.5	1916	S[1396]	-9492	184.5
1851 S[1331] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309 1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548 184 1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618	1851 S[1331] -8582 309.5 1885 S[1365] -9058 309.5 1919 S[1399] -9534 309.5 1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548 184.5 1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309.5 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1402] -9576 184.5 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184.5 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9	1849	S[1329]	-8554	309.5	1883	S[1363]	-9030	309.5	1917	S[1397]	-9506	309.5
1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548 184 1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632	1852 S[1332] -8596 184.5 1886 S[1366] -9072 184.5 1920 S[1400] -9548 184.5 1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309.5 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309.5 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184.5 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309.5 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9	1850	S[1330]	-8568	184.5	1884	S[1364]	-9044	184.5	1918	S[1398]	-9520	184.5
1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646	1853 S[1333] -8610 309.5 1887 S[1367] -9086 309.5 1921 S[1401] -9562 309.5 1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309.5 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184.5 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309.5 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9	1851	S[1331]	-8582	309.5	1885	S[1365]	-9058	309.5	1919	S[1399]	-9534	309.5
1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660	1854 S[1334] -8624 184.5 1888 S[1368] -9100 184.5 1922 S[1402] -9576 184.5 1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309.5 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184.5 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309.5 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309.5 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9	1852	S[1332]	-8596	184.5	1886	S[1366]	-9072	184.5	1920	S[1400]	-9548	184.5
1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674	1855 S[1335] -8638 309.5 1889 S[1369] -9114 309.5 1923 S[1403] -9590 309.5 1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184.5 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309.5 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309.5 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184.5 1861 S[1341] -8722 309.5 1895 S[1375] -9188 309.5 1929 S[1409] -9	1853	S[1333]	-8610	309.5	1887	S[1367]	-9086	309.5	1921	S[1401]	-9562	309.5
1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688	1856 S[1336] -8652 184.5 1890 S[1370] -9128 184.5 1924 S[1404] -9604 184.5 1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309.5 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309.5 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184.5 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9	1854	S[1334]	-8624	184.5	1888	S[1368]	-9100	184.5	1922	S[1402]	-9576	184.5
1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309.5 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184	1857 S[1337] -8666 309.5 1891 S[1371] -9142 309.5 1925 S[1405] -9618 309.5 1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309.5 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184.5 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184.5 1863 S[1343] -8750 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9	1855	S[1335]	-8638	309.5	1889	S[1369]	-9114	309.5	1923	S[1403]	-9590	309.5
1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184	1858 S[1338] -8680 184.5 1892 S[1372] -9156 184.5 1926 S[1406] -9632 184.5 1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309.5 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184.5 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184.5 1863 S[1343] -8750 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9702 309.5	1856	S[1336]	-8652	184.5	1890	S[1370]	-9128	184.5	1924	S[1404]	-9604	184.5
1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184	1859 S[1339] -8694 309.5 1893 S[1373] -9170 309.5 1927 S[1407] -9646 309.5 1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184.5 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184.5 1863 S[1343] -8750 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9702 309.5	1857	S[1337]	-8666	309.5	1891	S[1371]	-9142	309.5	1925	S[1405]	-9618	309.5
1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184	1860 S[1340] -8708 184.5 1894 S[1374] -9184 184.5 1928 S[1408] -9660 184.5 1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184.5 1863 S[1343] -8750 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9702 309.5	1858	S[1338]	-8680	184.5	1892	S[1372]	-9156	184.5	1926	S[1406]	-9632	184.5
1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184	1861 S[1341] -8722 309.5 1895 S[1375] -9198 309.5 1929 S[1409] -9674 309.5 1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184.5 1863 S[1343] -8750 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9702 309.5	1859	S[1339]	-8694	309.5	1893	S[1373]	-9170	309.5	1927	S[1407]	-9646	309.5
1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184	1862 S[1342] -8736 184.5 1896 S[1376] -9212 184.5 1930 S[1410] -9688 184.5 1863 S[1343] -8750 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9702 309.5	1860	S[1340]	-8708	184.5	1894	S[1374]	-9184	184.5	1928	S[1408]	-9660	184.5
	1863 S[1343] -8750 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9702 309.5	1861	S[1341]	-8722	309.5	1895	S[1375]	-9198	309.5	1929	S[1409]	-9674	309.5
		1862	S[1342]	-8736	184.5	1896	S[1376]	-9212	184.5	1930	S[1410]	-9688	184.5
1863 S[1343] -8/50 309.5 1897 S[1377] -9226 309.5 1931 S[1411] -9/02 309	1864 S[1344] -8764 184.5 1898 S[1378] -9240 184.5 1932 S[1412] -9716 184.5	1863	S[1343]	-8750	309.5	1897	S[1377]	-9226	309.5	1931	S[1411]	-9702	309.5
1864 S[1344] -8764 184.5 1898 S[1378] -9240 184.5 1932 S[1412] -9716 184		1864	S[1344]	-8764	184.5	1898	S[1378]	-9240	184.5	1932	S[1412]	-9716	184.5

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Abolatorolloo PIN Name XX PAD No. PIN Name X PEN Name PAD No. PRAD No. PIN Name X Y 1333 SIN1441 36734 3034 SIN1441 36744 1845 1868 VISLO -10208 3035 2001 DMY -10682 308.6 1333 SIN1419 -9788 3036 1969 VISLO -10248 3036.5 2001 DMY -10740 108.6 1334 SIN419 -9780 1845 1970 VISLO -10248 304.5 2004 DMY -10774 408.6 1333 SIN419 -9800 1845 1972 VISLO -10248 306.5 2006 DMY -10788 308.6 1333 SIN419 -9804 1845 309.5 1972 VISLO -10248 306.5 200 DMY -10788 2016 1974 VISLO -10348 2016 DMY -10788 2016 2014 10												
1944 19744 19.744 184.5 1968 VGLO -10220 184.5 2002 DMY -10686 184.5 1935 S[1415] -9758 309.5 1969 VGLO -10234 309.5 2003 DMY -10710 309.5 1936 S[1416] -9772 184.5 1970 VGLO -10248 184.5 2004 DMY -10724 184.5 1938 S[1417] -9786 309.5 1971 VGLO -10262 309.5 2005 DMY -10732 308.5 1938 S[1419] -9814 309.5 1973 VGLO -10260 309.5 2007 DMY -10766 309.5 1940 S[1420] -9884 184.5 1976 VGHO -10304 184.5 2000 DMY -10760 184.5 1944 S[1423] -9870 309.5 1977 VGHO -10332 184.5 2010 DMY -10682 184.5		PIN Name	x	Y		PIN Name	х	Y		PIN Name	х	Y
1935 S 1416 .9758 .309.5 .1969 VGLO .10234 .309.5 .2003 .DMY .10710 .309.5 .1968 .S 1416 .9772 .184.5 .1970 .VGLO .10248 .184.5 .2004 .DMY .10724 .184.5 .1937 .S 1417 .9786 .309.5 .1971 .VGLO .10248 .184.5 .2006 .DMY .10738 .309.5 .1938 .S 1418 .9800 .184.5 .1972 .VGLO .10262 .309.5 .2005 .DMY .10738 .309.5 .1938 .S 1418 .9814 .309.5 .1973 .VGLO .10280 .309.5 .2007 .DMY .10760 .309.5 .1940 .S 1420 .9828 .184.5 .1974 .VGHO .10304 .184.5 .2008 .DMY .10760 .184.5 .1941 .S 1421 .9842 .309.5 .1975 .VGHO .10318 .309.5 .2009 .DMY .10760 .10814 .1941 .S 1421 .9842 .309.5 .1976 .VGHO .10318 .309.5 .2010 .DMY .10764 .309.5 .1944 .S 1422 .9865 .184.5 .1976 .VGHO .10336 .308.5 .2011 .DMY .10822 .309.5 .1944 .S 1424 .9884 .184.5 .1978 .VGHO .10346 .308.5 .2011 .DMY .10836 .184.5 .1944 .S 1428 .9898 .309.5 .1979 .VGHO .10360 .184.5 .2012 .DMY .10864 .184.5 .1944 .S 1428 .9912 .184.5 .1980 .VGHO .10346 .10845 .2014 .DMY .10864 .184.5 .1944 .S 1428 .9990 .184.5 .1980 .VGHO .10346 .10845 .2014 .DMY .10864 .184.5 .1944 .S 1428 .9994 .399.5 .1981 .VGHO .10402 .309.5 .2015 .DMY .10878 .309.5 .1944 .S 1428 .9994 .399.5 .1981 .VGHO .10402 .309.5 .2015 .DMY .10878 .309.5 .1945 .51432 .9996 .184.5 .1982 .DMY .10416 .184.5 .2016 .DMY .10962 .1945 .1945 .1945 .51432 .9996 .184.5 .1986 .DMY .10444 .184.5 .2016 .DMY .10962 .1945 .1945 .1945 .51432 .9996 .184.5 .1986 .DMY .10468 .309.5 .2017 .DMY .10962 .1945 .1945 .51432 .19096 .184.5 .1986 .DMY .10468 .309.5 .2021 .DMY .10962 .1945 .1945 .1945 .51432 .10004 .184.5 .1986 .DMY .10506 .184.5 .2022	1933	S[1413]	-9730	309.5	1967	VGLO	-10206	309.5	2001	DMY	-10682	309.5
1936 S 1416 99772 194.5 1970 VGLO -10248 194.5 2004 DMY -10724 194.5 1937 S 1417 -9786 399.5 1971 VGLO -10262 309.5 2005 DMY -10738 309.5 1938 S 1418 -9800 184.5 1972 VGLO -10276 184.5 2006 DMY -10766 309.5 1938 S 1419 -9814 309.5 1973 VGLO -10276 184.5 2006 DMY -10766 309.5 194.	1934	S[1414]	-9744	184.5	1968	VGLO	-10220	184.5	2002	DMY	-10696	184.5
1937 Sit1471 -9786 309.5 1971 VGLO -10262 309.5 2005 DMY -10738 309.5 1938 Sit1418 -9800 184.5 1972 VGLO -10276 184.5 2006 DMY -10752 184.5 1939 Sit1419 -9814 309.5 1973 VGLO -10280 309.5 2007 DMY -10766 309.5 1940 Sit1420 -9828 184.5 1974 VGHO -10318 309.5 2009 DMY -10764 309.5 1942 Sit1421 -9886 184.5 1976 VGHO -10332 184.5 2010 DMY -10808 184.5 1943 Sit1423 -9870 309.5 1977 VGHO -10346 309.5 2011 DMY -10822 309.5 1944 Sit14261 -9884 184.5 1978 VGHO -10380 184.5 2012 DMY -10826 184.5	1935	S[1415]	-9758	309.5	1969	VGLO	-10234	309.5	2003	DMY	-10710	309.5
1938 S[1418] .9800 184.5 1972 VGLO .10276 184.5 2006 DMY .10752 184.5 1939 S[1419] .9814 309.5 1973 VGLO .10290 309.5 2007 DMY .10766 309.5 1940 S[1420] .9828 184.5 1974 VGHO .10304 184.5 2008 DMY .10780 184.5 1941 S[1421] .9842 309.5 1975 VGHO .10318 309.5 2009 DMY .10794 309.5 1942 S[1422] .9866 184.5 1976 VGHO .10332 184.5 2010 DMY .10802 309.5 1944 S[1423] .9870 309.5 1979 VGHO .10374 309.5 2011 DMY .10806 184.5 1945 S[1428] .9912 184.5 1980 VGHO .10374 309.5 2013 DMY .10804 184.5	1936	S[1416]	-9772	184.5	1970	VGLO	-10248	184.5	2004	DMY	-10724	184.5
1939 S[1419] .9814 309.5 1973 VGLO .10290 309.5 2007 DMY .10766 309.5 1940 S[1420] .9828 184.5 1974 VGHO .10304 184.5 2008 DMY .10780 184.5 1941 S[1421] .9842 309.5 1975 VGHO .10318 309.5 2009 DMY .10794 309.5 1942 S[1422] .9856 184.5 1976 VGHO .10346 309.5 2010 DMY .10808 184.5 1943 S[1423] .9870 309.5 1977 VGHO .10346 309.5 2011 DMY .10806 184.5 1944 S[1428] .9884 184.5 1979 VGHO .10374 309.5 2012 DMY .10866 184.5 1946 S[1428] .9912 184.5 1880 VGHO .10388 184.5 2014 DMY .10864 184.5	1937	S[1417]	-9786	309.5	1971	VGLO	-10262	309.5	2005	DMY	-10738	309.5
1940 S[1420] .9828 184.5 1974 VGHO .10304 184.5 2008 DMY .10780 184.5 1941 S[1421] .9842 309.5 1976 VGHO .10318 309.5 2009 DMY .10794 309.5 1942 S[1422] .9856 184.5 1976 VGHO .10332 184.5 2010 DMY .10808 184.5 1943 S[1423] .9870 309.5 1977 VGHO .10360 184.5 2011 DMY .10822 309.5 1944 S[1424] .9884 184.5 1978 VGHO .10360 184.5 2012 DMY .10866 184.5 1945 S[1425] .9898 309.5 1979 VGHO .10374 309.5 2013 DMY .10860 309.5 1946 S[1426] .9912 184.5 1980 VGHO .10374 309.5 2013 DMY .10864 184.5 1947 S[1427] .9926 309.5 1981 VGHO .10402 309.5 2015 DMY .10864 184.5 1948 S[1428] .9940 184.5 1982 DMY .10402 309.5 2015 DMY .10876 309.5 1950 S[1430] .9968 184.5 1983 DMY .10404 184.5 2016 DMY .10906 309.5 1950 S[1430] .9968 184.5 1984 DMY .10444 184.5 2018 DMY .10906 309.5 1951 S[1431] .9982 309.5 1985 DMY .10458 309.5 2019 DMY .10948 184.5 1953 S[1433] .10010 309.5 1987 DMY .10486 309.5 2021 DMY .10948 184.5 1953 S[1434] .10024 184.5 1988 DMY .10500 184.5 2022 DMY .10948 184.5 1955 S[1436] .10052 184.5 1990 DMY .10568 184.5 2026 GO[17] .1104 184.5 1956 S[1438] .10080 184.5 1992 DMY .10568 184.5 2026 GO[17] .1104 309.5 1958 S[1439] .10080 184.5 1992 DMY .10594 184.5 2028 GO[18] .11060 184.5 1961 SDUM2 .10168 184.5 1996 DMY .10568 309.5 2031 GO[19] .11060 184.5 1962 SDUM3 .10168 184.5 1996 DMY .10568 309.5 2031 GO[19] .11060 184.5 1963 DMYAOND .10164 184.5 1998 DMY .10668 309.5 2031 GO[19] .11108 309.5 1964 DMYAOND .10164 184.5 1998 DMY .10660 309.5 2033 GO[20] .11116 184.5 1965 VGLO .10	1938	S[1418]	-9800	184.5	1972	VGLO	-10276	184.5	2006	DMY	-10752	184.5
1941 1942 1942 309.5 1975 VGHO 10318 309.5 2009 DMY 10794 309.5 1942 1942 1942 1986 184.5 1976 VGHO 10332 184.5 2010 DMY 10808 184.5 1943 1942 19870 309.5 1977 VGHO 10346 309.5 2011 DMY 10822 309.5 1944 1942 19884 184.5 1978 VGHO 10360 184.5 2012 DMY 10836 184.5 1945 1945 1942 19888 309.5 1979 VGHO 10374 309.5 2013 DMY 10864 184.5 1946 1946 19912 184.5 1980 VGHO 10374 309.5 2013 DMY 10864 184.5 1947 1947 19926 309.5 1981 VGHO 10402 309.5 2015 DMY 10878 309.5 1948 1942 1940 184.5 1982 DMY 10416 184.5 2016 DMY 10862 184.5 1949 1942 19940 184.5 1982 DMY 10400 309.5 2017 DMY 10862 184.5 1949 1942 19954 309.5 1983 DMY 10400 309.5 2017 DMY 10966 309.5 1950 19430 19968 184.5 1984 DMY 10444 184.5 2018 DMY 10920 184.5 1951 1943 19996 184.5 1986 DMY 10472 184.5 2020 DMY 10948 184.5 1953 19430 19000 309.5 1987 DMY 10486 309.5 2021 DMY 10962 309.5 1954 19430 10000 309.5 1989 DMY 10500 184.5 2022 DMY 10990 309.5 1955 19430 10000 184.5 1990 DMY 10528 184.5 2026 GO[17] 1104 184.5 1958 19430 10000 184.5 1990 DMY 10586 184.5 2026 GO[17] 11040 184.5 1959 19440 10100 184.5 1990 DMY 10586 184.5 2026 GO[17] 11040 184.5 1960 19440 10100 184.5 1990 DMY 10588 309.5 2027 GO[17] 11046 309.5 1960 19440 10100 184.5 1990 DMY 10586 184.5 2026 GO[17] 11046 309.5 1960 19440 10100 184.5 1990 DMY 10588 309.5 2029 GO[18] 11060 184.5 1961 19000 10160 184.5 1990 DMY 10588 309.5 2029 GO[18] 11060 184.5 1962 19000 10100 309.5 1995 DMY 10586 309.5 2020 GO[18] 111060 184.5 1963 1000	1939	S[1419]	-9814	309.5	1973	VGLO	-10290	309.5	2007	DMY	-10766	309.5
1942 S[1422] -9856 184.5 1976 VGHO -10332 184.5 2010 DMY -10808 184.5 1943 S[1423] -9870 309.5 1977 VGHO -10346 309.5 2011 DMY -10822 309.5 1944 S[1424] -9884 184.5 1978 VGHO -10360 184.5 2012 DMY -10836 184.5 1945 S[1425] -9898 309.5 1979 VGHO -10374 309.5 2013 DMY -10850 309.5 1946 S[1426] -9912 184.5 1980 VGHO -10374 309.5 2013 DMY -10864 184.5 1947 S[1427] -9826 309.5 1981 VGHO -10402 309.5 2015 DMY -10878 309.5 1948 S[1428] -9940 184.5 1982 DMY -10416 184.5 2016 DMY -10878 309.5 1948 S[1428] -9954 309.5 1983 DMY -10440 184.5 2016 DMY -10862 184.5 1949 S[1429] -9954 309.5 1983 DMY -10440 309.5 2017 DMY -10966 309.5 1950 S[1430] -9968 184.5 1984 DMY -10440 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10472 184.5 2020 DMY -10934 309.5 1952 S[1432] -996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10466 309.5 2021 DMY -10962 309.5 1956 S[1436] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1957 S[1437] -1066 309.5 1989 DMY -10528 184.5 2022 DMY -11090 309.5 1958 S[1438] -1000 184.5 1990 DMY -10566 184.5 2026 GO[17] -11046 309.5 1958 S[1438] -1008 184.5 1992 DMY -10566 184.5 2026 GO[17] -11046 309.5 1959 S[1439] -10094 309.5 1993 DMY -10566 184.5 2026 GO[17] -11046 309.5 1960 S[1440] -10168 184.5 1996 DMY -10568 309.5 2021 GO[17] -11046 309.5 1961 SDUM2 -10122 309.5 1995 DMY -10668 309.5 2021 GO[17] -11046 309.5 1962 SDUM3 -10164 184.5 1996 DMY -10668 309.5 2021 GO[17] -11046 309.5 1964 DMYGND -10164	1940	S[1420]	-9828	184.5	1974	VGHO	-10304	184.5	2008	DMY	-10780	184.5
1943 S[1423] -9870 309.5 1977 VGHO -10346 309.5 2011 DMY -10822 309.5 1944 S[1424] -9884 184.5 1978 VGHO -10360 184.5 2012 DMY -10836 184.5 1945 S[1425] -9898 309.5 1979 VGHO -10374 309.5 2013 DMY -10860 309.5 1946 S[1426] -9912 184.5 1980 VGHO -10388 184.5 2014 DMY -10864 184.5 1947 S[1427] -9926 309.5 1981 VGHO -10402 309.5 2015 DMY -10878 309.5 1948 S[1428] -9940 184.5 1982 DMY -10416 184.5 2016 DMY -10892 184.5 1949 S[1429] -9954 309.5 1983 DMY -10430 309.5 2017 DMY -10966 309.5 1950 S[1430] -9968 184.5 1984 DMY -10440 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10472 184.5 2020 DMY -10934 309.5 1952 S[1432] -996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10466 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10962 309.5 1955 S[1435] -10038 309.5 1989 DMY -10528 184.5 2022 DMY -10976 184.5 1957 S[1437] -1066 309.5 1991 DMY -10528 184.5 2022 DMY -11040 184.5 1959 S[1438] -1000 184.5 1992 DMY -10566 184.5 2026 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1992 DMY -10566 184.5 2026 GO[17] -11046 309.5 1961 SDUM2 -10122 309.5 1993 DMY -10568 309.5 2027 GO[17] -11046 309.5 1962 SDUM3 -10164 184.5 1996 DMY -10666 309.5 2021 GO[19] -11102 309.5 1963 DMYAGND -10164 184.5 1998 DMY -10666 309.5 2021 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10666 309.5 2031 GO[19] -11102 309.5 1965 VGLO -10178 309.5 1999 DMY -10664 309.5 2033 GO[20] -11116 184.5 1965 VGLO -10178	1941	S[1421]	-9842	309.5	1975	VGHO	-10318	309.5	2009	DMY	-10794	309.5
1944 S 1424 -9884 184.5 1978	1942	S[1422]	-9856	184.5	1976	VGHO	-10332	184.5	2010	DMY	-10808	184.5
1945 S[1425] -9898 309.5 1979 VGHO -10374 309.5 2013 DMY -10850 309.5 1946 S[1426] -9912 184.5 1980 VGHO -10388 184.5 2014 DMY -10864 184.5 1947 S[1427] -9926 309.5 1981 VGHO -10402 309.5 2015 DMY -10878 309.5 1948 S[1428] -9940 184.5 1982 DMY -10416 184.5 2016 DMY -10892 184.5 1949 S[1429] -9954 309.5 1983 DMY -10430 309.5 2017 DMY -10906 309.5 1950 S[1430] -9968 184.5 1984 DMY -10444 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10472 184.5 2020 DMY -10934 309.5 1952 S[1432] -9996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10486 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1436] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10066 309.5 1991 DMY -10566 184.5 2026 GO[17] -11046 309.5 1958 S[1438] -10000 184.5 1992 DMY -10566 184.5 2026 GO[17] -11032 184.5 1969 S[1439] -10094 309.5 1993 DMY -10588 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1996 DMY -10568 309.5 2029 GO[18] -11074 309.5 1962 SDUM3 -10136 184.5 1996 DMY -10668 309.5 2031 GO[19] -11088 184.5 1963 DMYAGND -10164 184.5 1998 DMY -10666 309.5 2031 GO[19] -11088 184.5 1964 DMYAGND -10164 184.5 1998 DMY -10668 309.5 2033 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1997 DMY -10664 309.5 2033 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10664 309.5 2033 GO[20] -11116 184.5 1965 VGLO	1943	S[1423]	-9870	309.5	1977	VGHO	-10346	309.5	2011	DMY	-10822	309.5
1946 S[1426] -9912 184.5 1980 VGHO -10388 184.5 2014 DMY -10864 184.5 1947 S[1427] -9926 309.5 1981 VGHO -10402 309.5 2015 DMY -10878 309.5 1948 S[1428] -9940 184.5 1982 DMY -10416 184.5 2016 DMY -10892 184.5 1949 S[1429] -9954 309.5 1983 DMY -10430 309.5 2017 DMY -10906 309.5 1950 S[1430] -9968 184.5 1984 DMY -10444 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10448 184.5 2020 DMY -10934 309.5 1952 S[1432] -9996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10466 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1435] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10066 309.5 1991 DMY -10528 184.5 2026 GO[17] -1104 309.5 1958 S[1438] -10080 184.5 1992 DMY -10566 184.5 2026 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10564 184.5 2028 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10586 184.5 2020 GO[18] -11060 184.5 1962 SDUM3 -10164 184.5 1996 DMY -10562 309.5 2021 GO[18] -11060 184.5 1963 DMYAGND -10160 309.5 1997 DMY -10626 309.5 2021 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10640 309.5 2033 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10640 309.5 2033 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10640 309.5 2033 GO[20] -111116 309.5 1966 VGLO -1	1944	S[1424]	-9884	184.5	1978	VGHO	-10360	184.5	2012	DMY	-10836	184.5
1947 S[1427] -9926 309.5 1981 VGHO -10402 309.5 2015 DMY -10878 309.5 1948 S[1428] -9940 184.5 1982 DMY -10416 184.5 2016 DMY -10892 184.5 1949 S[1429] -9954 309.5 1983 DMY -10403 309.5 2017 DMY -10906 309.5 1950 S[1430] -9968 184.5 1984 DMY -10444 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10458 309.5 2019 DMY -10934 309.5 1952 S[1432] -9996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10406 309.5 2021 DMY -10962 309.5 <td>1945</td> <td>S[1425]</td> <td>-9898</td> <td>309.5</td> <td>1979</td> <td>VGHO</td> <td>-10374</td> <td>309.5</td> <td>2013</td> <td>DMY</td> <td>-10850</td> <td>309.5</td>	1945	S[1425]	-9898	309.5	1979	VGHO	-10374	309.5	2013	DMY	-10850	309.5
1948 S[1428] -9940 184.5 1982 DMY -10416 184.5 2016 DMY -10892 184.5 1949 S[1429] -9954 309.5 1983 DMY -10430 309.5 2017 DMY -10906 309.5 1950 S[1430] -9968 184.5 1984 DMY -10444 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10458 309.5 2019 DMY -10934 309.5 1952 S[1432] -9966 184.5 1986 DMY -10466 309.5 2021 DMY -10982 309.5 1953 S[1433] -10010 309.5 1987 DMY -10466 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 <td>1946</td> <td>S[1426]</td> <td>-9912</td> <td>184.5</td> <td>1980</td> <td>VGHO</td> <td>-10388</td> <td>184.5</td> <td>2014</td> <td>DMY</td> <td>-10864</td> <td>184.5</td>	1946	S[1426]	-9912	184.5	1980	VGHO	-10388	184.5	2014	DMY	-10864	184.5
1949 S[1429] -9954 309.5 1983 DMY -10430 309.5 2017 DMY -10906 309.5 1950 S[1430] -9968 184.5 1984 DMY -10444 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10458 309.5 2019 DMY -10934 309.5 1952 S[1432] -9996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10486 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1436] -10082 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 <td>1947</td> <td>S[1427]</td> <td>-9926</td> <td>309.5</td> <td>1981</td> <td>VGHO</td> <td>-10402</td> <td>309.5</td> <td>2015</td> <td>DMY</td> <td>-10878</td> <td>309.5</td>	1947	S[1427]	-9926	309.5	1981	VGHO	-10402	309.5	2015	DMY	-10878	309.5
1950 S[1430] -9968 184.5 1984 DMY -10444 184.5 2018 DMY -10920 184.5 1951 S[1431] -9982 309.5 1985 DMY -10458 309.5 2019 DMY -10934 309.5 1952 S[1432] -9996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10486 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1435] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10066 309.5 1991 DMY -10528 184.5 2025 DMY -11018 309.5 1958 S[1438] -10080 184.5 1992 DMY -10566 184.5 2026 GO[17] -11032 184.5 1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10598 309.5 2029 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11060 184.5 1962 SDUM3 -10136 184.5 1996 DMY -10626 309.5 2031 GO[19] -11088 184.5 1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[20] -11116 184.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10640 184.5 2032 GO[20] -11110 309.5 1966 VGLO -10178 309.5 1999 DMY -10640 184.5 2032 GO[20] -11116 184.5 1967 VGLO -10178 309.5 1999 DMY -10640 184.5 2032 GO[20] -11110 309.5 1967 -10640	1948	S[1428]	-9940	184.5	1982	DMY	-10416	184.5	2016	DMY	-10892	184.5
1951 S[1431] -9982 309.5 1985 DMY -10458 309.5 2019 DMY -10934 309.5 1952 S[1432] -9996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10486 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1436] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10666 309.5 1991 DMY -10542 309.5 2025 DMY -11018 309.5 <	1949	S[1429]	-9954	309.5	1983	DMY	-10430	309.5	2017	DMY	-10906	309.5
1952 S[1432] -9996 184.5 1986 DMY -10472 184.5 2020 DMY -10948 184.5 1953 S[1433] -10010 309.5 1987 DMY -10486 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1435] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -1066 309.5 1991 DMY -10528 184.5 2024 DMY -11018 309.5 1958 S[1438] -10080 184.5 1992 DMY -10556 184.5 2026 GO[17] -11032 184.5	1950	S[1430]	-9968	184.5	1984	DMY	-10444	184.5	2018	DMY	-10920	184.5
1953 S[1433] -10010 309.5 1987 DMY -10486 309.5 2021 DMY -10962 309.5 1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1435] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10666 309.5 1991 DMY -10542 309.5 2025 DMY -11018 309.5 1958 S[1438] -10080 184.5 1992 DMY -10556 184.5 2026 GO[17] -11032 184.5 1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 <td>1951</td> <td>S[1431]</td> <td>-9982</td> <td>309.5</td> <td>1985</td> <td>DMY</td> <td>-10458</td> <td>309.5</td> <td>2019</td> <td>DMY</td> <td>-10934</td> <td>309.5</td>	1951	S[1431]	-9982	309.5	1985	DMY	-10458	309.5	2019	DMY	-10934	309.5
1954 S[1434] -10024 184.5 1988 DMY -10500 184.5 2022 DMY -10976 184.5 1955 S[1435] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10066 309.5 1991 DMY -10542 309.5 2025 DMY -11018 309.5 1958 S[1438] -10080 184.5 1992 DMY -10566 184.5 2026 GO[17] -11032 184.5 1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10584 184.5 2028 GO[18] -11060 184.5	1952	S[1432]	-9996	184.5	1986	DMY	-10472	184.5	2020	DMY	-10948	184.5
1955 S[1435] -10038 309.5 1989 DMY -10514 309.5 2023 DMY -10990 309.5 1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10066 309.5 1991 DMY -10542 309.5 2025 DMY -11018 309.5 1958 S[1438] -10080 184.5 1992 DMY -10556 184.5 2026 GO[17] -11032 184.5 1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10584 184.5 2028 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11074 309.	1953	S[1433]	-10010	309.5	1987	DMY	-10486	309.5	2021	DMY	-10962	309.5
1956 S[1436] -10052 184.5 1990 DMY -10528 184.5 2024 DMY -11004 184.5 1957 S[1437] -10066 309.5 1991 DMY -10542 309.5 2025 DMY -11018 309.5 1958 S[1438] -10080 184.5 1992 DMY -10556 184.5 2026 GO[17] -11032 184.5 1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10584 184.5 2028 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11074 309.5 1962 SDUM3 -10136 184.5 1996 DMY -10612 184.5 2030 GO[19] -1108 184.	1954	S[1434]	-10024	184.5	1988	DMY	-10500	184.5	2022	DMY	-10976	184.5
1957 S[1437] -10066 309.5 1991 DMY -10542 309.5 2025 DMY -11018 309.5 1958 S[1438] -10080 184.5 1992 DMY -10556 184.5 2026 GO[17] -11032 184.5 1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10584 184.5 2028 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11074 309.5 1962 SDUM3 -10136 184.5 1996 DMY -10612 184.5 2030 GO[19] -11088 184.5 1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[20] -11116	1955	S[1435]	-10038	309.5	1989	DMY	-10514	309.5	2023	DMY	-10990	309.5
1958 S[1438] -10080 184.5 1992 DMY -10556 184.5 2026 GO[17] -11032 184.5 1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10584 184.5 2028 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11074 309.5 1962 SDUM3 -10136 184.5 1996 DMY -10612 184.5 2030 GO[19] -11088 184.5 1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 <	1956	S[1436]	-10052	184.5	1990	DMY	-10528	184.5	2024	DMY	-11004	184.5
1959 S[1439] -10094 309.5 1993 DMY -10570 309.5 2027 GO[17] -11046 309.5 1960 S[1440] -10108 184.5 1994 DMY -10584 184.5 2028 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11074 309.5 1962 SDUM3 -10136 184.5 1996 DMY -10612 184.5 2030 GO[19] -11088 184.5 1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10654 309.5 2033 GO[20] -11130	1957	S[1437]	-10066	309.5	1991	DMY	-10542	309.5	2025	DMY	-11018	309.5
1960 S[1440] -10108 184.5 1994 DMY -10584 184.5 2028 GO[18] -11060 184.5 1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11074 309.5 1962 SDUM3 -10136 184.5 1996 DMY -10612 184.5 2030 GO[19] -11088 184.5 1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10654 309.5 2033 GO[20] -11130 309.5	1958	S[1438]	-10080	184.5	1992	DMY	-10556	184.5	2026	GO[17]	-11032	184.5
1961 SDUM2 -10122 309.5 1995 DMY -10598 309.5 2029 GO[18] -11074 309.5 1962 SDUM3 -10136 184.5 1996 DMY -10612 184.5 2030 GO[19] -11088 184.5 1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10654 309.5 2033 GO[20] -11130 309.5	1959	S[1439]	-10094	309.5	1993	DMY	-10570	309.5	2027	GO[17]	-11046	309.5
1962 SDUM3 -10136 184.5 1996 DMY -10612 184.5 2030 GO[19] -11088 184.5 1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10654 309.5 2033 GO[20] -11130 309.5	1960	S[1440]	-10108	184.5	1994	DMY	-10584	184.5	2028	GO[18]	-11060	184.5
1963 DMYAGND -10150 309.5 1997 DMY -10626 309.5 2031 GO[19] -11102 309.5 1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10654 309.5 2033 GO[20] -11130 309.5	1961	SDUM2	-10122	309.5	1995	DMY	-10598	309.5	2029	GO[18]	-11074	309.5
1964 DMYAGND -10164 184.5 1998 DMY -10640 184.5 2032 GO[20] -11116 184.5 1965 VGLO -10178 309.5 1999 DMY -10654 309.5 2033 GO[20] -11130 309.5	1962	SDUM3	-10136	184.5	1996	DMY	-10612	184.5	2030	GO[19]	-11088	184.5
1965 VGLO -10178 309.5 1999 DMY -10654 309.5 2033 GO[20] -11130 309.5	1963	DMYAGND	-10150	309.5	1997	DMY	-10626	309.5	2031	GO[19]	-11102	309.5
	1964	DMYAGND	-10164	184.5	1998	DMY	-10640	184.5	2032	GO[20]	-11116	184.5
1966 VGLO -10192 184.5 2000 DMY -10668 184.5 2034 GO[21] -11144 184.5	1965	VGLO	-10178	309.5	1999	DMY	-10654	309.5	2033	GO[20]	-11130	309.5
	1966	VGLO	-10192	184.5	2000	DMY	-10668	184.5	2034	GO[21]	-11144	184.5

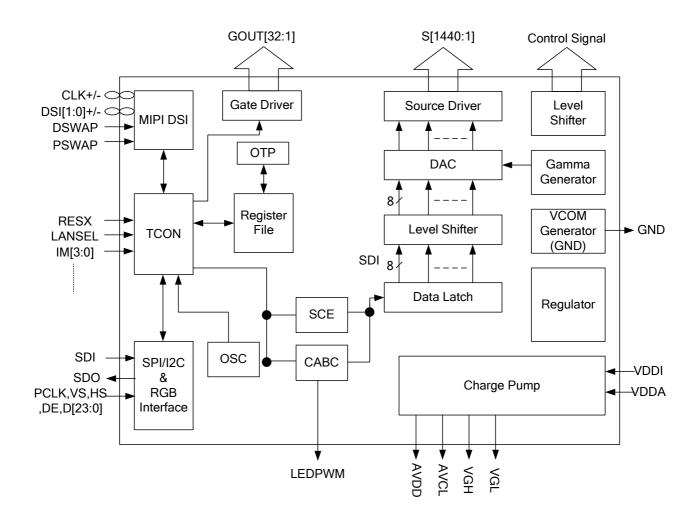
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PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y	PAD No.	PIN Name	х	Y	
2035	GO[21]	-11158	309.5	2050	GO[29]	-11368	184.5	2065	GO[32]	-11578	309.5	
2036	GO[22]	-11172	184.5	2051	GO[29]	-11382	309.5	2066	GO[32]	-11592	184.5	
2037	GO[22]	-11186	309.5	2052	GO[30]	-11396	184.5	2067	VGLO	-11606	309.5	
2038	GO[23]	-11200	184.5	2053	GO[30]	-11410	309.5	2068	VGLO	-11620	184.5	
2039	GO[23]	-11214	309.5	2054	VGLO	-11424	184.5	2069	VGLO	-11634	309.5	
2040	GO[24]	-11228	184.5	2055	VGLO	-11438	309.5	2070	VGHO	-11648	184.5	
2041	GO[24]	-11242	309.5	2056	VGLO	-11452	184.5	2071	VGHO	-11662	309.5	
2042	GO[25]	-11256	184.5	2057	DMY	-11466	309.5	2072	VGHO	-11676	184.5	
2043	GO[25]	-11270	309.5	2058	DMY	-11480	184.5	2073	PADA4	-11690	309.5	
2044	GO[26]	-11284	184.5	2059	DMY	-11494	309.5	2074	PADB4	-11704	184.5	
2045	GO[26]	-11298	309.5	2060	VGL	-11508	184.5	2075	DMY	-11718	309.5	
2046	GO[27]	-11312	184.5	2061	VGL	-11522	309.5	2076	DMY	-11732	184.5	
2047	GO[27]	-11326	309.5	2062	VGL	-11536	184.5	2077	DMY	-11760	309.5	
2048	GO[28]	-11340	184.5	2063	GO[31]	-11550	309.5	2078	ALIGN_L	-11870	302	
2049	GO[28]	-11354	309.5	2064	GO[31]	-11564	184.5	2079	ALIGN_R	11870	302	



5 BLOCK DIAGRAM





6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDDI	I	Power Supply for I/O System.	VDDI
VDDA	I	Power Supply for Analog, Digital System and Booster Circuit.	VDDA
VDDM	ı	Power Supply for MIPI Circuit.	VDDA
VDDB	ı	Power Supply for internal Circuit.	VDDA
VDDB2	ı	Power Supply for internal Circuit.	VDDA
VDDR	I	Power Supply for internal Circuit.	VDDA
VDDR1	I	Power Supply for internal Circuit.	VDDA
VSSB	I	System Ground for internal Circuit.	AGND
VSSB2	ı	System Ground for internal Circuit.	AGND
VSSR	I	System Ground for internal Circuit.	AGND
VSSA	ı	System Ground for internal Circuit.	AGND
VSSM	I	System Ground for MIPI Circuit.	AGND
AGND	ı	System Ground for Analog System and Booster Circuit.	AGND
DGND	I	System Ground for I/O System and Digital System.	DGND
VPP	I	When programming NVM, it needs external power supply voltage (7.5V); the current of lvpp must be more than 10mA. Leave the pin open when not in use.	External Power



6.2 Bus Interface Pins

Name	I/O	Description				Connect Pin				
					Dig	ital Cor	ntrol			
		-The Syste	em inte	rface r	node se	lect.				
			IM3	IM2	IM1	IM0	MPU Interface Mode			
	0 0 0					1	RGB+8b SPI(fall)			
			0	0	1	0	RGB+9b_SPI(fall)			
			0	0	1	1	RGB+16b_SPI(rise)			
				0	1	0	0	RGB+I2C		
			0	1	0	1	MIPI			
IM3, IM2,	ı		0	1	1	0	MIPI+16b SPI(rise)		VDDI/DGND	
IM1, IM0	-		0	1	1	11	MIPI+I2C			
			1	0	0	11	RGB+8b SPI(rise)			
			1	0	1	0	RGB+9b SPI(rise)			
			1	0	1	1	RGB+16b_SPI(fall)			
			1 1	1	0	0 1	RGB+I2C MIPI			
			1	1	0 1	0	MIPI+16b SPI(fall)			
				1	1	1	1	MIPI+I2C		
		<u>L</u>		<u> </u>		<u>'</u>	WIII TTIZO			
		- The exter	rnal re	set inp	ut					
RESETSX	l	- Initializes	the cl	nip with	a low ir	nout. Be	sure to execute a power-on		MPU	
		reset after		•		.,,			•	
						oltage le	evel sequence of V0~V255.			
				_		_	•			
NBWSEL	I	Low: V0 >					•		VDDI/DGND	
		High: V255	5 > V2	54 >:	> V1 > \	/0, norm	ally black			
		Fix to VDD)I level	when n	ot in use	2.				
		General pu	urpose	output	pins. Tl	he outpu	ut voltage swing is VDDI to			
GO [3:0]	0	DGND.							MPU	
		Leave the p	in ope	n.					VDDI/DGND	
					SPE /	12C Inte	erface			
		- A chip se	elect si	nnal						
		Low: the c		_	d and a	oo oo ibla	^			
CSX	ı		•						MPU	
	High: the chip is not selected and not accessible									
		Fix to VDDI or DGND level when not in use.								
		- The SPI interface (DCX): The signal for command or								
	parameter select.									
DCX							MPU			
									IVIPU	
		_	High: Parameter Fix to VDDI or DGND level when not in use.							
		Fix to VDD	or D	GND le	vet when	not in u	ise.			

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Name	I/O	Description	Connect Pin				
CCL /		SCL: Serial clock input for SPI interface.					
SCL/	- 1	I2C_SCL:Serial input clock for I2C Interface.	MPU				
I2C_SCL		Fix to VDDI or DGND level when not in use.					
SDA/		SDA: Serial data input/output bidirectional pin for SPI Interface.					
I2C_SDA	I	I2C_SDA:Serial input data for I2C Interface.	MPU				
120_3DA		Fix to DGND level when not in use.					
SDO	ı	Serial data output pin used for the SPI Interface.	MPU				
300	'	Leave the pin open when not in use.	IVIFU				
		Selection of I2C slave address.					
		2'b00 : Slave Address=1001100					
100 0010.41		2'b01 : Slave Address=1001101	MPU				
I2C_SA[0:1]	l	2'b10 : Slave Address=1001110	IVIPU				
		2'b11 : Slave Address=1001111					
		Fix to VDDI or DGND level when not in use.					
		RGB Interface					
PCLK	ı	Dot clock signal for RGB interface operation	MPU				
I OLK	'	Fix to VDDI or DGND level when not in use.	IVII O				
VS	ı	Frame synchronizing signal for RGB interface operation	MPU				
	•	Fix to VDDI or DGND level when not in use.					
HS	ı	Line synchronizing signal for RGB interface operation	MPU				
110	•	Fix to VDDI or DGND level when not in use.	IVII O				
		Data enable signal for RGB interface operation					
DE		Low: access enabled	MPU				
DL DL		High: access inhibited	IVII O				
		Fix to VDDI or DGND level when not in use.					
		A 24-bit parallel data bus for RGB Interface.					
		24-bit/pixel: D[23:16]=R,D[15:8]=G,D[7:0]=B					
DB [23:0]	I/O	18-bit/pixel: MDT=0:D[21:16]=R,D[13:8]=G,D[5:0]=B	MPU				
DD [20.0]	1/0	MDT=1:D[17:12]=R,D[11:6]=G,[5:0]=B	IVII O				
		16-bit/pixel: D[20:16]=R,D[13:8]=G,[4:0]=B					
		Fix to VDDI or DGND level when not in use.					
		CABC Control					
LEDON	0	Used for turning On/Off external LED backlight control.	CABC				
		Leave the pin open when not in use.	JABO				
LEDPWM	0	The PWM frequency output for LCD driver control.	CABC				
	0	Leave the pin open when not in use.	3, 123				

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Name	I/O					Descri	ption				Connect Pin
					M	IIPI Interi	face				
CP CN	I	Th	MIPI DSI differential clock pair. That the COG resistance is less than 10 ohm. If MIPI are not in use, they should be connected to VSSM.							MIPI	
DP0 DN0 DP1 DN1	I/O	MI Th	IPI DSI differential data pair. nat the COG resistance is less than 10 ohm. MIPI are not in use, they should be connected to VSSM							MIPI	
ERR	0	S/ thi	W comma	RC and ECC error output pin for the MIPI interface, activated by W command. This pin is output low when it is not activated. When is pin is activated, it is output high if CRC/ECC error is found.						MIPI	
LANSEL	I	Lo	put pin to bw: 1 data gh: 2 data x to VSSI	lane a lanes			lanes in	MIPI/MD	DI interfa	ace.	MIPI
DSWAP			Differential clock polarity swap for MIPI interface Pins DSWAP PSWAP								
PSWAP	P			0	CLK_P	CLK_N CLK_N	D0_P D0_P	D0_N D0_N	D1_P D1_P	D1_N D1_N	VDDI/DGND
				0	CLK_N CLK_P	CLK_P CLK_N	D0_N D1_P	D0_P D1_N	D1_N D0_P	D1_P D0_N	
			1	1	CLK_N	CLK_P	D1_N	D1_P	D0_N	D0_P	

Note1. "1" = VDDI level, "0" = DGND level.

Note2. When in parallel mode, unused data pins must be connected to "1" or "0".

Note3. When CSX="1", there is no influence to the parallel and serial interface.



6.3 Driver Output Pins

Name	I/O	Description	Connect pin	
S [1:1440]	0	Source output voltage signals applied to a LCD panel	LCD	
GOUT [1:32]	0	Gate control signals and the swing voltage level is VGHO to VGLO	LCD	
CDUM (0.21	0	Dummy Source	LCD	
SDUM [0:3]	0	Leave the pin open when not in use.	LCD	
VCOM	0	Regulator output for common voltage of panel.	LCD	
VCOIVI		Fix to AGND level.	LCD	
VGL	0	Connect to VGL or OPEN.	LCD	
VGLO	0	Negative Output voltage from the regulator.	LCD	
VGL_REG	0	Connect to VGL or OPEN.	LCD	
VGHS	0	Connect to VGH.	LCD	
VGHO	0	Positive Output voltage from the regulator.	LCD	

6.4 Test and other pins

VCC	0	Used for monitoring.	OPEN
VCCMA	0	Used for monitoring.	OPEN
V20	0	Used for monitoring.	OPEN
VPS1/VPS2	0	Used for monitoring.	OPEN
VCCMD	0	Used for monitoring.	OPEN
V12TX	0	Used for monitoring.	OPEN
AVDD	0	Power Pad for analog Circuit.	OPEN
AVCL	0	Power Pad for analog Circuit.	OPEN
VAN	0	A power output of grayscale voltage.	OPEN
VAP	0	A power output (negative) of gray scale voltage.	OPEN
RDX	ı	Input pin for testing.	VDDI/DGND
KDA	'	Fix to VDDI or DGND level.	VDDI/DGND
DSTB_SEL		input pin for testing.	DGND
D31B_3EE	'	Fix to DGND level.	DGND
EXB1T	ı	This pin is for test	DGND
LABIT	'	Fix to DGND level when not in use.	DGND
VGSW[0:3]	ı	Input pins for testing.	VDDI/DGND
VG3VV[0.3]	'	Fix to DGND level when not in use.	עטטווטטאוט
TESTO[0:3]	0	Output pins for testing.	OPEN
12310[0.3]		Please keep these pins floating.	OPEN
TE_L	0	For IC Test.	OPEN

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		Leave the pin open when not in use.	
VGHP	0	Power Pad for analog Circuit.	OPEN
VCUEO2	0	Output pins for testing.	ODEN
VGHEQ2		Please keep this pin floating.	OPEN
VSSIDUM0~3	ı	GND Dummy pads. Connect to AGND.	AGND
PADA1		These test pins for chip attachment detection.	
PADB1		PADA1 to PADA2 are output pins and PADB1 to PADB2 are input pins.	
PADA2	I/O	-For normal operation:	OPEN
PADB2		Connect PADA1 and PADB1 together by ITO trace.	
PADBZ		Connect PADA2 and PADB2 together by ITO trace.	
CNTACT1	1/0	Test his for test handing quality	OPEN
CNTACT2	I/O	Test pin , for test bonding quality.	OPEN
		These pins are dummy (no electrical characteristic)	
DUMMY	-	Can pass signal through these pads on TFT panel.	OPEN
		Please open these pins.	



7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +3.6	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +3.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	$^{\circ}$ C
Storage Temperature Range	TSTG	-40 ~ +125	$^{\circ}\!\mathbb{C}$

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

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7.2 DC Characteristics

			S	pecification	on		Related
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Pins
		Power & Operation	n Voltage				
System Voltage	VDD	Operating voltage	2.5	2.8	3.6	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		11.5		18	V	
Gate Driver Low Voltage	VGL		-7.6		-12	V	
Gate Driver Supply Voltage		VGH-VGL	-		30	V	
		Input / Outp	ut				
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Differential Input High Threshold Voltage	VIT+			0	50	mV	
Differential Input Low Threshold Voltage	VIT-		-50	0		mV	MIPI_CLK MIPI_Data
Single-ended Receiver Input Operation Voltage Range	VIR		0.5		1.2	V	
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		0.1	uA	Note 1
		VCOM Volta	ge				
VCOM amplitude	VCOM			VSS		V	
		Source Driv	er				
Gamma Reference Voltage(Positive)	VAP		4.4		6.4	V	
Gamma Reference Voltage(Negative)	VAN		-2.6		-4.6	V	
Source Output Settling Time	Tr	Below with 99% precision			10	us	Note 2

Table 2 Basic DC Characteristics

Notes:

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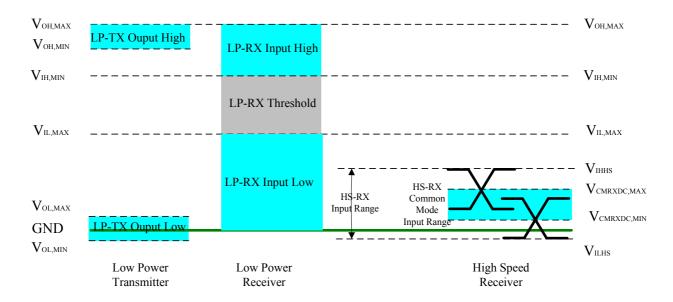




- 2. The Max. value is between measured point of source output and gamma setting value.
- 3. When evaluating the maximum and minimum of VGH, VDD=2.8V.
- 4. The maximum value of |VGH-VGL| can no over 30V.



7.3 DC Characteristics



VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25~%

		,,,,	DD1=1.0, VDD=2.0, F		1
Parameter	Cumbal		Unit		
Farameter	Symbol	MIN	TYP	MAX	Unit
Operation	n Voltage for I	MIPI Receiver			
Low power mode operating voltage	Vlph	1.1	1.2	1.3	V
MIPI Characte	ristics for Higl	Speed Rece	iver	•	-
Single-ended input low voltage	VILHS	-40	-	-	mV
Single-ended input high voltage	Vihhs	-	-	460	mV
Common-mode voltage	VCMRXDC	70	-	330	mV
Differential input impedance	ZID	80	100	125	ohm
MIPI Charac	teristics for Lo	ow Power Mod	de		
Pad signal voltage range	Vı	-50	-	1350	mV
Logic 0 input threshold	VIL	0-	-	550	mV
Logic 1 input threshold	Vін	880	-	1350	mV
Output low level	Vol	-50	-	50	mV
Output high level	Vон	1.1	1.2	1.3	V



7.4 Power Consumption

Ta=25 $^{\circ}$ C, Frame rate = 60Hz, Registers setting are IC default setting.

		Current Consumption					
Operation Mode	Image	Тур	ical	Maximum			
Operation Mode	Image	IDDI	IDD	IDDI	IDD		
		(uA)	(uA)	(uA)	(uA)		
Sleep-in mode		5	45	10	60		

Table 3 Power Consumption

Notes:

1. The Current Consumption is DC characteristics of ST7701.

2. *Typical: VDDI=1.8V, VDD=2.8V;*



7.5 AC Characteristics

7.5.1 Serial Interface Characteristics (3-line serial):

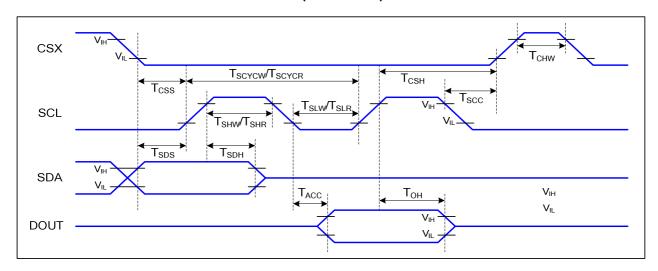


Figure 1 3-line serial Interface Timing Characteristics

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 $^{\circ}$ C

Signal	Symbol	Parameter	Min	Max	Unit	Description
	T _{CSS}	Chip select setup time (write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
CSX	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	60		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
	T _{SCYCW}	Serial clock cycle (Write)	66		ns	
	T _{SHW}	SCL "H" pulse width (Write)	15		ns	
SCL	T _{SLW}	SCL "L" pulse width (Write)	15		ns	
SCL	T _{SCYCR}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA	T_{SDS}	Data setup time	10		ns	
(DIN)	T _{SDH}	Data hold time	10		ns	

Table 4 3-line serial Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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7.5.2 Serial Interface Characteristics (4-line serial):

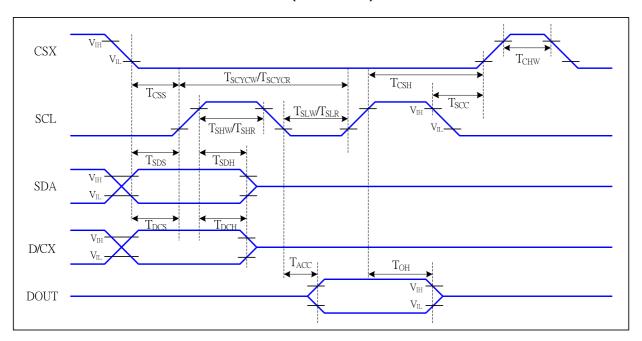


Figure 2 4-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 $^{\circ}$ C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
	T _{CSS}	Chip select setup time (write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
CSX	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
	T _{SCYCW}	Serial clock cycle (Write)	66		ns	wite command 9 date
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	-write command & data
SCL	T _{SLW}	SCL "L" pulse width (Write)	15		ns	ram
SCL	T _{SCYCR}	Serial clock cycle (Read)	150		ns	road command 9 data
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	-read command & data
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	ram
D/CX	T _{DCS}	D/CX setup time	10		ns	
D/CX	T _{DCH}	D/CX hold time	10		ns	
SDA	T _{SDS}	Data setup time	10		ns	
(DIN)	T _{SDH}	Data hold time	10		ns	

Table 5 4-line serial Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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7.5.3 Serial Interface Characteristics (I2C):

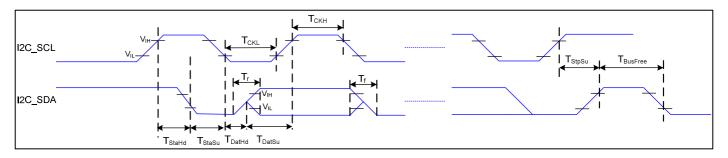


Figure 3 I2C Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 $^{\circ}$ C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
I2C	T _{CKL+} T _{CKH}	Working frequency	-	400	KHz	
SCL	T _{CKL}	SCL "H" pulse width	1.3	-	us	
COL	T _{CKH}	SCL "L" pulse width	0.6	-	us	
	T _r	Data rising timg	20	300	ns	
	T_f	Data falling timg	20	300	ns	
	T_{SDS}	Data setup time	100	-	ns	
I2C	T_{SDH}	Data hold time	0	0.9	us	
SDA	T_{StaSU}	Start condition setup time	0.6	-	us	
	T _{StaHD}	Start condition hold time	0.6	-	us	
	T_{StpSU}	Stop condition setup time	0.6	-	us	
	$T_{BusFREE}$	Bus free time	1.3	-	us	

Table 6 I2C serial Interface Characteristics

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7.5.4 RGB Interface Characteristics:

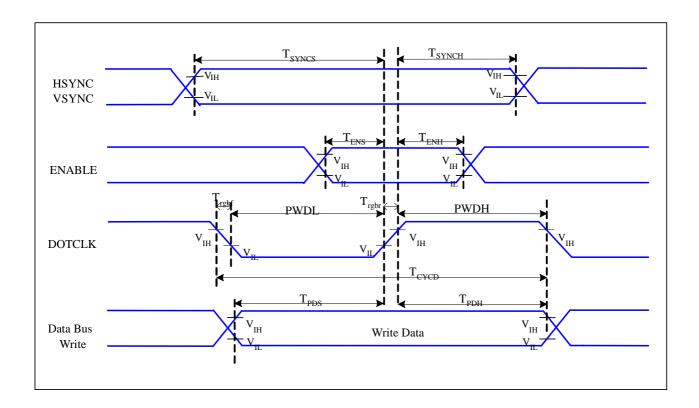


Figure 4 RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC,	т	VOVNO LICVNO Cotus Time	_		20	
VSYNC	T _{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T _{ENS}	Enable Setup Time	5	-	ns	
ENABLE	T _{ENH}	Enable Hold Time	5	-	ns	
	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
DOTCLK	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
DOTCLK	T _{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T _{PDS}	PD Data Setup Time	5	-	ns	
DB	T_{PDH}	PD Data Hold Time	5	-	ns	

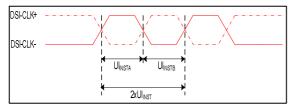
Table 7 18/16 Bits RGB Interface Timing Characteristics

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7.5.5 MIPI Interface Characteristics:

7.5.5.1 High Speed Mode



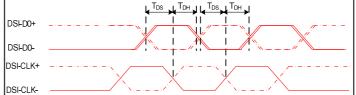


Figure 5 DSI clock channel timing

Figure 6 Rising and falling time on clock and data channel

 $VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25~^{\circ}C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	2xUI _{INSTA}	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI _{INSTA} UI _{INSTB}	UI instantaneous halfs	2	12.5	ns	UI = UI _{INSTA} = UI _{INSTB}
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 8 Mipi Interface- High Speed Mode Timing Characteristics

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7.5.5.2 Lowe Power Mode

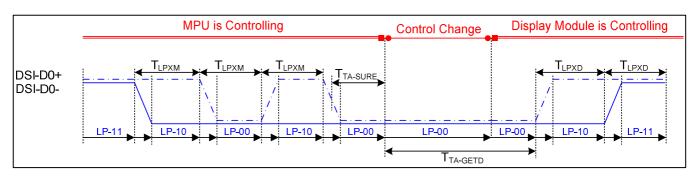


Figure 7 Bus Turnaround (BTA) from display module to MPU Timing

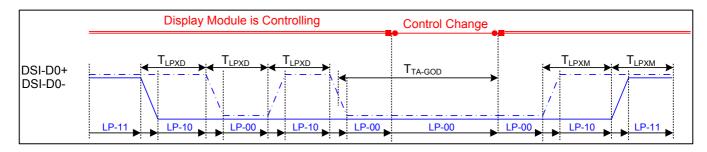


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
		Length of LP-00,LP-01,				
DSI-D0+/-	TLPXM	LP-10 or LP-11 periods	50	75	ns	Input
		MPU→Display Module				
		Length of LP-00,LP-01,				
DSI-D0+/-	TLPXD	LP-10 or LP-11 periods	50	75	ns	Output
		MPU→Display Module				
DSI-D0+/-	TTA-SURED	Time-out before the MPU	T _{LPXD}	2xT _{LP}	ns	Output
D3I-D0 1 /-	TIA-SUNLD	start driving	I LPXD	XD	20	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by	5vT	T		Input
D3I-D0 1 /-	TIA-GLID	display module	5xT _{LPXD}		ns	
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after	4xT _{LPXD}		ns	Output
D31-D0 1 7-	TIA-GOD	turnaround request-MPU	47.1	LPXD	113	Output

Table 9 Mipi Interface Low Power Mode Timing Characteristics

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7.5.5.3 DSI Bursts Mode

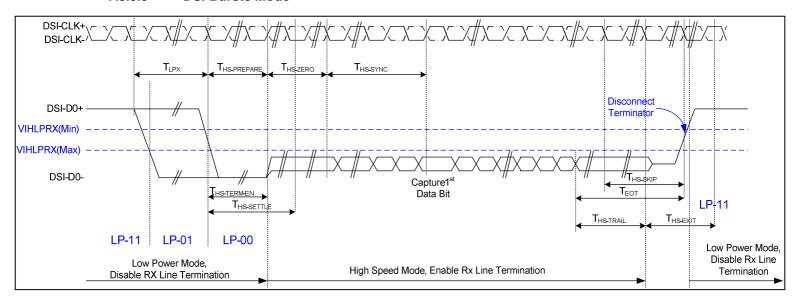


Figure 8 Data lanes-Low Power Mode to/from High Speed Mode Timing

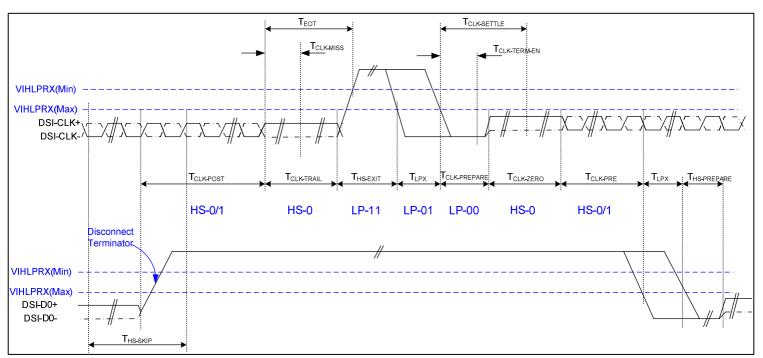


Figure 9 Clock lanes- High Speed Mode to/from Low Power Mode Timing

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 $VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 \ \ ^{\circ}\!\!C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
	I	Low Power Mode to High Speed Mo	ode Timi	ng		ı
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
	ŀ	High Speed Mode to Low Power Mo	ode Timi	ng		
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
	Hig	h Speed Mode to/from Low Power	Mode Ti	ming		
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission		38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/- TEOT		Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input



7.5.6 Reset Timing:

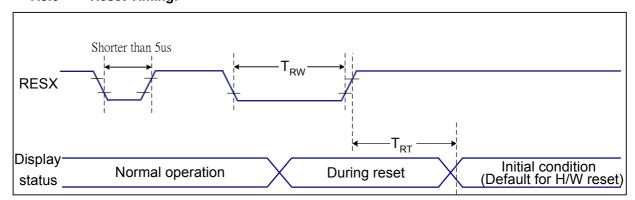


Figure 10 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
	TRW	Reset pulse duration	10	-	us
RESX	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 10 Reset Timing

Notes:

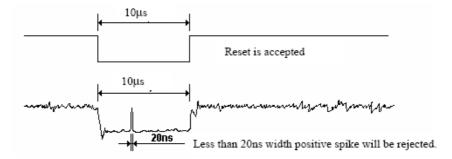
- 1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
 - 2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- 3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
 - 4. Spike Rejection also applies during a valid reset pulse as shown below:

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- 5. When Reset applied during Sleep In Mode.
- 6. When Reset applied during Sleep Out Mode.
- 7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



8 FUNCTION DESCRIPTION

8.1 System Interface

ST7701 supports RGB serial interfaces, I2C and MIPI serial interfaces. Selection of these interfaces are set by IM[3:0] pins as shown below.

IM3	IM2	IM1	IMO	Interface	Data pins
	0	0	1	RGB+8b_SPI(fall)	D[0~23]
	0	1	0	RGB+9b_SPI(fall)	D[0~23]
	0	1	1	RGB+16b_SPI(rise)	D[0~23]
0	1	0	0	RGB+I2C	D[0~23]
	1	0	1	MIPI	HSSI_D1_P/N,HSSI_D0_P/N
	1	1	0	MIPI+16b_SPI(rise)	HSSI_D1_P/N,HSSI_D0_P/N
	1	1	1	MIPI+I2C	HSSI_D1_P/N,HSSI_D0_P/N
	0	0	1	RGB+8b_SPI(rise)	D[0~23]
	0	1	0	RGB+9b_SPI(rise)	D[0~23]
	0	1	1	RGB+16b_SPI(fall)	D[0~23]
1	1	0	0	RGB+ I2C	D[0~23]
	1	0	1	MIPI	HSSI_D1_P/N,HSSI_D0_P/N
	1	1	0	MIPI+16b_SPI(fall)	HSSI_D1_P/N,HSSI_D0_P/N
	1	1	1	MIPI+I2C	HSSI_D1_P/N,HSSI_D0_P/N

Table 11 Interface Type Selection

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8.2 Serial Interface

The serial interface is either 3-lines/9-bits,16-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Pin description

3-line serial interface (9 bits)

Pin Name	Description	
CSX	Chip selection signal	
SCL	Serial input CLK	
SDA	Serial input data	
SDO	Serial output data	

4-line serial interface (8 bits)

Pin Name	Description		
CSX	Chip selection signal		
DCX	Data is regarded as a command when WRX is low		
DCX	Data is regarded as a parameter or data when WRX is high		
SCL	Clock signal		
SDA	Serial input data		
SDO	Serial output data		

I²C serial interface

Pin Name	Description	
SCL	Clock signal	
SDA	Serial input data	
SDO	Serial output data	
I ² C_SA[0:1]	I ² C slave address	

Table 12 pin description of serial interface

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8.2.1 Serial Interface (SPI)

8.2.1.1 Command write mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is "low", the transmission byte is interpreted as a command byte. If D/CX is "high", the transmission byte is command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

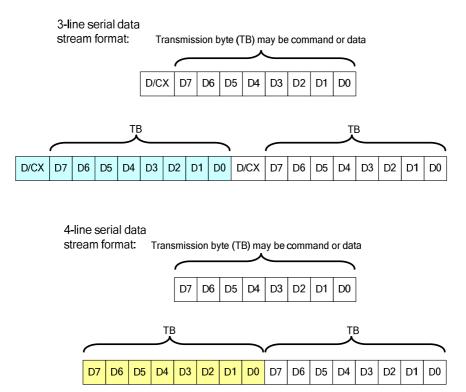


Figure 11 Serial interface data stream format

When CSX is "high", SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX='0') or parameter data (D/CX='1'). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL..

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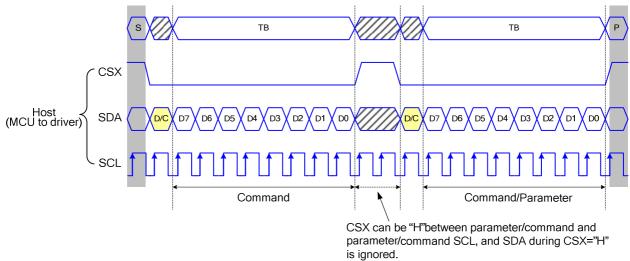


Figure 12 3-line serial interface write protocol (write to register with control bit in transmission)

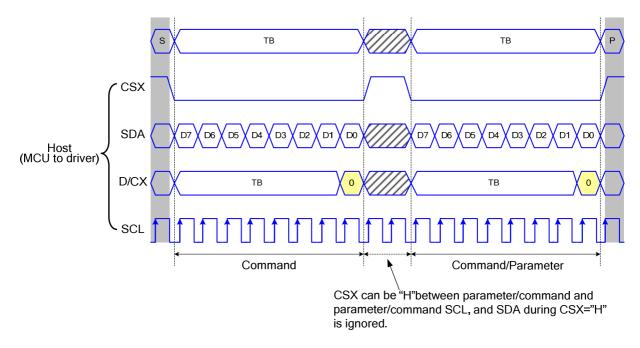


Figure 13 4-line serial interface write protocol (write to register with control bit in transmission)

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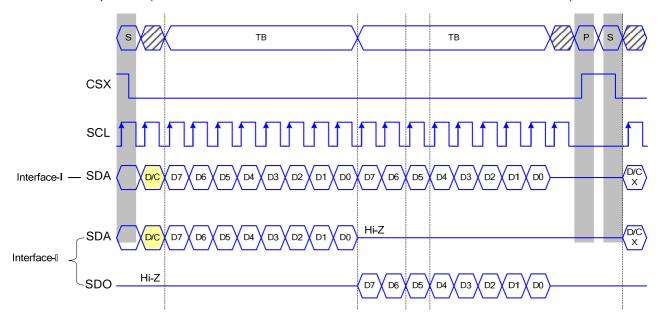
8.2.2 Read function

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

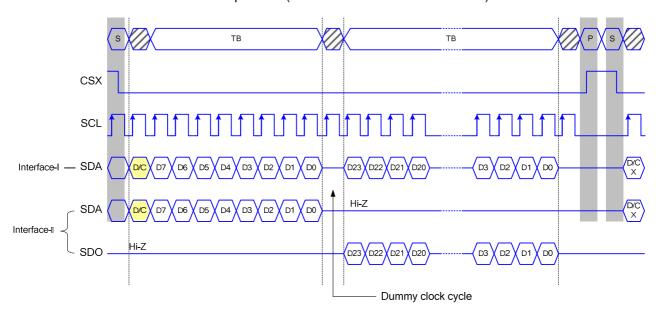
3-line serial interface protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



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3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

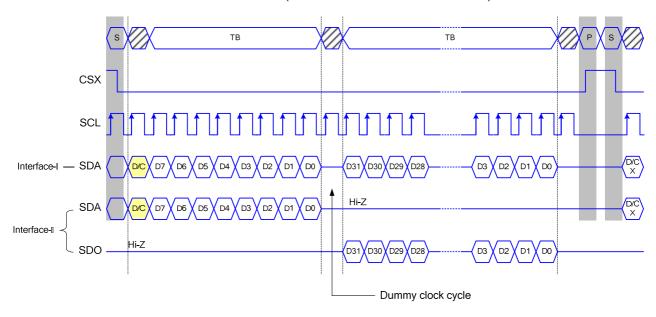


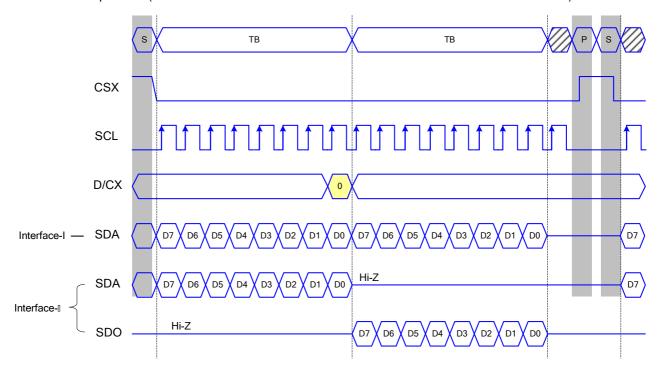
Figure 14 3-line serial interface read protocol

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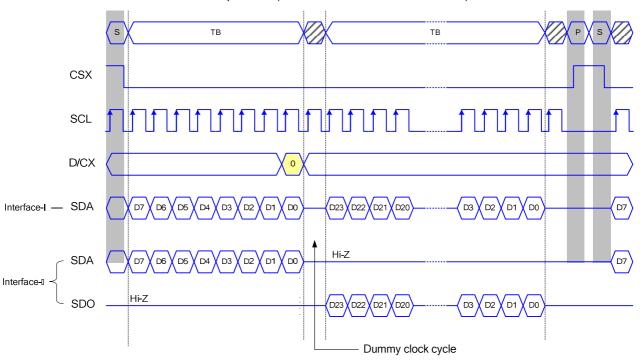
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4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

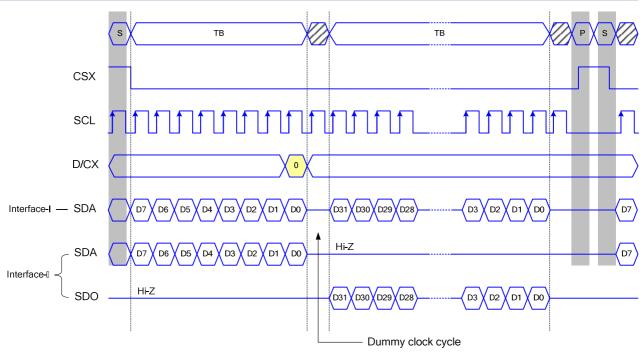


Figure 15 4-line serial interface read protocol

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8.3 16 bit Serial Interface

8.3.1 Write Mode

The write mode of the interface means the micro controller writes commands and data to the ST7701. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low. SDI/SDO are sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

Figure 16 serial 16 bit interface write mode

Hi-Z

Hi-Z

Hi-Z

Hi-Z

SDI

SDO

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8.3.2 Read Mode

The read mode of the interface means that the micro controller reads register value from the ST7701. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The ST7701 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. It doesn't need any dummy clock when execute the command data read.

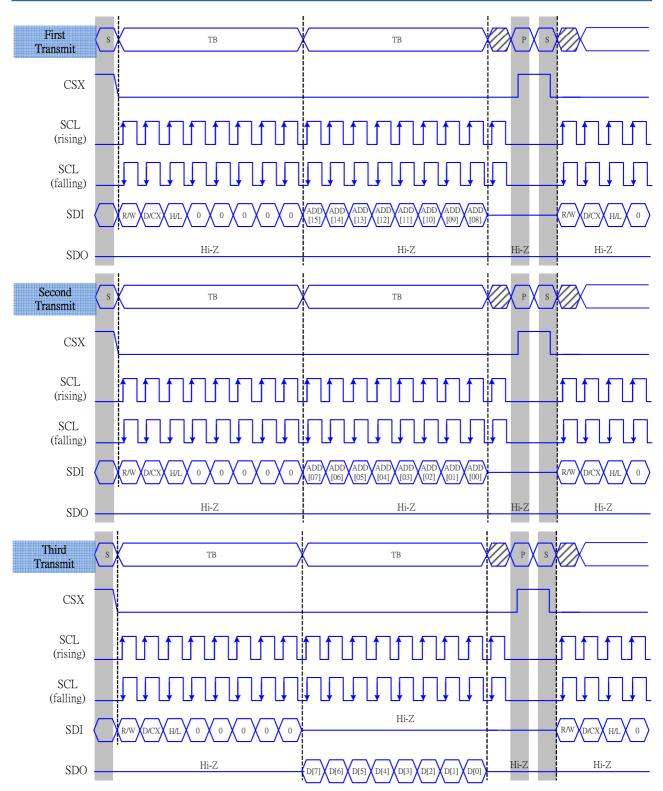


Figure 17 serial 16 bit interface read mode

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8.4 I²C serial Interface

8.4.1 Characteristics of I²C bus

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines compose of a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.4.1.1 System configuration

- (1) Transmitter: the device which sends the data to the bus
- (2) Receiver: the device which receives the data from the bus
- (3) Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- (4) Slave: the device addressed by a master
- (5) Multi-Master: more than one master attempts to control the bus at the same time without corrupting the message
- (6) Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- (7) Synchronization: procedure to synchronize the clock signals of two or more devices.

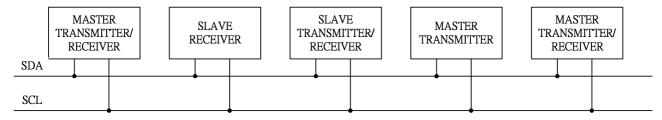


Figure 18 I²C System configuration

8.4.1.2 Bit transfer

One data bit is transferred during each clock pulse. The data on SDA line must remain stabilized during the HIGH period of the clock pulse.

As changes in the data line at this time will be interpreted as a control signal.

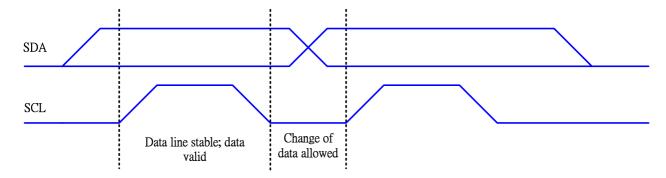


Figure 19 I2C Bit transfer.

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8.4.1.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition on the data line is defined as the STOP condition (P) while the clock is HIGH.

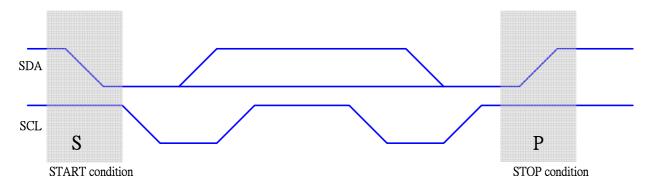


Figure 20 I2C Definition of START and STOP conditions.

8.4.1.4 Acknowledgment

Each bit in a byte (8 bits) is followed by an acknowledgment bit. The acknowledgment bit is a HIGH signal placed on the bus by the transmitter during the master generating an extra acknowledgment related clock pulse.

An addressed slave receiver must generate an acknowledgment after the reception of each byte. Also a master receiver must generate an acknowledgment after the reception of each byte that has been clocked out of the slave transmitter.

The acknowledged device must pull-down the SDA line during the acknowledgment clock pulse, so that the SDA line remains LOW during the HIGH period of the acknowledgment related clock pulse (setup and hold times must be considered).

A master receiver must signal an end of data to the transmitter by not generating an acknowledgment on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

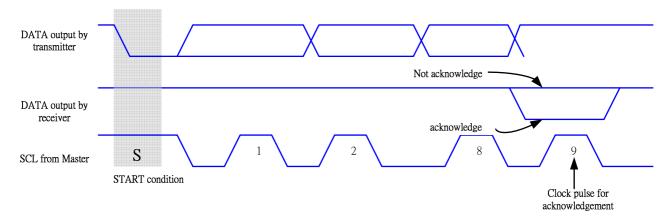


Figure 21 Acknowledgement of the I²C bus.

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8.4.1.5 I²C bus protocol

Before any data is transmitted on the I^2C -bus, the device to respond is addressed first. Two 7-bit slave addresses (10011xx) are reserved for the ST7701. The least significant bit of the slave address is set by connecting the input $I^2C_SA[1:0]$.

I2C_SA1	I2C_SA0	Slave address	Notes
0	0	1001100	Other sleve address
0	1	1001101	Other slave address
1	0	1001110	are reversed for other IC.
1	1	1001111	10.

Table 13 Reserve address for ST7701

8.4.1.6 I2C bus Write Instruction and parameter

- (1) Data transfers for register writing follow the format is shown in Table 14.
- (2) After the START condition (Str), a slave address is sent. R/W bit is setting to "zero" for WRITE.
- (3) The slave issues an ACK to master.
- (4) 16 bits register high byte address transfer first. Then transfer the register low byte address.
- (5) 16 bits register high byte data of parameter transfer first. Then transfer the register low byte data parameter .
- (6) A data transfer is always terminated by a STOP condition.

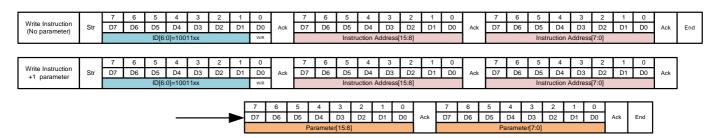


Table 14 I²C write stream for write command

8.4.1.7 I2C bus read

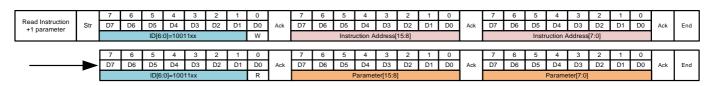


Table 15 I2C read stream

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8.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

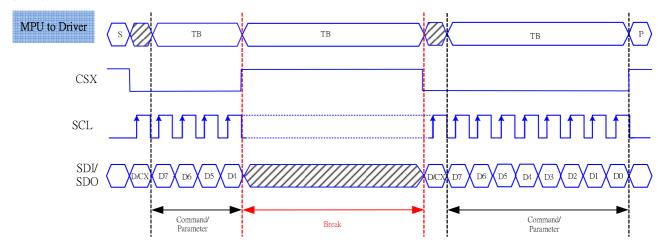


Figure 22 Data Transfer Break and Recovery.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

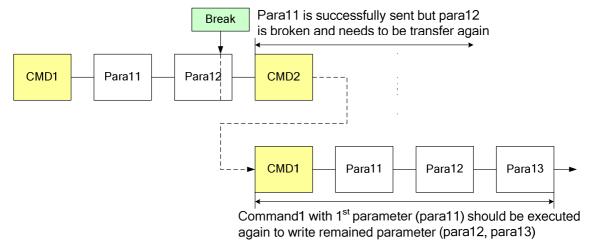


Figure 23 Write interrupts recovery

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If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

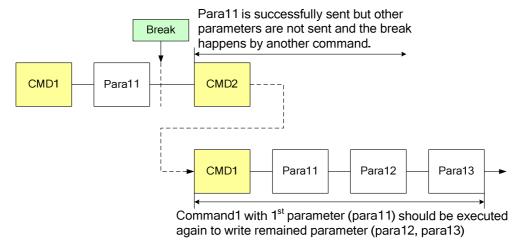


Figure 24 Write interrupts recovery



8.6 Data Transfer Pause

Transferring a Command, Frame Memory Data, or Multiple Parameter Data might invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the ST7701 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters or a new command when the Chip Select Line is enabled again, as shown below.

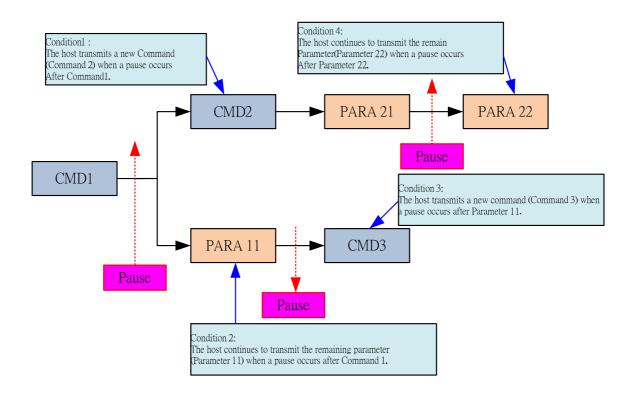


Figure 25 Data Transfer Pause

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MPU to Driver S TB TB TB P CSX SCL SDI/ SDA O D7 D6 D5 D4 D3 D2 D1 D0 Command Command/ Parameter The CSX can be in high level between the data and the next command. The SDI(SDA) and SCL are invalid if the CSX is in high level.

Figure 26 Serial Data Transfer Pause

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter



8.7 RGB Interface

The ST7701 support RGB interface Mode 1 and Mode 2. The interface signals as shown in table 6.3.1.

The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state.

The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7701.

In RGB Mode 2, back porch of Vsync is defined by VBP[5:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command. And front porch of Hsync is defined by HFP[5:0] of RGBPRCTR command.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit,18-bit and 24-bit format

Table 16 The interface signals of RGB interface



8.7.1 RGB Color Format

ST7701 supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	24 bits configuration	18 bits cor VIPF[3:	nfiguration 0]=0110	16 bits configuration
	VIPF[3:0]=0111	MDT=0	MDT=1	VIPF[3:0]=0101
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	В7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	В3	B3	B3	В3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	В0	В0	В0	В0

Table 17 The interface color mapping of RGB interface

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8.7.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

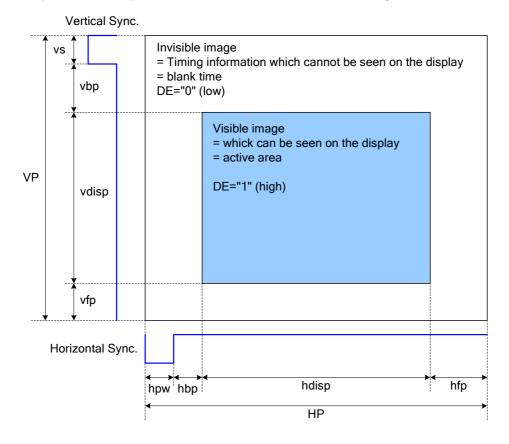


Figure 27 Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Тур.	Max.	Unit
Horizontal Sync. Width	hpw	1	-	255	Clock
Horizontal Sync. Back Porch	hbp	1		255	Clock
Horizontal Sync. Front Porch	hfp	1		-	Clock
Vertical Sync. Width	VS	1		254	Line
Vertical Sync. Back Porch	vbp	1		254	Line
Vertical Sync. Front Porch	vfp	2			Line

Note:

1. Typical value are related to the setting frame rate is 60Hz..

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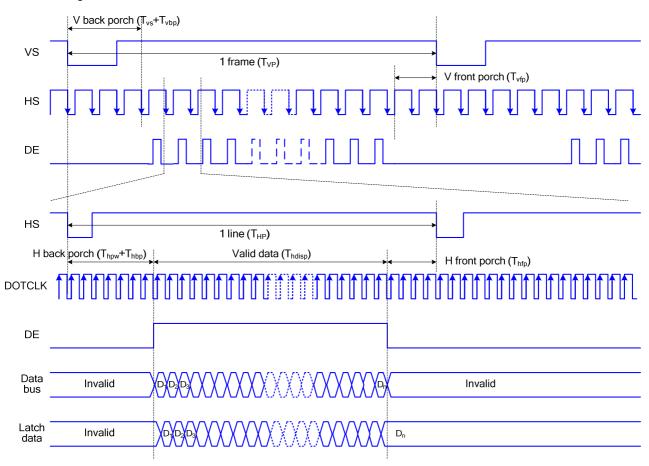
8.7.3 RGB Interface Mode Selection

ST7701 supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode							
0	DE mode							
1	HV mode							

8.7.4 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 28 Timing Chart of Signals in RGB Interface DE Mode

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The timing chart of RGB interface HV mode is shown as follows.

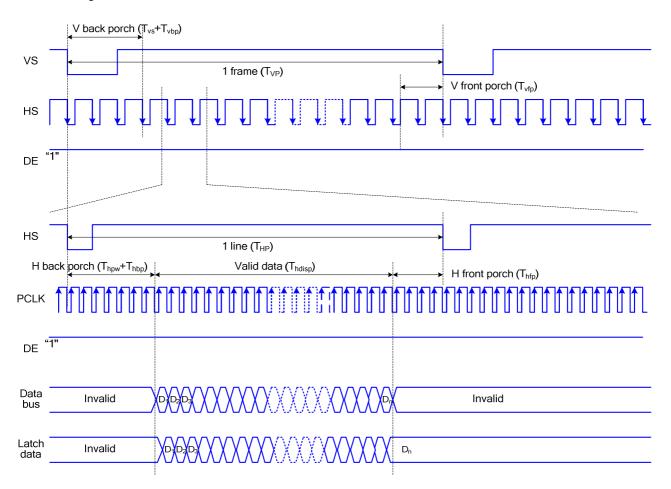


Figure 29 Timing chart of RGB interface HV mod

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8.8 MIPI-DSI interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

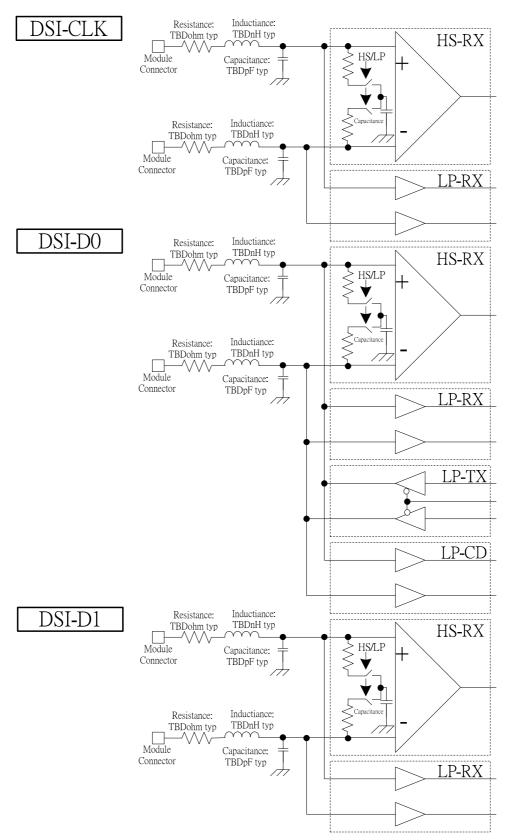
Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

Lane Pair	MCU (Master) Display Module (Slave)							
	Unidirectional Lane							
Clock Lane	■ Clock Only							
	■ Escape Mode(ULPS Only)							
	Bi-directional Lane							
Data Lane 0	■ Forward High-Speed							
Data Lane 0	■ Bi-directional Escape Mode							
	■ Bi-directional LPDT							
	Unidirectional Lane							
Data Lane 1	■ Forward High-Speed							
Dala Lalle I	■ Escape Mode (ULPM only)							
	■ No LPDT							



8.8.1 Display Module Pin Configuration for DSI





8.8.2 Display Serial Interface (DSI)

8.8.2.1 General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level: High level communication

8.8.2.2 Interface level communication

8.8.2.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1 and Data lane2 can be driven High Speed mode only.

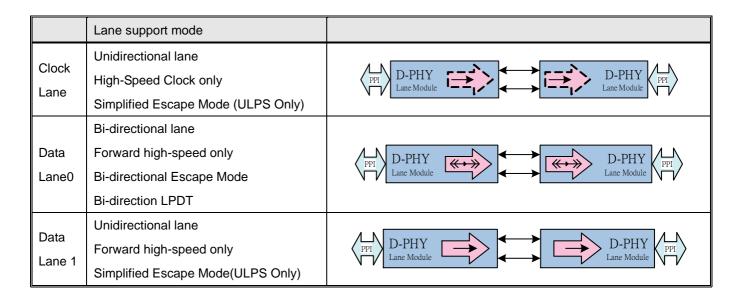


Table 18 The interface color Lane types and support mode

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Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair	Line DC vol	Itage Levels	High Speed(HS)	Low-Power(LP)					
State Code	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode				
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1				
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1				
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space				
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0				
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1				
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2				

Table 19 High Speed and Low-Power Lane Pair State Descriptions

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

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8.8.2.2.2 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

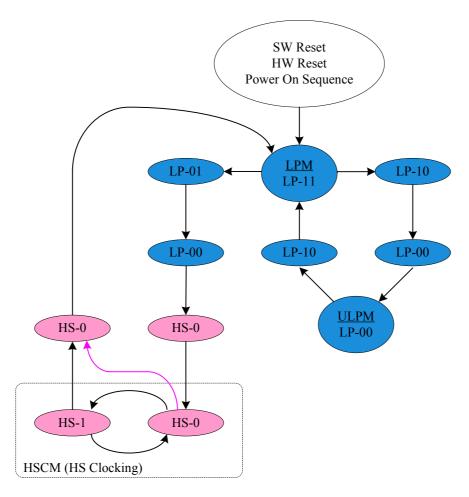


Figure 30 Clock Lanes Power Modes

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8.8.2.2.2.1 Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode(LMP), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

After SW Reset, HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM,LP-00 State Code)=>LP10=>LP-11(LPM).

This sequence is illustrated below.

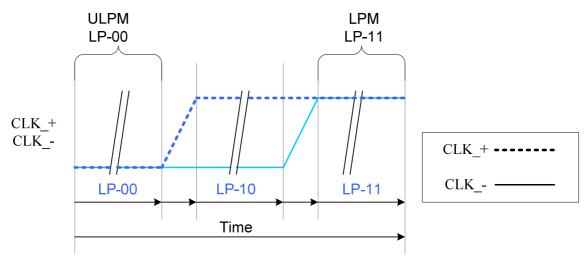


Figure 31 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.

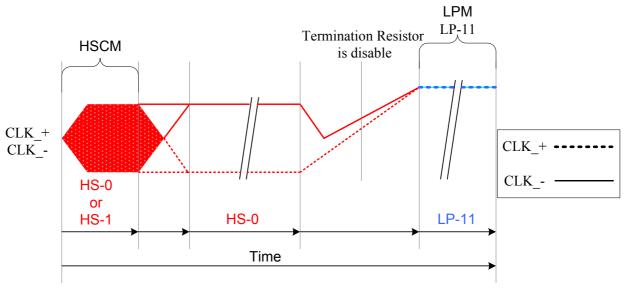


Figure 32 From HSCM to LPM

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All three mode changes are illustrated a flow chart below.

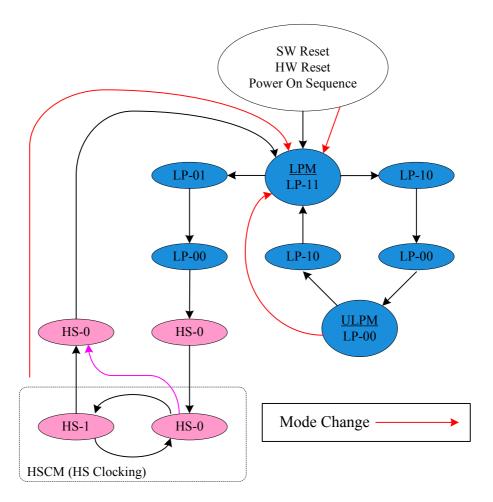


Figure 33 All three mode changes to LPM



8.8.2.2.2.2 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00(ULPM). This sequence is illustrated below.

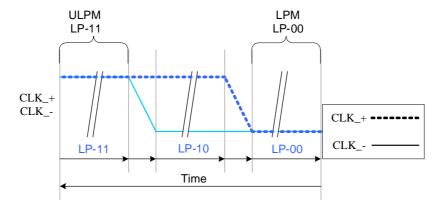


Figure 34 From LPM to UPLM

The mode change is also illustrated below:

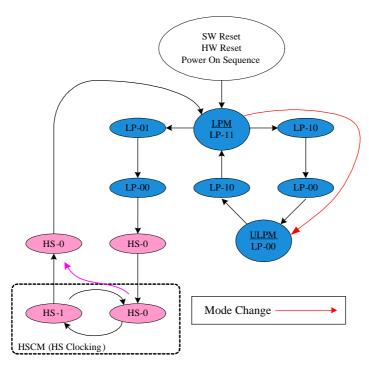


Figure 35 The mode change from LPM to UPLM

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8.8.2.2.2.3 High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.

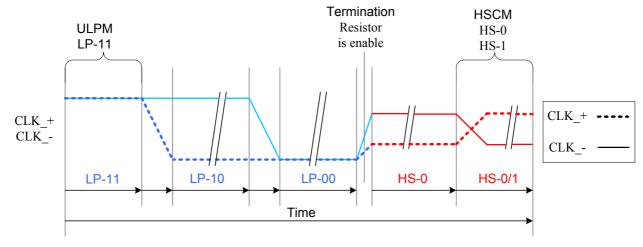


Figure 36 From LPM to HSCM

The mode change is also illustrated below:

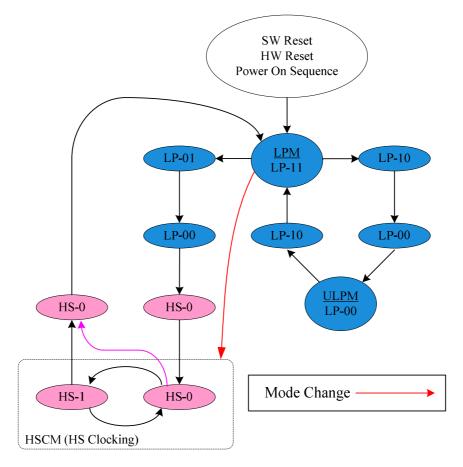


Figure 37 Mode Change from LPM to HSCM on the Flow Chart

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The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

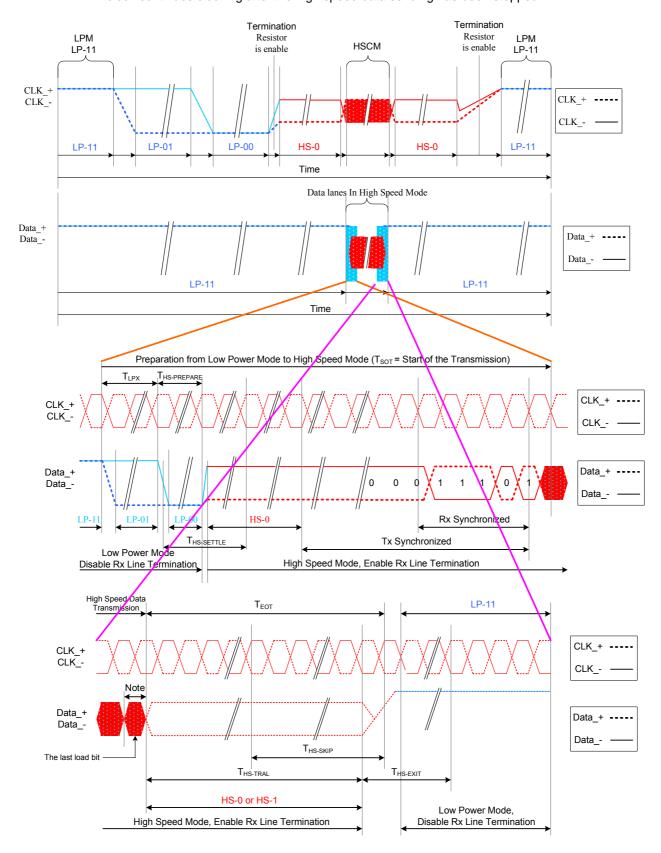


Figure 38 High Speed Clock Burst

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8.8.2.2.3 DSI-DATA LANES

8.8.2.2.3.1 GENERAL

DSI-D0+/- Data Lanes can be driven in different modes which are:

- Escape Mode (Only DSI-D0+/- data lanes are used)
- High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)
- Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence					
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)					
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11					
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z					

Notes:

- 1. Only DSI-D0+/- data lanes are used.
- 2. DSI-D1+/- and DSI-D0+/- data lanes are used.
- 3. More information on section "Bus Turnaround (BTA)"



8.8.2.2.3.2 **ESCAPE MODE**

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

- Send "Low-Power Data Transmission" (LPDT) e.g. from the MCU to the display module
- Drive data lanes to "Ultra-Low Power State" (ULPS)
- Indicate "Remote Application Reset" (RAR), which is reset the display module
- Indicate "Tearing Effect" (TEE), which is used for a TE trigger event from the display module to the MCU
- Indicate "Acknowledge" (ACK), which is used for a non-error event from the display module to the MCU The basic sequence of the Escape Mode is as follow
- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- · A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction is illustrated below:

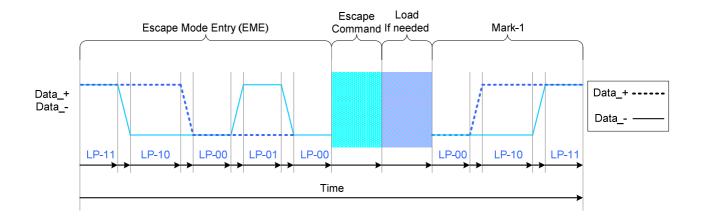


Figure 39 General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

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Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit→Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 _{bin}	-	0
Ultra-Low Power Mode	Mode	0001 1110 _{bin}	0	0
Underfined-1, Note 1	Mode	1001 1111 _{bin}	1	-
Underfined-2, Note 1	Mode	1101 1110 _{bin}	-	-
Remote Application Reset	Trigger	0110 0010 _{bin}	1	0
Tearing Effect	Trigger	0101 1101 _{bin}	-	-
Acknowledge	Trigger	0010 0001 _{bin}	-	0
Unknow-5,Note 1	Trigger	1010 0000 _{bin}	-	-

Notes:

- 1. This Escape command support has not been implemented on the display module.
- 2. n=1.
- 3. "O"=Supported
- 4. "-"=Not Supported
- 5. Tearing Effect Trigger can not be used in MIPI Video mode.



Low-Power Data Transmission(LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

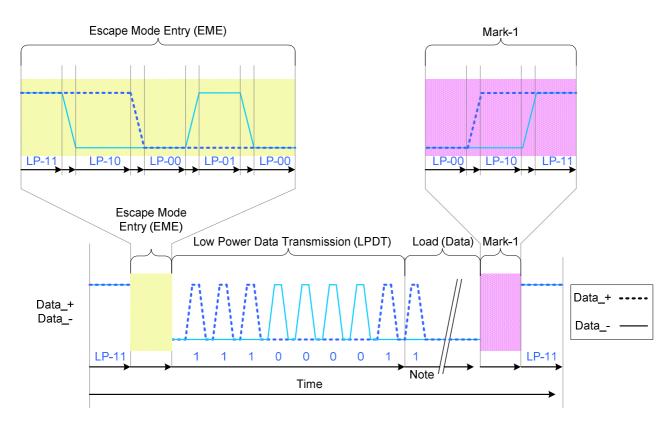
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data): One or more bytes (8 bits)

Data lanes are in pause mode when data lanes are stopped (Bothe lanes are low) between bytes

- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logical "1" in this Exsample

Figure 40 Low-Power Data Transmission (LPDT)

Notes:

Load(Data) is presenting that the first bit is logical '1' in this example



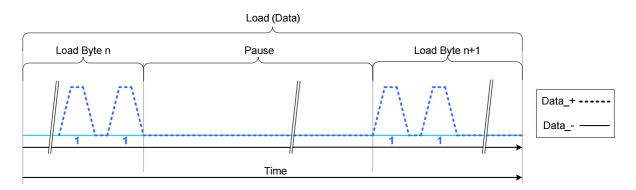


Figure 41 Pause (Example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

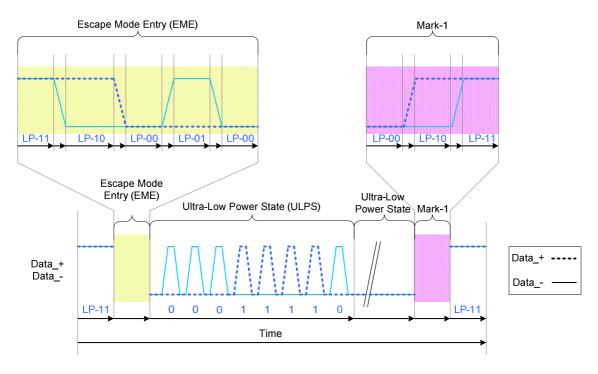


Figure 42 Ultra-Low Power State (ULPS)

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Remote Application Reset (RAP)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

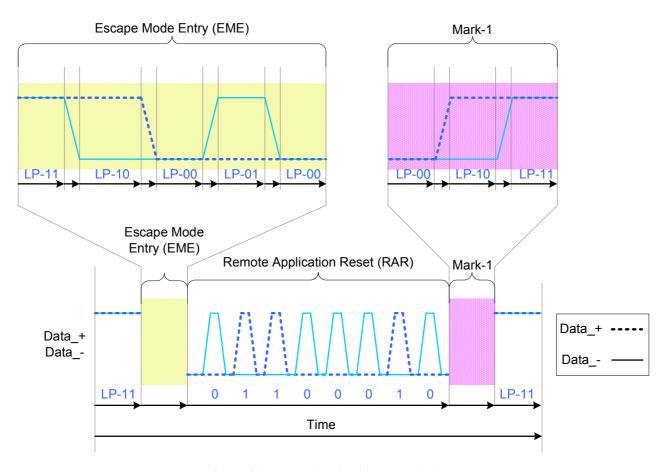


Figure 43 Remote Application Reset (RAR)

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Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

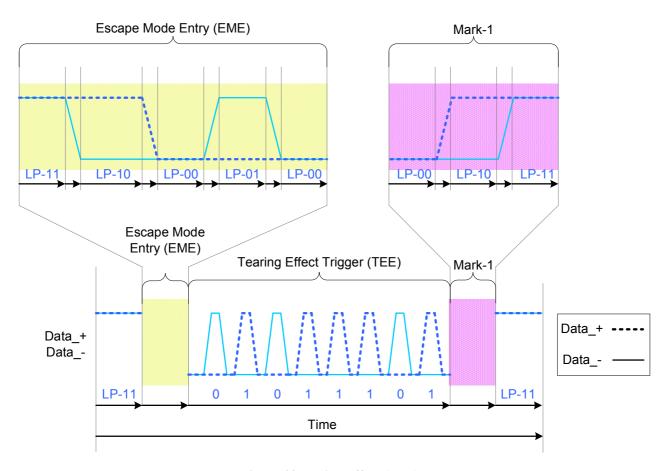


Figure 44 Tearing Effect (TEE)

Note: Tearing Effect (TEE) can not be used in MIPI Video Mode

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Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

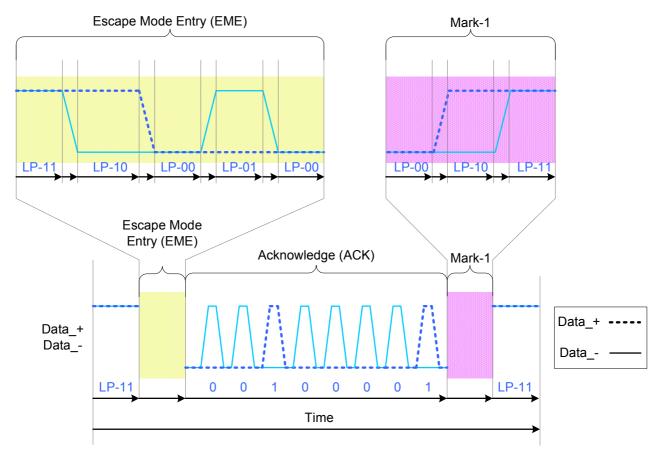


Figure 45 Acknowledge (ACK)

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8.8.2.2.3.3 HIGH SPEED DATA TRANSMISSION (HSDT)

Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "8.8.2.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

• Start: LP-11

• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) - Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below

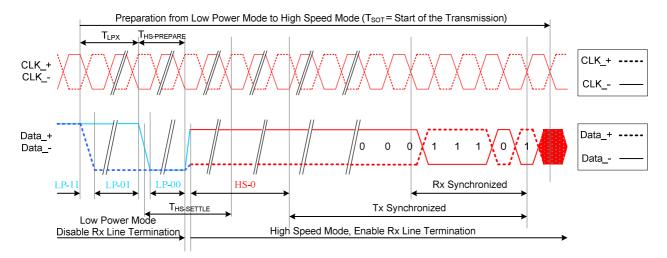


Figure 46 Entering High-Speed Data transmission (T_{SOT} of HSDT)

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Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter "5.3.2.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

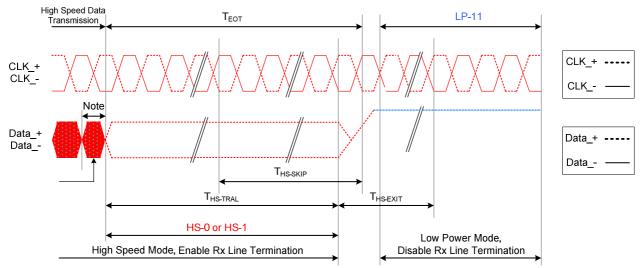


Figure 47 Levaving High-Speed data Transmission (T_{EOT} of HSDT)



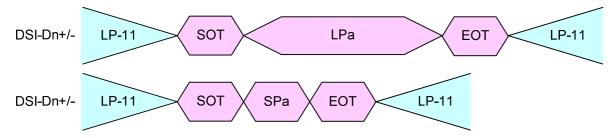
Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission

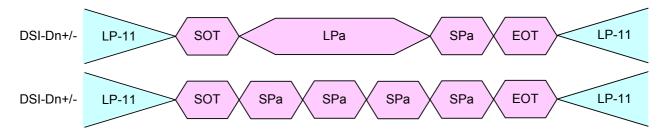
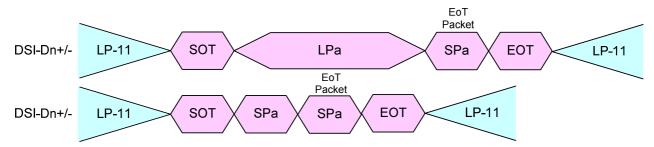


Figure 48 HS Transmission Example with EoT packet disabled

Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission

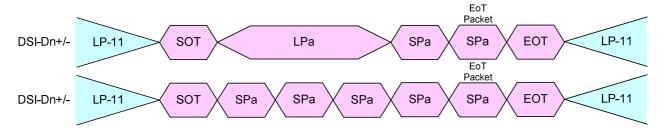


Figure 49 HS Transmission Example with EoT packet enable

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Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are'1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission



Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

- Start (MCU):LP-11
- Turnaround Request (MCU): LP-11 _ LP-10 _ LP-00 _ LP-10 _ LP-00
- The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)
- The display module changes to the stop mode: LP-00 _ LP-10 _ LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.

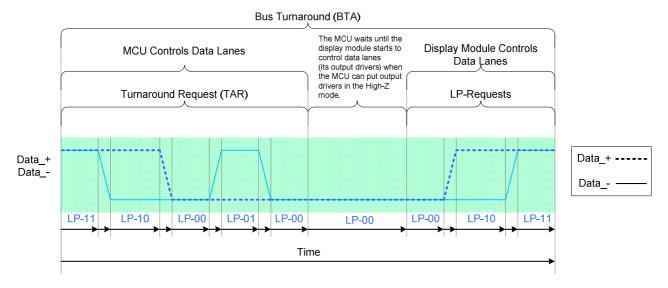


Figure 50 Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

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8.8.2.3 Packet Level Communication

8.8.2.3.1 Short Packet (SPA) And Long Packet (LPA) Structure

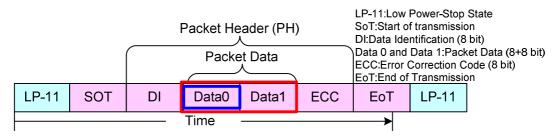
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

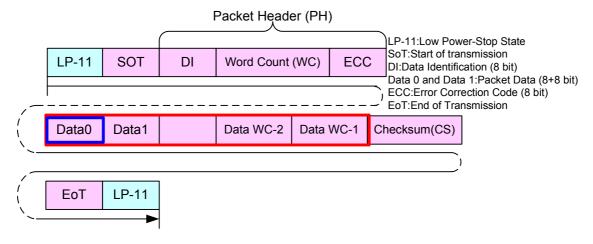
- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

Short Packet (Spa) Structure:



Long Packet (Spa) Structure:



Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11,

SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

- * LP-11 =>SoT =>SPa =>LPa =>SPa =>EoT =>LP-11
- * LP-11 =>SoT =>SPa =>SPa =>EoT =>LP-11
- * LP-11 =>SoT =>LPa =>LPa =>EoT =>LP-11

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8.8.2.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

DI WC (LSB)										WC (MSB)						ECC															
29 hex 01 hex										00 hex								06 hex													
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
L							М	L							М	L	L					М	L							М	
S							S	S							S	S							s	S							s
В	<u>B</u> B											В	В	в В					В	BB						В					
	Time —												\rightarrow																		

Figure 51 Bit Order of Byte on Packets

8.8.2.3.1.2 Bit Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last. This same order is illustrated for reference purposes below.

	1	N) (LS	B)	WC (MSB)											
	01 hex									00 hex								
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В			
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7			
T							М	L							М			
S							s	s							s			
В							В	В							В			
\vdash					_	•	Tir	ne)	_					→			

Figure 52 Byte Order of the Multiple Byte on Packets

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8.8.2.3.1.3 Pack Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

• 4th byte: Error Correction Code (ECC)

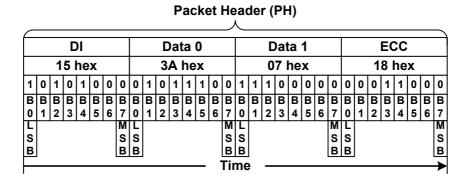


Figure 53 Packet Header (PH) on Short Packet(Spa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

Packet Header (PH) DI **ECC** WC (LSB) WC (MSB) 29 hex 01 hex 00 hex 06 hex 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 1 0 0 0 1 1 0 0 B 0 BBBBB В В ВВ В ВВВ В ВВВ ВВВВ В В В ВВВ В В В В 1 2 3 4 5 7 0 1 2 3 4 6 7 0 1 2 3 4 7 0 1 2 3 4 S ss s s S s S вв ВВ ВВ В Time

Figure 54 Packet Header (PH) on Long Packet (LPa)

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Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated on a table below.

		Data Identification (DI)													
Virtual Ch	annel (VC)			Data Ty	pe (DT)										
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0								

Figure 55 Data Identification (DI) Structure

DI								WC (LSB)							WC (MSB)								ECC								
29 hex								01 hex							00 hex								06 hex								
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
E							M	F							М	Г							М	Ц							M
S	sl Is						S	s							s	s	lsl ls							s							S
L S B	в в							в в						в в								B									
													_	•	Tir	ne		_													_

Figure 56 Data Identification (DI) on the Packet Header(PH)



Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU.

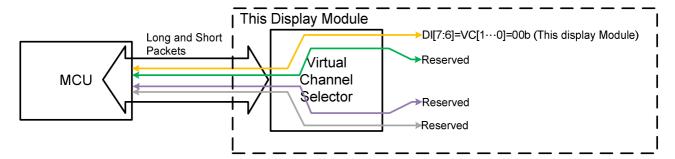
Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

	Packet Header (PH)															ac	de	r (Pŀ	ł)											
_																$\overline{}$															
	DI WC (LSB)									WC (MSB)											EC										
	29 hex									01 hex						00 hex								06 hex							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
T							M	ᆫ							М	L							М	L							М
S	sl IsIsI									S	S	s s s										s									
В	B B B E								В	B B B												В									
													_	•	Tir	ne)	_													→

Figure 57 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU This functionality is illustrated below.



Virtual Channel (VC) Configuration

Virtual Channel (VC) always 0 (D[7...6]=VC[1...0]00b) when the MCU is sending "End of Transmission Packet" to the display module. See section "End of Transmission Packet (EoTP)

This display module is not supporting the virtual channel selector for other device (1 to 3) when only possible virtual channel (VC[1...0]) is 00b for this display module.

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Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

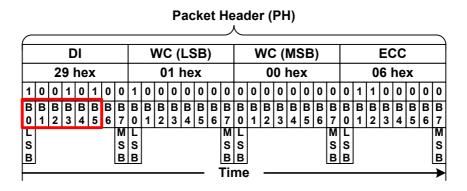


Figure 58 Data Type (DT) on the Packet Header (PH)



This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type	Data Type	5	Packet
Hex	Binary	Description	Size
01h	00 0001	Sync Event, V Sync Start.	Short
11h	01 0001	Sync Event, V Sync End.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
31h	11 0001	Sync Event, H Sync End.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
04h	00 0100	Generic READ, no parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB,5-6-5 Format.	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB,6-6-6 Format.	Long
2Eh	10 1110	Loosely Packed Pixel Stream,18-bit RGB,6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

Table 20 Data Type (DT) from MCU to the Display Module (or Other Devices)

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						Fro	m the Display Module (or Other Devices) to the MCU		
Llev	В	В	В	В	В	В	Description	Doolsot	Abbreviation
Hex	5	4	3	2	1	0	Description	Packet	Appreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
1Ch	0	1	1	1	0	0	DCS Read Long Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2_S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Short	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response,2 byte returned	Short	GENRR2-S

Table 21 Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or "Data Type (DT) from the Display Module (or Other Devices) to the MCU".



Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)

											Ρ	ac	:ke	et	He	a	de	r (Pŀ	ł)											
\bigcap			С)				Γ		С)a1	ta	0					С)at	a	1						ΕC	CC	;		$\overline{}$
		15 hex 35 hex 01 hex														1	Ε	he	X												
1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	0
В	- 1	В	В	I –	l _	ı	В		В	В		В	ı	В	В	В	Ι.	В	ı	В		В	В		В		В	В	I — I	В	В
P	1	2	3	4	5	6	7 M	0	1	2	3	4	5	6	7 M	0	1	2	3	4	5	6	7 М	0	1	2	3	4	5	6	7 M
S												S	S							S	S							S			
В		BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB																													
_													_		Tir	ne)	_						_					_		→

Figure 59 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)

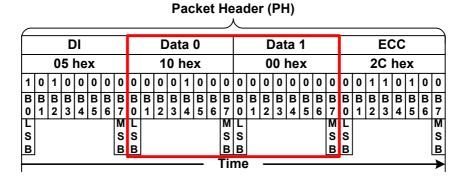


Figure 60 Packet Data(PD) fo Short Packet (Spa), 1 Bytes Information

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Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

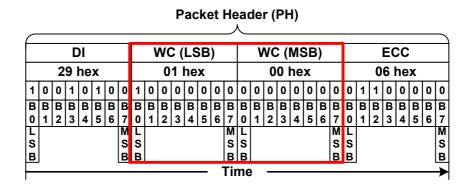
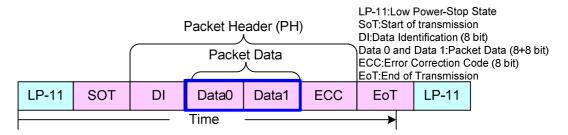
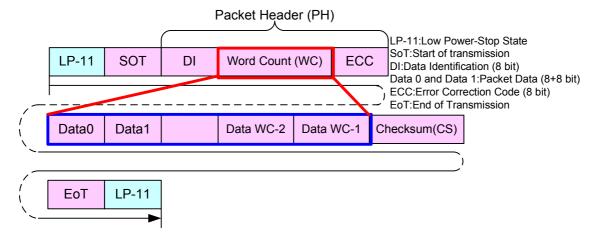


Figure 61 Word Count (WC) on the Long Packet (LPa)

Short Packet:



Long Packet:



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Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field"

- Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0...7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0...7]), Word Count (WC) bytes (16 bits: D[8...23]) and ECC (8 bits, P[0...7])

D[23...0] and P[7...0] are illustrated for reference purposes below.

_											Р	ac	:ke	et	He	eac	e	r (Pŀ	ł)											_
Ĺ			С)I						С	at	ta	0					С	at	a	1						ΕC	C			
		05 hex 10 hex 00 hex 2C hex																													
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	P	P	P 2	P	P	P	P	P
0 B	В	2 R	3 B	4 B	5 B	6 B	7 B	8 B	9 B	10 B		B		14 B		В	17 B		В	B	В			0 R	1 B	_	3 B	4 B	5 B	6 B	В
0	1	2	3	4	ΙΞ.	6	7	0	1	2	3	4	_	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Ľ							M	L							M	ŗ							M	L							M
S B							S B	S B							S B	S B							S B	S B							S B
F													_	•	Tir	ne)	_													→

D[23..0] and P[7...0] on the Short Packet (SPa)

Packet Header (PH) DI WC (LSB) WC (MSB) **ECC** 01 hex 29 hex 00 hex 06 hex 0 0 0 0 0 0 0 0 0 0 0 0 D 4 D 6 D D D D 10 11 12 13 D 14 D D D 15 16 17 D D D D 18 19 20 21 D D 22 23 D 8 P 0 B 0 L S B ВВВВ В 0 6 0 1 2 0 1 2 s S s SS S S В В В

D[23···0] and P[7···0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

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Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63...0]), but this implementation is based on 24 bit value (D[23...0]). Therefore, there is only needed 6 bits (P[5...0]) for Error Correction Code (ECC).

Packet Header (PH) ECC DI Data 0 Data 1 05 hex 10 hex 2C hex 00 hex 00000000 1000 0 0 0 0 1 0 0 0 1 1 0 1 0 B B B 0 1 2 B B B 4 5 6 S B S S B B S S B B S S B B S B

XOR Functionality on the Short Packet (SPa)

											Р	ac	kε	et	Hε	a	ək	r (Pŀ	ł)											
\subseteq		2	9 I	_					\	NC		LS he)			٧) (0			3)					E(
1	О	_	1	0	<u>^</u>	О	О	1	О	6	0	1	Ô	0	О	0	О	6	6	0	<u>ہ</u>	О	0	0	1	1	0	0	ि	О	Г
D 0	D 1	D 2		D 4	D 5		D 7			D 10	D 11		D 13			D 16				D 20	D 21	D 22	D 23	P ₀							П
D 0	D 1		D 3	D 4		D 6		D 8		D 10		D 12		D 14			D 17			D 20	D 21	D 22	D 23		P 1						
D 0		D 2	D 3		D 5	D 6			D 9		D 11	D 12			D 15			D 18		D 20	D 21	D 22				P 2					
	D 1	D 2	Dз				D 7	D 8	D 9				D 13	D 14	D 15				D 19	D 20	D 21		D 23				P 3				
				D 4	D 5	D 6	D 7	D 8	D 9							D 16	D 17	D 18	D 19	D 20		D 22	D 23					P 4			
										D 10	D 11	D 12	D 13	D 14	D 15	D 16	D 17	D 18	D 19		D 21	D 22	D 23						P 5		
В 0	В 1	В 2	В 3	B 4	B 5	В 6	B 7	Во	В 1	В 2	В 3	В 4	B 5	B 6	В 7	В 0	В 1		В 3	В 4	В 5	В 6	В 7	Во	В 1	B 2	В 3	B 4	В 5	В 6	В 7
L S B				-			M S B	S							M S B	L S B							M S B	L S B		<u> </u>					M S B
-													_		111	ne	•	_												_	➛

XOR Functionality on the Long Packet (LPa)

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The transmitter (The MCU or the Display Module) is sending data bits D[23...0] and Error Correction Code (ECC) P[7...0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7...0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

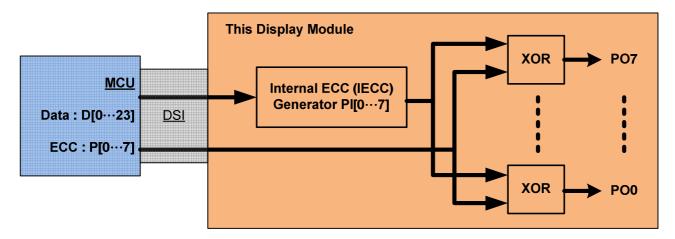


Figure 62 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23...0]) and ECC (P[7...0]) are received correctly, if a value of the PO[7...0]) is 00h. The sent data bits (D[23...0]) and ECC (P[7...0]) are not received correctly, if a value of the PO[7...0]) is not 00h.

ECC P[70]	1	1	0	0	0	0	0	0	03h
IECC PI[70]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC)	0	0	0	0	0	0	0	0	=00h=>No Error
=>PO[70]									
	L							М	
	S							S	
	В							В	

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[70]	1	1	0	0	0	0	0	0	03h
IECC PI[70]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC)	0	0	1	1	0	0	0	0	=0Ch=> Error
=>PO[70]									
	L							М	
	S							S	
	В							В	

Internal XOR Calculation between ECC and IECC Values- Error

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The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23...0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7...0] is compared to values on the following table.

Data Bit	P07	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7...0] is on: One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO[7...0] = 0Eh
- The bit of the data (D[23...0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7...0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7...0] = 0Ch.

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8.8.2.3.1.4 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter "Word Count (WC) on the Long Packet (LPa)".

8.8.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial

X16+X12+X5+X0 as it is illustrated below.

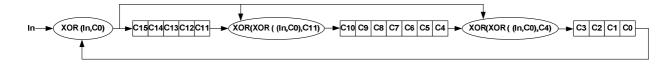


Figure 63 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



		V07//- 00)	045		040	040	044	VOD/VOD/(= 00) 044/0== 4))	040			07	-00	0.5	-	VOD/VOD/I 00) 04/0/ 4))			04		
Stop	ln	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	х	х	1	1	1	1	1	x	1	1	1	1	1	1	1	x	1	1	1	1	х
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 Byte	CRC Resoult	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
		•	LSB					-								•				LSB	

Figure 64 CRC Calculation – Packet Data (PD) is 01h

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A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

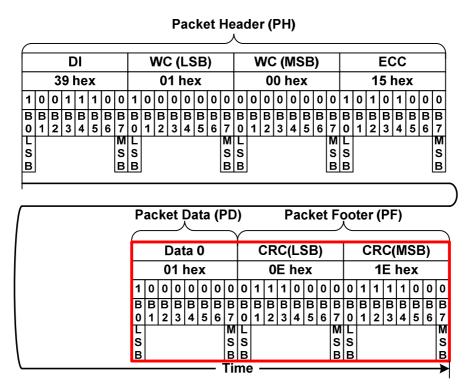


Figure 65 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

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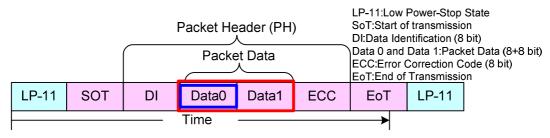
8.8.2.3.2 Packet Transmissions

8.8.2.3.2.1 Packet from the MCU to the Display Module

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter "9 Instruction Description", is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

Short Packet



Long Packet:

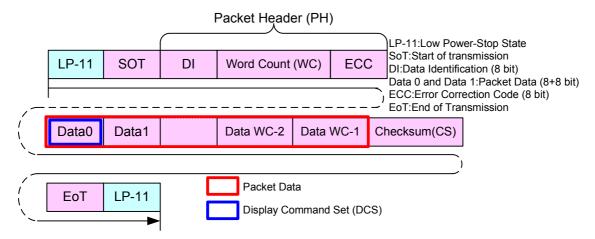


Figure 66 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

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Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

"Generic Write, 1 Parameter" (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and 00h.

These commands are defined on a table (See chapter "9 Instruction Description") below

Command
NOP (00h)
SWRESET (01h)
SLPIN (10H)
SLPOUT (11h)
PTLON (12h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
IDMOFF (38h)
IDMON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0011b
- Packet Data (PD)
 - Data 0: "Sleep In (10h)", Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

_															ر																_
													P	ac	ke	t [Эa	ta)
\vdash			Е	<u>, , , , , , , , , , , , , , , , , , , </u>					٠,	NIC	<u> </u>	LS	<u>. D</u>	<u>, </u>			v	VC	` /	М	20	<u> </u>					<u>=</u>	CC			
				<u>''</u>					•	-	<u>ر</u>	L	0	<u>, </u>			V	V C	<u>' (</u>	WI.	םכ	<u>'' </u>						<u>, </u>			
		1	3	he	X					1	0 I	he	X					0	0 I	he	X					3	9	he	X		
1	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
T		•					М	L							М	L							М	L							М
s							s	s							s	S							S	S							s
В							В	В							В	В							В	В							В
\vdash													_	•	Tir	ne)	_													→

Figure 67 Generic Write,1 Parameter (GENW1-S)-Example

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Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

"Generic Write, 2 Parameter" (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and "parameter". These commands are defined on a table (See chapter "6 Instruction Description") below.

Command	
GAMSET (26h)	
COLMOD (3Ah)	
WRDISBV (51h)	
WRCTRLD (53h)	
WRCABC (55h)	
WRCABCMB (5Eh)	

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0011b
- Packet Data (PD)
 - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

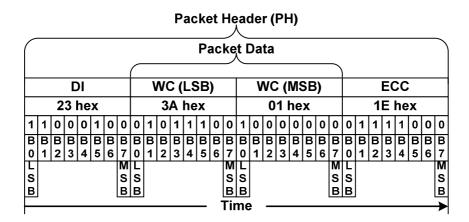


Figure 68 Generic Write, 2 Parameter (GENW2-S) – Example

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Generic Write Long (GENW-L), Data Type = 10 1001 (29h)

"Generic Write Long" (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below.

	Command	
NOP (00h), Note1	INVON (21h), Note1	IDMOFF (38h), Note1
SWRESET (01h) , Note1	ALLPOFF (22h)	IDMON (39h), Note1
SLPIN (10H), Note1	ALLPON (23h)	COLMOD (3Ah) , Note2
SLPOUT (11h), Note1	GAMSET (26h), , Note2	WRDISBV (51h), Note2
PTLON (12h), Note1	DISPOFF (28h), Note1	WRCTRLD (53h), Note2
NORON (13h), Note1	DISPON (29h), Note1	WRCABC (55h), Note2
INVOFF (20h), Note1	PARLINES (C5h)	WRCABCMB (5E) , Note2

Notes: 1. Also Short Packet (SPa) can be used; See Generic Write, 1 Parameter.

2. Also Short Packet (SPa) can be used; See Generic Write, 2 Parameter.c

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
 - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

Packet Header (PH)

\vdash			_						_	81/	_		_								_							_			\rightarrow
			L	<u> </u>						N) ز	L	98	<u>) </u>			V	VC	ا) د	IVI	SB	<u>) </u>					E	C			
		2	9	he	X					0	1	he	X					0	0	he	X					0	6	he	X		
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5		7
ļ٢							M								М	ᆫ							M	L							M
S							S	_							S	s							S	s							S
В	J						В	В							В	В							В	В							В

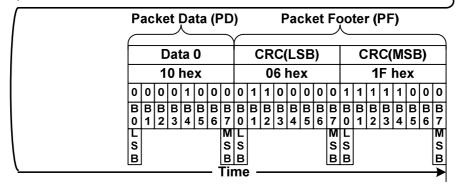


Figure 69 Generic Long Write(GENW-L) with DCS Only – Example

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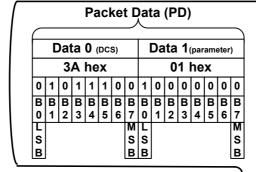
Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Gamma Set (3Ah)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

Packet Header (PH)

F			_)I				Γ	_	N	2 (LS	SB	<u> </u>		Γ	V	VC	: (MS	SB						ΕC	CC	<u> </u>		\rightarrow
		2		he	X			┢			_	_` he		<u>, </u>			_		0			,						he			
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B 0	B 1	B 2	В 3	B 4	B 5	B 6	B 7	B 0	B 1	B 2	B 3	B 4	В 5	B 6	B 7	B 0	В 1	B 2	ı —	B 4	B 5	B 6	B 7	В 0	В 1	B 2	B 3	B 4	B 5	B 6	B 7
L S B					•	•	M S B	L S B		•		•	•	•	M S B	L S B				•			M S B	L S B			•	•			M S B



Packet Footer (PF) CRC(LSB) CRC(MSB) E3 hex AA hex 0 0 0 1 1 0 1 0 1 0 1 1 0 М s S S S В В

Figure 70 Generic Long Write (GENW-L) with DCS and 1 Parameter-Example

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В



Long Packet (Lpa), when a Write (4 parameters) was sent, is defined e.g.

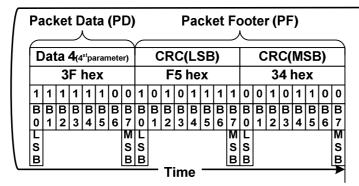
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "PARLINES (30h)", Display Command Set (DCS)
 - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15...8]
 - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7...0]
 - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15...8]
 - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7...0]
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.

Packet Header (PH)

\subseteq																_															\rightarrow
)					١	N	C (LS	B	(V	VC	; (MS	SB	3)					EC	C	;		
		2	9 I	ne	X					0	5	he	X					0	0	he	X					2	5	he	X		
1	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F							М	L							М	L							М	Ц							М
S							S	S							S	S							S	S							S
В							В	В							В	В							В	В							В

Packet Data (PD) Data 0 (DCS) Data 1(1stparameter) Data 2(2stparameter) Data 3(3stparameter) 00 hex 30 hex 00 hex 01 hex 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 7 S B ΜL L S S B B S S B B s s s



вв

Generic Write Long (GENW-L) with DCS and 4 Parameters-Example

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Generic Read, 1 Parameter (GENR1-S), Data Type = 01 0100 (14h)

"Generic Read, 1 Parameter (GENR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT,01 0100b), from the MCU to the display module. This command is defined on a table (See chapter "9 Instruction Description") below.

Com	mand
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - Data 0: 01hex
 - Data 1: 00hex
- Error Correction Code (ECC)

Packet Header (PH)

							M	ax	im	ıuı	m	Re	etu	ırr	۱ F	ac	ck	et	Si	ze	(1	MF	RP.	S)							
			С)I					M	RI	PS	(L	SI	3)			M	RF	PS	(N	IS	B)					EC	C			
		3	7	he	X					0	1	he	X					0	0 I	he	X					1	D	he	X		
1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
T							М	L							М	L							М	L							M
S							s	S							S	S							S	s							S
В							В	В							В	В							В	В							В
														_	Τi	m	e ·														→

Figure 72 Set Maximum Return Packet Size (SMRPS-S)- Example

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Step 2:

- The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Generic Read, 1 Parameter" to the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0100b
- Packet Data (PD)
 - Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

Packet Header (PH) **Maximum Return Packet Size (MRPS)** DI MRPS(LSB) MRPS(MSB) **ECC** 14 hex DA hex 00 hex 07 hex B</t 0 L S B S S B B S S B B S S B B S B Time

Figure 73 Generic Read, 1 Parameter (GENR1-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

- 1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section "Acknowledge with Error Report (AwER)".
- 2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

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Display Command Set (DCS) Write, No Parameter (DCSWN-S), Data Type = 00 0101 (05h)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Com	mand
NOP (00h)	INVON (21h)
SWRESET (01h)	ALLPOFF (22h)
SLPIN (10h)	ALLPON (23h)
SLPOUT (11h)	DISPOFF (28h)
PTLON (12h)	DISPON (29h)
NORON (13h)	IDMOFF (38h)
INVOFF (20h)	IDMON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0101b
- Packet Data (PD)
 - Data 0: "Sleep In (10h)", Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

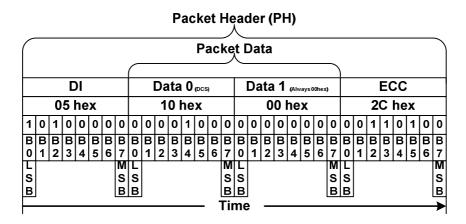


Figure 74 Display Command Set (DCS) Write, No Parameter (DCSWN-S)-Example

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Display Command Set (DCS) Write, 1 Parameter (DCSW1-S), Data Type = 01 0101 (15h)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command
GAMSET (26h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0101b
- Packet Data (PD)
 - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

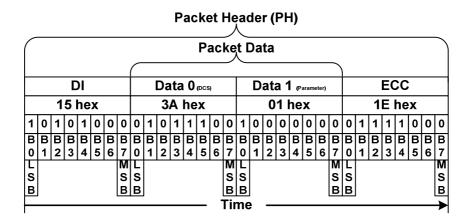


Figure 75 Display Command Set (DCS) Write,1 Parameter (DCSW1-S)-Example

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Display Command Set (DCS) Write Long (DCSW-L), Data Type = 11 1001 (39h)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "9 Instruction Description") below

	Command	
NOP (00h), Note1	INVON (21h), Note1	COLMOD (3Ah) , Note2
SWRESET (01h), Note1	GAMSET (26h), Note2	WRDISBV (51h), Note2
SLPIN (10h), Note1	DISPOFF (28h), Note1	WRCTRLD (53h)
SLPOUT (11h), Note1	DISPON (29h), Note1	WRCABC (55h), Note2
PTLON (12h), Note1	PARLINES (30h)	WRCABCMB (5Eh)
NORON (13h), Note1	IDMOFF (38h), Note1	
INVOFF (20h), Note1	IDMON (39h), Note1	

Notes: 1. Also Short Packet (SPa) can be used; See_Display Command Set (DCS) Write, No Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

Packet Header (PH)

																														\rightarrow
		С)					١	N	ે (LS	B)			۷	VC	; (I	MS	SB)					E	C	,		
	3	9 I	he	X					0	1	he	X					0	0	he	X					1	5	he	X		
0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
						M	L							M	L							М	L							М
						S	S							S	S							S	S							S
						<u>B</u>	В							B	В							В	В							В
	0 B 1	0 0 B B 1 2	39 I 0 0 1 B B B 1 2 3	0 0 1 1 B B B B 1 2 3 4	39 hex 0 0 1 1 1 B B B B B B B 1 2 3 4 5	39 hex 0 0 1 1 1 1 0 B B B B B B 1 2 3 4 5 6	39 hex 0 0 1 1 1 1 0 0 B B B B B B B B B B 1 2 3 4 5 6 7 M S	39 hex 0 0 1 1 1 1 0 0 1 B B B B B B B B B B B B B 1 2 3 4 5 6 7 0 M L S S	39 hex	39 hex 0 0 0 1 1 1 0 0 1 0 0 B B B B B B B B B B B B B B B B B B	39 hex 01 0 0 0 0 0 0 0 0 0	39 hex 01 he 0 0 1 1 1 0 0 1 0 0 0 0 B B B B B B B B B B B B B B B B	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex	39 hex					

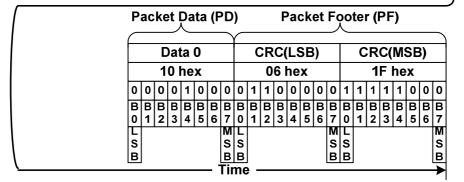


Figure 76 Display Command Set (DCS) Write Long (DCSW-L) with DCS Only-Example

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^{2.} Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.



Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Gamma Set (26h)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows

Packet Header (PH)

\vdash)					١	N) (LS	ЗB)			٧	۷C	; (MS	SB	5)					ΕC	CC	;		\neg
		3	9	he	X					0	2	he	X					0	0	he	X					1	3	he	X		
1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
L							М	L							M	L							M	L							М
S							S	s							S	S							S	S							S
В							В	В							В	В							В	В							В

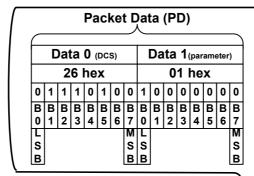


Figure 77 Display Command Set (DCS) Write Long with DCS and 1 Parameter-Example

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Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "PARLINES (30h)", Display Command Set (DCS)
 - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15...8]
 - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7...0]
 - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15...8]
 - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7...0]
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

Packet Header (PH)

ECC
36 hex
0 0 1 1 0 1 1 0 0
BBBBBBBB
7 0 1 2 3 4 5 6 7
M L M
s s s
ВВ В

Packet Data (PD)

\subseteq																																\supset
		D	at	a	0 (DC	S)		C)at	ta	1 (1	st pa	ırar	nete	er))at	a	2 (2	2 st pa	ıran	nete	er)	C	at	ta	3 (3	s ^t pa	aran	nete	∍r)
Г	30 hex 00 hex														0	0	he	X					0	1	he	X						
0	C	7	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
В	BE	3	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Γ	·T							M	┖							M	L							M	Ц							М
S	: -							S	S							S	S							S	S							S
LB	3	ВВ										В	В							В	В							В				

Packet Data (PD) Packet Footer (PF)

				_				$\overline{}$	_							_	_							
)ai	ta	4(4	l st pa	ıran	nete	er)		C	R	C(LS	SB	3)			C	R	C(M:	SE	3)	
			3	F	he	X					F	5	he	X					3	4 I	he	X		
	1																0							
	15															В	В	В						
	0	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6															7							
	T							M	L							М	L							М
	S							S	S							S	S							s
	В							В	В							В	В							В
`										_	Т	im	е	_								_	_	~

Figure 78 Display Command Set (DCS) Write Long with DCS and 4 Parameters-Example

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Display Command Set (DCS) Read, No Parameter (DCSRN-S), Data Type = 00 0110 (06h)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Com	mand
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - Data 0: 01hex
 - Data 1: 00hex
- Error Correction Code (ECC)

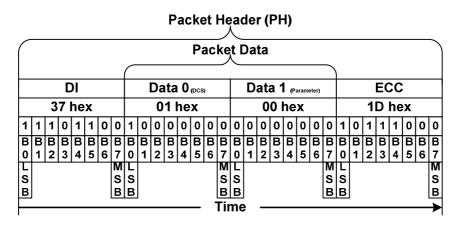


Figure 79 Set Maximum Return Packet Size (SMRPS-S) - Example

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Step 2:

- The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0110b
- Packet Data (PD)
 - Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

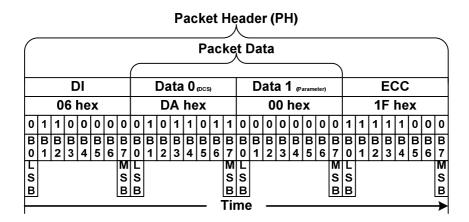


Figure 80 Display Command Set (DCS) Read, No Parameter (DCSRN-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

- 1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section "Acknowledge with Error Report (AwER)".
- 2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

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Null Packet, No Data (NP-L), Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending. Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h (Random data)
 - Data 1: 23h (Random data)
 - Data 2: 12h (Random data)
 - Data 3: A2h (Random data)
 - Data 4: E2h (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

Packet Header (PH)

\subseteq															_	_															\supseteq
			D) I					١	N	C (LS	8B)			٧	VC	; (MS	SB)					E	CC	;		
	09 hex 05 hex											0	0	he	X					3	0	he	×								
0	1	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
ᆫ	Г.						М	L			•			•	М	L							М	Г	Г	•	_		_	_	М
S							s	s							s								s	s							S
В							В	В							В	В							В	В							В

$\int_{-\infty}^{\infty}$													Pa	ıcl	кe	t C	at	a	(P	D)	1											$\overline{}$
r	Data 0 (DCS) Data 1(1st parameter) Data 2(2st parameter) Data 3(3st parameter)																															
	89 hex 23 hex 12 hex A2 hex																															
1	1001000111000100010001000100001000100														1																	
E	3 E	- 1	_ I	_			ı	В	В						ı	В	В				В		В	В	В	В	ı	В	В	_	_	В
ļ) 1	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	_	7
ال	:							IM	느							M	片							M	片							M
								S	S							S	S							s	S	l						S
\ L	3							В	В]						В	В							В	В	J						В

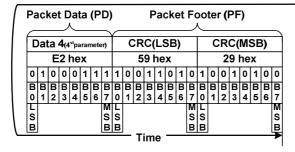


Figure 81 Null Packet, No Data (NP-L)-Example

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End of Transmission Packet (EoTP), Data Type = 00 1000 (08h)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it want to use the "End of Transmission Packet" (EoTP) or not. The ST7701 has the capability to support both: i.e. If MCU applies the EoTP, it shall report the "DSI Protocol Violation" error when the EoTP is not detected in the high speed (HS). This error reporting can be enable/disable by bit DIS_EoTP_HS of command B100h (page 0).

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Marked-1" (=leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to MCU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Direction	Display Module (DM) in	Display Module (DM) in
Direction	High Speed Data Transmission (HPDT)	Low Power Data Transmission (LPDT)
MCU=>Display Driver	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Driver=>MCU	HS Mode is not available	EoTP can not be sent by the Display
	(EoTP is not available)	Driver

Table 22 Receiving and Transmitting EoTP during LPDT



Short Packet (SPa) is using a fixed format as follow

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1000b
- Packet Data (PD):
 - Data 0: 0Fh
 - Data 1: 0Fh
- Error Correction Code (ECC)
- ECC: 01h

											Ρ	ac	ke	et	He	ac	de	r (Pŀ	ł)											
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	DI Data 0 Data 1 ECC																														
	08 hex 0F hex 0F hex 01 hex																														
0																															
В	В	В				ı	В		В	В			В				В			В	В		В	В	В		В	۱.	В	_	В
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В							В	B]						B Tir	ne							В	В							В
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Figure 82 End of Transmission Packet (EoTP)

Some use case of the "End of Transmission Packet" (EoTP) are illustrated only for reference purpose below.

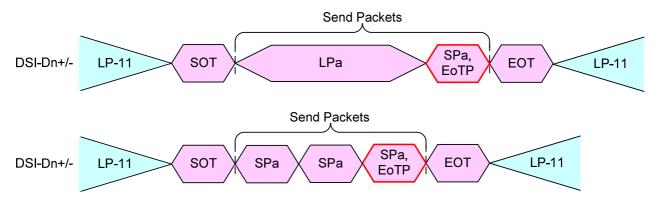


Figure 83 End of Transmission Packet (EoTP)-Example

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Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As "start" and "end" are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA..

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

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Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)

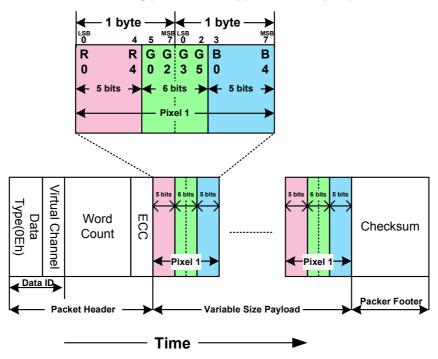


Figure 84 16-bit per Pixel-RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the "Green" component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)

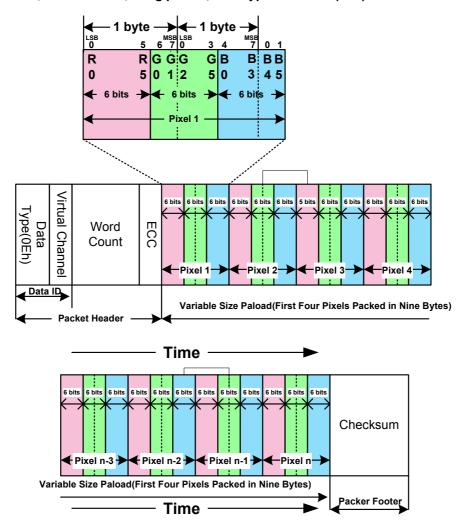


Figure 85 18-bit per Pixel-RGB Color Format, Long pack

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device.

For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)

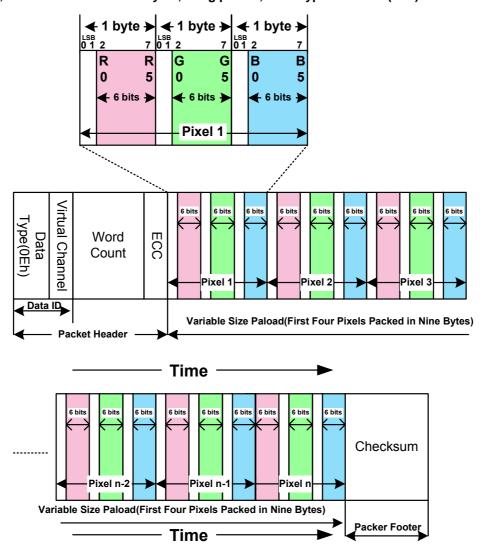


Figure 86 18-bit per Pixel (Loosely Packed)-RGB Color Format, Long pack

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the "packed" format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.



Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

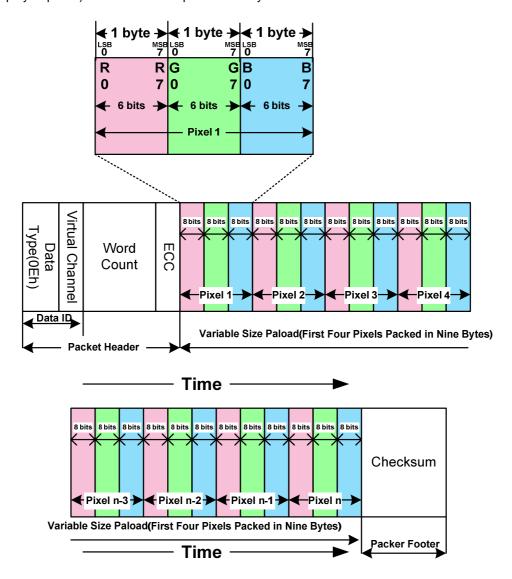


Figure 87 24-bit per Pixel -RGB Color Format, Long packet

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8.8.2.3.2.2

PACKET FROM THE DISPLAY MODULE TO THE MCU

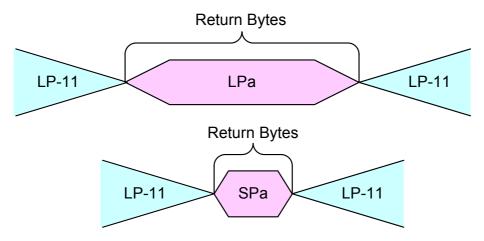
Used Packet Types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) Read, No Parameter",(DCSRN-S)) or an Acknowledge with Error Report .The used packet type is defined on Data Type (DT)..

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.



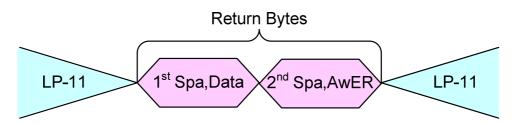
Return Bytes on Signal Packet



Data Type Hex	Data Type Binary	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	SCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	01 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Long Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Long Read Response, 2 Byte returned	Short

Table 23 Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" where has been detected and corrected a single bit error by the EEC (See bit 8 on Table" Acknowledge with Error Report (AwER) for Short Packet (SPa) Response"). This return packets are illustrated for reference purpose below.



Exception When Return Bytes on Several Packet

AwER=Acknowledge with Error Report



Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 24 Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to "0" internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 25 Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

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These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0010b
- Packet Data (PD):
 - Bit 8: ECC Error, single-bit (detected and corrected)
 - AwER: 0100h
- Error Correction Code (ECC)

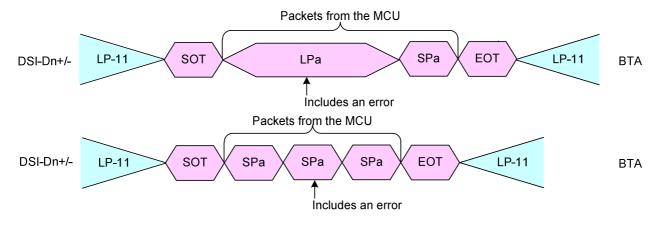
This is defined on the Short Packet (SPa) as follows.

	ader (Ph)
Packet D	Data(PD)
DI AWER(LSB)	AWER(MSB) ECC
02 hex 00 hex	01 hex 3A hex
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 1 0 1 1 1 0 0
	88888888888888
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
L M L M I	
S S S S S	
B BB BI	B BB B
Tir	me —

Dacket Header (DH)

Acknowledge with Error Report (AwER)-Example

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA). Some examples are illustrated below for reference purpose.



Error Packet

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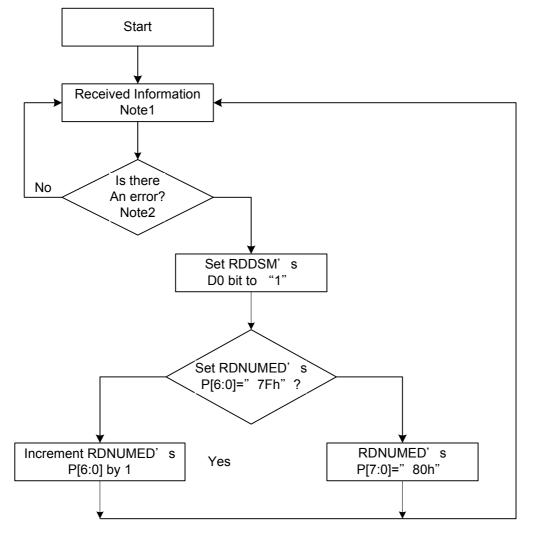


Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands.

The bit D0 of the "Read Display Signal Mode (0Eh)" command has been set to '1' if a received packet includes an error.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the "Read Display Signal Mode (0Eh)" command to '0' after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:

- 1. This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.
- 2. CRC or ECC error.

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DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT,01 1100b), from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

"DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1100b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h
 - Data 1: 23h
 - Data 2: 12h
 - Data 3: A2h
 - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



Packet Header (PH)

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			Е)I					١	NC) (LS	B)			٧	۷C	; (MS	SB	(E	C	:		
		1	С	he	×					0	5	he	X					0	0	he	X					2	9	he	X		
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E	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
C	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
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Ρ	ac	ket	Data	(PD)

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Ī	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
-	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
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Ш	s							S	s							s	s							s	s	l						S
l	В							В	В							В	В							В	В							В

Packet Data (PD) Packet Footer (PF)

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			Е	2	he	X					5	9	he	X					2	9	he	X		
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DCS Read Long Response(DCSRR-L)-Example



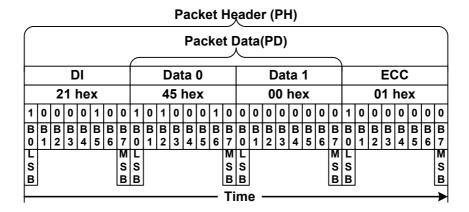
DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0001b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



DCS Read Short Response,1 Byte Returned(DCSRR1-S)-Example

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DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0010b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

Packet Header (PH) Packet Data(PD) DI Data 0 **ECC** Data 1 22 hex 45 hex 32 hex 0F hex 0 1 0 0 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 0 0 0 1 0 0 1 0 0 1 1 1 0 0 0 1 1 1 1 0 0 0 0
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DCS Read Short Response,2 Bytes Returned (DCSRR2-S) -Example

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Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

"Generic Read Long Response" (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. "Generic Read Long Response" (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1010b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h
 - Data 1: 23h
 - Data 2: 12h
 - Data 3: A2h
 - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.

Packet Header (PH)

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l			С)					١	NC	C (LS	βB)			۷	VC	; (MS	3B)					E	C	;		
		1,	Α	he	X					0	5	he	X					0	0	he	X					2	F	he	X		
0	1	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
匸							М	┖							М	┖							М	L							M
S							S	S							S	s							S	S							S
В]						В	В							В	В							В	В							В

												Pa	ıcl	кe	t C	a	ta	(P	D))											$\overline{}$
	I	Data 0 (DCS) Data 1(1stparame										nete	er)	Е	a	ta	2 (2	st _{pa}	aran	nete	er)	Е	a	ta	3(3	s ^t pa	aran	nete	er)		
		8	9	he	X					2	3	he	X					1	2	he	X					Α	2	he	X		
0	0	0	1	1	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1
В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В		ı		В		В	В	В	_	ı	_	В	В	В
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
L							M	ᄔ							М	ᄔ							М	ᄔ							M
S	1						s	S							s	S							ı –	S							S
\ <u>B</u>							В	В							В	В							В	В							В

	Pa	ıcl	(e	t [Dat	ta	(P	D)	1			F	a	ck	et	Fo	00	te	r (I	PF)			_
		at	a	4(4	st pa	ıran	nete	r)		C	R	C(LS	SB)			С	R	C(M	SE	3)	`
			Е	2	he	X					5	9	he	X					2	9 I	he	X		
	0	1	1	1	0	1	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
	В	В	В		В		В	В	1 =	В	В	В	В	I – I		В		В	В	В	В	В	В	В
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	╙							М	┖							М	Г							M
	S							s	s							s	S							S
\	В							В	В		_	_				В	В							В
_											T	im	е											~



Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

"Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. "Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0001b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

Packet Header (PH) Packet Data(PD) DI Data 0 Data 1 **ECC** 22 hex 45 hex 32 hex 0F hex |1|0|0|0|1|0|0|1|0|1|0|0|0|1|0|0|1|0|0|1|1|0|0|1 |1|1|1|0|0|0|0 |7|0|1|2|3|4|5|6|7|0|1|2|3|4 5 6 7 0 1 2 3 4 5 6 1 2 3 4 7 M L S S B B LSB МL МL M S S B B S S B B S **Time**

Generic Read Short Response, 1 Byte Returned (GENRR1-S)-Example



Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

"Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. "Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0010b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

Packet Header (PH) Packet Data(PD) DI Data 0 Data 1 **ECC** 12 hex 45 hex 32 hex 09 hex |0|0|1|0|0|0|0 88888888888888888888888888888 5 6 7 0 1 2 5 6 7 0 3 4 5 6 |7|0|1|2|3|4 3 4 1 2 3 4 6 7 M L S S B B Ľ S ML МL М S S B B S S B B S В В **Time**

Generic Read Short Response, 2 Bytes Returned (GENRR2-S)-Example



8.8.2.3.3 COMMUNICATION SEQUENCES

8.8.2.3.3.1 GENERAL

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters "Interface Level Communication" and "Packet Level Communication".

This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Mode	Abbreviation	Interface Action Description
	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
Low Power	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Table 26 Interface Level Communication

Functions of the packet level communication are described on the following table.

Packet Sender	Abbreviation	Packet Size	Packet Description
	DCSW1-S	SPa	DCS Write,1 Parameter
	DCSWN-S	SPa	DCS Write, No parameter
MCU	DCSW-L	LPa	DCS Write,Long
WICO	DCSRN-S	SPa	DCS Read,No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
	AwER	SPa	Acknowledge with error report
Diaplay Madula	DCSRR-L	LPa	DCS Read, Long Response
Display Module	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

Table 27 Packet Level Communication

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8.8.2.3.3.2 **SEQUENCES**

DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined on chapter "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write,1 Parameter Sequence - Example 1

	MCL	J		Display M	/lodule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write,1 Parmeter Sequence – Example2

_	MCL	J		Display M	/lodule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	•	-	
3	EoTP	HSDT	=>	•	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

	MCU			Display M	1odule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	ı	-	
3	EoTP	HSDT	=>	1	-	End of Transmission Packet
4	-	LP-11	=>	ı	-	
5	-	ВТА	<=>	ВТА	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	ı	<=	ACK	-	No error
9	-	1	<=	LP-11	-	
10	-	ВТА	<=>	ВТА	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

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DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence-Example 1

	MCL	J		Display N	/lodule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parmeter Sequence – Example2

	MCL	l		Display M	/lodule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	•	-	
3	EoTP	HSDT	=>	•	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

	MCU			Display M	lodule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	•	
3	EoTP	HSDT	=>	-	ı	End of Transmission Packet
4	-	LP-11	=>	-	•	
5	-	ВТА	<=>	ВТА	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	ı	<=	ACK	ı	No error
9	-	1	<=	LP-11	•	
10	-	ВТА	<=>	ВТА	1	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	•	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End



DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined on chapter "Display Command Set (DCS) Write Long (DCSW-L)" and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence-Example 1

	MCL	J		Display M	1odule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence – Example2

	MCL	l		Display M	/lodule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	•	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

	MCU			Display M	/lodule	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	1	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	ı	-	
5	-	ВТА	<=>	ВТА	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	ı	<=	ACK	-	No error
9	-	1	<=	LP-11	-	
10	-	ВТА	<=>	ВТА	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	ı	-	End
12						
13	-	1	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

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DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence - Example 1

Line Packet Interface Information Interface Packet Co	
Sender Mode Direction Mode Sender Control	omment
1 - LP-11 => -	Start
2 SMRPS-S HSD => -	many data byte is to read: 1 byte
	a response ID1 (DAh)
4 EoTP HSDT => - End of Tran	nsmission Packet
5 - LP-11 => -	
	rol change from the e display module
7 - <= LP-11 - If error=	or=>goto line 9 > goto line 14 orrected by ECC o to line 19
8	
9 - <= LPDT DCSRR1-S Response	ed 1 byte return
10 - <= LP-11 -	
11	rol change from the odule to the MCU
12 - LP-11 =>	End
13	
14 - <= LPDT AWER Err	or report
15 - <= LP-11 -	
16 - BIA <=> BIA -	trol change from the odule to the MCU
17 - LP-11 =>	End
18	
19 - <= LPDT DCSRR1-S Response	ed 1 byte return
20 - - /- DIN AWER	or Report orrected by ECC)
21 - <= LP-11 -	
22 - BIA <-> BIA -	rol change from the dule to the MCU
23 - LP-11 =>	End



Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined on chapter "Null Packet, No Data (NP-L)" and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

	MCU	J		Display I	Module	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

End of Transmission Packet

A Short Packet (SPa) of "End of Transmission (EoT)" is defined on chapter "End of Transmission Packet (EoT)" and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet - Example

	MCL	l		Display	Module	
Line	Packet Sender	Interface Mode Control	Information Direction	Interface Mode Control	Packet Sender	Comment
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

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8.8.2.4 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

8.8.2.4.1 TRANSMISSION PACKET SEQUENCES

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

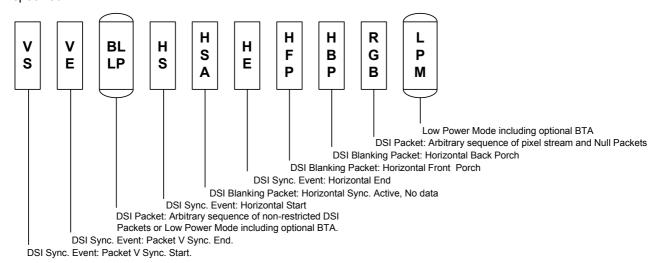
The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

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Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted. There are two limitation for MIPI Video mode 2 Lane:

- (1) The packet number for H-porch or 1-line data should be even.
- (2) Packet Pixel Stream should be start at Lane0.



8.8.2.4.2 NON-BURST MODE WITH SYNC PULSES

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

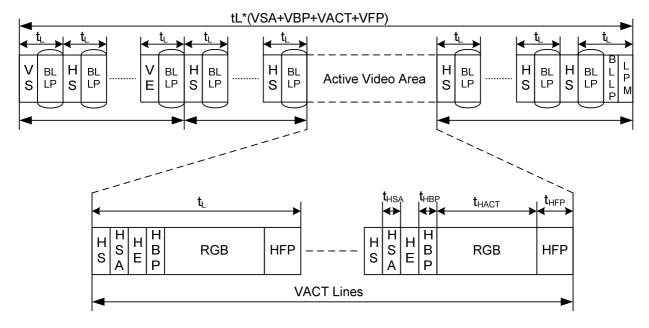


Figure 88 DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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8.8.2.4.3 NON-BURST MODE

This mode is a simplification of the format described in section 5.3.2.4.2 "Non-Burst Mode with Sync Pulse" .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

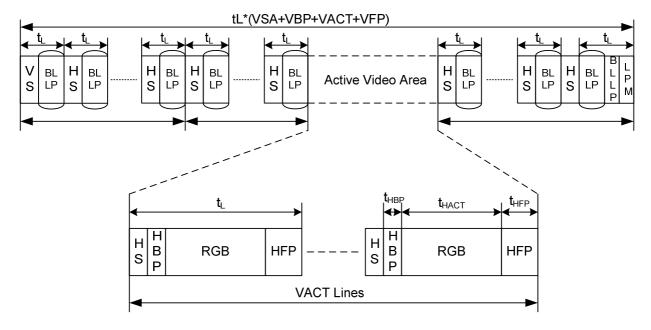


Figure 89 DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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8.8.2.4.4 BURST MODE

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.

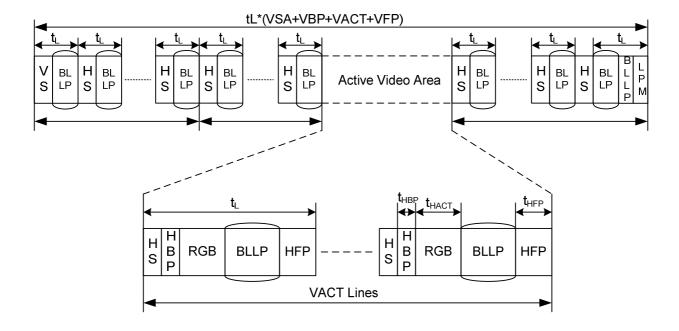


Figure 90 DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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9 POWER ON/OFF SEQUENCE

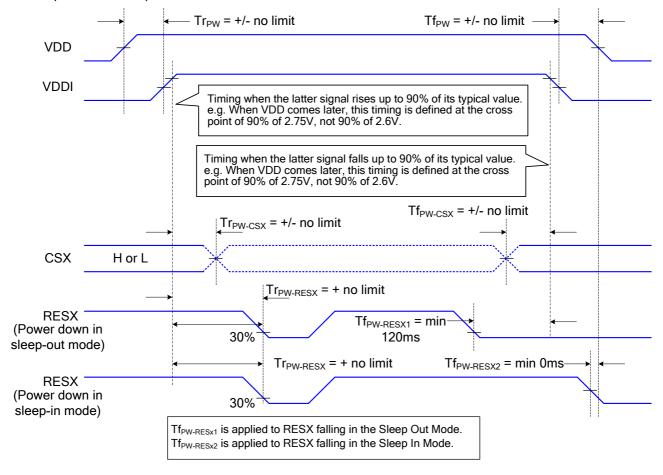
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

- 1. There will be no damage to the ST7701 if the power sequences are not met.
- 2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
- 3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
- 4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



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9.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

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10 POWER LEVEL DEFINITION

10.1 Power Level

7 level modes are defined they are in order of maximum power consumption to minimum power consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply.

6. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working.

7. Power Off Mode

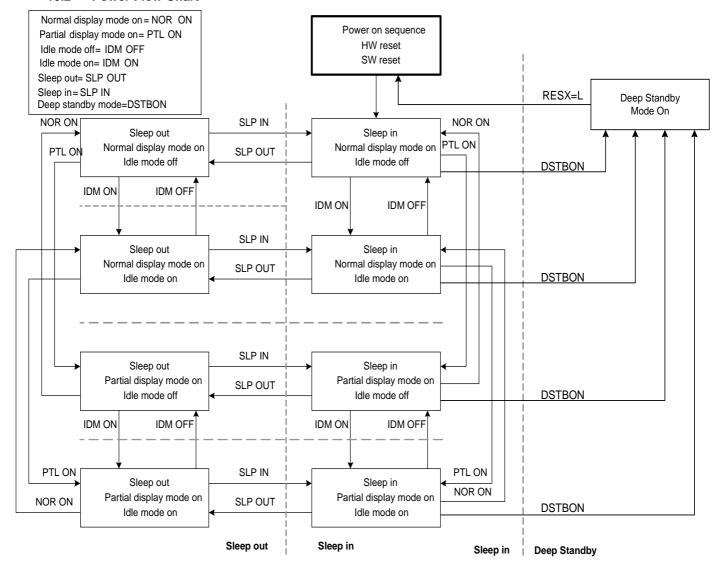
In this mode, VDDI and VDDA/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with

both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.



10.2 Power Flow Chart



NOTES:

- 1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.
- 2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode



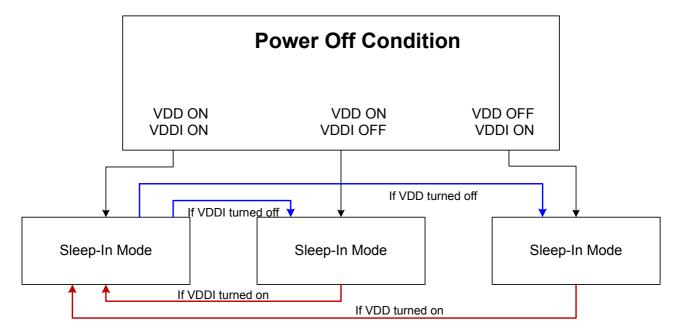
The following table represents the Registers its mode state.

Mode	Register	Control		
		Enter	Exit	
Sleep in mode	Keep	Command		
Deep-standby mode	Loss	Command Rese		
Reset=L	Keep(Default Value)	Reset (H/W)		

The condition for irregular power off mode is shown below.

Power Off Mode	VDD	VDDI	RESX	I/O
Mode 1	ON	OFF	High to Low	Low
Mode 2	OFF	ON	High to Low	Low

Note: VDD means VDDA, VDDB





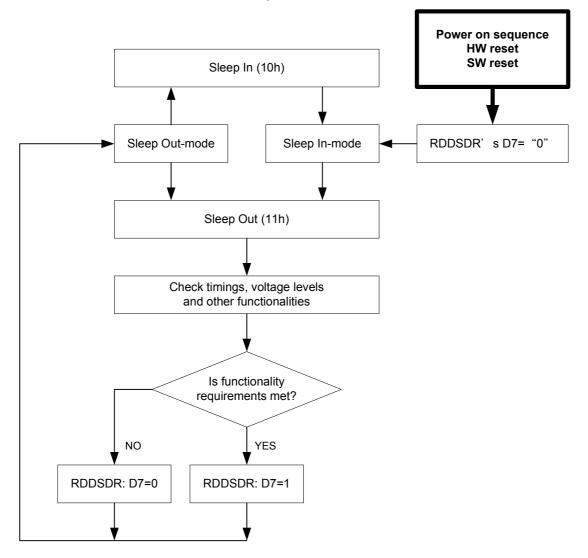
10.3 Sleep Out -Command and self-diagnostic functions of the display module

10.3.1 Register loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from ROM to registers of the display controller is working properly.

There are compared factory values of the ROM and register values of the display controller by the display controller (1st step: compare register and ROM values, 2nd step: loads ROM values to registers). If those both values (ROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command RDDSDR (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:



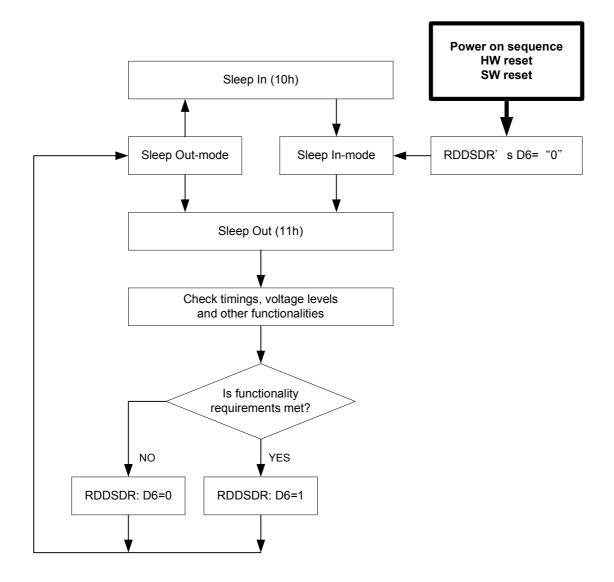


10.3.2 Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module.

The internal function (= the display controller) is comparing if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, bit-6 of RDDSDR is set to 1, which defined in command Read Display Self-Diagnostic Result (RDDSDR). The used bit of this command is D6. If functionality requirement is not same, this bit (D6) is set to 0.

The flow chart for this internal function is following:





11 GAMMA CORRECTION

ST7701 incorporate the gamma correction function to display 16M colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities, and RGB can be adjusted individually.

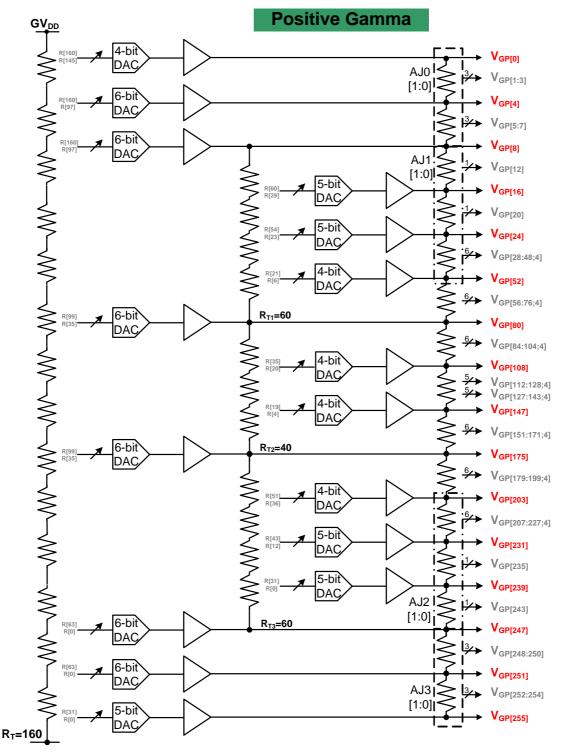


Figure 91 Gray scale Voltage Generation (Positive)

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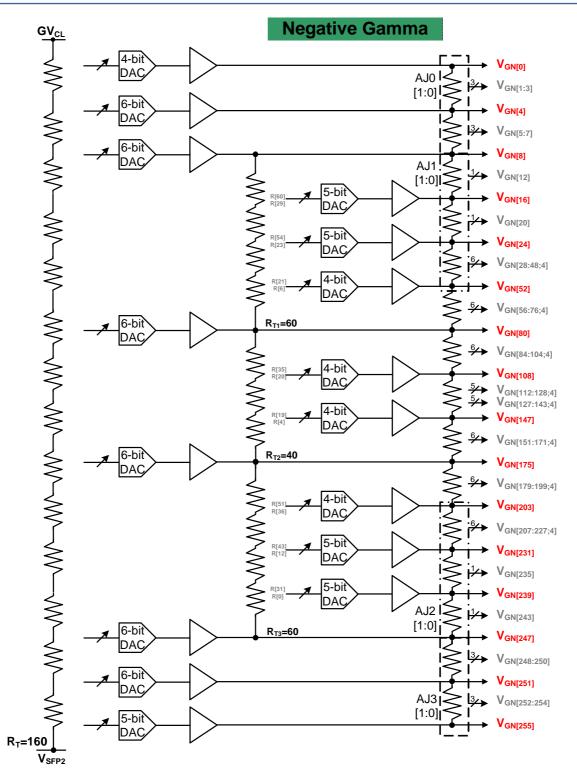


Figure 92 Gray scale Voltage Generation (Positive)



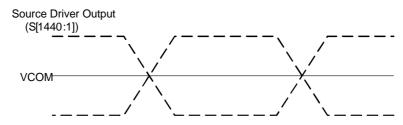


Figure 93 Relationship between Source Output and VCOM

Percentage adjustment:

AJ0P[1:0], AJ1P[1:0], AJ2P[1:0], AJ3P[1:0], AJ0N[1:0], AJ1N[1:0], AJ2N[1:0], AJ3N[1:0], these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

AJ0P[1:0]/AJ0N[1:0]:

	00h	01h	02h	03h
VP1/VN1	64%	75%	70%	53%
VP2/VN2	27%	50%	41%	17%
VP3/VN3	9%	25%	15%	3%
VP5/VN5	75%	75%	88%	88%
VP6/VN6	50%	50%	58%	58%
VP7/VN7	25%	25%	29%	29%

AJ1P[1:0]/AJ1N[1:0]:

	00h	01h	02h	03h
VP12/VN12	50%	54%	50%	60%
VP20/VN20	50%	44%	50%	42%
VP28/VN28	86%	71%	80%	66%
VP32/VN32	71%	57%	63%	49%
VP36/VN36	57%	40%	49%	34%
VP40/VN40	43%	29%	34%	23%
VP44/VN44	29%	17%	20%	14%
VP48/VN48	14%	6%	9%	6%



AJ2P[1:0]/AJ2N[1:0]:

	00h	01h	02h	03h
VP207/VN207	86%	86%	86%	89%
VP211/VN211	71%	71%	77%	80%
VP215/VN215	57%	60%	63%	69%
VP219/VN219	43%	43%	46%	51%
VP223/VN223	29%	34%	31%	37%
VP227/VN227	14%	17%	14%	20%
VP235/VN235	50%	56%	47%	47%
VP243/VN243	50%	50%	50%	53%

AJ3P[1:0]/AJ3N[1:0]:

	00h	01h	02h	03h
VP248/VN248	75%	75%	71%	71%
VP249/VN249	50%	50%	42%	42%
VP250/VN250	25%	25%	13%	13%
VP252/VN252	91%	75%	85%	97%
VP253/VN253	73%	50%	59%	83%
VP254/VN254	36%	25%	30%	48%

Table 28 voltage level percentage adjustment description



11.1 Gray voltage generator for digital gamma correction

ST7701 digital gamma function can implement the RGB gamma correction independently. ST7701 utilizes look-up table of digital gamma to change ram data, and then display the changed data from source driver. The following diagram shows the data flow of digital gamma.

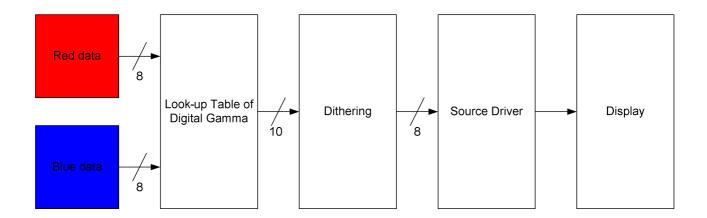


Figure 94 Block diagram of digital gamma

There are 2 registers and each register has 260 bytes to set R, G, B gamma independently. When bit DGMEN be set to 1, R and B gamma will be mapped via look-up table of digital gamma to gray level voltage.

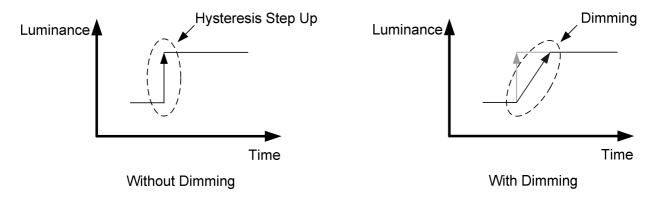
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11.2 Display Dimming

General Description

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement. The basic idea is described below.



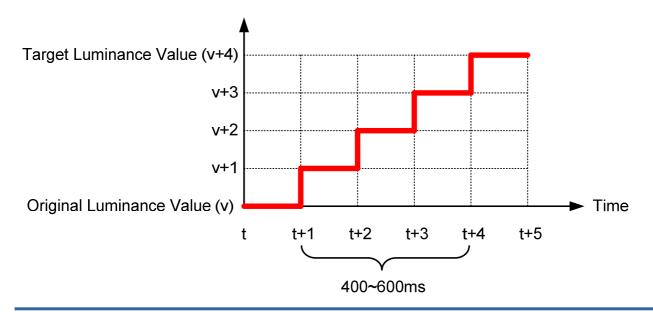
Dimming function can be enable and disable. See "Write CTRL Display (53h)" (bit DD) for more information.

Dimming Requirement

Dimming function in the display module should be implemented so that 400-600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

An upward example is illustrate below



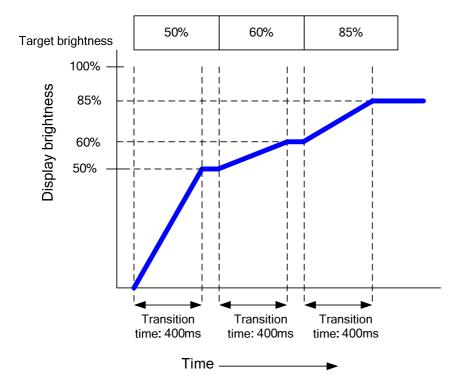
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Definition of brightness transition time

Shorter transition time than 500ms.

There is some stable time between transitions. Below drawing is for transition time: 400ms.

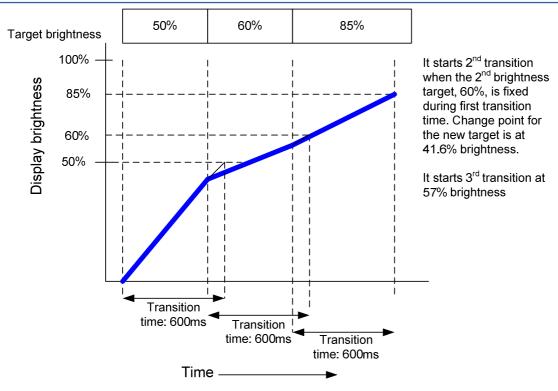


Longer transition time than 500ms

There is no any stable time between transitions. Below drawing is for transition time: 600ms.

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11.3 Content Adaptive Brightness Control (CABC)

Definition of CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus the power consumption reduction

Definition of Modes and target power reduction ratio:

- Off mode: Content Adaptive Brightness Control functionality is totally off.
- UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.
- Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.
- Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

Note 1: Updating partial area of the image data should be supported by CABC functionality.

Note 2: Processing power consumption of CABC should be minimized.

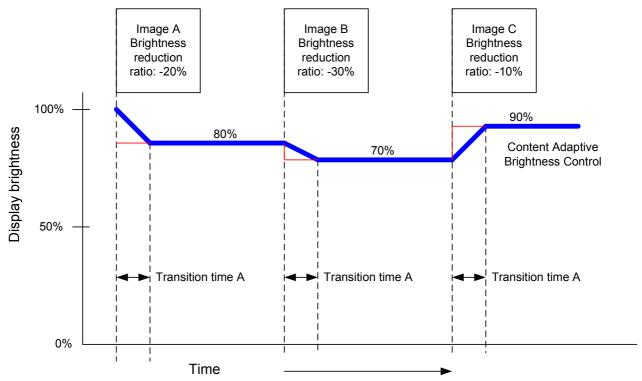
Note 3: Customer need program OTP GAMMA when using CABC.



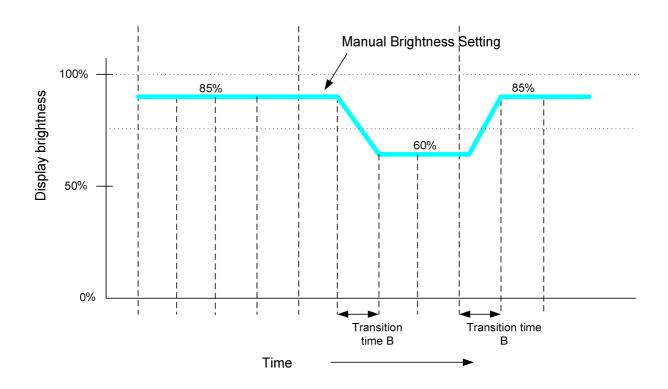
The transition time for dimming function is illustrated below.

- Content Adaptive Brightness Control
 Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.
- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -30% brightness reduction

Transition time from the previous image to the current displayed image is "transition time A".



Manual brightness setting and Dimming function

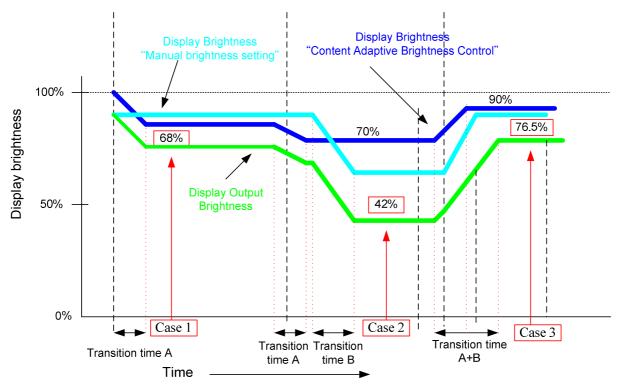




Combine Display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A+B.



Brightness level calculates with the following formula.

Display Output brightness = Manual Brightness setting * CABC brightness ratio

	Manual Brightness setting	Brightness ratio [CABC]	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Transition time from the current brightness to target brightness is A+B in the worst case.



Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

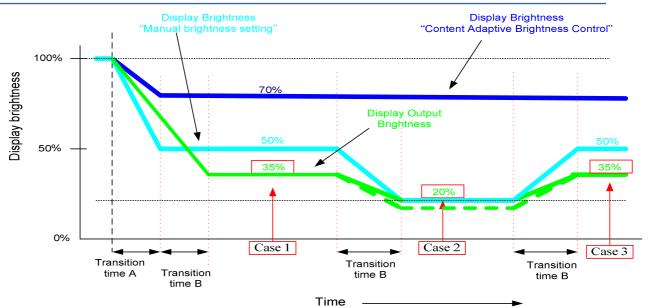
When display brightness is turned off (BCTRL=0 of the Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. "Read CABC minimum brightness (5Fh)" always read the setting value of "Write CABC minimum brightness (5Eh)".

	WRCABC (55h)	Function	RDCABCMB (5Fh)	Image
Sleep-in		NA	WRCABCMB (5Eh)	
CABC off	00b	Disable	WRCABCMB (5Eh)	Original
CABC on	01b/10b/11b	Enable	WRCABCMB (5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.



CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness	Brightness ratio	Calculation result	Display Output	Image
	[manual setting]	[CABC]	of the display	Brightness	
			brightness formula		
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.



12 COMMAND

12.1 Command Transmission Mode on MIPI Interface

Command	MIPI Transmission Mode
Command Table1	LPDT / HSDT
Command Table2	LPDT

12.2 System Function Command Table 1

Instruction	Add	ress SPI-16	R/W/	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOP	00h	0000h	С	0	0	0	0	0	0	0	0	0	No operation
SWRESET	01h	0100h	С	0	0	0	0	0	0	0	0	1	Software reset
		0400h						ID1 read					
RDDID	04h	0401h	R	3				ID2	[7:0]				ID2 read
		0402h						ID3	[7:0]				ID3 read
RDNUMED	05h	0500h	R	1	ErrOver Err[6:0]								Read No. of the Errors on DSI only
RDRED	06h	0600h	R	1				R_1s	st[7:0]				Read the first pixel of Color R
RDGREEN	07h	0700h	R	1				G_1s	st[7:0]				Read the first pixel of Color G
RDBLUE	08h	0800h	R	1				B_1s	st[7:0]				Read the first pixel of Color B
RDDPM	0Ah	0A00h	R	1	BSTON	0	0	SLPOUT	1	DISON			Read Display Power Mode
RDDMADCTL	0Bh	0B00h	R	1				ML	BGR	МН		-	Read Display MADCTR
RDDCOLMOD	0Ch	0C00h	R	1		VIPF	[2:0]						Read Display Pixel Format
RDDIM	0Dh	0D00h	R	1			INVON	ALPXLON	ALPXLOFF		GCS[2:0]		Read Display Image Mode
RDDSM	0Eh	0E00h	R	1	TEON	TELMD							Read Display Signal Mode
RDDSDR	0Fh	0F00h	R	1	RLD	FUND	0	0				-	Read Display Self-diagnostic result
SLPIN	10h	1000h	С	0	0	0	0	0	0	0	1	0	Sleep in
SLPOUT	11h	1100h	С	0	0	0	0	1	0	0	0	1	Sleep out
PTLON	12h	1200h	С	0	0	0	0	1	0	0	1	0	Partial mode on
NORON	13h	1300h	С	0	0	0	0	1	0	0	1	1	Normal display mode on
INVOFF	20h	2000h	С	0	0	0	1	0	0	0	0	0	Display inversion off (normal)
INVON	21h	2100h	С	0	0	0	1	0	0	0	0	1	Display inversion on
ALLPOFF	22h	2200h	С	0	0	0	1	0	0	0	1	0	All pixel off (black)
ALLPON	23h	2300h	С	0	0	0	1	0	0	0	1	1	All pixel on (white)
GAMSET	26h	2600h	W	1	1	1				GC	[3:0]		Gamma curve select
DISPOFF	28h	2800h	С	0	0	0	1	0	1	0	0	0	Display off
DISPON	29h	2900h	С	0	0	0	1	0	1	0	0	1	Display on

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	Add	ress	R/W/										
Instruction	MIPI	SPI-16	С	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
TEOFF	34h	3400h	С	0	0	0	1	1	0	1	0	0	Tearing effect line off
TEON	35h	3500h	W	0	0	0	1	1	0	1	0	1	Tearing effect line on
MADCTL	36h	3600h	W	1				ML	BGR				Display data access control
IDMOFF	38h	3800h	С	0									Idle mode off
IDMON	39h	3900h	С	0									Idle mode on
COLMOD	3Ah	3A00h	W	0			VIPF[2:0]						Interface Pixel Format
		4500h						TESI	_[15:8]	•	•	•	
GSL	45h	4501h	R	2				TES	L[7:0]				Read Tear line
WRDIBV	51h	5100h	W	1				DB\	/[7:0]				Write display brightness
RDDISBV	52h	5200h	R	1				DB\	/[7:0]				Read display brightness value
WRCTRLD	53h	5300h	W	1			BCTRL		DD	BL			Write control display
RRCTRLD	54h	5400h	R	1			BCTRL		DD	BL			Read control display value
WRCABC	55h	5500h	W	1	CE_ON		CE_M	D[1:0]			CABC_	MD[1:0]	Write CABC mode
RRCABC	56h	5600h	R	1	CE_ON		CE_M	D[1:0]			CABC_	MD[1:0]	Read CABC mode
WRCABCMB	5Eh	5E00h	W	1				СМІ	3[7:0]				Write CABC minimum brightness
RRCABCMB	5Fh	5F00h	R	1				СМІ	3[7:0]				Read CABC minimum brightness
RDABCSD	68h	6800h	R	1	RLD	FUND							Read Automatic Brightness Control Self-Diagnostic Result
RDBWLB	70h	7000h	R	1	BKx1	BKx0	BKy1	BKy0	Wx1	Wx0	Wy1	Wy0	Read Black/White Low Bits
RDBkx	71h	7100h	R	1	BKx9	BKx8	BKx7	BKx6	BKx5	BKx4	ВКх3	BKx2	Read BKx
RDBky	72h	7200h	R	1	ВКу9	BKy8	ВКу7	BKy6	BKy5	BKy4	ВКу3	BKy2	Read Bky
RDWx	73h	7300h	R	1	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	Read Wx
RDWy	74h	7400h	R	1	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	Read Wy
RDRGLB	75h	7500h	R	1	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	Read Red/Green Low bits
RDRx	76h	7600h	R	1	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Read Rx
RDRy	77h	7700h	R	1	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	Read Ry
RDGx	78h	7800h	R	1	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	Read Gx
RDGy	79h	7900h	R	1	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	Read Gy
RDBALB	7Ah	7A00h	R	1	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	Blue/AColour Low Bits
RDBx	7Bh	7B00h	R	1	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	Read Bx
RDBy	7Ch	7C00h	R	1	Ву9	By8	Ву7	By6	By5	By4	Ву3	By2	Read By
RDAx	7Dh	7D00h	R	1	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	Read Ax
RDAy	7Eh	7E00h	R	1	Ay9	Ay8	Ау7	Ay6	Ay5	Ay4	At3	Ay2	Read Ay

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Instruction	Add	ress	R/W/	DNILIM	D7	DC	D.F.	D4	Do	Do	D4	Do	Forestina																																		
Instruction	MIPI	SPI-16	С	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function																																		
		A100h						0x	77				Read the DDB from the provided location																																		
		A101h						0x	01																																						
RDDDBS/	A1h	A102h	R	5				MID[15:8]																																						
CHKSUM		A103h																																													
		A104h			8'hff																																										
		A800h			SID[15:8]								Continue reading the DDB from the last read location																																		
		A801h						SID	[7:0]				nom the last read recalled.																																		
RDDDBC	A8h	A802h	R	5				MID[15:8]																																						
		A803h						MID	[7:0]																																						
		A804h						8'	hff																																						
RDFCS	AAh	AA00h	R	1	FCS[7:0]				FCS[7:0]				FCS[7:0] F				Read First Checksum																														
RDCCS	AFh	AF00h	R	1	CCS[7:0]				CCS[7:0]				CCS[7:0]				CCS[7:0]				CCS[7:0]				CCS[7:0]				CCS[7:0]				CCS[7:0]				CCS[7:0]							CCS[7:0]			Read Continue Checksum
RDID1	DAh	DA00h	R	1	ID1[7:0]							ID1[7:0]				ID1[7:0]					Read ID1																										
RDID2	DBh	DB00h	R	1	ID2[7:0] Read ID2						Read ID2																																				
RDID3	DCh	DC00h	R	1	ID3[7:0]								Read ID3																																		

Table 29 System Function Command List

Note:

- 1. In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. This note is valid when a number of the parameters is equal or less than 32.
- 2. The 8-bit address code for "MIPI" in above table and following command description means include 3-wire 9-bit SPI and 4-wire 8-bit SPI.

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12.2.1 NOP (00/0000h)

00H		NOP (No Operation)												
Inst / Para	R/W	Add	lress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
IIISt / Pala	K/VV	MIPI	SPI-16	D15-6	וט	Do	Do	D4	DS	DZ	וט	DU		
NOP	W	00h	0000h				No Arg	gument						
Parameter	No Para	ameter												
Description				command. It doe to terminate para				display ı	module.					
Restriction														
		Status Availability												
		Nor	mal Mod	e On, Idle Mode	Off, Sle	ep Out			Yes					
Register		Nor	mal Mod	e On, Idle Mode	On, Sle	ep Out			Yes					
Availability		Pai	rtial Mode	e On, Idle Mode	Off, Slee	p Out			Yes					
		Pai	rtial Mode	e On, Idle Mode	On, Slee	ep Out	Yes							
				Sleep In					Yes					
				Status				Defa	ult Value)				
Default			Pow	er On Sequence)				N/A					
Delauit			S/W Reset N/A											
				H/W Reset					N/A					
Flow Chart														



12.2.2 SWRESET (01h/0100h): Software Reset

				SWRESE	T (Softwa	are Reset	:)				
	Add	dress									
R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
W	01h	0100h	xx	0	0	0	0	0	0	0	1
No Parai	meter	•									•
"-" Don't	care										
-The disp	olay mod	lule perfor	ms a software res	et, registe	rs are wri	tten with	their SW	eset defa	ult values	3.	
-Frame r	nemory (contents a	re unaffected by tl	nis comma	and.						
It will be	necessa	ry to wait	5msec before sen	ding new	command	d following	g software	reset.			
The disp	lay modu	ule loads a	all display supplier	s' factory	default va	lues to th	e register	s during t	his 5mse	C.	
If softwa	re reset i	s sent dur	ing sleep in mode	, it will be	necessar	y to wait	120msec	before se	nding sle	ep out co	mmand.
Software	reset co	mmand c	annot be sent duri	ng sleep o	out seque	nce.					
When M	IPI Video	Mode ap	plication, the shut	down pac	ket shoul	d be sent	(leave to	video mo	ode) befor	re	
S/W rese	et										
			•								
				0" 0	O .				ty		
		Partial Mo		On, Sleep	Out						
			Sleep In					Yes			
			Status				Defa	ult Value			
		Po	wer On Sequence					N/A			
			S/W Reset					N/A			
			H/W Reset					N/A			
			Display w Blank sci	rhole reen Ind		Par D A A Sec	mmand rameter isplay action Mode quential				
	No Parar "-" Don't -The disp -Frame r It will be The disp If software When M	R/W MIPI W 01h No Parameter "-" Don't care -The display mode -Frame memory of It will be necessa The display mode If software reset is Software reset of When MIPI Video S/W reset	MIPI SPI-16 W 01h 0100h No Parameter "-" Don't care -The display module perfor -Frame memory contents a It will be necessary to wait The display module loads a If software reset is sent dur Software reset command of When MIPI Video Mode ap S/W reset Normal Mo Partial Mo Partial Mo	R/W SPI-16 W O1h O100h XX No Parameter "-" Don't care -The display module performs a software resersor Frame memory contents are unaffected by the lit will be necessary to wait 5msec before sent The display module loads all display suppliers If software reset is sent during sleep in mode. Software reset command cannot be sent during When MIPI Video Mode application, the shut S/W reset Status	R/W MIPI SPI-16 W 01h 0100h xx 0 No Parameter "-" Don't care -The display module performs a software reset, registery of the display module loads all display suppliers' factory of software reset is sent during sleep in mode, it will be software reset command cannot be sent during sleep of When MIPI Video Mode application, the shut down pactor of S/W reset Status Normal Mode On, Idle Mode Off, Sleep Partial Mode On, Idle Mode On, Sleep Sleep In Status Power On Sequence S/W Reset H/W Reset SWRESET (01h) Display whole Blank screen Set Command To S/W Default Value	R/W SPI-16 D15-8 D7 D6	R/W MIPI SPI-16 W 01h 0100h xx 0 0 0 0 No Parameter "-" Don't care -The display module performs a software reset, registers are written with software reset is sent during sleep in mode, it will be necessary to wait 5msec before sending new command following. The display module loads all display suppliers' factory default values to the if software reset is sent during sleep in mode, it will be necessary to wait Software reset command cannot be sent during sleep out sequence. When MIPI Video Mode application, the shut down packet should be sent S/W reset Status Normal Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Status Power On Sequence S/W Reset H/W Reset L Signal Whole Blank screen Display whole Blank screen Display whole Blank screen Display whole Blank screen Display whole Sct Command To S/W Default Value Scc	R/W MIPI SPI-16 W 01h 0100h xx 0 0 0 0 0 0 No Parameter "-" Don't care -The display module performs a software reset, registers are written with their SW or Frame memory contents are unaffected by this command. It will be necessary to wait 5msec before sending new command following software The display module loads all display suppliers' factory default values to the register If software reset is sent during sleep in mode, it will be necessary to wait 120msec Software reset command cannot be sent during sleep out sequence. When MIPI Video Mode application, the shut down packet should be sent (leave to S/W reset Status	R/W Address MIPI SPI-16 D15-8 D7 D6 D5 D4 D3 W 01h 0100h xx 0 0 0 0 0 0 No Parameter "-" Ont care -The display module performs a software reset, registers are written with their SW reset defe-Frame memory contents are unaffected by this command. It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during tilf software reset is sent during sleep in mode, it will be necessary to wait 120msec before set Software reset command cannot be sent during sleep out sequence. When MIPI Video Mode application, the shut down packet should be sent (leave to video mo S/W reset Status	R/W	R/W Address D15-8 D7 D6 D5 D4 D3 D2 D1 W O1h O100h XX O O O O O O O O No Parameter "" Don't care The display module performs a software reset, registers are written with their SW reset default values. -Frame memory contents are unaffected by this command. It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out co Software reset command cannot be sent during sleep out sequence. When MIPI Video Mode application, the shut down packet should be sent (leave to video mode) before SW reset Status



12.2.3 RDDID (04h/0400h~0402h): Read Display ID

04H					RDDID	(Read Dis	splay ID)					
		Add	lress				. , -/					
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
			0400h	00h				ID1	[7:0]	1		1
RDDID	R	04h	0401h	00h					[7:0]			
			0402h	00h					[7:0]			
Description	-The 1 st -The 2 nd -The 3 rd -The 4 th	paramete paramete paramete paramete	er is dumm er (ID1): L er (ID2): L0 er (ID3): L0	oit display identific ny data CD module's man CD module/driver CD module/driver Ah, DBh, DCh) r	ufacturer version ID	ID.	ond to th	ne param	neters 2,3	3,4 of th	e comma	and 04h,
Restriction	-											
				Status					Availabili	ty		
		N	lormal Mo	de On, Idle Mode	Off, Sleer	o Out			Yes			
Register		N	lormal Mo	de On, Idle Mode	On, Sleer	p Out			Yes			
availability		F	Partial Mo	de On, Idle Mode	Off, Sleep	Out			Yes			
		F	Partial Mo	de On, Idle Mode	On, Sleep	Out			Yes			
				Sleep In					Yes			
								Dofo	ult Value			
				Status			ID1		ID2	l ır	03	
Default			Pov	wer On Sequence			0xFF		0xFF		:FF	
				S/W Reset			0xFF		OxFF		:FF	
				H/W Reset			0xFF		OxFF		:FF	
Flow Chart				Send 1st Parame ID1[7:0] Send 2nd Parame ID2[7:0] Send 3rd Parame ID3[7:0]	eter	H Dri	Iost I C	Lege Comr Paran Disp Act: Mo Seque trans	nand neter play ion de	7 7 7 7 7 7 7 7 7 7		



12.2.4 RDNUMED (05h/0500h): Read Number of Errors on DSI

05H	RDNUMED													
last / Dans	DAA	Addr	ress	D45.0	D7	Do	Dr	D.4	Do	Do	D4	Do		
Inst / Para	R/W	Others	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDNUMED	R	05h	Χ	X	Errover				Err[6:0]					
	The first	paramete	r is telling	g a number of the p	parity erro	rs on DSI	. The mo	re detaile	d descript	ion of the				
	bits is be													
Description				mber of the parity										
				is overflow with P[
		nmand is i	used for I	MIPI DSI only. It is	no functio	n for othe	ers interfa	ce operat	ion.					
Restriction	-													
				Status					Availabili	to r				
		N	ormal Mc		Off Sleer	Out				ıy				
Register		Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Yes												
availability		Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes												
		Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Yes												
				Sleep In	. ,				Yes					
							l							
				Statu	S				t Value					
			_				Er	rover	Err[6					
Default				r On Sequence				0	000-0					
			S/W F					0	000-0					
			H/W I	Reset				0	000-0	000				
Flow Chart			-	RDNUMED(0) Send 1st Parame	•••••		[ost] [lever] /	Lega Comr Paran Disp Acti Mo Seque trans	nand neter blay de ential					



12.2.5 RDRED (06h/0600h): Read the first pixel of Red Color

06H						RDRED							
In at / Dame	DAM	Add	ress	D45.0	D.7	Do	DE	D.4	Do	Do	D4	Do	
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDRED	R	Χ	0600h	X				R_1s	t[7:0]				
				red component val									
	-			sed according to p				set to "0".					
Description				nd R0 is LSB. R7, nd R0 is LSB. R7									
				nd R0 is LSB.	ana ito a	10 301 10 0							
Restriction	-												
				Status					Availabili	ty			
		N	Normal Mo	ode On, Idle Mode	Off, Slee	p Out			Yes				
Register		N	Normal Mo	ode On, Idle Mode	On, Slee	p Out			Yes				
availability				de On, Idle Mode					Yes				
		F	Partial Mo	de On, Idle Mode	On, Sleep	Out			Yes				
		Sleep In Yes											
	Stat	ius							Default	t Value (D	7 to D0)		
5.4	Pov	ver On Se	equence						00h	,	,		
Default	S/M	/ Reset							00h				
	H/W	/ Reset							00h				
							۲ -		· - -	٦			
							1	Lege	end	1			
				RDRED(06h)	11]			
			-	······	•••••	Dri	ost [Comn	nand	j I ⊸I			
			_	V Dummy Rea	d	7	VCI _	Paran	neter	/ ¦			
Flow Chart			_	Dunning Rea		/	<u> </u>	Disp	lay) [
Flow Chart				0 107011		7		Acti	on	,			
				Send R[7:0] da	ata		i)			1			
							1 (Мо	de) [
							! [Seque trans]			
								trails	,101] 			
										- '			



12.2.6 RDGREEN (07h/0700h): Read the first pixel of Green Color

07H						RDGREE	N					
Inst / Para	R/W	Add MIPI	ress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDGREEN	R	Х	0700h	Х			1	G_1s	st[7:0]		l	
Description	Only the -16-bit fo -18-bit fo	relevant rmat: G4 rmat: G5	bits are u is MSB a is MSB a	green component of sed according to point of the sed according to point of the sed according to point of the sed according to the sed a	ixel forma	at, unuse G5 are se	d bits are et to "0".	active fran	me.			
Restriction	-											
Register availability		1	Normal Mo	Status ode On, Idle Mode ode On, Idle Mode ode On, Idle Mode ode On, Idle Mode Sleep In	On, Slee Off, Sleep	p Out			Availabilii Yes Yes Yes Yes Yes Yes	ty		
Default		F	Status Power On S/W Reset			0	Default Va DOh DOh	alue (D7 to	D0)			
Flow Chart				Dummy Read	d		Host Host I	Leg Comr Paran Disp Act Mc Seque tran:	mand neter play ion de ential	7 7 7 7 7 7 7 7 7 7		



12.2.7 RDBLUE (08h/0800h): Read the first pixel of Blue Color

08H						RDBLUI						
Inst / Dave	DAM	Add	Iress	D45.0	D7	DC	DE	D4	Do	Do	D4	Do
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDBLUE	R	Χ	0800h	X				B_1s	t[7:0]			
				blue component va					Э.			
	-			sed according to p				set to "0".				
Description				nd B0 is LSB. B7,								
				nd B0 is LSB. B7 a	and B6 ar	e set to "	0".					
Destriction		illial. D7	is ivisb a	nd B0 is LSB.								
Restriction	-											
				Status					Avoilobili	h		
			Jormal Mo	ode On, Idle Mode	Off Slee	n Out			Availabili Yes	ıy		
Register				ode On, Idle Mode					Yes			
availability				ode On, Idle Mode					Yes			
				ode On, Idle Mode					Yes			
				Sleep In					Yes			
		S	status			[Default Va	ue (D7 to	D0)			
Default		Р	ower On	Sequence		(00h					
2 oraun		S	/W Reset			(00h					
		Н	I/W Reset	i		(00h					
							٢-		· - -	٦ .		
							!	Lege	end	l I		
				RDBULE(08)	1)	1	Host [Comn	1			
			-			• • • • • • • • •	river			」 ' →【		
				Dummy Read	4	7 - 7		Paran	neter	/ '		
Flow Chart			_	Bunning Read		/	; (Disp	lay	· 		
1 low Chart				G 1 DF7 01 1		7	, 	Acti	on	1		
				Send B[7:0] da	ata ———	/	i ì	Acti	OII	1		
							1 (Mo	de	1		
							I	Seque] [
							I	trans	sier] [
							┕			_		
	<u> </u>											



12.2.8 RDDPM (0Ah/0A00h): Read Display Power Mode

0AH							RDDP	M					
			Add	ress									
Inst / Para	R/V	V M	1IPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDDPM	R	0	Ah	0A00h	Χ	BSTON	0	0	SLPOUT	1	DISON		
	This	comma	and in	dicates th	ne current status o	of the disp	lay as de	scribed	in the table b	elow:			
		Bit	t		Description				١	/alue			
		D7	7	Booster	Voltage Status		"1"=B	ooster C	n, "0"=Boost	er Off			
		D6	6	Not Def	ined			"0" (not	,				
Description		D5		Not Def				"0" (not	,				
'		D4		Sleep Ir					ut Mode, "0" :	= Sleep I	n Mode		
		D3		Not Def				"1" (not					
		D2		Display					s On, "0" = D	isplay is	Off		
		D1 D0		Not Def				"0" (not "0" (not					
	<u> </u>	DC	,	Not Del	ineu		Serio	0 (1101	useu)				
Restriction	-												
					Status					Availabili	itv		
				Normal M	ode On, Idle Mod	le Off, Sle	ep Out			Yes	,		
Register					ode On, Idle Mod					Yes			
availability					ode On, Idle Mod					Yes			
					ode On, Idle Mod					Yes			
					Sleep In					Yes			
			Ş	Status				Default	Value (D7 to	D0)			
			_		Sequence			08h	(= 1 = 1				
Default				S/W Rese				08h					
			H	H/W Rese	t			08h					
							<u> </u>						
Flow Chart					RDDPM(0). Send 1st Para	••••••		Host	Lege Comm Param Disp Acti Mod Seque trans	nand neter lay on de	7 		



12.2.9 RDDMADCTL (0Bh/0B00h): Read Display MADCTL

0BH					R	DDMADO	CTL					
Last / Dave	D 44		ddress	D45.0	D7		D.	D.1	Do	D0	D4	Do
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDDMADCTL	R	0Bh	0B00h	X				ML	BGR	МН		
	This	command	ndicates th	e current status of	the displa	ay as des	cribed in t	he table b	elow:			
		Bit	Descript	ion		Value						
		D7~D5	Not Defi	ned		Set to '	'0" (not us	sed)				
		D4	Vertical i	refresh Order (ML)		"0" = Ir	crement,	"1" = Dec	crement			
Description		D3	RGB-BG	GR Order				sequence sequence				
		D2	Horizont	al refresh Order (N	/H)	"0" = Ir	crement,	"1" = Dec	crement			
		D1	Not Defi	ned		Set to '	'0" (not us	sed)				
		D0	Not Defi	ned		Set to '	'0" (not us	sed)				
Restriction	<u> -</u>											
				Status					Availabili	ty		
	Normal Mode On, Idle Mode Off, Sleep Out Yes											
Register			Normal Mo	ode On, Idle Mode	On, Slee	p Out			Yes			
availability			Partial Mo	de On, Idle Mode	Off, Sleep	Out			Yes			
			Partial Mo	de On, Idle Mode	On, Sleep	Out			Yes			
				Sleep In					Yes			
		Ī	Status				Default Va	lue (D7 to	D0)			
			Power On	Seguence			10h	(= : ::	/			
Default			S/W Reset			(10h					
			H/W Reset			(0h					
						·						
Flow Chart			_	RDDMADCTL(Host [iver / ((Leg Comr Paran Disp Act Mc Seque trans	mand neter play ion de ential			



12.2.10 RDDCOLMOD (0Ch/0C00h): Read Display Pixel Format

0CH						RI	DDCOLMO)D					
In at / Dans	1	.,	Add	dress	D45.0	D7	Do	Dr	D4	D 0	Do	D4	Do
Inst / Para	R/	W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDDCOLMOD	R	2	0Ch	0C00h	X		,	/IPF[2:0]					
	This	com	mand in	dicates the	e current status of	the displa	y as desc	ribed in t	he table b	elow:			
		Bit		Descripti	ion		Value						
		D7		Not Defin	ned		Set to "C	" (not us	ed)				
							"101" =	16-bit / p	ixel				
		D6	~D4	RGB Inte	erface Color Forma	at	"110" =	18-bit / pi	ixel				
Description								24-bit / pi					
		D3		Not Defin				" (not us					
		D2		Not Defin				" (not us					_
		D1		Not Defin				" (not us					
		D0		Not Defi	ned		Set to "C	" (not us	ed)				
Restriction	-												
								ſ					
					Status		_			Availabili	ty		
					ode On, Idle Mode			+		Yes			
Register					ode On, Idle Mode					Yes			
availability					ode On, Idle Mode					Yes			
				Partial IVIO	de On, Idle Mode Sleep In	On, Sieep	Out			Yes Yes			
					Оссрии					103			
			5	Status			De	efault Val	ue (D7 to	D0)			
			F	ower On	Sequence		70)h					
Default			5	S/W Reset	:		70)h					
			F	H/W Reset			70)h					
								۲ -		. — —	٦		
								i	Leg	end	1		
					RDDCOLMOD(0Cb)		į			1		
				-	RDDCOLMOD((CII)		ost	Comr	nand	1		
				_	<u> </u>		Dri	ver /	Paran	neter .	₇ 1		
					Send 1st Parame	eter							
Flow Chart								1	Disp	lay)		
								<	Acti	on	, <u> </u>		
									Mo	de			
								1 /			′ I . I		
								!	Seque trans				
] ' 		
											- '		



12.2.11 RDDIM (0Dh/0D00h): Read Display Image Mode

0DH								RDDIM					
			Addre	ess									
Inst / Para	R/V	M		SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDDIM	R	0	Dh (0D00h	Χ			INVO	ALPXLON	ALPXLOFF		GCS[2:0]
	This	comm	and in	dicates	the current statu	us of the	displa	y as desc	ibed in the table	e below:			
		Bit		Descri	ption			Value					
		D7~[D6	Not De	efined			Set to "C	0" (not used)				
		D5		Invers	ion On/Off				sion On, "0"=Ir				
Description		D4		All Pix					e display,"0"=N				
		D3		All Pix	el Off				k display,"0"=N	ormal display			
		D 0 F	20	0	0 0 1 1				C0, "001"=GC1				
		D2~[00	Gamm	na Curve Selecti	on			C2, "011"=GC3				
			ļ					110 10	111"=not define	eu			
Restriction	-												
reconicion													
					Status	S				Availability			
	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register			١	Normal	Mode On, Idle M	1ode On	, Sleep	Out		Yes			
availability			ı	Partial N	Mode On, Idle M	lode Off,	Sleep	Out		Yes			
			ı	Partial N	Mode On, Idle M	ode On,	, Sleep	Out		Yes			
					Sleep	In				Yes			
				M = 1 · · · =					(II-) (-I (D7	(- D0)		1	
			_	status	n Sequence			00	fault Value (D7	to D0)			
Default				3/W Res				00					
			—	I/W Res				00					
			<u> </u>	1/ VV 1\C3				00	11			_	
									l I	egend			
							\neg						
					RDDIM	I(ODh)		Н	ost Co	mmand			
						,		Dri	/er /				
				/	Send 1st P	arameter		7	Pa	rameter			
Flow Chart				_			/			risplay			
									i 🗸	Action			
										Mode			
										quential			
									l tr	ransfer			
									L	'			



12.2.12 RDDSM (0Eh/0E00h): Read Display Signal Mode

0EH						R	RDDSN	М					
		Add	ress										
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	6	D5	D4	D3	D2	D1	D0
RDDSM	R	0Eh	0E00h	Х	TEON	TELM	ИD						
Description		3it D7 D6 D4~D0		g Effect Line O			"1"=Mo	n,"0"=Of ode2,"0" "00000"		l)			
Restriction	-												
Register availability			Normal Partial I	Statu Mode On, Idle I Mode On, Idle I Mode On, Idle I Mode On, Idle I Sleep	Mode Off, Mode On, Mode Off, S Mode On, S	Sleep C Sleep O	Out Out			Availab Yes Yes Yes Yes	ility		
Default		-	Status Power O S/W Res				(Default \ 00h 00h 00h	Value (D7	to D0)			
Flow Chart			_		M(0Eh) Parameter			Host Host Driver 	Co Pau D A Sec	egend mmand rameter isplay action Mode quential ansfer			



12.2.13 RDDSDR (0Fh/0F00h): Read Display Self-Diagnostic Result

0FH						RDE	SDR					
Inst / Para	R/W	Add MIPI	ress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDDSDR	R	0Fh	0F00h	Х	RLD	FUND	0	0				
Description	<u> </u>	Bit D7 D5 D5~D0		iption ter Loading Det		Se	e section e section		ed)			
Restriction	-											
Register availability			Normal Partial I	Statu Mode On, Idle M Mode On, Idle M Mode On, Idle M Sleep	Mode Off, S Mode On, S Mode Off, S Mode On, S	Sleep Out	t		Availab Yes Yes Yes Yes	:		
Default			Status Power C S/W Res H/W Res				Defau 00h 00h 00h	It Value (Dī	7 to D0)			
Flow Chart				RDDSI Send Ist I	OR(OFh)		Host Driver		Legend Ommand arameter Display Action Mode equential ransfer			



12.2.14 SLPIN (10h/1000h): Sleep in

10H						SLP	rin					
		Add	fress									
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	W	10h	1000h	Х				No Arg	gument			
Description Restriction Register availability	In this m stopped Control User ca this info Sleep C Dimmin	node the Interfac In send I Immation out-mode	e as will a PCLK, HS is valid d e. on does n n internal Normal Normal	Statu Mode On, Idle Mode On, I	and register ation on Rafter Sleep were is charank displayed Mode Off, Stode On, Stode Off, Stode O	ers are still GB I/F for In comma nging mod y Sleep Out Sleep Out	v oscillato working blank dis	or is stoppe . splay after \$ ere is used N	Availab Yes Yes	ommand a de On in		
				Mode On, Idle M Sleep		sieep Out	D.()	W.Vk (D.7	Yes Yes			
Default			Power C S/W Res H/W Res				Sleep Sleep	It Value (D7 In Mode In Mode In Mode	10 00)			
Flow Chart			Disposer off	SPLIN(10h) SPLIN(10h) play whole blank en(Automatic No ct to DISP On/Off Command) in Charge Form Panel		(OAh) com	ff state) a	after SLPIN 7.	Command Lege Comm Param Displ Action Sequentrans	nd eter lay on htial		



12.2.15 SLPOUT (11h/1100h): Sleep Out

11H						SLPC	DUT					
Inst / Para	R/W	Ad MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	W	11h	1100h	Х		I	I	No Arg	gument	I		l
Description	In this m User ca at least There is	node the n start t 2 frame s used a	e DC/DC of send PC of	sleep mode. converter is ena CLK, HS and VS Sleep Out comn oscillator for bla e control about g	information nand, if the ank displa	on on RGE ere is left S y.	3 I/F befo Sleep In-r	re Sleep Or mode to Sle	ut commar	nd and this	informati	on is valid
Restriction	-											
Register availability			Normal Partial I	Statu Mode On, Idle M Mode On, Idle M Mode On, Idle M Sleep	Mode Off, S Mode On, S Mode Off, S Mode On, S	Sleep Out			Availab Yes Yes Yes Yes			
Default			Status Power C S/W Res				Sleep Sleep	It Value (D7 In Mode In Mode In Mode	to D0)			
Flow Chart	It takes	about 1	Int DO All	Start ernal Oscillator Start C/DC Converter control signals glass are normal	o In mode	Display w screen(Au Effect to D Com	hole bland		Common Dispi Action Sequentrans	nand leter / lay on leter lete	 	



12.2.16 PTLON (12h/1200h): Partial Display Mode On

12H						PTL	NC								
Inst / Para	R/W	Add	Iress	D15-8	D7	De	D5	D4	D3	Da	D1	D0			
inst / Para	K/VV	MIPI	SPI-16	8-פוים	D7	D6	D5	D4	D3	D2	ויט	DU			
PTLON	W	12h	1200h	Χ				No Arg	gument						
	This cor	mmand t	turns on I	Partial mode. Th	e partial m	node windo	ow is des	cribed by tl	ne Partial	Area					
	comma	nd .													
Description	To leave	e Partial	mode, th	e Normal Displa	y Mode O	n commar	nd (13H) s	should be v	vritten.						
	There is	no abn	ormal vis	ual effect during	mode cha	ange betwe	een Norm	nal mode O	n to Partia	al mode Oi	n.				
Restriction	This cor	mmand l	has no ef	fect when Partia	ıl Display r	node is ac	tive.								
		Status Availability													
			Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register				Mode On, Idle N		•			Yes						
availability				Mode On, Idle M		•			Yes						
			Partial I	Mode On, Idle M		leep Out			Yes						
				Sleep	In				Yes						
			Status				Default	: Value (D7	to D0)						
Default			Power C	n Sequence			Norma	Mode On							
Delault			S/W Res	set			Norma	Mode On							
			H/W Res	set			Norma	Mode On							
	0 5	-1'-1 A	(001-)												
Flow Chart	See Pa	πiai Area	a (30n)												



12.2.17 NORON (13h/1300h): Normal Display Mode On

13H						NOR	ON							
Inst / Para	R/W	Add MIPI	ress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
NORON	W	13h	1300h	Х		<u> </u>		No Ard	gument	<u> </u>	<u> </u>			
Description	This cor Normal Exit fror	mmand i	returns the mode on DN by the	X e display to non means Partial n Partial mode O ual effect during	node off. n commar	nd (12h)	Partial mo			ode On.				
Restriction	This cor	s command has no effect when Normal Display mode is active.												
Register availability			Normal Partial I	Statu Mode On, Idle M Mode On, Idle M Mode On, Idle M Mode On, Idle M Sleep	Mode Off, S Mode On, S Mode Off, S Mode On, S	Sleep Out			Availab Yes Yes Yes Yes					
Default			Status Power C S/W Res				Normal Normal	Value (D7 Mode On Mode On Mode On	to D0)					
Flow Chart	See Pa	rtial Area	a Definitio	on Descriptions f	or details	of when to	use this	command						



12.2.18 INVOFF (20h/2000h): Display Inversion Off

20H						INVO)FF						
		Add	dress										
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
INVOFF	W	20h	2000h	Х				No Arg	gument				
	This cor	nmand	is used to	recover from d	isplay inve	rsion mod	e.						
	This cor	nmand	does not	change any oth	er status.								
								Display					
Description							_r E		\exists				
				H			'		Ħ				
							VE		8				
									<u> </u>				
Restriction	This cor	nmand	has no ef	fect when modu	lle is alrea	dy in Inver	sion Off	mode.					
				Statu	S				Availab	ilitv			
			Normal			Sleep Out			Yes				
Register		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes											
availability				Mode On, Idle N					Yes				
			Partial N	Mode On, Idle N		Sleep Out			Yes				
				Sleep	in				Yes				
			Status				Defaul	t Value (D7	to D0)				
Default				n Sequence				y Inversion					
			S/W Res					y Inversion					
		L	n/w kes	SEL			Dispia	y Inversion	OII				
							r -		¬				
							i	Legeno	d				
							1		!				
				Dienley I	nversion On			Commai	nd l				
				Display 1	IIVEISIOII OII		1/	Paramet	er /				
Flow Chart				INIVE	¥	1	(Display	y .				
				INVC	FF(20h)		İ<	Action	\rightarrow !				
				Display I	version Off		1	Mode					
				Display II	TVCISION OII	_/	\	Sequenti	:				
							 	transfe					
							L		I				



12.2.19 INVON (21h/2100h): Display Inversion On

21H						INV	NC					
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
INIVONI	10/	MIPI	SPI-16 2100h					No Are	www.ont			
INVON	W This cou	21h	1	X enter display in	nversion m	nde		No Arg	gument			
				change any oth		louc.						
				rsion On, the D		raion Off a	ammand	(20h) ahai	ıld bo writt	on		
	IO EXILI	IIOIII DIS	ріаў піче	ision on, the D	ispiay irive	ISION ON C	Ommanu		iiu be wiitt	en.		
Description				F		Ħ		Display	•			
						∄┌─						
						▋┕	$V \blacksquare$					
						<u> </u>						
Restriction	This co	mmand	has no ef	fect when modu	ule is alrea	dy in Inver	sion On n	node.				
				Statu	JS				Availab	ilitv		
			Normal	Mode On, Idle I		Sleep Out			Yes	-		
Register			Normal	Mode On, Idle I	Mode On,	Sleep Out			Yes			
availability				Mode On, Idle N					Yes			
			Partial I	Mode On, Idle N		Sleep Out			Yes			
				Sleep	ın				Yes			
		_										
			Status				Default	Value (D7	to D0)			
Default				n Sequence				Inversion				
		-	S/W Res					Inversion				
		L	H/W Res	set			Display	Inversion	Off			
								Legend	i İ			
							i		!			
				D'aulas I		<u> </u>	1	Comma	nd			
				Display I	nversion Of		1/	Paramet	er			
Flow Chart					<u> </u>	1		Display	y ;			
1 low onart				INV	ON(21h)			Action	<u> </u>			
				D'aulau I	*							
				Display I	nversion On			Mode	i			
								Sequent transfe				
							L					



12.2.20 ALLPOFF (22h/2200h): All Pixel Off

22H						ALLP	OFF					
		Ado	fress									
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
ALLPOFF	W	22h	2200h	Х				No Arç	gument			
	This cor	nmand	turns the	display panel b	lack in Sle	ep Out mo	ode and	a status of t	the Displa	y On/Off re	egister car	n be on or
	off. This	comma	and does	not change any	other stat	us.						
								Display				
Description							N					
				H		$H \sqcap$,) .					
							V					
D	·		. ,	<u> </u>	<u> </u>	<u> </u>	10"	·				
Restriction	I his cor	nmand	nas no ef	fect when modu	ile is alrea	ay in All Pi	xei Off n	node.				
				Statu	S				Availab	oility		
			Normal	Mode On, Idle N		Sleep Out			Yes			
Register			Normal	Mode On, Idle I	Mode On,	Sleep Out			Yes			
availability			Partial I	Mode On, Idle N	Node Off, S	Sleep Out			Yes	1		
			Partial I	Mode On, Idle N		Sleep Out			Yes			
				Sleep	In				Yes	i		
		Γ	Status				Defau	It Value (D7	to D0)			
		- 1		n Sequence			All pix					
Default			S/W Res				All pix					
			H/W Res	set			All pix	el off				
							٢-	 ·	¬			
							- 1	Legen	d			
									-			
					isplay Mod	e		Comma	nd			
					On		- 1/	Paramet	er/			
Flow Chart					¥	1	<u> </u>	Displa	y ,			
I low onait				ALLP	OFF(22h)			Action	<u> </u>			
					*		ĺ,					
				Black	Display		1 (Mode	i			
							! [Sequent transfe				
								- Hunsie				
									'			



12.2.21 ALLPON (23h/2300h): All Pixel ON

23H			,	30011). All F		ALLF	ON							
2311		۸۵	dress		Ī	ALLF	ON	1		l	l			
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
ALLPOFF	W	23h	2300h	Х				No Arg	gument					
				display panel w			ode and a		he Displa	y On/Off re	egister ca	n be on or		
Description								Display						
				l Display Mode				eave this m	ode. The	display pai	nel			
				ta after "Norma										
Restriction	This cor	nmand	has no ef	fect when modu	ule is alrea	dy in all Pi	xel On m	ode.						
		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register				Mode On, Idle I					Yes					
availability			Partial I	Mode On, Idle N	Mode Off, S	Sleep Out			Yes	i				
			Partial I	Mode On, Idle N	Лode On, S		Yes							
				Sleep	In				Yes					
		Ī	Status				Default	: Value (D7	to D0)					
		ľ		n Sequence			All Pixe		10 00)					
Default			S/W Res				All Pixe							
		İ	H/W Res				All Pixe							
Flow Chart				ALLF	Display Mode On PON(23h)			Legend Comman Paramet Display Action Mode Sequentitransfe	er					



12.2.22 GAMSET (26h/2600h): Gamma Set

26H						GAM	SET					
		Add	dress									
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
GAMSET	W	23h	2300h	Х						GC	[3:0]	
	This co	mmand	is used to	select the des	ired Gamm	na curve fo	r the cu	rrent display	. A maximu	ım of 4 cu	rves can b	ре
	selected	d. The c	curve is sel	ected by settir	ng the appr	opriate bit	in the pa	arameter as	described	in the Tab	ole.	
				GC[3:0]	Para	ameter		Curve Se	elected			
Description				01h	G	GC0 Gamma Curve 1 (G=2.			e 1 (G=2.2)		
Bosonphon				02h	G	GC1		Reser	ved			
				04h	G	C2		Reser				
				08h	G	GC3		Reser	ved			
	Note :All	Note :All other values are undefined.										
Restriction			7:0] not sh	own in table a	bove are in	valid and	will not o	change the	current sele	ected gam	ma curve	until valid
	is receiv	ved.										
				Stati	IIS				Availab	ility		
			Normal N	Node On, Idle		Sleep Out			Yes	inty		
Register				Node On, Idle					Yes			
availability				lode On, Idle					Yes			
			Partial M	lode On, Idle I	Mode On, S	Sleep Out			Yes			
				Sleep) In				Yes			
			01-1				Defe	-li V-li - (D=	/ I - DO)			
			Status O	Coguence			Rese	ılt Value (D7	to D0)			
Default			S/W Res	Sequence			Rese					
			H/W Res				Rese					
		J	,									
							r —		. — ¬			
							i I	Legend	i			
					MCCT/OCK		i		1			
				_ GA	MSET(26h	1)	i⊆	Comman	ı I			
							1/	Paramete	<u></u>			
					GC[3:0]		1_					
Flow Chart					\downarrow		i	Display	/			
					ew Gamma	!<	Action	>¦				
	Curve Loaded Mode								\neg i			
								Sequentia				
							i	transfer				
							∟ .		I			



12.2.23 DISPOFF (28h/2800h): Display Off

28H						DISP	OFF					
In at / Dana	DAA	Ad	dress	D45.0	D.7	Do	Dr	D.4	Do	Do	D4	Do
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	W	28h	2800h	Χ				No Arg	jument			
	This co	mmand	is used to	enter into DISI	PLAY OFF	mode. In t	his mode	, the displa	ıy data is d	lisables ar	nd blank p	age
	inserted	d.										
	This co	mmand	does not	change any oth	er status .	There will b	ne no abr	normal visih	ole effect o	n the disn	lav	
	11110 00	mmana	4000 1101	onango any oan	or otatao.		70 110 abi		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	ii iiio diop	.ay.	
Description						П	. П	Display				
						# ,	$\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $					
				F		# 🖳	₁ <i>〉</i>					
				E		\blacksquare	$^{ u}$ \exists					
Restriction	This co	mmand	has no ef	fect when modu	ıle is alrea	dy in Displ	ay Off mo	ode.				
				Statu	ıs				Availab	ility		
			Normal	Mode On, Idle I	Mode Off,	Sleep Out			Yes			
Register			Normal	Mode On, Idle I	Mode On,	Sleep Out			Yes			
availability			Partial I	Mode On, Idle N	Node Off, S	Sleep Out			Yes			
			Partial I	Mode On, Idle N	∕lode On, S	Sleep Out			Yes			
				Sleep	In				Yes			
			Status				Default	t Value (D7	to D0\			
				n Sequence			Display		10 00)			
Default			S/W Res				Display					
			H/W Res				Display					
		I	.,				2.00.00	,				
							r -					
							 	Legen	i İ			
							i					
							iſ	Comma	nd I			
				Display	On Mode		. – I /	Paramet	er /			
					\downarrow	/ ¬	i [∠]					
Flow Chart				DISPO	OFF(28h)		1	Display	<u>/) </u>			
					Ţ	_		Action	\rightarrow !			
				Dieploy	Off Mode		1	Mode				
				Display	OII IVIOUE							
								Sequent: transfe				
									$\overline{}$			
									'			



12.2.24 DISPON (29h/2900h): Display On

29H						DISF	ON					
	D 444	Add	dress	5.15.0				5.	5.0			D 0
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	W	29h	2900h	Χ				No Arg	gument			
	This co	mmand	is used to	enter into DISI	PLAY OFF	mode. In t	this mode	e, the displa	y data is o	disables ar	nd blank p	age
	inserted	d.										
	This co	mmand	does not	change any oth	er status.	There will I	be no abr	normal visib	ole effect o	n the disp	lay.	
Description								Display				
·				Е		B	ν Н		3			
						\sharp \sqsubset	,					
							$V \mid \exists$		3			
							Ц					
Restriction	This co	mmand	has no ef	fect when modu	ule is alrea	dy in Displ	ay Off mo	ode.				
				Statu	10				Availab	ility		
			Normal	Mode On, Idle I		Sleen Out			Yes			
Register				Mode On, Idle I					Yes			
availability				Mode On, Idle N					Yes			
			Partial I	Mode On, Idle N	∕lode On, S	Sleep Out			Yes			
				Sleep	In				Yes			
		Ī	Status				Dofaul	t Value (D7	to DO)			
		ľ		n Sequence			Display		10 00)			
Default		Ì	S/W Res				Display					
			H/W Res	set			Display					
		_										
							Γ-		¬			
							ĺ	Legen	d			
							_ ا					
				Dienlas	Off Mode			Comma	nd l			
				Display	T Wiode		- 1/	Paramet	er			
Flow Chart					<u> </u>	1	\ \ (Displa	y i			
1 low Griant				DISP	ON(29h)			Action	<u> </u>			
					<u> </u>		į,					
				Display	On Mode)	1	Mode)			
							! [Sequent transfe				
								- Hunste	·			
									'			



12.2.25 TEOFF (34h/3400h):Tearing Effect Line OFF

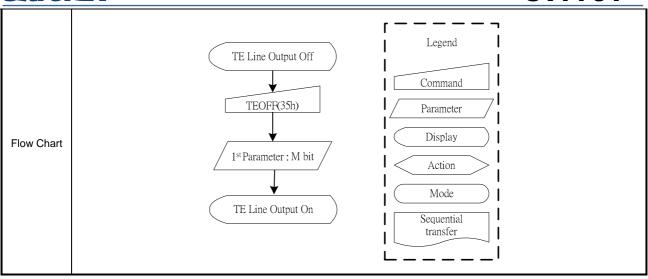
34H		,		oon). I caring		TEC	FF					
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
TEOFF	W	34h	3400h	Х				No Arg	gument			
Description	This co	mmand	is used to	turn off the Dis	play modu	ıle's Tearin	g Effect o	utput signa	al (Active I	_ow) on th	e TE signa	al line.
Restriction	This co	mmand	has no ef	fect when the Te	earing Effe	ct output i	s already	OFF.				
Register availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes										
Default	Status Default Value (D7 to D0) Power On Sequence 00h S/W Reset 00h H/W Reset 00h											
Flow Chart				TEO	Output On FF(34h) Output OFF			Legend Comma Paramet Display Action Mode Sequent transfe	nd I			



12.2.26 TEON (35h/3500h):Tearing Effect Line ON

35H	TEON											
Inst / Para	R/W	Add	lress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
IIISt/Fala	IX/VV	MIPI	SPI-16	D13-6	D1	D0	D3	D4	D3	DZ	Di	DO
TEOFF	W	35h	3500h	Х								М
	This cor	mmand i	s used to	turn ON the Tea	aring Effec	t output si	gnal on th	e TE signa	al line. Cha	anging the	MADCTL	bit B4 will
	not affe	ct this o	utput. The	e Tearing Effect	Line On h	as one par	ameter, w	hich descr	ibes the n	node of the	e Tearing E	Effect
	Output	Line.										
	When M	1 = 0: Th	ne Tearing	g Effect Output li	ne consis	ts of V-Bla	nking info	rmation on	ly:			
				l_			T_{vdl}			T _{vdh}	_	
Description	Vertica	Il time s	scale									
	When M	1 = 1: Th	ne Tearinç	g Effect Output L	ine consis	sts of both	V-Blankin	g and H-B	lanking inf	ormation:	·	
							T_{vdl}			T _{vdh}	•	
	Vertica	ıl time s	scale				vai			Van	\rightarrow	
	Note: D	uring the	e Sleep Ir	n Mode with Tea	ring Effect	Line On,	Гearing Ef	fect Outpu	ıt pin will b	e active L	ow.	
Restriction	This cor	mmand l	has no ef	fect when the Te	earing Effe	ct output is	s already	OFF.				
				Statu					Availab	-		
5				Mode On, Idle N					Yes			
Register availability				Mode On, Idle M					Yes Yes			
avaliability				Mode On, Idle M					Yes			
			T ditidi	Sleep		лоор очт			Yes			
				·			ı				ļ	
							1				_	
		ŀ	Status					Value (D7	to D0)			
Default		-		n Sequence			00h				_	
			S/W Res				00h				_	
		L	H/W Res	set			00h					

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12.2.27 MADCTL(36h/3600h): Display data access control

36H						IDMO	OFF								
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
IDMOFF	W	36h	3600h	X				ML	BGR						
	ML: GE	T Scan	direction	selection.		•		•	•	•		•			
	ML= 0 G	et norr	mal scan.												
	ML=1 G	et reve	rse scan.												
Description	BGR:														
	BGR=0	→RGB	3												
	BGR=1	→ BGR	1												
Restriction	This con	nmand	has no ef	fect when modu	ıle is alrea	dy in Idle (Off mode								
												İ			
		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes													
Register		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes													
availability		Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes													
			Partial	Mode On, Idle N	/lode On, S	Sleep Out			Yes	i					
				Sleep	In				Yes	i					
		I	Status				Defaul	t Value (D7	' to D0)						
Datault				n Sequence			00H	,	,						
Default			S/W Res	set			00H								
			H/W Re	set			00H								
Flow Chart	Legend ML=0 / BGR=0 Parameter Display Action Revese scan/BGR Mode Sequential transfer														



12.2.28 IDMOFF (38h/3800h): Idle Mode Off

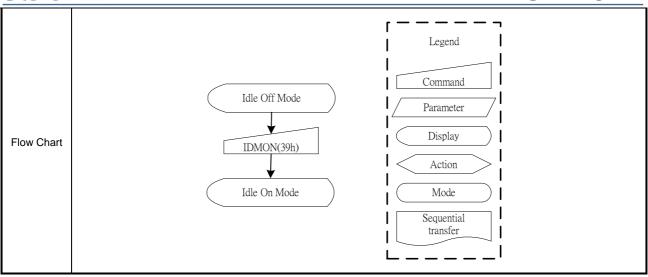
38H						IDMO	OFF							
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
IDMOFF	W	38h	3800h	Х				No Arg	gument	l		1		
	This co	mmand	is used to	recover from Id	dle mode d	on								
Description	In the ic	lle off m	ode, disp	lay panel can di	splay max	imum 16.7	'M colors	S.						
Restriction	This co	mmand	has no ef	fect when modu	ıle is alrea	dy in Idle (Off mode).						
				Statu	ıs				Availab	ility				
			Normal	Mode On, Idle I	Mode Off,	Sleep Out			Yes					
Register			Normal	Mode On, Idle N	Mode On,	Sleep Out			Yes					
availability		Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Yes												
		Partial Mode On, Idle Mode On, Sleep Out Yes												
		Sleep In Yes												
Default		Status Default Value (D7 to D0) Power On Sequence Idle Mode off S/W Reset Idle Mode off H/W Reset Idle Mode off												
Flow Chart				IDMO	On Mode OFF(38h) Off Mode			Comma Paramet Displa Action Mode Sequent transfe	nd I					



12.2.29 IDMON (39h/3900h): Idle Mode On

39H						IDM	ON								
Inst / Para	R/W	Add MIPI	ress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
IDMON	W	39h	3900h	Х				No Arg	gument						
				(Examp	le)Fram	e Data	Ī	Display	<u> </u>						
		Тор	o-Left (_											
	This co	mmand	is used to	enter into Idle	mode on.										
	In the id	dle on m	ode, colo	r expression is	reduced. T	he primary	and the	secondary	colors usi	ng MSB o	f				
Description	each R	ach R, G, and B in Frame Data, 8 color depth data is displayed. Color R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B4 B1 B0													
		Co	lor	R5 R4 R	3 R2 R1 R	0	G5 G4 G	3 G2 G1 G	60	B5 B4 B3	B4 B1 B0				
		Bla	ack	0>	xxxx		0×	xxxx		0x	ххх				
		BI	ue	0>	CXXXX		0×	XXXX		1x)	XXX				
		Re		1>	XXXX		0×	XXXX		0xx	XXX				
		Mag			CXXXX			XXXX			CXXX				
			een		XXXX			XXXX			XXX				
		Cy			(XXXX			XXXX			XXX				
		Yel	nite		(XXXX			XXXX			(XXX				
		VVI	III.G	17			17			17.7					
Restriction	This co	mmand	has no ef	fect when mode	ule is alrea	dy in Idle (On mode.								
				Statu	ıs				Availab	ility					
			Normal	Mode On, Idle	Mode Off,	Sleep Out			Yes						
Register				Mode On, Idle		-			Yes						
availability				Mode On, Idle N					Yes						
,				Mode On, Idle N					Yes						
				Sleep					Yes						
							l l								
			Status				Default	Value (D7	to D0)						
Defects			Power C	n Sequence			Idle Mo	de off							
Default			S/W Res	set			Idle Mo	de off							
			H/W Res	set			Idle Mo	de off							
	I	_													

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12.2.30 COLMOD (3Ah/3A00h): Interface Pixel Format

ЗАН						COL	ИOD							
		Ado	dress											
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
COLMOD	W	3Ah	3A00h	Х			VIPF[2	2:0]						
	This co	mmand	is used to	define the for	mat of RGE	picture da	ata.							
	The form	mats are	e shown in	the table:										
				Bit	NAME			DESCRIF	TION					
Description								"101"=16	-					
				VIPF[2:0]	Pixel Forma	t for RGB Ir	iterface	"110"=18- "111"=24-	•					
									s=not defined	d				
Destriction	Thoro is		blo offoot :	until the dienle	ov doto io un	itton to								
Restriction	THERE IS	S NO VISII	nie eitect (until the displa	ay uala IS W	illen to.								
		Status Availability Normal Mode On Idle Mode Off Sleep Out Yes												
		Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register									Yes					
availability				lode On, Idle					Yes					
			Partial iv	lode On, Idle Slee		sieep Out			Yes Yes					
					<u>r</u>		<u> </u>							
			Status	_				ult Value (E	7 to D0)					
Default		-	Power Or S/W Res	Sequence			70h 70h							
		_	H/W Res				70h							
		L												
							۲.							
				241:	- /- ' 1 N / 1 -		i	Lege	nd					
				24-01	t/pixel Mode		1		!					
						1		Comm	and					
				COI	MOD(3Ah)		- 1/	/ Param	eter /					
Flow Chart					<u> </u>		i (Displ	ay					
				VIPF	arameter [2:0]=" 110"		,	Actio						
					\downarrow		1	Mod	le I					
				18-bi	t/pixel Mode		'	Sequer	;					
								trans	er I					
							Ĺ							



12.2.31 GSL (45h): Get Scan Line

45H						GS	SL						
Inot / Dara	R/W	Add	dress	D15 0	D7	De	DE	D4	D3	D2	D1	DO	
Inst / Para	R/VV	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
GSL	R	45h	4500h	Х				TELS	[15:8]				
		4011	4501h	Χ				TELS	S[7:0]				
	The disp	olay rea	ds the cu	rrent scan line N	N, used to	update the	display	device. The	total num	ber of sca	n lines on	a display	
Description	device i	s define	d as VSY	NC + VBP + VA	ACT + VFF	P. The first :	scan line	is defined	as the first	line of V-S	Sync and is	s denoted	
	as Line	0.											
Restriction													
				Statu	IS				Availab	ility			
				Mode On, Idle I					Yes				
Register				Mode On, Idle I					Yes				
availability		-		Mode On, Idle N					Yes				
		Partial Mode On, Idle Mode On, Sleep Out Sleep In Yes											
				Оісер					103				
			Status				Defau	lt Value (D7	to D0)				
Default		-	Power C	n Sequence			00h						
20.00.1		-	S/W Res				00h						
			H/W Res	set			00h						
Flow Chart				Dumm 2nd Par N[1 3rd Par	(45h) y Read rameter 5:8] rameter 7:0]		Host Driver	Pa Ccc Pa	egend ommand rameter Display Action Mode quential ransfer	7			



12.2.32 WRDISBV (51h): Write Display Brightness

51H						WRDI	SBV								
Inst / Para	R/W	Add MIPI	ress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
WRDISBV	W	51h	5100h	Х		1		DBV	/ [7:0]		ı	1			
	This cor	nmand i	is used to	adjust the brig	htness val	ue of the d	isplay.								
	It should	be che	cked wha	at the relationsh	ip betweei	n this writte	en value a	and output	brightness	of the dis	play is. Th	is			
Description	relations	ship is d	efined on	the display mo	dule speci	fication.									
				s that 00h value			rightness	and FFh va	alue mean	s the high	est brightn	ess.			
Restriction	The disp	olay sup	plier can	not use this con	nmand for	tuning (e.g	j. factory	tuning, etc.).						
				2: :											
		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes													
Register		Normal Mode On, Idle Mode On, Sleep Out Yes													
availability		·													
		· · · · · · · · · · · · · · · · · · ·													
		Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
		П	Otatus				Default	. \ /ala /D7	t- D0\						
		- 1	Status Power C	n Sequence			00h	: Value (D7	10 DU)						
Default		ŀ	S/W Res	-			00h								
		Ī	H/W Res	set			00h								
		_													
Flow Chart				Par	Ameter DBV	[[7:0]	7	Legend Comman Paramete Display Action Mode Sequenti- transfer							



12.2.33 RDDISBV (52h/5200h): Read Display Brightness Value

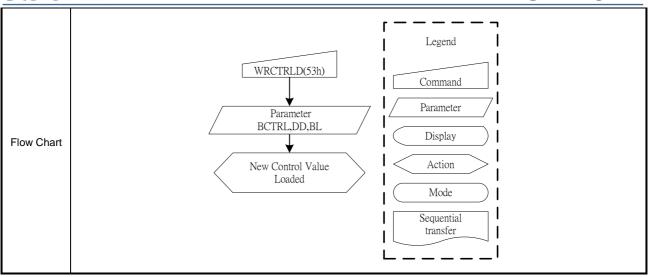
52H						RDDI	SBV							
		Add	dress											
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
WRDISBV	R	52h	5200h	X				DBV	/[7:0]					
	This co	mmand	returns th	e brightness va	lue of the	display.								
	It shoul	d be che	ecked wha	at the relationsh	ip betweer	n this retur	ned value	and outpu	ut brightne	ss of the d	lisplay. Th	is		
	relation	ship is c	lefined on	the display mo	dule speci	fication is.								
Description	In princ	iple the	relationsh	ip is that 00h va	alue mean	s the lowes	st brightne	ess and FF	h value m	eans the h	nighest bri	ghtness.		
	DBV[7:	0] is res	et when d	isplay is in slee	p in mode.									
	DBV[7:	0] is '0' v	when bit E	CTRL of write (CTRL disp	ay comma	ind (53h)	is '0'						
	DBV[7:	0] IS ma	ınual set b	orightness speci	fied with w	rite CTRL	display c	ommand (53h) when	bit BCTR	L is '1'			
Restriction														
				Statu					Availab	-				
D				Mode On, Idle M		-			Yes					
Register availability		Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Yes Yes												
availability				Mode On, Idle N					Yes					
				Sleep					Yes					
		ī												
		ŀ	Status	n Coguenea				Value (D7	to D0)					
Default		-	S/W Res	n Sequence			00h 00h							
		ŀ	H/W Res				00h							
														
						<u> </u>	۱ –		¬	·	·			
							İ	Legend	l [
				F	RDDISB(52l	1)	1_							
						Ho Driv		Comman	nd I					
				Se	end Parame		<u> </u>	Paramete	er /					
Flow Chart					DBV[7:0]	/	` ¦ (Display	· i					
Tion Grian							i <	Action	<u> </u>					
									\leq !					
								Mode						
								Sequenti: transfer						
									i					
								_	_ _					



12.2.34 WRCTRLD (53h/5300h): Write CTRL Display

53H						WRC ⁻	ΓRLD								
Inst / Para	R/W	Add	lress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
IIISt/ I ala	17/77	MIPI	SPI-16	D13-0	<i>D1</i>	D0	D3	D4	D3	D2	Di				
WRCTRLD	W	53h	5300h	X			BCTRL		DD	BL					
	This cor	mmand	is used to	control display	brightnes	S.									
	BCTRL:	Brightn	ess Cont	trol Block On/Off	, This bit i	s always ι	sed to swi	tch brightr	ness for di	splay.					
	0 = Off ((Brightn	ess regis	ter are 00h, DB\	/[7:0])										
	1 = On	(Brightn	ess regis	ter are active, a	ccording to	the other	paramete	rs.)							
	DD: Dis	play Din	nming (O	nly for manual b	rightness	setting)									
	DD = 0:	Display	Dimming	g is off.											
Description	DD = 1:	Display	Dimmino	g is on.											
	BL: Bac	klight C	ontrol On	/Off											
	0 = Off ((Comple	etely turn	off backlight circ	uit. Contr	ol lines mu	st be low.)								
	1 = On	On													
	Dimmin														
		en BL bit changed from 'on' to 'off', backlight is turned off without gradual dimming, even if dimming-on (DD=1) are													
	selected			,	g				g,		9 (.,			
5	30100100														
Restriction															
				Statu	e				Availab	ility					
			Normal	Mode On, Idle N		Sleep Out			Yes	-					
Register				Mode On, Idle N					Yes						
availability			Partial	Mode On, Idle N	Node Off,	Sleep Out			Yes						
			Partial	Mode On, Idle N	lode On,	Sleep Out			Yes						
				Sleep	In				Yes						
		Г	a				5 ()	(5-	. 50)						
		-	Status	n Coguenos				Value (D7	to D0)						
Default		-	S/W Res	On Sequence			00h 00h								
			H/W Res				00h								
H/W Reset 00n															
<u> </u>	I.														

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12.2.35 RDCTRLD (54h): Read CTRL Value Display

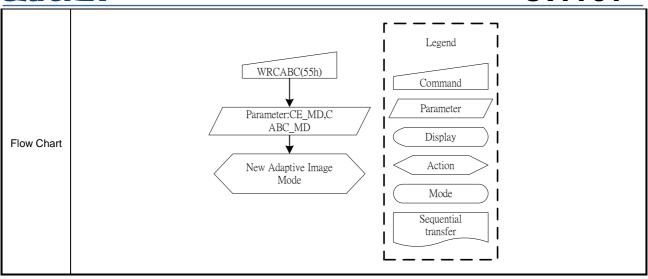
54H						WRC ⁻	ΓRLD								
		Add	dress												
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
RDCTRLD	R	54h	5400h	X			BCTRL		DD	BL					
	This con	nmand	returns a	mbient light and	brightnes	s control v	alues								
	BCTRL:	Brighti	ness Cont	rol Block On/Off	, This bit	is always ι	ised to sw	itch brighti	ness for di	splay.					
	0 = Off		1 = On												
Description	DD: Disp	olay Dii	mming (O	nly for manual b	rightness	setting)									
	DD = 0		DD = 1												
	BL: Back	klight C	Control On	/Off											
	0 = Off		1 = On												
Restriction															
		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes													
Register		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes													
availability															
,				Mode On, Idle M					Yes						
				Sleep	In				Yes						
			Ctatus				Default	Value (D7	to DO						
			Status Power C	n Sequence			00h	Value (D7	נט טט)						
Default			S/W Res				00h								
			H/W Res	set			00h								
Flow Chart					end Parame	Driv ter		Legend Commar Paramete Display Action Mode Sequenti transfer	er						



12.2.36 WRCACE (55h/5500h): Write Content Adaptive Brightness Control and Color Enhancement

55H						WR	CACE					
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
WRCACE	W	MIPI 55h	SPI-16 5500h	X	CE_ON		CEM	 D[1:0]			CARC	MD[1:0]
WINCAGE			1	o set parameter		l	1					
		ement f									,	
				ncement on	CE ON:	-"0" Colo	· enhancem	ent off				
				hancement leve			Ciliancen	icht on				
				CEMD[1]	CEMD[0]		Function					
				0	0		Low enhan	cement				
				0	1		Medium en	hancemer	nt			
Description				1	1		High enhar	cement				
	There is	s possib	le to use	d 4 different mo	des for cor	ntent adap	otive image	functional	ity, which	are define	d on a tab	le
	below.											
		CABC_MD[1] CABC_MD[0] Function										
				0	0		Off					
				0	1		User Interf	ace Mode				
				1	0		Still Picture)				
				1	1		Moving Im	age				
Restriction					•	•						
				Stati					Availab	-		
Register				Mode On, Idle Mode On, Idle					Yes Yes			
availability				Mode On, Idle I					Yes			
				Mode On, Idle I					Yes			
				Sleep	ln				Yes			
	Status Default Value (D7 to D0)											
		ľ		On Sequence			00h	10.1010 (2.1	10 2 0)			
Default			S/W Re	set			00h					
			H/W Re	set			00h					

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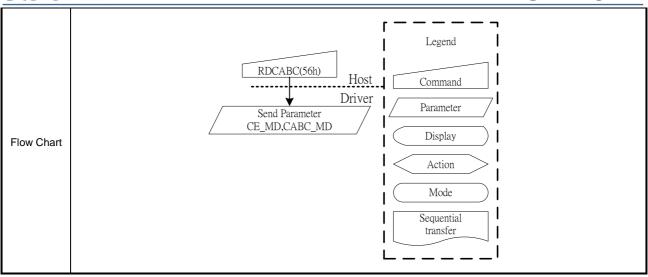
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12.2.37 RDCABC (56h/5600h): Read Content Adaptive Brightness Control

56H						RDO	CABC					
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
Inst / Para	R/VV	MIPI	SPI-16	D15-6	D7	Do	D5	D4	DS	DZ	וט	БО
RDCABC	R	56h	5600h	X	CE_ON		CEM	D[1:0]			CABC_	MD[1:0]
	This co	mmand	is used t	o read the settir	ngs for ima	ge conter	nt based ac	laptive brig	htness co	ntrol funct	ionality.	
	CE_ON	l="1",Co	lor enhai	ncement on	CE_ON:	="0",Colo	r enhancer	nent off				
	There a	re three	e color en	hancement leve	els can be s	set.						
				CEMD[1]	CEMD[0]		Function					
				0	0		Low enhar	cement				
				0	1		Medium er	hancemer	nt			
				1	1		High enha	ncement				
Description	There is	s possib	le to use	d 4 different mo	des for cor	ntent adap	otive image	functional	ity, which	are define	d on a tab	le
	below.											
				CABC_MD[1]	CABC_N	MD[0]	Function					
				0	0		Off					
				0	1		User Inter	face Mode				
				1	0		Still Pictur	е				
				1	1		Moving Im	age				
	'-': Don'	t care										
Restriction												
				Stat					Availab	-		
Desiletes				Mode On, Idle					Yes			
Register availability				Mode On, Idle Mode On, Idle					Yes Yes			
a.raa				Mode On, Idle					Yes			
				Sleep					Yes			
	Status Default Value (D7 to D0)											
		ŀ	Status Power (On Sequence			00h	value (D7	to D0)			
Default		ŀ	S/W Re				00h					
		ļ	H/W Re				00h					
							•					

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12.2.38 WRCABCMB (5Eh/5E00h): Write CABC Minimum Brightness

5EH						WRCAE	BCMB							
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
WRCABCMB	W	5Eh	5E00h	Х		1		CME	3[7:0]	I	I	ı		
	This con	nmand	is used to	set the minimu	m brightn	ess value o	f the disp	lay for CAI	BC functio	n.				
Description	In princip	ole rela	itionship is	s that 00h value	means th	e lowest br	ightness t	for CABC a	and FFh va	alue mear	s the brig	htness for		
	CABC.													
Restriction														
				Statu					Availab	ility				
		-		Mode On, Idle I					Yes					
Register availability				Mode On, Idle Mode On, Idle M		-			Yes Yes					
availability														
		Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
		Ī	Status				Default	Value (D7	to D0)					
Default			Power C	n Sequence			00h							
Delault		-	S/W Res				00h							
			H/W Re	set			00h							
Flow Chart				Pa New I	CABCME(arameter:CN Display Lun Value Loade	MB /	7	Commar Paramete Display Action Mode Sequenti transfer	ad ad ad ad ad ad ad ad					



12.2.39 RDCABCMB (5Fh/5F00h): Read CABC Minimum Brightness

5FH						WRCA	ВСМВ								
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
WRCABCMB	R	5Fh	5F00h	Х				CME	B[7:0]	I	I	,			
	This cor	nmand	returns th	ne minimum brig	htness va	lue of CAB	C function	١.							
Description	In princi	ple rela	itionship is	s that 00h value	means th	e lowest br	ightness f	or CABC a	and FFh va	alue mean	s the brigl	ntness for			
	CABC.														
Restriction															
				Statu	ıs				Availab	ility					
			Normal			Sleep Out									
Register		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes													
availability		· · · · · · · · · · · · · · · · · · ·													
		Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes													
		Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default															
Flow Chart	H/W Reset Description Legend														



12.2.40 RDABCSDR (68h/6800h): Read Automatic Brightness Control Self-Diagnostic Result

68H						WRCA	BCMB								
		Add	dress												
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
WRCABCMB	R	68h	6800h	Χ	RLD	FUND									
Description	sleep ou -RLD: Re	t -comi egister Functic				e display s	elf-diagn	ostic result	s for auto	matic brig	htness co	ontrol after			
Restriction															
Register availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default	Status Default Value (D7 to D0) Power On Sequence 00h S/W Reset 00h H/W Reset 00h														
Flow Chart															



12.2.41 RDBWLB (70h/7000h):Read Black/White Low Bits

70H						RDB\	NLB							
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDBWLB	R	70h	7000h	Х	BKx1	BKx0	BKy1	BKy0	Wx1	Wx0	Wy1	Wy0		
	This cor	mmand	reads the	e lowest bits of b	lack and v	vhite color	characte	istics.						
Description	Black: E	8kx and	Bky											
	White: \	Vx and	Wy											
Restriction														
				Statu	IS				Availab	ility				
			Normal	Mode On, Idle I		Sleep Out			Yes					
Register			Normal	Mode On, Idle I	Mode On,	Sleep Out			Yes					
availability			Partial	Mode On, Idle N	Node Off, S	Sleep Out			Yes					
			Partial	Mode On, Idle N		Sleep Out			Yes					
				Sleep	In				Yes					
Default		Status Default Value (D7 to D0) Power On Sequence XXh S/W Reset XXh H/W Reset XXh												
Flow Chart			2	Send 1st 1	LB(70h) Parameter Parameter		Host Driver	Co Pa Pa Pa Pa Pa Pa Pa Pa Pa Pa Pa Pa Pa	mmand rameter visplay Action Mode quential ansfer	7 7 7 7 7 7 7 7 7 7				



12.2.42 RDBkx (71h/7100h):Read Bkx

71H			•	oon,caa E		RDI	3kx							
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDBkx	R	71h	7100h	Х				BKx	[9:2]					
Description	This co	mmand	reads the	Bkx bits (Bkx [9:2]) of bla	ick color cl	naracterist	ics.						
Restriction	Only the	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not se	nt.						
Register availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value (D7 to D0)												
Default														
Flow Chart			2	Send 1st 1	9:2](71h) Parameter Parameter		Host Driver	Co Pau	egend mmand rameter risplay Action Mode quential ansfer	7				



12.2.43 RDBky (72h/7200h):Read Bky

72H						RDI	Зky						
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDBky	R	72h	7200h	Х		'		ВКу	[9:2]	•			
Description	This co	mmand	reads the	Bkx bits (Bky [9:2]) of bla	ick color cl	naracteristi	ics.					
Restriction	Only the	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not ser	nt.					
Register availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default		Status Default Value (D7 to D0) Power On Sequence XXh S/W Reset XXh H/W Reset XXh											



12.2.44 RDWx (73h/7300h):Read Wx

73H						RD'	Иx							
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDWx	R	72h	7200h	Х				Wx[9:2]					
Description	This co	mmand	reads the	Wx bits (Bky [9):2]) of bla	ck color ch	aracteristi	cs.						
Restriction	Only th	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not ser	nt.						
Register availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default	Status Default Value (D7 to D0) Power On Sequence XXh S/W Reset XXh H/W Reset XXh													



12.2.45 RDWy (74h/7400h):Read Wy

74H						RD'	Ny						
Inst / Para	R/W	Add MIPI	ress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDWy	R	74h	7400h	X				l Wy[9:2]				
Description		mmand	reads the	Wx bits (Bky [9	9:2]) of blad	ck color ch	aracteristi		-				
Restriction	Only th	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not sei	nt.					
Register availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default	Status Default Value (D7 to D0) Power On Sequence XXh S/W Reset XXh H/W Reset XXh												



12.2.46 RDRGLB (75h/7500h):Read Red/Green Low Bits

75H						RDR	GLB							
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDRGLB	R	MIPI 75h	SPI-16 7500h	X	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0		
KDKOLD				e lowest bits of re	l				OXI	O A O	- Cy i	Oyo		
Description	Red: Rx				g									
	Green:	Gx and	Gy											
Restriction	Only the	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not se	nt.						
		Status Availability												
		Status Availability												
		Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register				Mode On, Idle I		-			Yes					
availability				Mode On, Idle N					Yes					
			Partial	Mode On, Idle N		Sleep Out			Yes					
				Sleep	In				Yes					
Default	Status Default Value (D7 to D0) Power On Sequence XXh S/W Reset XXh H/W Reset XXh													



12.2.47 RDRx (76h/7600h):Read Rx

76H						RD	Rx								
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
		MIPI	SPI-16												
RDRx	R	76h	7600h	Χ				Rx[9:2]						
Description	This co	mmand	reads the	Rx bits (Rx [9:2	2]) of red (color chara	cteristics.								
Restriction	Only th	e 2nd pa	arameter i	s sent on the D	SI; the 1st	t paramete	r is not ser	nt.							
		Status Availability Normal Mode On Idle Mode Off, Sleep Out Yes													
			Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register			Normal Mode On, Idle Mode On, Sleep Out Yes												
availability			Partial	Mode On, Idle N	Mode Off,	Sleep Out			Yes						
			Partial	Mode On, Idle N	Mode On,	Sleep Out			Yes						
				Sleep	ln .				Yes						
Default			Status Power C S/W Res				Default XXh XXh XXh	Value (D7	to D0)						



12.2.48 RDRy (77h/7700h):Read Ry

77H						RD	Ry								
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
		MIPI	SPI-16												
RDRy	R	77h	7700h	Х				Ry[9:2]						
Description	This co	mmand	reads the	Rx bits (Ry [9:2	2]) of red o	color chara	cteristics.								
Restriction	Only the	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not ser	nt.							
		Status Availability Normal Mode On Idle Mode Off Sleep Out													
		Normal Mode On, Idle Mode Off, Sleep Out Yes													
Register			Normal Mode On, Idle Mode On, Sleep Out Yes												
availability		Partial Mode On, Idle Mode Off, Sleep Out Yes Yes													
			Partial	Mode On, Idle N	/lode On,	Sleep Out			Yes						
				Sleep	In				Yes						
Default			Status Power C S/W Res				Default XXh XXh XXh	Value (D7	to D0)						



12.2.49 RDGx (78h/7800h):Read Gx

78H						RD	Gx								
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
mot / r ara		MIPI	SPI-16	<i>D</i> 10 0	J.	50	50	<u> </u>			J.				
RDGx	R	77h	7700h	Х				Gx[9:2]						
Description	This co	mmand	reads the	Rx bits (Gx [9:2	2]) of red (color chara	cteristics.								
Restriction	Only th	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not ser	nt.							
			Status Availability Normal Mode On Idle Mode Off Sleep Out Yes												
			Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register			Normal Mode On, Idle Mode On, Sleep Out Yes												
availability			Partial Mode On, Idle Mode Off, Sleep Out Yes Yes												
			Partial	Mode On, Idle N	Mode On,	Sleep Out			Yes						
				Sleep	In				Yes						
Default			Status Power C S/W Res				Default XXh XXh XXh	Value (D7	to D0)						



12.2.50 RDGy (79h/7900h):Read Gy

79H						RD	Gy						
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDGy	R	79h	7900h	Х				Gy[9:2]				
Description	This co	mmand	reads the	Gx bits (Gx [9:2	2]) of red (color chara	cteristics.						
Restriction	Only the	e 2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not ser	nt.					
Register availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default		Status Default Value (D7 to D0) Power On Sequence S/W Reset H/W Reset XXh XXh											



12.2.51 RDBALB (7Ah/7A00h):Read Blue/A Color Low Bits

7AH						RDB	ALB								
Inst / Para	R/W		lress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
RDBALB	R	MIPI 7Ah	SPI-16 7A00h	X	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0			
NOBALD	·		l I	lowest bits of b	l	L			AXI	700	- Ay i	Ayo			
Description	Blue: Bx and By														
	A color: Ax and Ay														
Restriction	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.														
	Status Availability														
			Normal	Mode On, Idle N		Sloop Out		Yes							
D'(
Register				Mode On, Idle I		•			Yes						
availability				Mode On, Idle N					Yes						
			Partial	Mode On, Idle N		Sleep Out		Yes							
				Sleep	In			Yes							
		Ī	Status				Defaul	efault Value (D7 to D0)							
									XXh						
Default		ŀ	S/W Reset XXh												
		ľ	H/W Res				XXh								
		L					1								



12.2.52 RDBx (7Bh/7B00h):Read Bx

7BH						RD	Вх								
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
		MIPI	SPI-16												
RDBx	R	7Bh	7B00h	X		Bx[9:2]									
Description	This co	This command reads the Bx bits (Bx [9:2]) of red color characteristics.													
Restriction	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.														
		Status Availability													
	Normal Mode On, Idle Mode Off, Sleep Out Yes														
Register			Normal	Mode On, Idle I	Mode On,	Sleep Out			Yes						
availability			Partial	Mode On, Idle N	/lode Off, S	Sleep Out			Yes						
			Partial	Mode On, Idle N	/lode On, S	Sleep Out			Yes						
			Sleep In						Yes						
											,				
		r									_				
		l	Status				Default								
Default			Power C	n Sequence			XXh								
Dolault			S/W Reset					XXh							
			H/W Reset XXI						Xh						
		_													



12.2.53 RDBy (7Ch/7C00h):Read By

7CH						RD	Ву							
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDBx	R	7Ch	7C00h	Х	X By[9:2]									
Description	This co	This command reads the By bits (By [9:2]) of red color characteristics.												
Restriction	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.													
Register availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default			Status Power C S/W Res				Default XXh XXh XXh	Value (D7	to D0)					



12.2.54 RDAx (7Dh/7D00h):Read Ax

7DH						RD	Ax							
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDAx	R	7Dh	7D00h	Х	Ax[9:2]									
Description	This co	This command reads the Ax bits (Ax [9:2]) of red color characteristics.												
Restriction	Only th	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.												
Register availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default			Status Power C S/W Rea H/W Re				Default XXh XXh XXh	Value (D7	to D0)					



12.2.55 RDAy (7Eh/7E00h):Read Ay

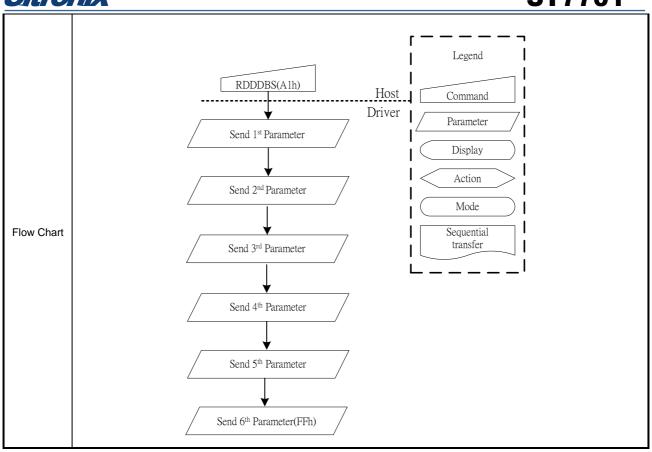
7EH						RD	Ay								
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
DDA		MIPI	SPI-16	V				Δ	0.01						
RDAy	R	7Dh	7D00h	Х		Ay[9:2]									
Description	This co	nis command reads the Ay bits (Ay [9:2]) of red color characteristics.													
Restriction	Only th	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.													
	Status Availability														
			Managal			Class Out			Yes	ility					
				Mode On, Idle I		•									
Register		-		Mode On, Idle I		•			Yes						
availability				Mode On, Idle N				Yes							
			Partial	Mode On, Idle N	/lode On, :	Sleep Out		Yes							
				Sleep	In			Yes							
			Status				Default	Value (D7	to D0)						
Defects			Power C	n Sequence			XXh								
Default			S/W Res	set			XXh								
			H/W Re	set			XXh	XXh							
		•		_											



12.2.56 RDDDBS (A1h/A100h): Read DDB Start

A1H						RDDI	OBS							
Inot / Doro	R/W	Add	lress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
Inst / Para	K/VV	MIPI	SPI-16	ס-כוע	יט	סט	DЭ	D4	D3	DZ	וט	DU		
			A100h					0x	77					
			A101h		0x01									
RDDDBS	R	A1h	A102h	Χ				MID[15:8]					
			A103h					MID	[7:0]					
			A104h					8'I	nff					
	This cor	mmand	reads the	supplier identifi	cation and	d display m	odule mod	de/revisior	n information	on.				
	Parame	ter 1: th	e ID of IC	C.(0x77).										
	Parame	rameter 2: the ID of IC.(0x01).												
	Parame	ameter 3: MRID [7:0] LCD module/driver ID.												
	Parame	ter 4: M	RID [15:8	B] IC version cod	le.									
Description	Parame	ter 5: F	Fh - Exit	code – there is r	o more da	ata in the D	escriptor	Block						
	This rea	ıd sequ	ence can	be interrupted b	y any con	nmand and	it can be	continued	by the Re	ad DDB C	ontinue (A	۸8h)		
	command.													
	For example, RDDDBS => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC =>													
	3rd para	ameter o	of the RD	DDBS has been	sent.									
Restriction														
				Statu	S		Availability							
			Normal	Mode On, Idle N	∕lode Off,	Sleep Out			Yes					
Register			Normal	Mode On, Idle M	Mode On,	Sleep Out			Yes					
availability			Partial	Mode On, Idle N	lode Off,	Sleep Out			Yes					
			Partial	Mode On, Idle N	lode On,	Sleep Out			Yes					
				Sleep	In				Yes					
			Status				Default	Value (D7	to D(1)					
		ľ		On Sequence			XXh	(21						
Default		ŀ	S/W Res				XXh							
	H/W Reset						XXh							
		L					•							

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12.2.57 RDDDBC (A8h/A800h): Read DDB Continue

A8H						RDDI	DBC								
/ D	D.444	Add	dress	D45.0	D.7	D.O.	5.5		D.C.	D.O.	D.4	D.o.			
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
			A800h					SID[15:8]						
			A801h					SID[[7:0]						
RDDDBC	R	A8h	A802h	Χ				MID[15:8]						
			A803h			MID[7:0]									
			A804h					8'l	nff						
Description				o read the suppler command.	ier's identi	fication an	d revisio	n informatio	n from the	point whe	ere RDDD	BS (A1h)			
Restriction															
												1			
				Statu	ıs				Availab	ility					
			Normal	Mode On, Idle I	Mode Off,	Sleep Out			Yes						
Register			Normal	Mode On, Idle I	Mode On,	Sleep Out			Yes						
availability			Partial	Mode On, Idle N	Node Off,	Sleep Out			Yes						
			Partial	Mode On, Idle N		Sleep Out			Yes						
				Sleep	In				Yes						
Default			Status Power C S/W Res				Default Value (D7 to D0) XXh XXh XXh								
Flow Chart				RDE	DBC(A8h) DBS Data)]Dn[7:0]	Host Driver		Legend Command Parameter Display Action Mode Sequential transfer							



12.2.58 RDFCS (AAh/AA00h): Read First Checksum

AAH						RDF	CS					
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDFCS	R	7Dh	7D00h	Х				FCS	[7:0]		•	
Description				e first checksum gisters and/or Fr				e User's aı	rea and the	e Frame M	lemory aft	er the
Restriction	Only the	2nd pa	arameter	is sent on the D	SI; the 1st	paramete	r is not se	nt.				
Register availability			Normal Partial	Statu Mode On, Idle M Mode On, Idle M Mode On, Idle M Sleep	Mode Off, Mode On, Mode Off, Mode On,	Sleep Out Sleep Out			Availab Yes Yes Yes Yes			
Default			Status Power C S/W Res				Default 00h 00h 00h	Value (D7	to D0)			
Flow Chart			2	Send 1st 1	S(AAh) Parameter CS[7:0]		Host Driver	Co	egend mmand rameter bisplay Action Mode quential ansfer	7 7 7 7 7 7 7 7 7 7		



12.2.59 RDCCS (AFh/AF00h): Read Continue Checksum

					RDC	cs								
R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
R	AFh	AF00h	Х				CCS	S[7:0]	ı		I			
This cor	nmand	reads the	following check	ksum that	is calculate	ed conti	nuously afte	r the first c	hecksum t	from regist	ers of the			
User's a	rea an	d the Frar	ne Memory afte	r the write	access to	those r	egisters and	or Frame I	Memory is	done.				
It is nec	essary	to wait 30	Oms after the la	st write ac	ccess to rec	gisters	of the User's	area befor	re this che	cksum val	ue can be			
read the	first tir	ne.												
Only the	2nd p	arameter	is sent on the D	SI; the 1st	t paramete	r is not	sent.							
			Statu	IS				Availab	ility					
								Yes						
	-				-									
	Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Yes													
	Partial Mode On, Idle Mode On, Sleep Out Sleep In Yes Yes													
	<u> </u>		Sieep	1111		l		162						
		Status				Defa	ult Value (D7	' to D0)						
		Power C	n Sequence			00h								
		S/W Res	set			00h								
		H/W Re	set			00h								
		2	Send 1st 1	Parameter				ommand urameter Display Action Mode quential						
	R This cor User's a It is necessarily read the	R/W MIPI R AFh This command User's area and It is necessary read the first tir	MIPI SPI-16 R AFh AF00h This command reads the User's area and the France It is necessary to wait 30 read the first time. Only the 2nd parameter Normal Normal Partial Partial Status Power C S/W Res	R/W MIPI SPI-16 R AFh AF00h X This command reads the following check User's area and the Frame Memory afte It is necessary to wait 300ms after the laread the first time. Only the 2nd parameter is sent on the D Statt. Normal Mode On, Idle I Partial Mode On, Idle I Partial Mode On, Idle I Sleep Status Power On Sequence S/W Reset H/W Reset RDCC Send 1st	R/W MIPI SPI-16 R AFh AF00h X This command reads the following checksum that User's area and the Frame Memory after the write It is necessary to wait 300ms after the last write acread the first time. Only the 2nd parameter is sent on the DSI; the 1st Status Normal Mode On, Idle Mode Off, Normal Mode On, Idle Mode Off, Partial Mode On, Idle Mode On, Sleep In Status Power On Sequence S/W Reset	R/W Address D15-8 D7 D6 R AFh AF00h X This command reads the following checksum that is calculate User's area and the Frame Memory after the write access to It is necessary to wait 300ms after the last write access to regread the first time. Only the 2nd parameter is sent on the DSI; the 1st parameter Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Sleep In Status Power On Sequence S/W Reset H/W Reset RDCCS(AFh) Send Ist Parameter	R/W MIPI SPI-16 R AFh AF00h X This command reads the following checksum that is calculated continuous area and the Frame Memory after the write access to those relative is necessary to wait 300ms after the last write access to registers area the first time. Only the 2nd parameter is sent on the DSI; the 1st parameter is not Status Normal Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Sleep In Status Power On Sequence Ooh S/W Reset H/W Reset D7 D6 D5 D5 D7 D6 D5 D7 D6 D5 D7 D6 D7 D6 D7 D7 D8 D8 D8 D8 D8 D8 D8 D8	R/W MIPI SPI-16 R AFh AF00h X CCS This command reads the following checksum that is calculated continuously after User's area and the Frame Memory after the write access to those registers and it is necessary to wait 300ms after the last write access to registers of the User's read the first time. Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent. Status Normal Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Sleep In Status Default Value (D77) Power On Sequence S/M Reset O0h H/W Reset Driver Send 1st Parameter Send CCS[7:0]	R/W Address MIPI SPI-16 R AFh AF00h X CCS[7:0] This command reads the following checksum that is calculated continuously after the first or User's area and the Frame Memory after the write access to those registers and/or Frame It is necessary to wait 300ms after the last write access to registers of the User's area beforead the first time. Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent. Status Availab Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Sleep In Yes Sleep In Yes Status Default Value (D7 to D0) Status Default Value (D7 to D0) Power On Sequence 00h S/W Reset 00h H/W Reset Driver Parameter Display Action	R/W	R/W Address MIPI SPI-16 D15-8 D7 D6 D5 D4 D3 D2 D1			



12.2.60 RDID1 (DAh/DA00h): Read ID1

DAH		•		Toony. Iteau		RD	D1					
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDID1	R	DAh	DA00h	Х				ID1	7:0]			
Description	-This re	ad byte	identifies	the LCD modul	e's manuf	acturer.						
Restriction												
Register availability			Normal Partial	Statu Mode On, Idle I Mode On, Idle I Mode On, Idle I Mode On, Idle I Sleep	Mode Off, Mode On, Mode Off, Mode On,	Sleep Out Sleep Out			Availab Yes Yes Yes Yes	ility		
Default			Status Power C S/W Res				Default 00h 00h 00h	Value (D7	to D0)			
Flow Chart			2	Send 1st 1	Parameter D1[7:0]		Host Driver	Co	egend mmand rameter risplay Action Mode quential ansfer	7		



12.2.61 RDID2 (DBh/DB00h): Read ID2

DBH				,		RDI	D2							
		Add	dress	D						-				
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
RDID2	R	DBh	DB00h	Χ				ID2[7:0]					
Description	-This rea	ad byte	identifies	the LCD modul	e's manu	facturer.								
Restriction														
				Statu					Availab	ility				
		-		Mode On, Idle I					Yes					
Register		-		Mode On, Idle I					Yes					
availability				Mode On, Idle N					Yes					
		-	Failiai	Mode On, Idle N		Sieep Out			Yes					
		Sleep In Yes												
Default			Status Power C S/W Res H/W Res				Default 00h 00h 00h	Value (D7	to D0)					
Flow Chart			2	Send 1st 1	2(DBh) Parameter D2[7:0]		Host Driver	Co Pau	mmand rameter isplay Action Mode quential ansfer					



12.2.62 RDID3 (DCh/DC00h): Read ID3

DCH				,		RDI	D3					
Inst / Para	R/W	Add	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RDID3	R	DCh	DC00h	Х				ID3[[7:0]			
Description	-This rea	ad byte	identifies	the LCD modul	e's manu	facturer.						
Restriction												
Register availability			Normal Partial	Statu Mode On, Idle I Mode On, Idle I Mode On, Idle I Mode On, Idle I Sleep	Mode Off, Mode On, Mode Off, Mode On,	Sleep Out Sleep Out			Availab Yes Yes Yes Yes	ility		
Default			Status Power C S/W Res				Default 00h 00h 00h	Value (D7	to D0)			
Flow Chart			2	Send 1st 1	3(DCh) Parameter D3[7:0]		Host Driver	Co Pau	egend mmand rameter risplay action Mode quential ansfer			



12.3 System Function Command Table 2

Instruction	Add	ress	R/W	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
mstruction	MIPI	SPI-16		PINUIVI	70	Do	סט	D4	טט	D2	וט	DO	Function
		FF00h			0	1	1	1	0	1	1	1	
		FF01h			0	0	0	0	0	0	0	1	
CN2BKxSEL	FFh	FF02h	W	5									Command2_BKx Function Selection
		FF03h											
		FF04h			0	0	0	CN2	0	0	0	BKSEL	

Command2_BK0

Lateration	Add	ress	DANIO	DAILINA	D.7	P.O.	5.5	5.4	Do.	P.O.	D4	D.O.	E
Instruction	MIPI	SPI-16	R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
		B000h			AJ0F	P[1:0]	1			VC0	P[3:0]		
		B001h				1			VC4F	P[5:0]			
		B002h			AJ1F	P[1:0]			VC8F	P[5:0]			
		B003h				-	-			VC16P[4:0]			
		B004h								VC24P[4:0]			
		B005h								VC52	P[3:0]		
		B006h							VC80	P[5:0]			
PVGAMCTRL	B0h	B007h	w	16				VC108P[3:0] VC147P[3:0] VC175P[5:0] VC203P[3:0]					Positive Voltage Gamma Control
1 VO/IMOTILE	2011	B008h		10									1 ositive voltage carrina control
		B009h											
		B00Ah								VC20	3P[3:0]		
		B00Bh							,	VC231P[4:0]		
		B00Ch							,	VC239P[4:0]		
		B00Dh			AJ2F	P[1:0]			VC247	7P[5:0]			
		B00Eh						Γ	VC25	IP[5:0]			
		B00Fh			AJ3F	P[1:0]			,	VC255P[4:0]		
		B100h			AJON	V[1:0]				VC0I	N[3:0]		
		B101h							VC4N	N[5:0]			
		B102h			AJ1N	V[1:0]		Γ	VC81	N[5:0]			
		B103h						VC16N[4:0]					
NVGAMCTRL	B1h	B104h	W	16				VC24N[4:0]					Negative Voltage Gamma Control
		B105h						VC52N[3:0]					
		B106h						VC80N[5:0]					
		B107h								VC10	BN[3:0]		
		B108h								VC14	7N[3:0]		

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	Add	Iress											
Instruction	MIPI	SPI-16	R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
		B109h							VC17	5N[5:0]			
		B10Ah								VC20	3N[3:0]		
		B10Bh								VC231N[4:0]		
		B10Ch								VC239N[4:0]		
		B10Dh			AJ2N	N[1:0]			VC247	7N[5:0]			
		B10Eh			1				VC25	1N[5:0]			
		B10Fh			AJ3N	N[1:0]				VC255N[4:0]		
DGMEN	B8	B800h	W	1	0	0	0	DGM_ON	0	0	0	0	Digital Gamma Enable
		B900						P0[7:0]				
		B901									P0[9:8]	
		B902									P4[1:0]	
		B903											
		B904					P8[7:0] P8[9:8]						
		B905									P8[9:8]	
		B906									P12[1:0]		
DGMLUTR	В9	B907	w	130									Digital Gamma Look-up Table for Red
		:							:				-
		:							:				
		B97C				ı	ı	P248	3[7:0]	Π	ı		
		B97D									P248	8[9:8]	-
		B97E									P252	2[1:0]	_
		B97F											-
		B980				I	I	P25	5[7:0]		I		-
		B981									P255	5[9:8]	
		BA00				<u> </u>			7:0]		<u> </u>		_
		BA01									P0[-
		BA02							-		P4[-
		BA03						 D0I	7:01				-
DGMLUTB	ВА		W	130					7:0]		Dot	0.01	Digital Gamma Look-up Table for Blue
		BA05 BA06									P8[-
		BA06 BA07									P12	[1:0]	-
		: :			:								-
		:			:								-
					٠								

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Instruction	MIPI	ress SPI-16	R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
		BA7C						P248	B[7:0]				
		BA7D									P248	8[9:8]	
		BA7E									P252	2[1:0]	
		BA7F											
		BA80						P255	5[7:0]				
		BA81									P255	5[9:8]	
LNECET	C0	C000	10/	2	LDE_EN				Line[6:0]				Display Line autting
LNESET	CO	C001	W	2				-	-		Line_D	elta[1:0]	Display Line setting
PORCTRL	C1	C100	W	2				VBP	[7:0]				Porch control
TOROTRE	O1	C101	**	2				VFP	[7:0]				T Gran control
INVSEL	C2	C200	W	2	0	0	1	1	0		NLINV[2:0]		Inversion selection & Frame Rate Control
IIIVOEE	02	C201	••	2						RTNI[4:0]	T		inversion selection a France Rate Schiller
		C300		3	DE/HV				VSP	HSP	DP	EP	
RGBCTRL	C3	C301	W	3				HBP_HV	RGB[7:0]				RGB control
		C302		3				VBP_HV	RGB[7:0]				
		C500		4		Т		PTS/	\[7:0]		Т		
PARCTRL	C5	C501	W	4							PTSA	N[9:8]	Partial mode Control
		C502		4		Т		PTE/	\ [7:0]		Π		
		C503		4					-		PTE	\ [9:8]	
SDIR	C7	C700	W	1						SS			Source direction control
PDOTSET	C8	C800	W	1	Z_EN	Z_SDM1S	Z_GltoR						Pesudo-Dot inversion driving setting
COLCTRL	CD	CD00	W	1			INV_LED PWM	INV_LED ON	MDT		EPF[2:0]		Color Control
SECTRL	E0	E000	W	1				SRE		SRE_al	pha[3:0]		Sunlight Readable Enhancement
NRCTRL	E1	E100	W	1				NRE			NR_m	nd[1:0]	Noise Reduce Control
SECTRL	E2	E200	W	1				SE		Y_ga	in[3;0]		Sharpness Control
CCCTRL	E3	E300	W	1				-	-			CCE	Color Calibration Control
SKCTRL	E4	E400	W	1				SKE			Skin_ce_	_mid[1:0]	Skin Tone Preservation Control
NVMSETE	EA	EA00	W	1								ADEN	NVM address Setting Enable
CABCCTRL	EE	EE00	W	1	'_ _	£	-	LEDPWR SEL	'	'	'	LED_EN	CABC Control



Command2_BK1

Instruction	Add	lress	R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
Instruction	MIPI	SPI-16	K/W/C	PINUM	70	סט	D5	D4	D3	D2	DI	DU	Function
VRHS	В0	B000	W	1				VRH	A[7:0]				Vop amplitude setting
VCOMS	B1	B100	W	1				VCO	M[7:0]				VCOM amplitude setting
VGHSS	B2	B200	W	1	ı	1				VGH	SS[3:0]		VGH Voltage setting
TESCMD	ВЗ	B300	W	1	1	1				0	0	0	TEST Command Setting
VGLS	B5	B500	W	1	0	1				VGL	S[3:0]		VGL Voltage setting
VRHDV	B6	B600	W	1	0	VRH_DV[6:0]						VRH_DV Voltage setting	
PWCTRL1	В7	B700	W	1	AP[1:0]	APIS[1:0] APOS[1:0]				S[1:0]	Power Control 1	
PWCTRL2	B8	B800	W	1			AVDI	AVDD[1:0] AVCL[1:0]			L[1:0]	Power Control 2	
PCLKS 1	ВА	BA00	W	1							KS[1:0]	Power pumping clk selection 1	
PCLKS 2	ВС	BC00	W	1			STP3C	KS[1:0]	STP2PCI	KS[1:0]	STP2S0	CKS[1:0]	Power pumping clk selection 2
PDR1	C1	C100	W	1	0	1	1	1		Т	2D		Source pre_drive timing set1
PDR2	C2	C200	W	1	0	1	1	1		Т	3D		Source pre_drive timing set2
MIPISET 1	D0	D000	W	1	1	0	0	0	EOTP_EN	0	ERR_S	EL[1:0]	MIPI Setting 1
		D100				Mpc_tl	px1[3:0]			Mpc_tl	px0[3:0]		
MIPISET 2	D1	D101	w	4		Mpc_txtir	neadj[3:0]			Mpc_tl	px2[3:0]		MIPI Setting 2
MIPISET 2	וט	D102	VV	4						Mpc_tt	ago[3:0]		MIPI Setting 2
		D103						Mpc_tta	aget[7:0]				
MIPISET 3	D2	D200	W	1	1		1	1	1 PHY_ttasure[3:0]				MIPI Setting 3
MIDICET 4	Da	D300	w	2							PHY_CSK[2:	0]	MIDI Catting 4
MIPISET 4	D3	D301	۷V	2	1	F	PHY_dsk1[2:	0]			PHY_dsk0[2	:0]	MIPI Setting 4

Command2_BK3

In a top vertice of	Add	ress	DAMIC	DAILINA	D7	D6	D5	D4	D3	D2	D1	D0	Formation
Instruction	MIPI	SPI-16	R/W/C	PNUM	Dγ	D6	סט	D4	D3	D2	וט	DU	Function
		C800			0	1	1	1	0	1	1	1	
NVMEN	C8	C801	w	4	0	0	0	0	0	0	0	1	NVM Enable
INVINIEIN	Co	C802	VV	4	1	1	1	0	1	1	1	0	INVINI ETIADIE
		C803			0	0	0	0	0	1	0	0	
		CA00					-	-			PA	9:8]	
NVMSET	CA	CA01	W	3				PA	[7:0]				NVM manual control Setting
		CA02						PDIN	I [7:0]				
PROMACT	СС	CC01	W	1	1	0	1	0	1	0	1	0	NVM Program Active



12.3.1 CND2BKxSEL (FFh/FF00h): Command2 BKx Selection

FFH						CND2E	3KxSEL							
Inst / Para	R/W	Add	iress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
1113171 414		MIPI	SPI-16	D10-0				D4	D0	DZ	Di	50		
	W		FF00h	X	0	1	1	1	0	1	1	1		
	W		FF01h	Х	0	0	0	0	0	0	0	1		
CN2BKxSEL	W	FFh	FF02h	X	0	0	0	0	0	0	0	0		
	W		FF03h	X	0	0	0	0	0	0	0	0		
	W		FF04h	Х	0	0	0	CN2	0	0	0	BKxSEL		
	This co	omman	d is used	d to select the	function	of Comm	and BK0	or Comr	nand BK	1.				
	When	CN2='	l'enable	the BK funct	ion of Co	mmand2,	CN2='0'	disable t	he BK fu	nction of	Commar	nd2.		
			BKxSEL BKx Function Select 00h BK0											
Description					00h	BK0								
					01h	BK1								
		01h BK1 03h BK3												
Restriction														
				Stat	us				Availa	bility				
			Normal	Mode On, Idle	Mode Off,	Sleep Out	t		Yes	3		_		
Register			Normal	Mode On, Idle	Mode On,	Sleep Ou	t		Yes	3				
availability			Partial	Mode On, Idle	Mode Off,	Sleep Out			Yes	3				
			Partial	Mode On, Idle	Mode On,	Sleep Out			Yes	3		_		
				Slee	o In				Yes	3		_		
			Status				Default	t Value (D7	7 to D0)					
Default			Power C	n Sequence			00h							
Doidan			S/W Res	set			00h							
			H/W Re	set			00h							



12.3.2 Command 2 BK0 Function

12.3.2.1 PVGAMCTRL (B0h/B000h): Positive Voltage Gamma Control

ВОН		PVGAMCTRL (BK0) Address D15-8 D7 D6 D5 D4 D3 D2 D1 D0											
Inst / Dave	DAM	R/W Address D15-8 D7 D6 D5 D4 D3 D2 D1 D0 W B000h X AJ0P[1:0] VC0P[3:0]										Do	
Inst / Para	R/VV	MIPI	SPI-16	D15-8	יט	D6	D5	D4	D3	D2	וט	DU	
	W		B000h	Х	AJOF	P[1:0]				VC0	P[3:0]		
	W		B001h	Х					VC4	P[5:0]			
	W		B002h	Х	AJ1F	P[1:0]		T	VC8	P[5:0]			
	W		B003h	Х						VC16P[4:	0]		
	W		B004h	Х						VC24P[4:	0]		
	W		B005h	Х						VC5	2P[3:0]		
	W		B006h	Х				1	VC80)P[5:0]			
PVGAMCTRL	W	B0h	B007h	Х							8P[3:0]		
	W		B008h	Х			VC147P[3:0]						
	W B009h X VC175P[5:0]												
	W		B00Ah	X							3P[3:0]		
	W		B00Bh	X						/C231P[4			
	W		B00Ch	X	 A 101					/C239P[4	:0]		
	W		B00Dh	X		P[1:0]			VC247P[5:0]				
	W		B00Eh B00Fh	X	۸ ۱۵۲	 P[1:0]	·		VC251P[5:0] VC255P[4:0]				
		e refer to		^	AJJI	[1.0]			<u> </u>	V C 2 3 3 F [4	.0]		
		It value:											
				Value(hex)			V	/alue(hex)					
	V	C0P[3:0]	l	00H	VC	203P[3:0]		00H					
	V	C4P[5:0]	ı	00H	VC	231P[4:0]		00H					
	V	C8P[5:0]	l	00H	VC	239P[4:0]		00H					
Description	VC	C16P[4:0)]	00H	VC	247P[5:0]		00H					
Boompaon	VC	C24P[4:0)]	00H	VC	251P[5:0]		00H					
	VC	C52P[3:0)]	00H	VC	255P[4:0]		00H					
	VC	C80P[5:0)]	00H	А	J0P[1:0]		00H					
	VC	108P[3:	0]	00H	A	J1P[1:0]		00H					
	VC	147P[3:	0]	00H	А	J2P[1:0]	00Н						
	VC	:175P[5:	0]	00H	A	J3P[1:0]		00H					
Restriction	on												

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	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Ole and In	
	Sleep In	Yes
		Yes fault Value (D7 to D0)
Default		fault Value (D7 to D0)
Default	Status Det	fault Value (D7 to D0)



12.3.2.2 NVGAMCTRL (B1h/B100h): Negative Voltage Gamma Control

B1H		NVGAMCTRL (BK0) R/W Address D15-8 D7 D6 D5 D4 D3 D2 D1 D0												
Inat / Dara	D / /	Add	Iress	D45.0	77	De	DE	D4	Da	50	D 1	DO		
Inst / Para	K/VV	MIPI	SPI-16	D15-0	וט	D6	Do	D4	D3	DZ	וט	DU		
	W		B100h	X	AJ0I	N[1:0]				VCC	N[3:0]			
	W		B101h	X					VC4	N[5:0]				
	W		B102h	X	AJ1I	N[1:0]			VC8	N[5:0]				
	W		B103h	X						VC16N[4:	0]			
	W		B104h	X						VC24N[4:	0]			
	W		B105h								2N[3:0]			
	W		B106h						VC80	ON[5:0]				
NVGAMCTRL	W	B0h	B107h								8N[3:0]			
	W		B108h								7N[3:0]			
	W		B109h						VC17	5N[5:0]				
	W		B10Ah						1	VC203N[3:0] VC231N[4:0]				
	W		B10Bh							VC231N[4:0] VC239N[4:0]				
	W		B10Ch X B10Dh X AJ2N[1:0]							:0]				
	W B10					N[1:0] 			VC247N[5:0] VC251N[5:0]					
	W		B10Fr			N[1:0]			:01					
		refer t	l		7.001	41.01				VC255N[4:0]				
		t value:												
	Delaul	t value.												
				Value(hex)				Value(hex)					
	V	C0N[3:0]	00H	VC	203N[3:0]		00H						
	V	C4N[5:0]]	00H	VC	231N[4:0]		00H						
	V	C8N[5:0]	00H	VC	239N[4:0]		00H						
Description	VC	C16N[4:0)]	00H	VC	247N[5:0]		00H						
2 000	VC	24N[4:0)]	00H	VC	251N[5:0]		00H						
	VC	C52N[3:0)]	00H	VC	255N[4:0]		00H						
	VC	C80N[5:0)]	00H	А	J0N[1:0]		00H						
	VC	108N[3:	0]	00H	А	J1N[1:0]		00H						
	VC	147N[3:	0]	00H	А	J2N[1:0]		00H						
	VC	175N[5:	0]	00H	А	J3N[1:0]		00H						
Restriction														
				State	us				Availa	bility				
	Normal Mode On, Idle Mode Off, Sleep Out					t	Yes]			
Register	ter Normal Mode On, Idle Mode On, Sleep Out Yes													
availability	Partial Mode On, Idle Mode Off, Sleep Out Yes													
	Partial Mode On, Idle Mode On, Sleep Out Yes						<u> </u>							
				Sleep) In				Ye	S]		
	Зівер III													



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	Status	Default Value (D7 to D0)	
5 ()	Power On Sequence	All "O"	
Default	S/W Reset	All "O"	
	H/W Reset	All "O"	



12.3.2.3 DGMEN (B8h/B800h): Digital Gamma Enable

В8Н						DGM	EN (BK0)						
Inst / Para	R/W		ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
DGMEN	W	MIPI B8h	SPI-16 B800h	X	0	0		DCM ON	0	0	0	0	
DGIVIEN					0	U	0	DGM_ON	0	0	0	0	
	DGW_	UN:DIQ	gitai Gar	nma Enable									
Description	DGM_	ON="0	-"0" , disable this function.										
	DGM_	ON="1	-"1" , enable this function.										
Restriction													
				Stat	us				Availab	oility		1	
			Norma	l Mode On, Idle	Mode Of	f, Sleep O	ut		Yes				
Register			Norma	l Mode On, Idle	Mode Or	n, Sleep O	ut		Yes				
availability			Partia	Mode On, Idle	Mode Off	, Sleep O	ut		Yes				
			Partia	l Mode On, Idle	Mode On	, Sleep O	ut		Yes	i			
				Slee	p In				Yes	i			
			Status				Defa	ult Value (D7	to D0)				
Defects			Power On Sequence 00h										
Default			S/W Reset 00h										
			H/W Reset 00h										
				_									



12.3.2.4 DGMLUTR (B9h/B900h): Digital Gamma Look-up Table for Red

В9Н		DGMLUTR (BK0) Address										
		Add	dress									
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
	W		B900h	Х				P0[7:0]			
	W		B901h	Х							P0[9:8]
	W		B902h	Х							P4[1:0]
	W		B903h	Х					1	-	1	
	W		B904h	Х				P8[7:0]			
	W		B905h	Х							P8[9:8]
	W		B906h	Х							P12	[1:0]
DOM!!!TD	W	Dal	B907h	Х					1	-	1	
DGMLUTB	W	B9h	•	Х								
	W		•	Χ								
	W		B97Ch	Х				P248	8[7:0]			
	W		B97Dh	Χ					1	1	P248	3[9:8]
	W		B97Eh	Χ					1	1	P252	2[1:0]
	W		B97Fh	Χ								
	W		B980h	X				P255	[7:0]			
	W		B981h	Χ								5[9:8]
Description	Digital	Gamm	ıa Look-ι	up Table for R	ed							
Restriction												
			Namaal	Stati		Class Out			Availab	-		
Register		-		Mode On, Idle		•			Yes Yes			
availability				Mode On, Idle I		•			Yes			
,				Mode On, Idle I					Yes			
				Sleep	ln				Yes			
									·			
			Status				Default	Value (D7	to D0)			
				n Sequence	Default Value (D7 to D0) All "0"							
Default			S/W Res				All "0"					
		H/W Reset All "0"										





12.3.2.5 DGMLUTB (BAh/BA00h): Digital Gamma Look-up Table for Blue

BAH	DGMLUTB (BK0) Address											
	5	Add	dress	5					-	-		-
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
	W		BA00h	Х				P0[7:0]			
	W		BA01h	Х					1		P0[9:8]
	W		BA02h	Х					1		P4[1:0]
	W		BA03h	Х					-			-
	W		BA04h	Х				P8[7:0]			
	W		BA05h	Х					1		P8[9:8]
	W		BA06h	Χ					ŀ		P12	[1:0]
DOM!!!TD	W	D.4.1	BA07h	Х					-			-
DGMLUTB	W	BAh	:	Χ				;	•			
	W		:	Χ				;	•			
	W		BA7Ch	Х				P248	3[7:0]			
	W		BA7Dh	Х					1		P248	8[9:8]
	W		BA7Eh	Х					1		P252	2[1:0]
	W		BA7Fh	Х								
	W		BA80h	Х				P255	[7:0]			
	W		BA81h	Χ							P255	5[9:8]
Description	Digital	Gamm	ıa Look-ι	ıp Table for Bl	lue							
Restriction												
			NI I	Stati		01			Availab			
Pogiator				Mode On, Idle Mode On, Idle			+		Yes Yes			
Register availability				Mode On, Idle I					Yes			
aranazını,				Mode On, Idle I					Yes			
				Sleep					Yes	;		
			Status				Default	Value (D7	' to D0\			
				n Sequence		Default Value (D7 to D0) All "0"						
Default			S/W Res				All "0"					
		H/W Reset All "0"										
		•										



12.3.2.6 LNESET (C0h/C000h): Display Line Setting

C0H						LNESE	T (BK0)					
Inst / Para	R/W	Add MIPI	ress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
	W		C000h	X	LDE EN				Line[6:0]			
LNESET	W	C0h	C001h	X							Line de	elta[1:0]
	Line[6	6: 01 : di	splay lin	e setting							_	
	_	-		line enable								
				delta line ,N	IL= (Line[6:0]+1)*8	}					
Description	EX:(C	0:0x6b,	0x00) →	((0x6b+1) x 8	3)=864;							
	LDE_E	ΞN="1",	add delt	ta line , NL=	(Line[6:0]	+1)*8+ Li	ine_delta	[1:0]*2				
	EX: (C	0:0xe9	,0x03) -	•((0x69+1) x8) + (3x2))=854						
	SCNL	= NL+\	/BP+VF	Р								
Restriction												
				Sta	210				Availab	sility.		
			Norma	I Mode On, Idle		Sleep Ou	t		Yes	-		
Register				l Mode On, Idle					Yes			
availability			Partial	Mode On, Idle	Mode Off,	Sleep Out	t		Yes	;		
			Partial	Mode On, Idle	Mode On,	Sleep Out	t		Yes	;		
				Slee	p In				Yes	3		
		Sta	itus				Default Val	ue (D7 to I	D0)			
Default		Po	wer On S	equence		6	6bh/00h					
Delauit		S/\	V Reset			6	6bh/00h					
		HΛ	N Reset			6	6bh/00h					



12.3.2.7 PORCTRL (C1h/C100h):Porch Control

C1H			Address D15-8 D7 D6 D5 D4 D3 D2 D1 D0										
	,	Add	dress	D . D .		-				-		D 0	
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
DODOTO	W	0.11	C100h	Х				VBP	[7:0]				
PORCTRL	W	C1h	C101h	Х				VFP	[7:0]				
	VBP[7	': 0] : Ba	ck-Porc	h Vertical line	setting fo	or display.							
Description	VFP[7	:0]: Fro	ont-Porc	h Vertical line	setting fo	or display.							
Restriction													
			Status Availability										
			Norma	I Mode On, Idle	Mode Off	, Sleep Ou	t		Yes				
Register			Norma	l Mode On, Idle	Mode On	, Sleep Ou	t		Yes	3			
availability			Partial	Mode On, Idle	Mode Off,	Sleep Out	:		Yes	3			
			Partial	Mode On, Idle	Mode On,	Sleep Out	:		Yes	3			
				Slee	p In				Yes	3			
		Sta	Status Default Value (D7 to D0)										
Default		Ро	Power On Sequence 04h/02h										
Delauit		SΛ	V Reset			C	4h/02h						
		H/\	N Reset			C	4h/02h						
			04/1/02/1										





12.3.2.8 INVSET (C2h/C200h):Inversion selection & Frame Rate Control

C2H						INVSE	T (BK0)					
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
INVSET	W	C2h	C200h	Х	0	0	1	1	0		NLINV[2:0	
	W		C201h	Х						RTNI[4:0]		
	NLINV	/[2:0]: l	nversio	n Selection								
	NL	_INV[2:	0]	Inversion								
		0		1 Dot								
Description		1		2 Dot								
		7		Column								
	RTNI[4:0] :mi	nimum	number of pcll	k in each	line						
	PCLK:	=512+(RTNI[4	:0]x16)								
Restriction												
				Sta					Availab	-		
				al Mode On, Idle					Yes			
Register				al Mode On, Idle					Yes			
availability		-		ıl Mode On, Idle					Yes			
			Partia	Il Mode On, Idle		Sleep Ou	t		Yes			
				Slee	p In				Yes	3		
		Sta	atus			[Default Val	ue (D7 to	D0)			
Defect		Ро	wer On	Sequence		1	0h/00h					
Default		S٨	N Reset			1	0h/00h					
		H/\	W Reset			1	0h/00h					



12.3.2.9 RGBCTRL (C3h/C300h):RGB control

СЗН						RGBCT	RL (BK0)							
		Add	dress	5.5.0						-		D 0		
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
	W		C300h	Χ	DE/HV				VSP	HSP	DP	EP		
RGBCTRL	W	C3h	C301h	Χ				HBP_HV	RGB[7:0]					
	W		C302h	Χ				VBP_HV	RGB[7:0]					
	DE/HV	:RGB	Mode se	election										
	DE/HV:	="0",R	GB DE	mode.										
	DE/HV	="1",R	GB HV	mode.										
	VSP : S	Sets th	ne signal	polarity of the	e VSYNC	pin.								
	VSP="(0", Lov	v active											
	VSP="	1", Hig	h active											
	HSP :	P: Sets the signal polarity of the HSYNC pin.												
	HSP="(P="0", Low active												
Description	HSP="	P="1", High active												
·	DP : Se	: Sets the signal polarity of the DOTCLK pin.												
	DP = "(D" The	data is i	nput on the p	ositive ed	lge of DO	TCLK							
				nput on the n										
				oolarity of the										
				323-0 is writte			"1". Disa	able data	write ope	ration wh	en ENAB	LE = "0".		
				323-0 is writte					-					
				RGB interface					-					
				RGB interface	-	-	-				J			
Restriction														
Restriction														
				Sta	tus				Availab	oility				
				l Mode On, Idle		•			Yes					
Register availability				I Mode On, Idle Mode On, Idle					Yes Yes					
availability				Mode On, Idle		•			Yes					
	Sleep In Yes													
		Sta	atus			Г	Default Val	lue (D7 to I	D0)					
				Sequence			00h/10h/08							
Default		SΛ	N Reset			()0h/10h/08	3h						
	H/W Reset 00h/10h/08h													



12.3.2.10 PARCTRL (C5h/C500h):Partial Mode Control

C5H						PARCT	RL (BK0)					
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
inst / Para	R/VV	MIPI	SPI-16	8-15ע	D7	Dб	D5	D4	D3	D2	DI	DU
	W		C500h	X				PTSA	A[7:0]			
	W		C501h	Х							PTS/	\ [9:8]
PARCTRL	W	C5h	C502h	Х				PTE	\[7:0]	•		
	W		C503	Х	-						PTE/	A[9:8]
	PTSA	[9:0]: F	: Partial display start line address									
Description	PTEA	[9:0] : F	: Partial display end line address									
Restriction												
				Sta	itus				Availal	oility		
			Norma	ıl Mode On, Idle	Mode Off	, Sleep Οι	ıt		Yes	S		
Register			Norma	ıl Mode On, Idle	Mode On	, Sleep Οι	ut		Yes	3		
availability			Partia	l Mode On, Idle	Mode Off,	Sleep Ou	t		Yes	5		
			Partia	l Mode On, Idle	Mode On,	Sleep Ou	t		Yes	8		
				Slee	ep In				Yes	S		
		Sta	atus			ı	Default Val	ue (D7 to I	D0)			
Default		Ро	Power On Sequence 00h/00h/5fh/03h									
Delauit		S٨	S/W Reset 00h/00h/5fh/03h									
		H/\	W Reset			(00h/00h/5f	h/03h				



12.3.2.11 SDIR (C7h/C700): X-direction Control

C7H						PDOSE	ET (BK0)								
	D 444	Add	dress	D45.0	1	D 0	,			D 0		D.o.			
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
PDOSET	W	C7h	C500h	Х						SS					
	SS:To	selecti	on x-dire	ection.											
Description	SS="0	",sourc	e form () to 479											
	SS="1	,sourc	urce form 479 to 0												
Restriction															
			Status Availability												
			Norma	al Mode On, Idle		Sleen Ou	ıt		Availar	-					
Register				al Mode On, Idle		•			Yes	·					
availability				I Mode On, Idle					Yes						
				l Mode On, Idle					Yes	3					
				Slee	p In				Yes	5					
		Sta	atus				Default Val	ue (D7 to I	D0)						
Default		Ро	wer On S	Sequence		C	00h								
Derauit		S٨	N Reset			()0h								
		HΛ	W Reset			()0h								



12.3.2.12 PDOSET (C8h/C800h):Pseudo-Dot inversion diving setting

C8H						PDOSE	T (BK0)								
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
PDOSET	W	C5h	C500h	Х	Z_EN	Z_SDM1	Z_Gltor								
Description	Z_EN= Z_EN= Z_SDI Z_SDI Z_SMI	="0",en ="1",dis M1 : SD M1="0" DL="1"	able PD sable PD DUM_1 c ,SDUM_ ,SDUM_	udo-dot inversions of SET setting or SDUM_2 en _2 is enable _1 is enable ixel, source dr	l nable cor	ntrol (for Z-	inv only)								
		_Gltor: upper-left pixel,source drive to R-Side _Gltor="0",L-side first _Gltor="1",R-side first													
Restriction															
Register availability			Norma Partia	al Mode On, Idle al Mode On, Idle I Mode On, Idle I Mode On, Idle	e Mode Or	n, Sleep Out f, Sleep Out	İ		Availab Yes Yes Yes Yes						
Default Status Default Value (D7 to D0) Power On Sequence S/W Reset H/W Reset 00h 00h															



12.3.2.13 COLCTRL (CDh/CD00h):Color Control

CDH						COL	CTRL (BK0)							
/ 5	D 44/	Add	dress	D45.0	D.7	D 0	5.5	5.4	D.O.	D 0	5.4	D.o.		
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
COLCTRL	W	CDh	CD00h	Х			INV_LED PWM	INV_LED _ON	MDT		EPF[2:0]			
	INV_L	ED PV	VM: LED	DPWM polarit	y control									
	INV_L	.ED PV	VM="0",	polarity norm	nal.									
	INV_L	.ED PV	VM="1",	polarity reve	rse.									
				ON polarity										
				olarity norma										
			-	olarity revers										
			-	nat argument		K) See T	ahle 17							
Description		-		at argument r		11,000 1	able 17.							
Description		-		-										
		T="1", pixel collect to DB[17:0]. F[2:0]: end of pixel format (for 65k & 262k mode)												
		copy self MSB												
		y G MS												
		y self L	SB											
	4:FIX	0												
	5:FIX	1												
Restriction														
				C	atus				Avoilabil	ia.,				
			Norma	al Mode On, Id		Off, Sleen	Out		Availabil Yes	щу				
Register				al Mode On, Id					Yes					
availability			Partia	ıl Mode On, Idl	e Mode O	ff, Sleep (Out		Yes					
			Partia	ıl Mode On, Idl	e Mode O	n, Sleep (Out		Yes					
				Sle	ep In				Yes					
		Sta	atus				Default Val	lue (D7 to D0))					
Default	Power On Sequence 00h													
S/W Reset 00h											ſ			
		H/	W Reset				00h							
<u> </u>														



12.3.2.14 SECTRL (E0h/E000h):Sunlight Readable Enhancement

E0H		MIPI SPI-16 E0h E000h X SRE SRE_alpha[3:0] Sunlight Readable Enhancement (SRE) enable control. 70", Sunlight Readable Enhancement disable. 11", Sunlight Readable Enhancement enable.													
Inst / Para	R/W		1	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
SECTRL	W			Х				SRE		SRE_al	pha[3:0]				
	SRE:	Sunligh	t Reada	ble Enhancer	ment (SRI	E) enable	control.								
	SRE=	"0", Suı	nlight Re	eadable Enha	ncement	disable.									
Description	SRE=	"1", Suı	nlight Re	eadable Enha	ncement	enable.									
	SRE_	_alpha:Sunlight Readable Enhancemnet (SRE) level selection													
	[00:0F	- -] → [lo													
Restriction			7 [lower : Highest]												
				Sta	tus				Availat	oility					
			Norma	Il Mode On, Idle	Mode Off	, Sleep Ou	ıt								
Register			Norma	ıl Mode On, Idle	Mode On	, Sleep Ou	ıt		Yes	3					
availability			Partia	l Mode On, Idle	Mode Off,	Sleep Ou	t		Yes	3					
		-	Partia			Sleep Ou	t								
				Slee	p In				Yes	3					
		Sta	atus			[Default Val	ue (D7 to I	D0)						
Default				Sequence			00h								
			N Reset)0h								
		НΛ	N Reset			()0h								
		HΛ	N Reset			(00h								



12.3.2.15 NRCTRL (E1h/E100h):Noise Reduce Control

E1H						NRCT	RL (BK0)							
		Add	dress	D		-	-					D .		
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
NRCTRL	W	E1h	E100h	Х				NRE			NR_m	nd[1:0]		
	NRE:	Noise F	Reduce	Function Enal	ole Contro	ol.								
	NRE=	"0", No	ise Red	uce Function	disable.									
Description	NRE=	"1", No	ise Red	uce Function	enable.									
	NR_m	_md:Noise Reduce level selection.												
Restriction		IN MAINTENED TREASURE TO THE T												
		Status Availability												
			Norma	al Mode On, Idle		Sleep Ou	ıt		Yes	-				
Register				Il Mode On, Idle		•			Yes					
availability			Partia	l Mode On, Idle	Mode Off,	Sleep Ou	t		Yes	3				
			Partia	l Mode On, Idle	Mode On,	Sleep Ou	t		Yes	3				
				Slee	p In				Yes	3				
		Sta	atus			[Default Val	ue (D7 to I	D0)					
Default	Power On Sequence 00h													
Delauit		S٨	N Reset			()0h							
		HΛ	W Reset			()0h							



12.3.2.16 SECTRL (E2h/E200h):Sharpness Control

E2H			E200h X SE Y_gain[3:0] ess Function Enable Control. arpness Function disable. arpness Function enable.											
last / Dans	DAA	Add	dress	D45.0	D7	Do	Dr	D4	Do	Do	D4	Do		
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	Д6	D5	D4	D3	D2	D1	DU		
SECTRL	W	E2h	E200h	Х				SE		Y_gai	in[3:0]			
	SE: Sh	narpne	ss Func	tion Enable Co	ontrol.									
	SE="0	", Shar	pness F	unction disab	le.									
Description	SE="1	", Shar	pness F	unction enabl	e.									
	Y_gai	in :Sharpness level Selection.												
Restriction			· · · · · · · · · · · · · · · · · · ·											
		Ctotus Avoilability												
			N. a. man a			Class Ou				•				
Dogistor						-								
Register availability						•								
availability														
			i aitia	Slee		Olcop Ou			Yes					
				<u> </u>	P									
			atus					ue (D7 to I	D0)					
Default														
			N Reset)0h							
		НΛ	N Reset			C	00h							



12.3.2.17 CCCTRL (E3h/E300h):Color Calibration Control

ЕЗН						CCCTF	RL (BK0)								
/ 5	D 444	Add	dress	D45.0	5.7	D 0	D.	5.4	D 0	D 0	5.4	Do			
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
CCCTRL	W	E3h	E300h	Х								CCE			
	CCE:	Color C	Calibratio	on Function E	nable Cor	ntrol.									
Description	CCE=	"0", Co	lor Calib	ration Function	n disable) .									
	CCE=	"1", Co	Color Calibration Function enable.												
Restriction															
			Status Availability												
			Norma			Clean Ou			Avallar	·					
D				I Mode On, Idle						·					
Register				I Mode On, Idle					Yes	·					
availability				Mode On, Idle					Yes	·					
			Partia	l Mode On, Idle		Sleep Ou	i e		Yes						
				Slee	p In				Yes	<u> </u>					
		Sta	atus			[Default Val	ue (D7 to I	D0)						
Default	Power On Sequence 00h														
Delauit	S/W Reset 00h														
		HΛ	N Reset			C	00h								



12.3.2.18 SKCTRL (E4h/E400h):Skin Tone Preservation Control

E4H						SKCTF	RL (BK0)								
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D0	D1	D0			
inst / Para	R/VV	MIPI	SPI-16	ט־5-8	D7	Dб	סט	D4	D3	D2	DI	DU			
SKCTRL	W	E4h	E400h	Х				SKE			Skin_ce	_mid[1:0]			
	SKE:	Skin To	ne Pres	ervation enab	le control			•		•					
	SKE='	'0", Ski	n Tone F	Preservation of	lisable.										
Description	SKE='	'1", Ski	n Tone F	Preservation e	nable.										
	Skin_	n_ce_mid: Skin Tone Preservation enable control													
Restriction															
		Status Availability													
			Norma	al Mode On, Idle		Sleen Ou	t		Yes	-					
Register				al Mode On, Idle					Yes						
availability			Partia	l Mode On, Idle	Mode Off,	Sleep Ou	i		Yes	3					
			Partia	l Mode On, Idle	Mode On,	Sleep Ou	t		Yes	3					
				Slee	p In				Yes	S					
		Sta	atus			[Default Val	ue (D7 to I	D0)						
Default	Power On Sequence 00h														
Dorault		SΛ	N Reset			(00h								
		НΛ	N Reset			(00h								



12.3.2.19 NVMSETE (EAH/EA00H): NVM Address Setting Enable

EAH						NVMSE	TE (BK0)							
/ D	644	Add	dress	D45.0	1	D 0	,		D 0		1	D.o.		
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
NVMSETE	W	EAh	EA00h	Х								ADEN		
	ADEN	:NVM	Address	Setting Enab	le.									
Description	ADEN	="0", N	IVM Add	ress Setting o	lisable.									
	ADEN	N="1", NVM Address Setting enable.												
Restriction														
				Sta					Availal					
				al Mode On, Idle					Yes	·				
Register			Norma	al Mode On, Idle	Mode On	, Sleep Ou	t		Yes	3				
availability			Partia	l Mode On, Idle	Mode Off,	, Sleep Ou	t		Yes	3				
			Partia	l Mode On, Idle	Mode On,	, Sleep Ou	t		Yes	3				
				Slee	p In				Yes	3				
		Sta	atus				Default Val	ue (D7 to I	D0)					
Defect	Power On Sequence 00h													
Default		S٨	N Reset			(00h							
		H/\	W Reset			C	00h							



12.3.2.20 CABCCTRL (EEh/EE00h):CABC Control

EEH						CABCO	CTRL (BK	0)							
	D 444	Add	dress	D45.0	D-7	D 0	D.	5.4	D.O.	D 0	D 4	D .0			
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
CABCCTRL	W	EEh	EE00h	Х				LEDPWR				LED			
CABCOTTLE	VV		LLOON	Λ				SEL				ON			
	LED_0	ON: LE	D_ON c	output control											
	LED_0	O"= NC	",LED_C	ON output cor	ntrol off.										
	LED_0	ON ="1	", LED_	ON output co	ntrol on.										
Description	LEDP	PWR SEL: LED_ON output level selection.													
	LEDP\	PWR SEL ="0",output level is VDDI.													
	LEDP\	WR SE	R SEL ="1", output level is VDDB.												
Restriction		VVIX OLL = 1, output level is VDDD.													
							ľ				1				
					atus				Availab	ility					
				al Mode On, Idle					Yes						
Register				al Mode On, Idle					Yes						
availability		-		l Mode On, Idle					Yes						
			Partia	l Mode On, Idle		n, Sleep Or	ut		Yes						
				Slee	ep In				Yes						
		Status Default Value (D7 to D0)													
Default		Power On Sequence 00h													
Delault		S٨	W Reset				00h								
		H/\	W Reset				00h								



12.3.2.21 DSTB: Deep Standby Mode Enable

		MIPI SPI-16													
Inst / Para	R/W			D15-8	D7	D6	D5	D4	D3	D2	D1	D0			
	W		FF00h	Х	0	1	1	1	0	1	1	1			
	W		FF01h	Х	0	0	0	0	0	0	0	1			
	W		FF02h	Х	0	0	0	0	0	0	0	0			
PARCTRL	W	FFh	FF03	Х	0	0	0	0	0	0	0	0			
	W	W FF04 X 0 0 0 0 0 0 0									0				
	W	FF05 DSTB 0 0 0 0 0 0										0			
	DSTB	DSTB:DSTB Mode Enable Setting.													
Description	DSTB:	DSTB="0", DSTB Mode Setting disable.													
	DSTB:	DSTB="0", DSTB Mode Setting disable. DSTB="1", DSTB Mode Setting enable.													
Restriction															
				Sto	tue				Availak	sility					
			Norma			. Sleep Ou	ıt								
Register						-									
availability									Yes	3					
			Partia	Mode On, Idle	Mode On,	Sleep Ou	t		Yes	5					
				Slee	p In				Yes	S					
	Status Default Value (D7 to D0)														
Default		Po	wer On S	equence		(00h								
Delauit		SΛ	N Reset			(00h								
		HΛ	N Reset			(00h								



12.3.2.22 DSTBT: Deep Standby Mode Active

		MIPI SPI-16 W FF00h X 0 1 1 1 0 1 1 1 W FF01h X 0 0 0 0 0 0 0 0 1 W FFh FF02h X 0 0 0 0 0 0 0 0 0 FF03 X 0 0 0 0 0 0 0 0 0 FF04 X DSTBT 0 0 0 0 0 0 0 0 STBT:DSTB Mode Active. STBT="0", DSTB Mode Active.													
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	DO			
IIISt / T ala	10,00	MIPI	SPI-16	D10 0	D1	D0	55	54	D0	DZ	Di	D0			
	W		FF00h	Х	0	1	1	1	0	1	1	1			
	W		FF01h	X	0	0	0	0	0	0	0	1			
PARCTRL	W	FFh	FF02h	Х	0	0	0	0	0	0	0	0			
	W FF03 X 0 0 0 0 0 0 0										0				
	W	FF04 X DSTBT 0 0 0 0 0 0										0			
	DSTB	STBT:DSTB Mode Active.													
Description	DSTB	DSTBT="0", DSTB Mode not Active.													
	DSTB.	DSTBT= 0 , DSTB Mode not Active. DSTBT="1", DSTB Mode Active.													
Restriction															
				Sta	itus				Availat	oility					
			Norma	l Mode On, Idle	Mode Off	, Sleep Οι	ıt		Yes						
Register			Norma	l Mode On, Idle	Mode On	, Sleep Ou	ıt		Yes	3					
availability			Partia	Mode On, Idle	Mode Off,	Sleep Ou	t		Yes	5					
			Partia	Mode On, Idle	Mode On,	Sleep Ou	t		Yes	3					
				Slee	p In				Yes	3					
	Status Default Value (D7 to D0)														
Default		Po	wer On S	Sequence		(00h								
Dolaun		-	N Reset				00h								
		Η/\	N Reset			(00h								

Enter DSTB Mode Flow:

Step1: 0xFF:0x77/0x01/0x00/0x00/0x00/0x80

Step2:0xFF:0x77/0x01/0x00/0x00/0x80



12.3.3 Command 2 BK1 Function

12.3.3.1 VRHS (B0h/B000h):Vop Amplitude setting

ВОН	VRHS (BK1)													
Inst / Para	R/W	Add	dress	D15-8	D7			5.		Do	,	D.		
		MIPI	SPI-16			D6	D5	D4	D3	D2	D1	D0		
VRHS	W	B0h	B000h	Х	VRHA[7:0]									
Description	VRHA[7:0]: VRH Set.													
	Vop=3.5375+(VRHA[7:0]x0.0125);													
	VRHP=Vop+(Vcom+Vcom offset);													
	VRHN=-Vop+(Vcom+Vcom offset);													
Restriction														
			Status						Availability					
			Normal Mode On, Idle Mode Off, Sleep Out						Yes					
Register availability			Normal Mode On, Idle Mode On, Sleep Out						Yes					
			Partial Mode On, Idle Mode Off, Sleep Out						Yes					
			Partial Mode On, Idle Mode On, Sleep Out						Yes					
		Sleep In							Yes					
Default		Status						Default Value (D7 to D0)						
		Power On Sequence					4dh							
		S/W Reset					4dh							
		H/W Reset 4dh												



12.3.3.2 VCOMS (B1h/B100h):VCOM amplitude setting

B1H	VCOM (BK1)												
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
		MIPI	SPI-16										
VCOM	W	B0h	B000h	Х	VCOM[7:0]								
Description	VCOM[7:0]: VCOM Set.												
	VCOM=0.1+(VCOM[7:0] x 0.0125);												
Restriction													
		Status						Availability					
			Norma	al Mode On, Idl	ut	Yes							
Register				al Mode On, Idle Mode On, Sleep Out									
availability	· · ·												
			Partia	l Mode On, Idle	ut	Yes							
			Sleep In						Yes				
Default		Sta	atus				Default Value (D7 to D0)						
		Po	wer On S	Sequence			40h						
		S/	S/W Reset				40h						
		H/W Reset 40h											



12.3.3.3 VGHSS (B2h/B200h):VGH Voltage setting

B2H						VGH	SS (BK1)					
Inst / Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
VGHSS	W	B2h	B200h	Χ						VGHS	SS[3:0]	
	VGHS	SS[3:0]: Gate	High Voltag	ge settin	ıg.						
				VGHSS[3:	:0]	Voltage	VGH	SS[3:0]	Voltage			
				00H		11.5	C)7H	15.0			
				01H		12.0	C)8H	15.5			
Description				02H		12.5	C	9H	16.0			
Description				03H		13.0	C	0AH				
				04H		13.5		BH	17.0			
				05H		14.0		CH	17.5			
				06H		14.5	0	DH	18.0			
Restriction												
				C+	atus				Availab	ility		
			Norma	al Mode On, Idl		off Sleen C)ut					
Register				al Mode On, Idl					Yes Yes			
availability				I Mode On, Idle					Yes			
			Partia	l Mode On, Idle	e Mode O	n, Sleep O	ut		Yes			
				Sle	ep In				Yes			
		Sta	atus				Default V	alue (D7 to	D0)			
				Sequence			02h					
Default			W Reset	-			02h					
	H/W Reset 02h											
i												



12.3.3.4 TESTCMD (B3h/B300h):TEST Command Setting

ВЗН						TEST	CMD (BK1)					
	D 44/	Add	dress	D45.0	D.7	D 0	D.	5.4	D.o.	D 0	5.4	D.	
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
TESTCMD	W	B3h	B300h	Х	1					0	0	0	
Description	TEST	CMD	: 0x80l	4									
Restriction													
				Sta	atus				Availab	ility			
			Norma	al Mode On, Idl	e Mode O	ff, Sleep C	ut		Yes				
Register			Normal Mode On, Idle Mode On, Sleep Out Yes										
availability			Partia	ıl Mode On, Idle	e Mode Of	f, Sleep O	ut		Yes				
			Partia	Il Mode On, Idle	e Mode Or	n, Sleep O	ut		Yes				
				Sle	ep In				Yes				
	Status Default Value (D7 to D0)												
Defeat		Po	wer On S	Sequence			00h						
Default		S/	W Reset				00h						
		H/	H/W Reset					00h					



12.3.3.5 VGLS (B5h/B500h):VGL Voltage setting

B5H						VGI	S (BK1)					
Inst / Para	R/W	Add MIPI	dress SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
VGLS	W	B5h	B500h	Х		1				VGL	S[3:0]	
	VGLS	S[3:0]:	Gate L	ow Voltage	setting.	1						
				VGLS[3:0	0]	Voltage	VGH	SS[3:0]	Voltage			
				00H		-7.06)8H	-9.83			
				01H		-7.47	(9H	-10.17			
December				02H		-7.91	C	0AH				
Description				03H		-8.14	C	0BH				
				04H		-8.65	C	0CH				
				05H		-8.92	C	0DH				
				06H		-9.21		0EH				
			07H			-9.51	()FH	-12.69			
Restriction												
					atus		Availabi					
				al Mode On, Idl			1		Yes			
Register availability				al Mode On, Idl					Yes			
avallability				I Mode On, Idle I Mode On, Idle			+		Yes Yes			
			Failla			п, зіеер О	ut		Yes			
		<u> </u>	Sleep In						103			
			atus					alue (D7 to	D0)			
Default		-		Sequence			07h					
		-	S/W Reset				07h					
		H/	W Reset				07h					
<u> </u>												



12.3.3.6 PWCTRL1 (B7h/B700h):Power Control 1

В7Н		PWCTRL1 (BK1)										
Inst / Para	R/W	Add	Iress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
inst / Para	K/VV	MIPI	SPI-16	ס-פוע	וט	סט	סט	D4	טט	D2	וט	סם
PWCTRL1	W	B7h	B700h	Х	AP[1:0]			APIS	6[1:0]	APO	S[1:0]
	AP[1	: 0] : Ga	amma (OP bias curr	ent sele	ction.						
	AF	P[1:0]	Curr	ent								
	(00H	Of	ff								
	(01H	Mi	n								
	()2H	Mid	dle								
	()3H	Ma	ax								
	APIS	[1:0]:	Source	OP input st	age bias	current	selectio	n				
	AP	IS[1:0]	Curr	ent								
December	(00H	Ot	ff								
Description	()1H	Mi	n								
	()2H	Mid	dle								
	()3H	Ma	ax								
	APOS[1:0]: Source OP output stage bias current selection.											
APOS[1:0] Current												
	00H Off											
	()1H	Mi	n								
	()2H	Mid	dle								
	()3H	Ma	ax								
Restriction												
			Mana		atus	((Ola O			Availab	ility		
Danistan				al Mode On, Idl al Mode On, Idl					Yes Yes			
Register availability				al Mode On, Idle al Mode On, Idle					Yes			
availability									Yes			
		Partial Mode On, Idle Mode On, S Sleep In					at .		Yes			
				0.0	ор							
			atus	_			Default Value (D7 to D0)					
Default				Sequence			8Ch					
			W Reset				8Ch 8Ch					
		H/W Reset					оUП					



12.3.3.7 PWCTRL2 (B8h/B800h):Power Control 2

В8Н		PWCTRL2 (BK1)											
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
mst/raia	17,44	MIPI	SPI-16	D13-0	<i>D1</i>	Do	D3	D4	D3	DZ	ы	DO	
PWCTRL2	W	B8h	B800h	X			AVE	DD[1:0]			AVCI	_[1:0]	
	AVDI	D[1:0]:	: AVDD	voltage sett	ing.								
	AVE	DD[1:0]	AVE	DD									
	(D0H	6.2	V									
	()1H	6.4	V									
	()2H	6.6	V									
	()3H	6.8	V									
Description	AVCI	_[1:0]:	AVCL	voltage setti	ng								
	AVO	CL[1:0]	AVC	CL									
	(00H	-4.4	V									
	()1H	-4.6	V									
	()2H	-4.8	V									
	(03H -5.0 V											
Restriction													
		Status Availability											
			Norma	al Mode On, Idl		ff. Sleep C	-						
Register				al Mode On, Idl					Yes				
availability				Il Mode On, Idle					Yes				
			Partia	I Mode On, Idle	e Mode Or	n, Sleep O	ut		Yes				
				Sle	ep In				Yes				
		Sta	atus				Default Value (D7 to D0)						
				Sequence			21h						
Default			W Reset				21h						
	H/W Reset 21h												
·													



12.3.3.8 PCLKS1 (BAh/BA00h):Power pumping clk selection 1

BAH		PCLKS1 (BK1)											
Inst / Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
IIISt / Fala	IX/VV	MIPI	SPI-16	D13-6	Di	Do	D3	D4	DS	DZ	Di	DU	
PCLKS1	W	BAh	BA00h	X			STP4	CKS[1:0]			STP1C	KS [1:0]	
	STP4	CKS[1:0]: st	ep4 pumping	g clk sel	ection.							
	STP	4CKS[1:	:0] C	CLK									
		00H	3.3	MHz									
		01H	4.0	MHz									
		02H	2.5	MHz									
		03H	6.0	MHz									
Description	STP1	CKS[1:0]: st	ep1 pumping	g clk sel	ection.							
	STP ²	1CKS[1:	:0] C	CLK									
		00H	3.3	MHz									
		01H	4.0	MHz									
				MHz									
		03H 6.0 MHz											
Restriction													
				C+	atus				Availab	ility			
			Norma	al Mode On, Idl		ff Sleen C) ut		Yes	ility			
Register				al Mode On, Idl					Yes				
availability				Il Mode On, Idle					Yes				
,				Il Mode On, Idle					Yes				
					Sleep In Yes								
		Ct	-4				Defection	alva (DZ ta D	١٥١				
			atus	Sequence			Default Value (D7 to D0) 22h						
Default			W Reset	Dequence									
	S/W Reset 22h H/W Reset 22h												
	11/74 110301												
	l .												



12.3.3.9 PCLKS2 (BCh/BC00h):Power pumping clk selection 2

всн						PCLK	CLKS2 (BK1)						
Inot / Daw	DAY	Add	Iress	D45.0	D7	DC	הר	D4	D2	D0	D4	D0	
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
PCLKS2	W	BCh	BC00h	Х			STP3	CKS[1:0]	STP2C	KS[1:0]	STP2SC	CKS [1:0]	
	STP3	CKS[1:0]: st	ep3 pumpin	g clk sel	ection.							
	STP	4CKS[1:	0] (CLK									
		00H	2.5	MHz									
		01H	3.3	MHz									
		02H	4.0	MHz									
		03H	5.0	MHz									
	STP2	CKS[1:0]: st	ep2 VGHP	pumpin	g clk sel	ection.						
	STP	1CKS[1:	0] (CLK									
Description		00H	2.5	MHz									
Description		01H	3.3	MHz									
		02H	4.0	MHz									
		03H		MHz									
	STP2	SCKS	[1:0]:	step2 VGHS	pumpin	g clk sel	ection.						
	STP2SCKS[1:0] CLK												
	00H 2.5 MHz												
		01H		.3 MHz									
		02H	4	.0 MHz									
		03H	5	.0 MHz									
Restriction													
				C+	atus				Availab	ility			
			Norm:	al Mode On, Idl		ff Sleen O)ı ıt		Yes				
Register				al Mode On, Idl			+		Yes				
availability				al Mode On, Idle					Yes				
				al Mode On, Idle					Yes				
	Sleep In					•			Yes				
											-		
		Str	atus				Default V	alue (D7 to D	ın)				
				Sequence			Default Value (D7 to D0) 22h						
Default		Power On Sequence S/W Reset					22h						
	H/W Reset						22h						
		<u> </u>									-		



12.3.3.10 SPD1 (C1h/C100h): Source pre_drive timing set1

C1H		SPD1(BK1)										
In at / Dans	DAA	Add	dress	D45.0	7	6	55	64	Do	D 0	D4	Do
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
SPD1	W	C1h	C100h	Х	0	1	1	1		T2D	[3:0]	
	_	_		pre_drive tin	ning sett	ing.(GN	D to VD	D)				
Description	Adju	st Ran	ge : 0 ~	3 uS								
	1 ste	p is 0.2	2uS									
Restriction												
		Status Availability										
			· · · · · · · · · · · · · · · · · · ·									
Register			Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Yes									
availability				al Mode On, Idle					Yes			
availability				al Mode On, Idle					Yes			
			ranc		ep In	i, Gloop O	at		Yes			
		Sieep III										
		Sta	Status Default Value (D7 to D0)									
			Power On Sequence 75h									
Default			W Reset	•			75h					
	H/W Reset 75h											



12.3.3.11 SPD2 (C2h/C200h):Source EQ2 Setting

C1H		SPD2 (BK1)										
	5.41	Add	dress	5/50							5.	-
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
SPD2	W	C2h	C200h	Х	0	1	1	1		T3D	[3:0]	
	T3D	[3:0]:	source	pre_drive tir	ning sett	ting (VDI	D to 2*V	DD level)				
Description	Adju	st Ran	ge : 4 ~	12 uS								
Boompaon	1 ste	p is 0.8	3 uS									
Restriction												
				St.	atus				Availah	ility		
			Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes									
Register			Normal Mode On, Idle Mode On, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Yes									
availability			Partia	al Mode On, Idl	e Mode Of	f, Sleep O	ut		Yes			
			Partia	al Mode On, Idl	e Mode Or	n, Sleep O	ut		Yes			
				Sle	ep In				Yes			
		Sta	Status Default Value (D7 to D0)									
Default		Po	Power On Sequence 75h									
Delauit		S/	W Reset				75h					
		H/	W Reset				75h					



12.3.3.12 MIPISET1 (D0h/D000h):MIPI Setting 1

D0H						MIPIS	SET1 (BK	1)				
In at / D	D.444	Add	ress	D45.0	D-	Do	D-		B.C.	D.C.	D.1	Do
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
MIPISET1	W	D0h	D000h	Х	1	0	0	0	EOT_EN	0	ERR_S	EL[1:0]
	EOT_	EN: p	rotocol	selection e	rror repo	orting en	able					
	EOT_	EN="0"	,disable	e eotp report	error.							
	EOT_	EN="1"	,enable	eotp report	error.							
	ERR_	_SEL[′	1:0]: E	RR pin outp	ut signa	l setting	•					
Description	ERR.	_SEL[1:	0]	output								
		00H	Dis	able								
		01H	CR	C error only								
		02H	EC	C error only								
		03H CRC+ECC error										
Restriction												
				Si	tatus				Availabi	litv		
			Norm	al Mode On, Id	le Mode C	Off, Sleep	Out		Yes	,		
Register				al Mode On, Id					Yes			
availability			Partia	al Mode On, Idi	e Mode C	ff, Sleep 0	Out		Yes			
			Partia	al Mode On, Idl	e Mode O	n, Sleep (Out		Yes			
		Sleep In							Yes			
		Sta	atus				Default Value (D7 to D0)					
Default		Ро	wer On	Sequence		00h						
Default		S٨	N Reset			00h						
		H/	W Reset				00h					



12.3.3.13 MIPISET2 (D1h/D100h):MIPI Setting 2

D1H)							
		Ado	dress				ET2 (BK1	,				
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
			D100h	Х		Mpc_tl	ox1[3:0]			Mpc_tlp	(0:E}0xc	
MIPISET2	W	D1h	D101h	Х		Mpc_txtir	neadj[3:0]			Mpc_tlp	ox2{3:0}	
WIII IOL 12	VV	Dill	D102h	Х						Mpc_tta	ago[3:0]	
			D103h	Х				Mpc_tta	aget[7:0]			
Description	D: acce g i:	C:T _{TA-SURE} :Time-out before new Tx side start driving D:T _{TA-GET} :Time to drive LP_00 by new Tx A B A B C C D E B A B A B A B A B C C C D E B C C D E B C C D E B C C D E B C C D E B C C D E B C C D E B C C D E B C C D E B C C D E B C C D E C D E C D E C D E C D C D C D C D C D C D C D C D C D C D C D C D C D C D C D C D C D C D D										
		REG		D	escription				Va	alue		
	Мрс	_tlpx0	F	Rx LPM state t	timeout si	ignal	ste	p:				
		_tlpx1		Rx LPM state t		ignal	ste					
		_tlpx2		RX_to_TX LP1			ste					
		_txtime		PM transmitti		nal	ste					
		Mpc_ttago Tx->Rx BTA t Mpc_ttaget Tx BTA settin					ste					
							ı	-				
Restriction												1
		Normal Mode On, Id			tatus	off Sleen C)ı ıt	Availability				
Register				nal Mode On, Id				Yes Yes				
availability				al Mode On, Id					Ye			
						dle Mode On, Sleep Out				s		
		Sleep				Yes						



ST7701

Default

Status	Default Value (D7 to D0)
Power On Sequence	31h/03h/04h/05h
S/W Reset	00h/03h/04h/05h
H/W Reset	00h/03h/04h/05h

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12.3.3.14 MIPISET3 (D2h/D200h):MIPI Setting 3

D2H	MIPISET3 (BK1)											
		Ado	dress									
Inst / Para	R/W	MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
MIPISET3	W	D2h	D200h	Х			1	1		Phy_ttas	sure[3:0]	
Description	A:Host to Display BTA B:T _{TA-GO} : Time to drive LP_00 after Turnaround Request C:T _{TA-SURE:} Time-out before new Tx side start driving D:T _{TA-GET} : Time to drive LP_00 by new Tx A B B A B C C D C D C D C D C D C D C D C D C D											
Restriction	1											
		Status						Availability				
		Normal Mode On, Idle Mode Off, Slee										
Register			Norm	al Mode On, Id	lle Mode C	n, Sleep C	Out	Yes				
availability			Partia	al Mode On, Id	le Mode O	ff, Sleep O	ut	Yes				
		Partial Mode On, Idle Mode On, Sleep O						Yes				
					eep In	-		Yes				
Default	Status Default Value (D7 to D0) Power On Sequence 31h S/W Reset 31h H/W Reset 31h											

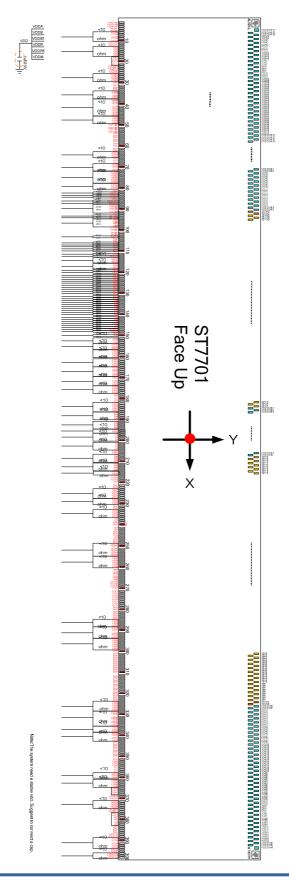


12.3.3.15 MIPISET4 (D3h/D300h):MIPI Setting 4

D3H	MIPISET4 (BK1)												
Inst / Para	R/W M	Add	dress					-	Do.	Do	5.4	D .0	
		MIPI	SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
MIPISET4	W	D3h	D300h	Х						Pl	HY_CSK[2	2:0]	
			D301h	Х		Pł	HY_dsk1[2	:0]	1	Pl	HY_dsk0[2	[2:0]	
	PHY_	_CSK:	CSK: MIPI Clock Lane Delay										
	Step: 1 step 200ps												
Description	PHY_dsk1: MIPI Data 1 Lane Delay												
	Step: 1 step 200ps												
	PHY_dsk0: MIPI Data 0 Lane Delay												
	Step: 1 step 200ps												
Restriction	iction												
		Status						Availability					
			Norm	al Mode On, Id	dle Mode C	rff, Sleep Out			Yes				
Register			Normal Mode On, Idle Mode On, Sleep Out						Yes				
availability		Partial Mode On, Idle Mode Off, Sleep											
		Partial Mode On, Idle Mode On, Slee					ut						
	Sleep In Yes												
Default		Status				Default Value (D7 to D0)							
		Power On Sequence				00h/00h							
			S/W Reset				00h/00h						
		H/W Reset						00h/00h					



13 APPLICATION CIRCUIT





13.1 Voltage Generation

The following is the ST7701 analog voltage pattern diagram:

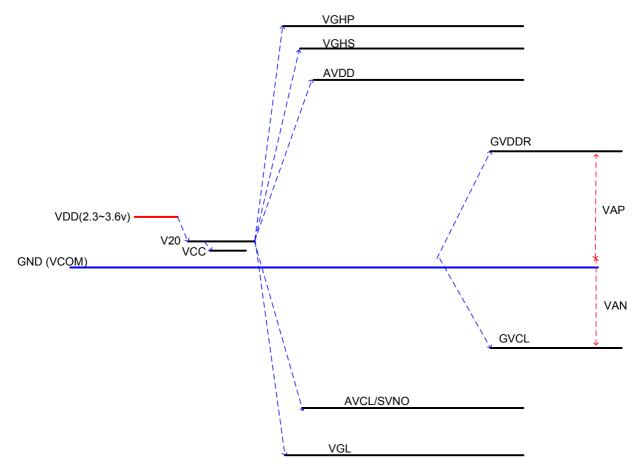


Figure 95 Power Booster Level



13.2 Relationship about source voltage

The relationship about source voltage is shown as below:

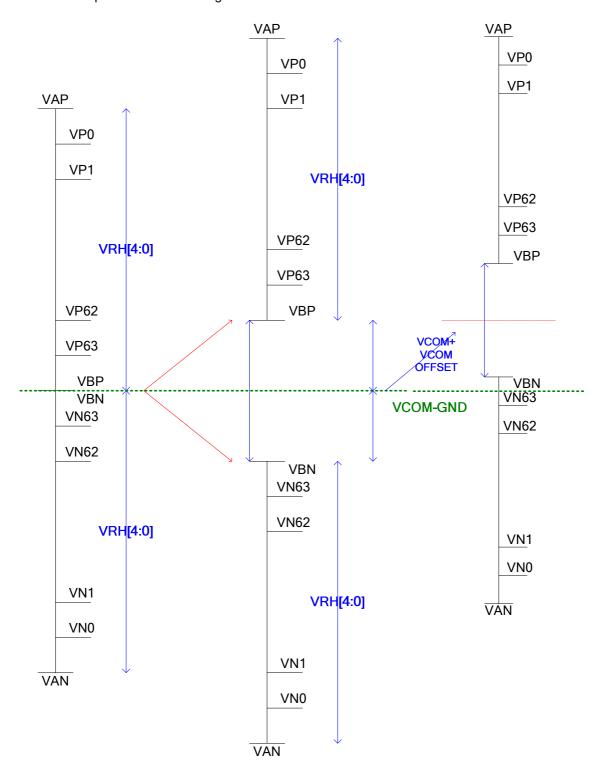


Figure 96 Relationship about source voltage

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14 REVISION HISTORY

Version	Date	Description			
V0.0	2015/05	Preliminary V0.0			
V1.0	2015/10	Release Version 1.0.			
V1.1	2016/03	1.Modify RGB Timing			
		2.Add DSTB Command			
		3.Modify operation voltage			
		4.Modify application Circuit			