# Problem Set 1 Solutions

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Prove that  $\log_4 6$  is irrational.

*Proof.* We use proof by contradiction. Suppose that  $\log_4 6$  is rational. Then  $\log_4 6 = \frac{n}{d}$  where n and d are integers, d > 0, and n and d do not share any common factors. Consider the following:

$$4^{\log_4 6} = 4^{\frac{n}{d}}$$

Apply the definition of the log function:

$$6 = 4^{\frac{n}{d}}$$

$$6^d = 4^n$$

$$2^d 3^d = 2^{2n}$$

$$3^d = 2^{2n-d}$$

Since both 3 and 2 are prime numbers, we conclude from the *Fundamental Theorem of Arithmetic* that the above equation can only satisfied if both sides equal 1. I.e d=0 and 2n-d=0, which implies that d=n=0. This is a contradiction since d>0. Hence, the claim must be true.

Prove that

$$n \le 3^{\frac{n}{3}} \ \forall \ n \in \mathbb{N} \tag{1}$$

*Proof.* The proof is by case analysis. Consider the following cases:

- 1. n = 0
- 2. n = 1
- 3. n = 2
- 4. n = 3
- 5. n = 4
- 6.  $n \ge 5$

Case 1:

$$3^{\frac{0}{3}} = 3^0 = 1 > 0$$

(1) holds for Case 1.

Case 2:

$$3^{\frac{1}{3}} = 3^{\frac{1}{3}} > 1.4422 > 1$$

(1) holds for Case 2.

Case 3:

$$3^{\frac{2}{3}} = 3^{\frac{2}{3}} > 2.0800 > 2$$

(1) holds for Case 3.

Case 4:

$$3^{\frac{3}{3}} = 3$$

(1) holds for Case 4.

Case 5:

$$3^{\frac{4}{3}} > 4.3267 > 4$$

(1) holds for Case 5

**Case 6:** The proof for this case is by the WOP. Let C be the set of counterexamples to (1). We will prove by contradiction that C is empty. Suppose that C is not empty. By the WOP, there is a least  $m \in C$ . Since (1) holds in Cases 1-5, we know that  $m \geq 5$  and  $m-4 \in \mathbb{N}$ . Since m is the least element in C, (1) must hold for m-1:

$$m - 1 \le 3^{\frac{m-1}{3}}$$

$$(m-1)^3 \le 3^{m-1}$$

$$3 \cdot (m-1)^3 \le 3^m$$
Since  $m \in C, m > 3^{\frac{m}{3}} \implies 3^m < m^3$ 

$$3 \cdot (m-1)^3 \le 3^m < m^3$$

$$\frac{(m-1)^3}{m^3} < \frac{1}{3}$$

$$\frac{m-1}{m} < \frac{1}{3^{\frac{1}{3}}}$$

$$1 - \frac{1}{m} < \left(\frac{1}{3}\right)^{\frac{1}{3}}$$

$$\frac{1}{m} > 1 - \left(\frac{1}{3}\right)^{\frac{1}{3}}$$

$$m < \frac{1}{1 - \left(\frac{1}{3}\right)^{\frac{1}{3}}} < 3.2612$$

This is a contradiction since we established by Cases 1-5 that  $m \geq 5$ . Therefore, C is empty and (1) holds for Case 6.

(1) holds for Cases 1-6. Therefore, (1) must be true.

## 3.1 (a)

Prove by truth table that

$$(P \implies Q) \lor (Q \implies P) \tag{2}$$

is valid.

Proof.

P	Q	$(P \implies Q)$	$\vee$	$(Q \implies P)$
T	T	T	$\mathbf{T}$	T
T	F	F	${f T}$	T
F	T	T	${f T}$	F
F	F	T	$\mathbf{T}$	T

(2) evaluates to True in all of the rows of its truth table. Hence, (2) is valid.  $\hfill\Box$ 

### 3.2 (b)

$$R ::= (P \wedge Q) \vee (\neg P \wedge \neg Q)$$

I.e.  $R \equiv P \iff Q$ .

#### 3.3 (c)

Explain why

$$Q ::= Pisvalid \iff \neg P$$

is not satisfiable.

 $A \iff B$  is True only when A and B are both True or when A and B are both false. If P is valid is True, then  $\neg P$  is always False. Hence, Q is not satisfiable.

#### 3.4 (d)

Let

$$S ::= \neg P_1 \vee \neg P_2 \vee ... \neg P_k$$

S is True iff at least one of the  $P_i$ 's are False. Hence,  $P_1,...,P_k$  is not consistent iff S is valid.

#### 4.1 (a)

$$p_0 ::= \neg a_0$$
$$c ::= a_0$$

#### 4.2 (b)

If b = 1, we add 1 to a. Otherwise, a is unchanged:

$$o_i = (b \wedge p_i) \vee (\neg b \wedge a_i)$$

#### 4.3 (c)

c=1 only if  $a_i=1$   $\forall i$  such that  $0 \leq i \leq a_{2n+1}$ . However, if this is the case, then both of the single size add1-modules carry. Hence:

$$c = c_{(1)} \wedge c_{(2)}$$

### 4.4 (d)

If the lower half does not carry, the upper half should remain unchanged. I.e. output of the upper half should be equal to its input. On the other hand, if the lower half does carry, the upper half should be incremented by 1. I.e. the output of the upper half should be equal to the output of the upper single-size add1=module. Hence:

$$p_i = (\neg c_{(1)} \land a_i) \lor (c_{(1)} \land r_{i-(n+1)})$$

#### 4.5 (e)

We found that there is 1 propositional operator for computing each output bit of a add-1 module. Furthermore, up to two more gates can be added for the upper bits when choosing between the output of the upper add-1 module and the raw input. I.e. the number of gates on the path from the input to output of any given bit of a add1-module is bounded by a constant: 3.

One may object by pointing out that the carry of the lower add-1 module must resolve before we can choose the output of the upper module. However, the power of the parallel half-adder is that we can grow it by adding add-1 modules of a constant size such that we only ever need to wait for one level of add-1 modules to resolve. The number of operators on the output path of the ripple carry half-adder, however, continues to increase. Hence, for each subsequent doubling of n, the latency of the parallel half adder remains nearly constant (but not quite; part (b) shows us that two gates are added to the maximum output

path for each add-1 module added; the rate of growth is actually proportional to  $\log_2 n$ ) for each doubling of n while latency of the ripple carry half-adder continues to double.