Overview

The IObundle KNN core provides an implementation of the KNN algorithm. It is written in C language and includes a peripheral described in Verilog that accelerates the execution. This circuit allows the processing of multiple test points in parallel, thereby increasing the performance of the algorithm implementation in comparison with the original sequential execution on the software end.

Features

- Verilog KNN algorithm accelerator.
- Read/write data from/to hardware(Reset, enable, test point, data point and neighbours' label).
- IOb-SoC native CPU interface.
- AXI4 Lite CPU interface (premium option).

Benefits

- Compact hardware implementation
- Can fit many instances in low cost FPGAs
- Can fit many instances in small ASICs
- Low power consumption
- Accelerates the algorithm's implementation

Deliverables

- Verilog source code
- User documentation
- Example integration in IOb-SoC (premium)
- FPGA synthesis and implementation scripts (premium)
- ASIC synthesis and place and route scripts (premium)

Block Diagram

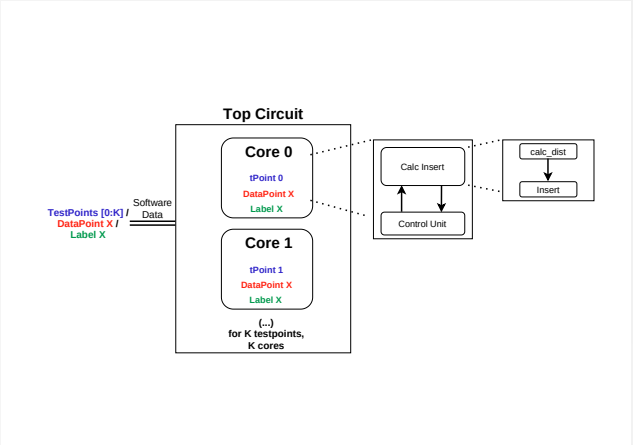

Figure 1: High-level block diagram

FPGA Results

The following are FPGA implementation results for two FPGA device families.

LUT'S	796
Registers	1690
DSP's	8
BRAM	0
Resource	**Used**

Table 1: Implementation Resources for Xilinx Kintex Ultrascale Devices

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.