CMPE 413

Fall 2023

Lab 2: Schematic Design and Simulation

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Friday 1:00-4:00

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1. Objective

The first objective of this lab is to design multiple schematics including an inverter, NOR, and NAND gate using the schematic editor. The second objective is to simulate the rise/fall time/delay of the schematics.

2. Schematic and Simulation

2.1: Minimum Sized Inverter

In 2.1 the task is to simulate one inverter with four inverters a load. The goal of this is to change the PMOS width to find the perfect ration between W and L for an inverter. The goal was to find a width where the rise and fall times only have a difference in 5%. The width found that resulted in this was 2.4 uM as shown in Table 1.

Table 1

PMOS Width	Rt	Ft	Rd	Fd
1.5	0.45	0.26	0.2	0.13
1.65	0.426	0.279	0.191	0.137
1.8	0.407	0.296	0.182	0.144
1.95	0.392	0.311	0.174	0.152
2.1	0.379	0.326	0.168	0.159
2.25	0.369	0.341	0.162	0.167
2.4	0.361	0.356	0.158	0.174

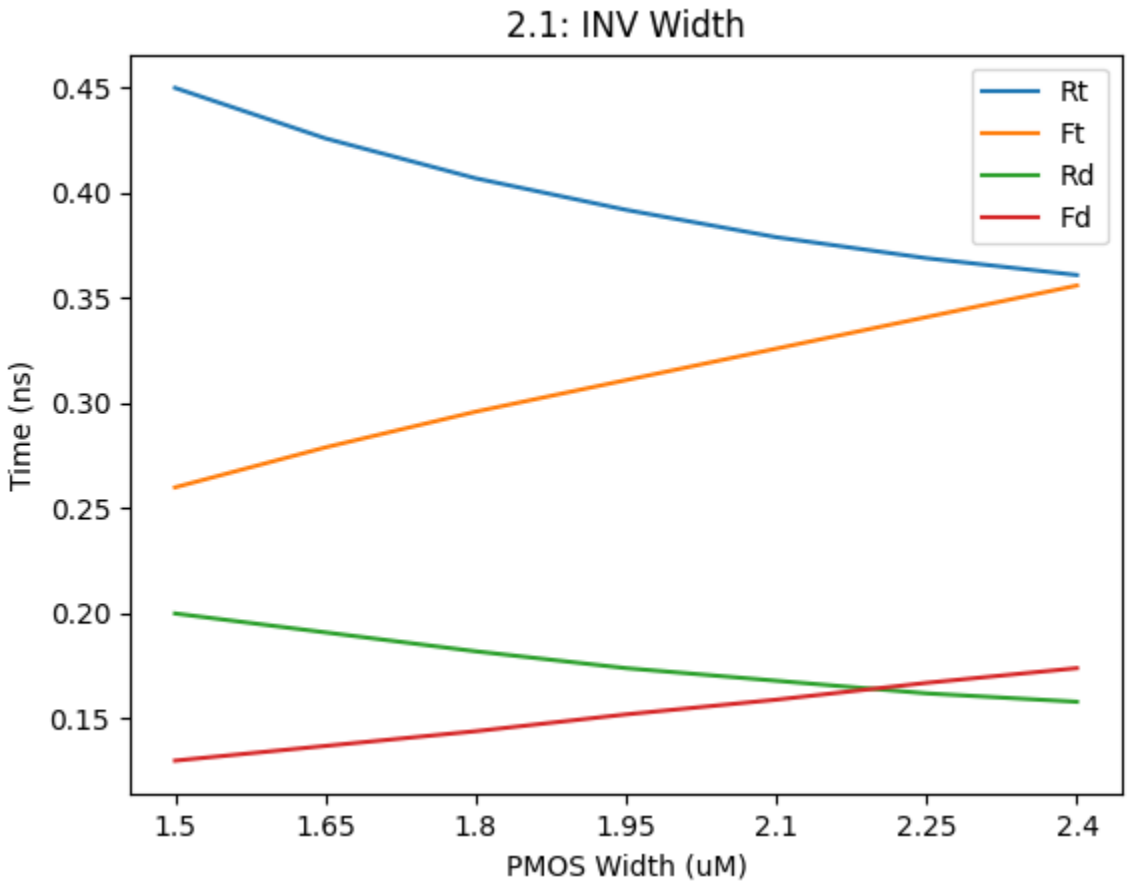
2.1: INV Width
Rt
Ft
Rd
Fd
0.45
0.40
0.35
0.30
0.25
0.20
0.15
Time (ns)
1.5
1.65
1.8
1.95
2.1
2.25
2.4
PMOS Width (uM)

Figure 1

2.2: Varying Load Simulation

The task in 2.2 is to simulate how a change in load capacitance will affect the rise and fall times of an inverter. This was done by changing the load between 16, 8, 4, 2, and 1 as shown in Figure 2. As the load increased exponentially, the rise and fall times also grew exponentially as shown in Table 2 and Figure 3.

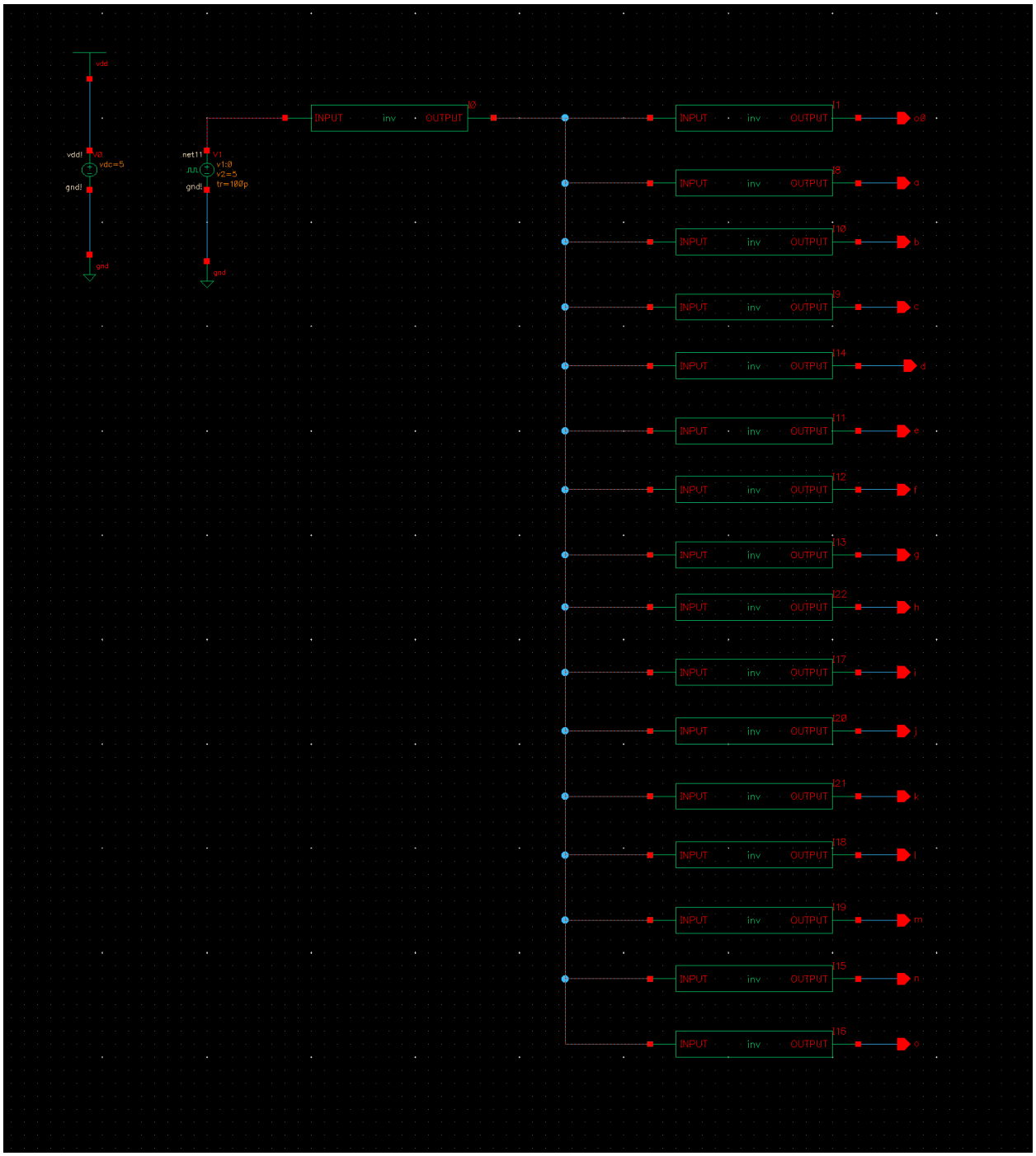

Figure 2

Table 2

	Rt	Ft	Rd	Fd
1	0.151	0.143	0.082	0.093
2	0.228	0.218	0.107	0.12
4	0.361	0.356	0.158	0.174
8	0.621	0.62	0.264	0.285
16	1.143	1.145	0.479	0.509

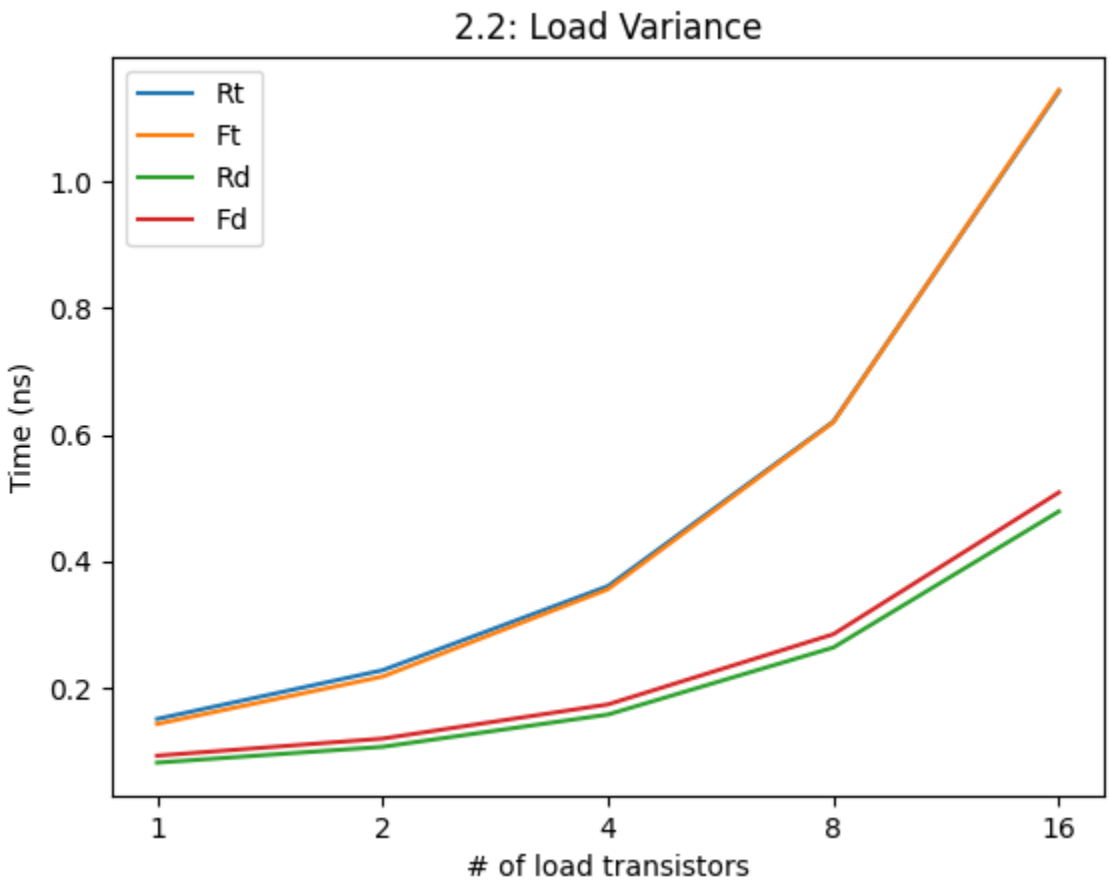

Figure 3

2.3: 2x and 4x Size

The task for 2.3 was to simulate an inverter with 2x and 4x dimensions against a varying load size as shown in . The load varied between 16, 8, 4, 2, and 1 inverters like in 2.2. The results showed the increase in speed of the pull up and pull down networks as width increased. This increase was not exponential like you would expect with the exponential increase in size as you would expect. These results are shown in Table 3, Figure 5, and Figure 6.

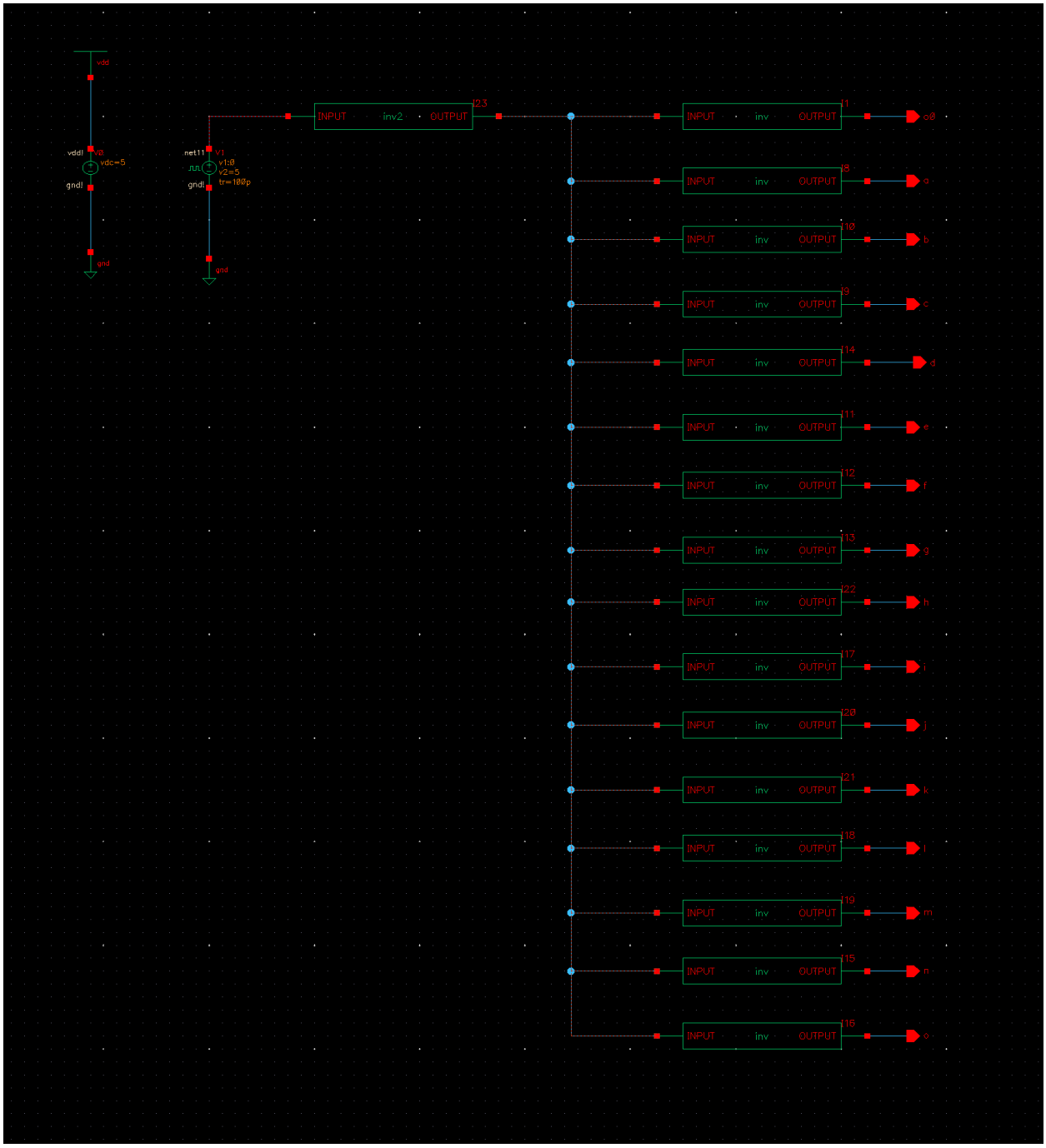

Figure 4

Table 3

2x	Rt	Ft	Rd	Fd
1	0.091	0.086	0.064	0.065
2	0.131	0.112	0.072	0.072
4	0.202	0.176	0.097	0.096
8	0.327	0.292	0.143	0.139
16	0.564	0.51	0.238	0.228
4x				
1	0.086	0.065	0.05	0.054
2	0.099	0.078	0.061	0.05
4	0.122	0.101	0.071	0.067
8	0.192	0.158	0.092	0.086
16	0.311	0.267	0.135	0.125

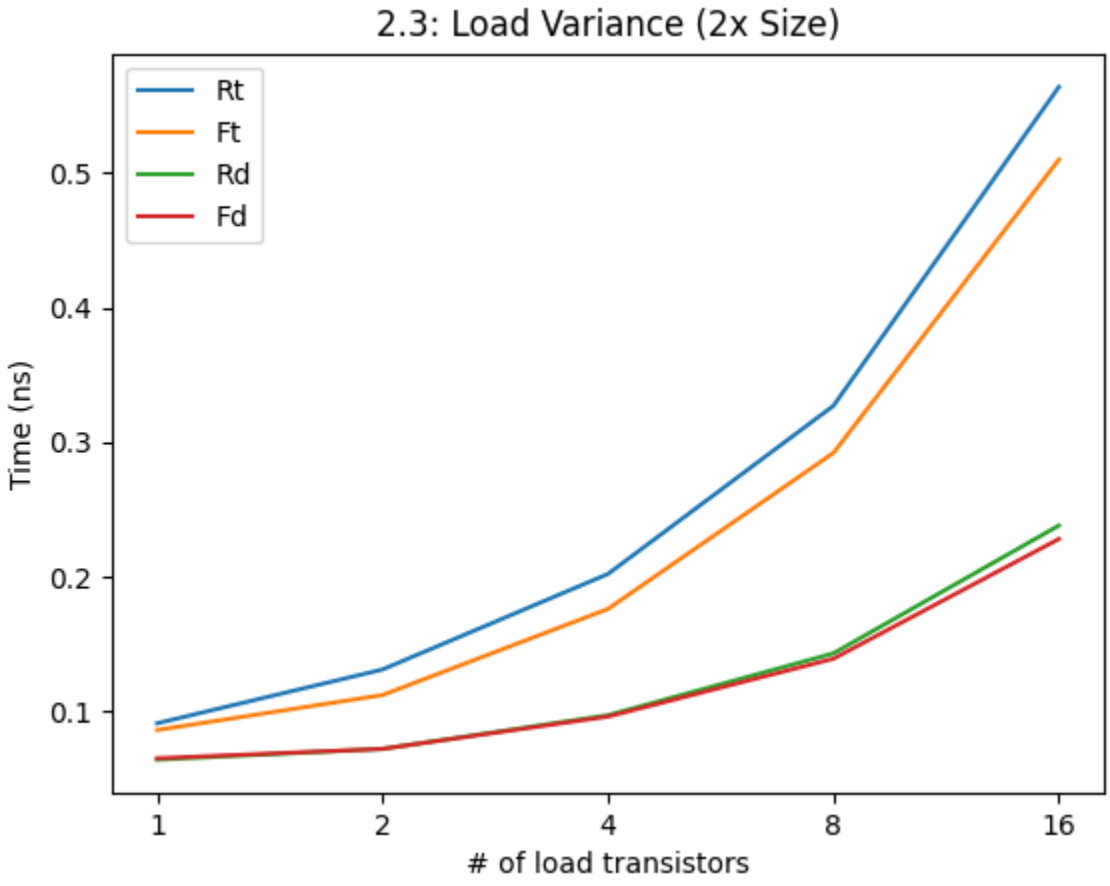

Figure 5

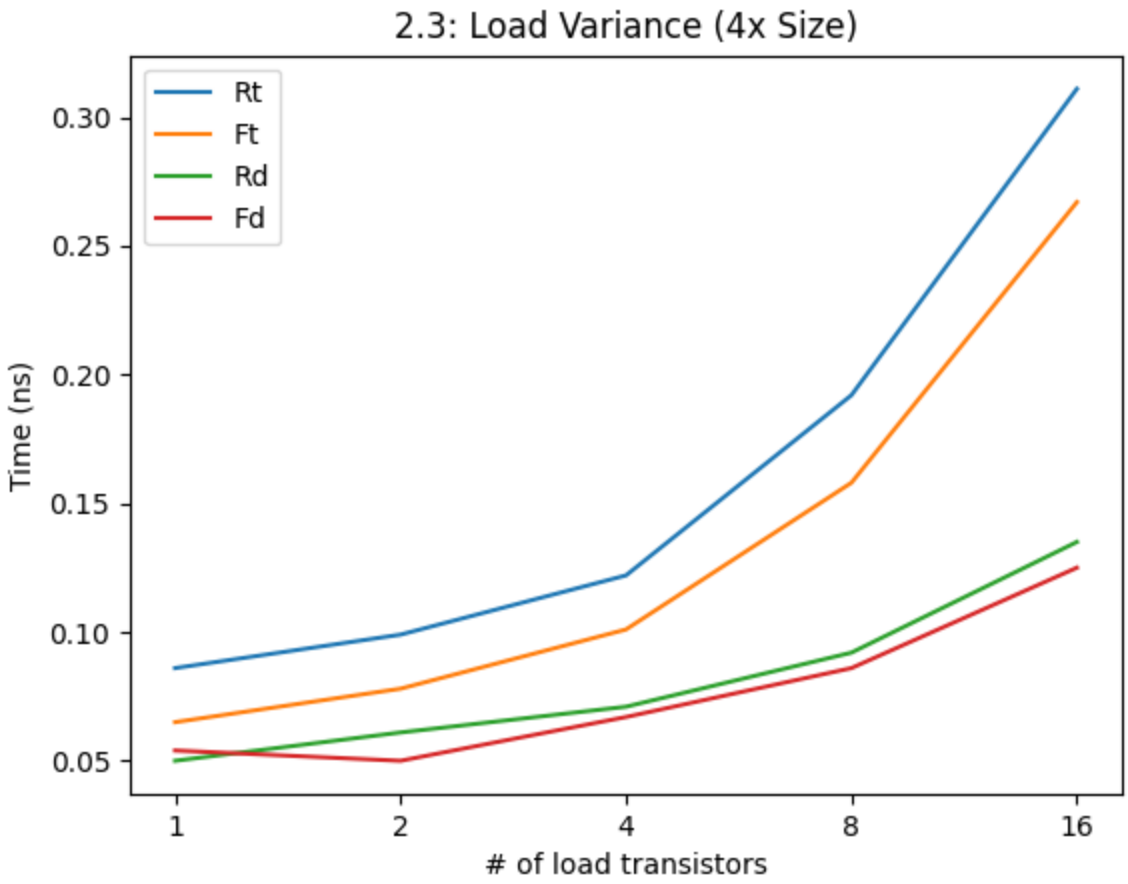
2.3: Load Variance (4x Size)
Rt
Ft
Rd
Fd
0.30
0.25
0.20
0.15
0.10
0.05
Time (ns)
1
2
4
8
16
# of load transistors

Figure 6

2.4: NAND and NOR

The task in 2.4 was to model a NAND and NOR gate against a variable load. The factor modeled was the difference between varying input A or input B to switch the output. The load varied between 4, 2, and 1 load resistors as shown in Figure 7. The results were interesting with the B input being significantly faster on the NOR gate and the A inputs being significantly faster on the NAND gates. Another interesting finding was that the NOR gates speed was only affected on the falling edge and the NAND gates speed was only significantly affected on the rising edge. This means that the networks in series were faster than the networks in parallel, the opposite of natural intuition. This maybe do to the capacitance of the opposite network.

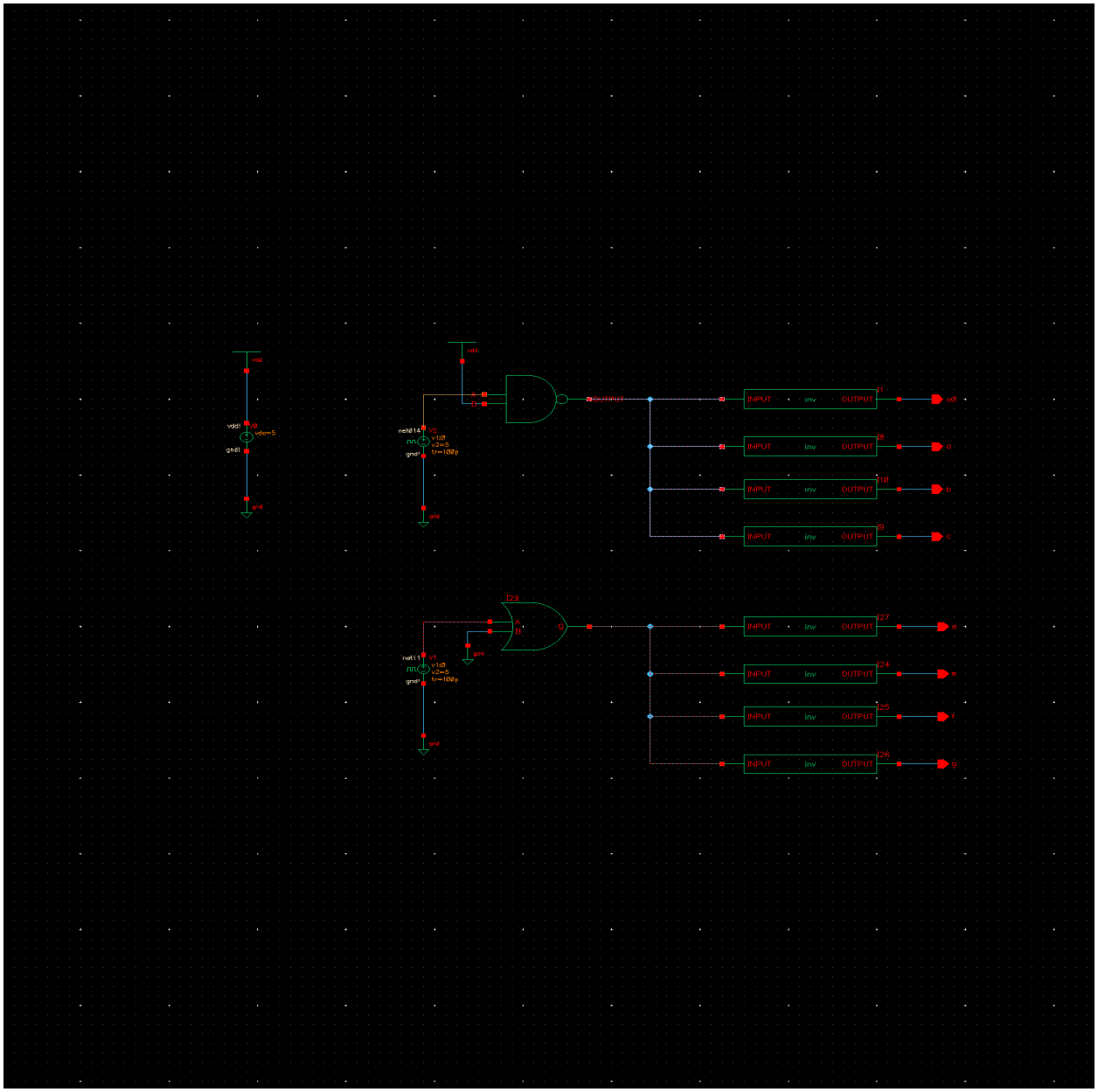

Figure 7

Table 3

NOR	Rt	Ft	Rd	Fd
A1	0.246	0.374	0.141	0.241
B1	0.236	0.21	0.093	0.113
A2	0.306	0.442	0.163	0.27
B2	0.297	0.282	0.115	0.174
A4	0.423	0.575	0.207	0.328
B4	0.413	0.418	0.158	0.23
NAND				
A1	0.215	0.181	0.121	0.088
B1	0.315	0.183	0.176	0.146
A2	0.287	0.235	0.146	0.106
B2	0.383	0.237	0.202	0.132
A4	0.421	0.337	0.199	0.142
B4	0.516	0.339	0.255	0.168

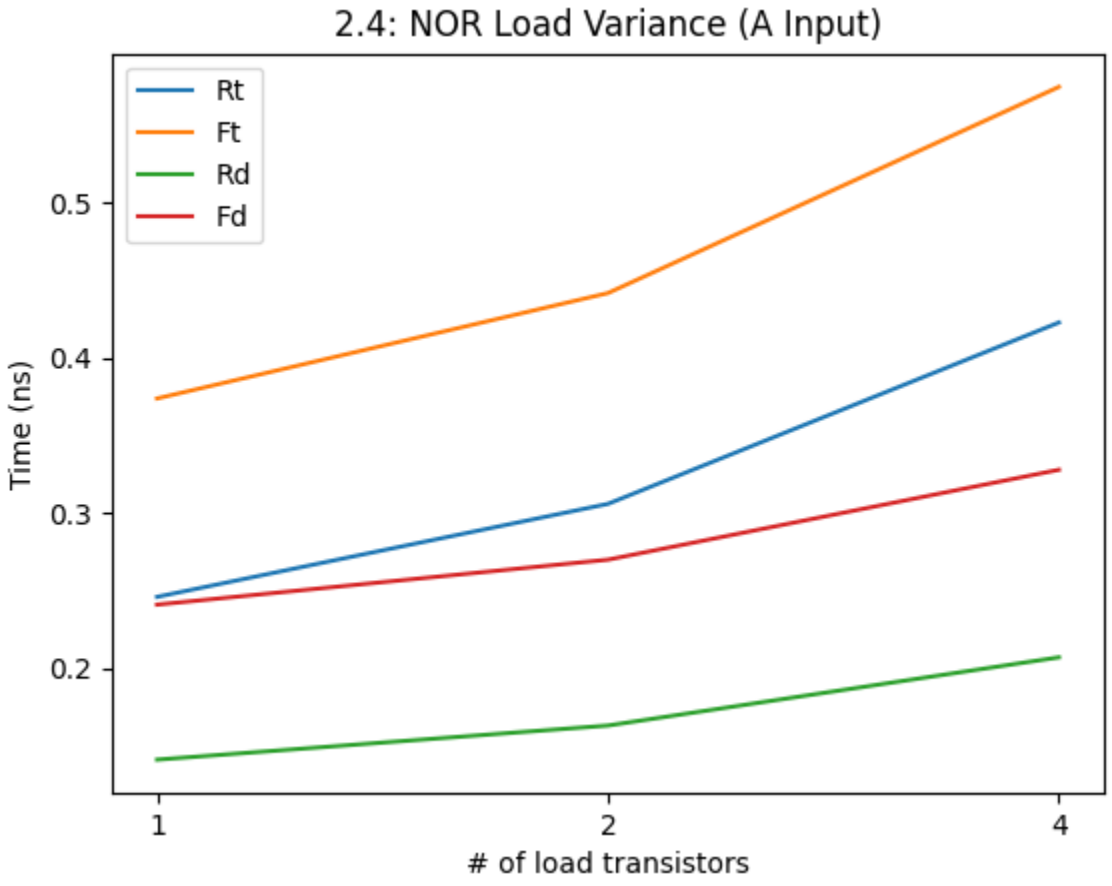

Figure 8

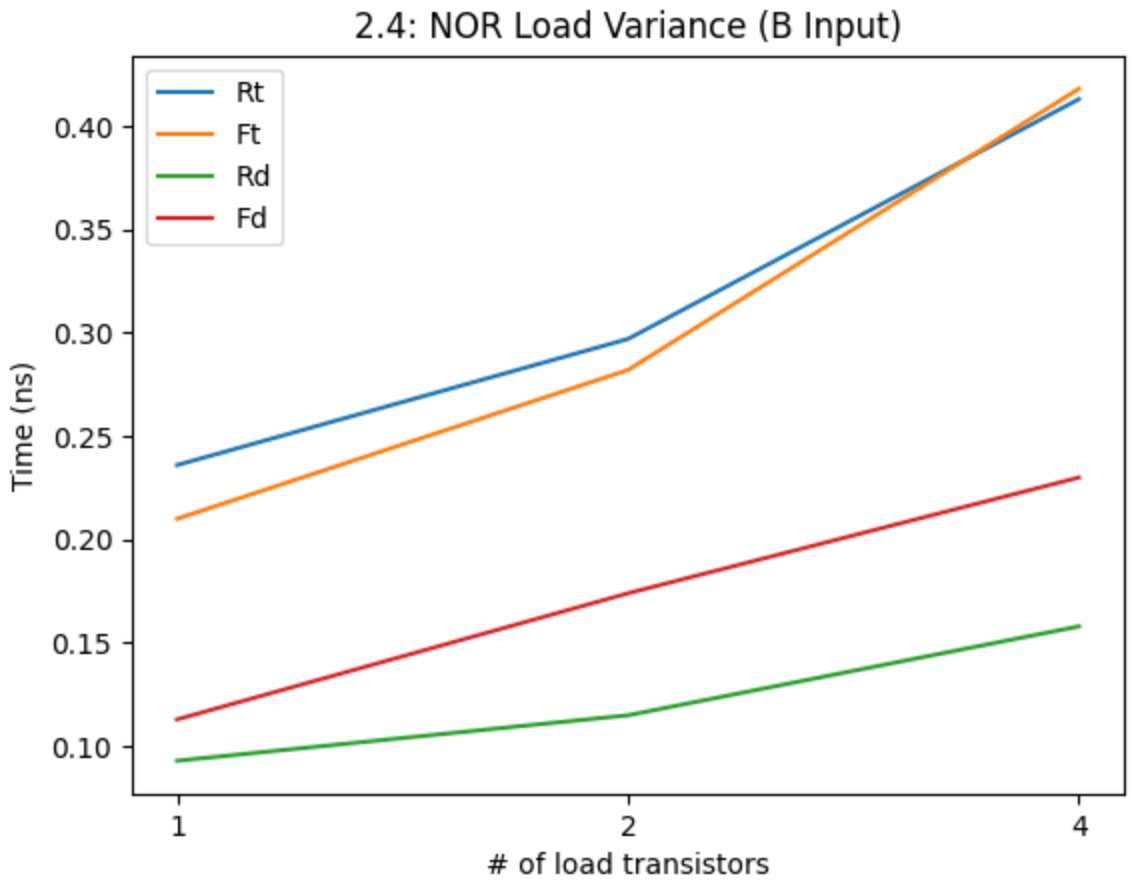
2.4: NOR Load Variance (B Input)
Rt
Ft
Rd
Fd
0.40
0.35
0.30
0.25
0.20
0.15
0.10
Time (ns)
1
2
4
# of load transistors

Figure 9