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CMPE 316

Homework 2

Problem: Use System Verilog to design and implement a microcontroller ALU. Create a testbench to test the module and verify it with a waveform output.

Hardware Interconnect Description

Signal Name	Width	Direction	Board Pin	Registered	Description
clk	1	input	N/A	no	Clock
rst	1	input	N/A	no	Reset
data_rd	8	input	N/A	yes	Register rd input
data_rr	8	input	N/A	yes	Register rr input
ci	1	input	N/A	yes	Carry flag input
opcode	8	input	N/A	yes	Opcode input
data_o	16	output	N/A	yes	Data out output
co	1	output	N/A	yes	Carry flag output
no	1	output	N/A	yes	Negative flag output
zo	1	output	N/A	yes	Zero flag output

Simulation results: