

Electronics

$$W = QV$$

$$1 \text{ eV} = 1.602 \times 10^{-19}$$

$$I_0 = I_s (e^{(V_0/nV_T) - 1})$$

$$V_T = \frac{kT}{q} \quad K = 1.38 \times 10^{-23} \text{ J/K}$$

$$V_K = 0.7 V_{Si} \quad 0.3 V_{Cue}$$

$$V_K = 1.2 V \text{ (GaAs)}$$

$$R_D = \frac{V_D}{I_D} \quad n_{Si} = 2$$

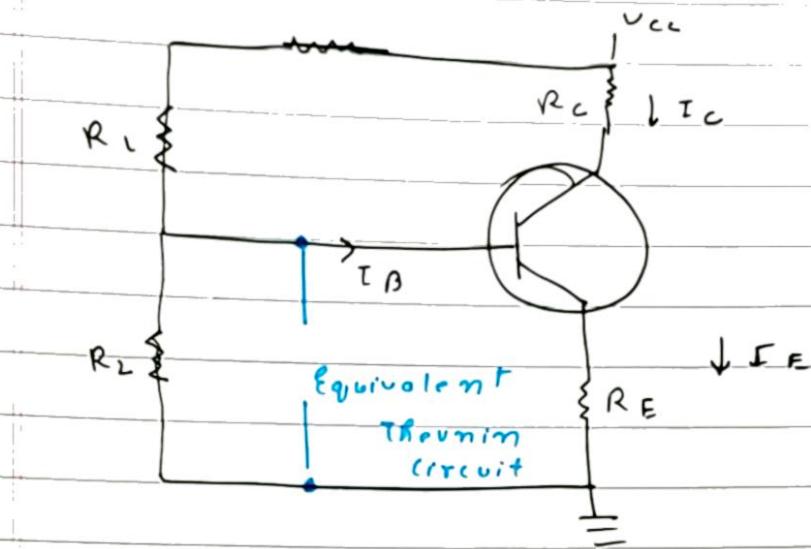
$$\gamma_d = \frac{nV_T}{I_D} \quad n_{Ge} = 1$$

$$I_S = I_{S0} \cdot (2)^{(DT/10)}.$$

$$V_{DC} = 0.318 V_m$$

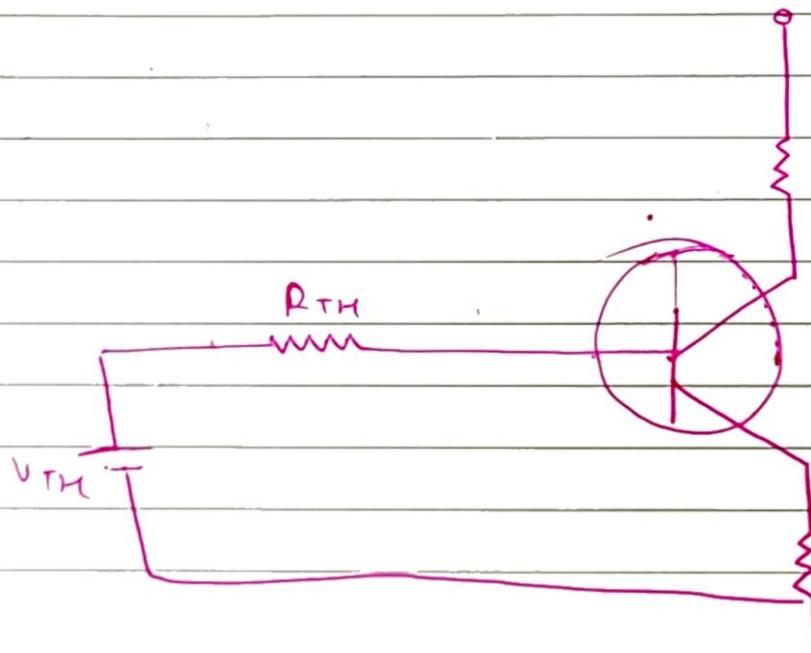
$$V_{rms} = \frac{V_{DC}}{\sqrt{2}}$$

Voltage Bias:



$$V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$



Input

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$

$$\begin{aligned} (I_E) &= (\beta + 1) I_Q \\ (\beta + 1) &= (\beta) \\ (\beta R_E) &\gg R_{TH} \end{aligned}$$

Output

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

↓

V_C = collector to ground.

$$V_E = I_E R_E$$

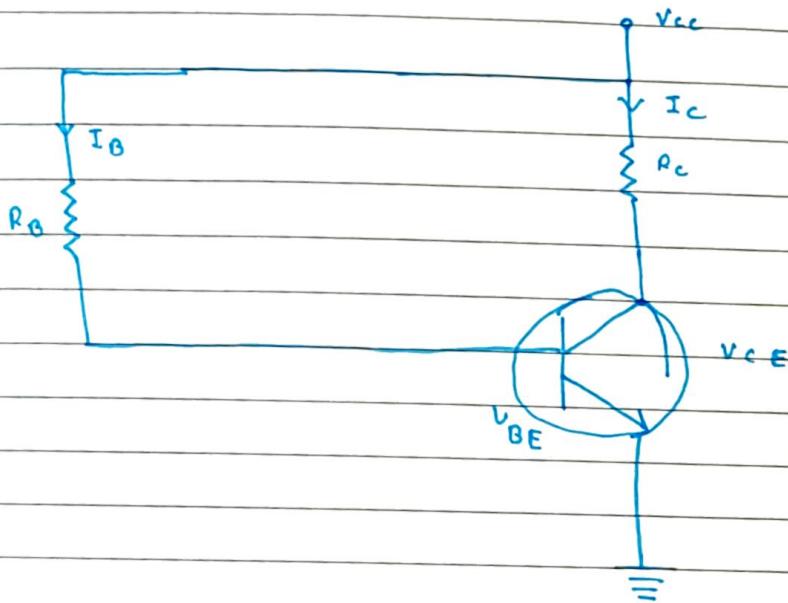
$$\beta I_Q = I_C = \frac{V_{TH} - V_{BE}}{R_E}$$

↓
No β independent of Temp

Biasing.

(common Emitter)

(Fixed Bias)



Input Characteristics.

$$V_{cc} - I_B R_B - V_{BE} = 0 \quad \text{--- (1)}$$

Output Characteristics.

$$V_{cc} - I_C R_C - V_{CE} = 0$$

b/w V_{CE} & I_C . Graph

Study the Variation properly.

$$V_{CE} = V_{cc} - I_C R_C \rightarrow \star\star$$

↳ eq of line

* From the bjt explain the graph acc
ordingly

$R_C \rightarrow$ changed }
 $V_{cc} \rightarrow$ changed }
 $R_B \rightarrow$ changed } decision
graph

Transistor Configuration

- All things are conceptual explain the graph on the basis of configuration You must know how the Eq & graph works.

All the regions saturated, unsaturated, cutoff (Active)

saturated - E-B junction & C junction forward

Active - E-B junction f.b & C junction R.B

Cutoff - Both junction Reverse Bias.

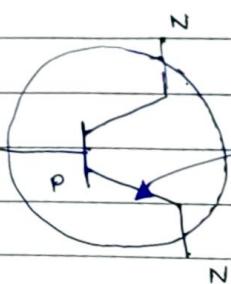
* Theory Concept Should be
Nice

$$\text{Common Emitter} \quad V_{CE} = V_{CB} + V_{BE} \longrightarrow *$$

B J T.

- * Emitter \rightarrow Highly doped (moderate)
- Base \rightarrow lightly doped (length small)
- Collector \rightarrow Moderately doped (Biggest)

Symbols.



→ always from p to N
blue base & emitter.

Equations.

- * For working of transistor E-B junction is always forward biased & B-C junction is Reverse Biased.

$$I_E = I_C + I_B$$

$$I_C = \alpha I_E + I_{CBO}$$

$I_{CBO} =$ Reverse sat Current when Emitter is open.
 $\rightarrow 10^{-6}$ (can be neglected).

α common-base dc current gain

* I_{CBO} also doubles for every change of $10^\circ C$.

* $I_C = R_{dc} I_B + I_{CEO}$

$$= \beta_{dc} I_B + I_{CEO}$$

// $\beta = \frac{\alpha}{1-\alpha}$ // $I_{CEO} = (\beta + 1) I_{CBO}$

Graphs

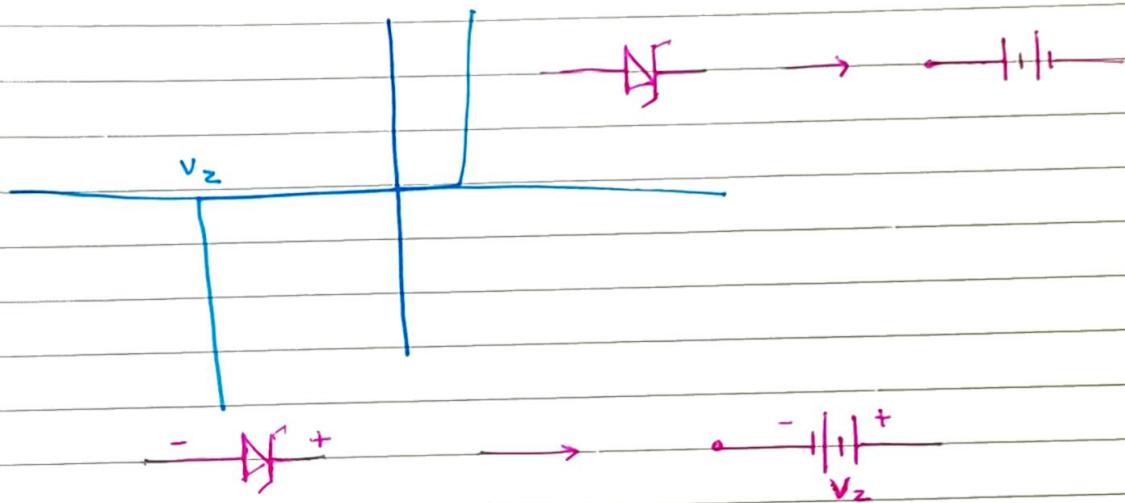
Input

$$\delta i^o = \frac{\Delta V_{EB}}{\Delta I_E} \quad (V_{CB} \text{ const})$$

$$A_v = \frac{\Delta V_{CB}}{\Delta V_{EB}} \quad (\text{Amplification factor})$$

$(I_E \text{ const})$

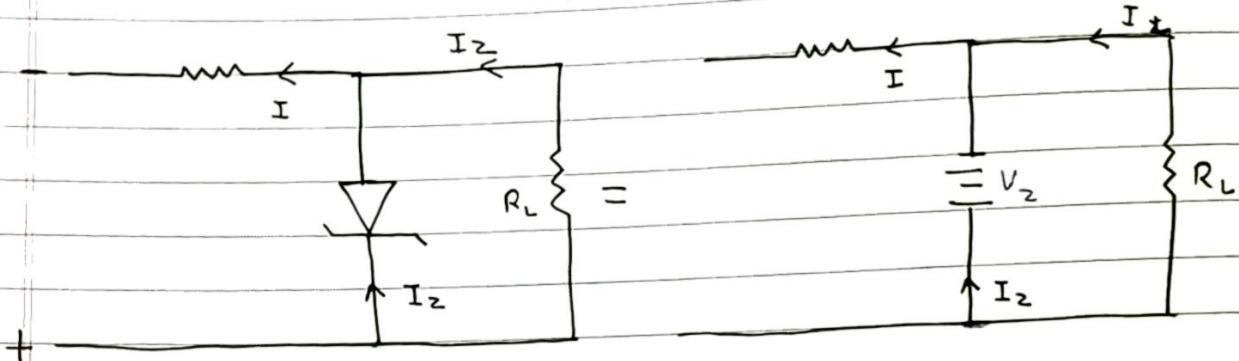
Zener Voltage



- * Zener diode is heavily doped;
- * Depletion layer will be thin. breakdown voltage $\downarrow \downarrow$



Voltage Regulator.



$$I = I_z + I_L$$

$$I = I_z + \frac{V_z}{R_L}$$

Const V_z across $R_L \rightarrow \star$

~~MATC~~
Ideal Values
are represented
in blocks.

CLASSMATE		
Test		
Date		
Page		

$$V_o = A_d (V_1 - V_2) + A_{cm} \left[\frac{V_1 + V_2}{2} \right]$$

(∞) (0)

Common-mode rejection ratio

It is a measure of ability of op-amp to reject signals common to both input terminals. (Noise) it

$$CMRR = \frac{A_d}{A_{cm}} \quad (\infty)$$

$$(CMRR)_{dB} = 20 \log_{10} \left(\frac{A_d}{A_{cm}} \right)$$

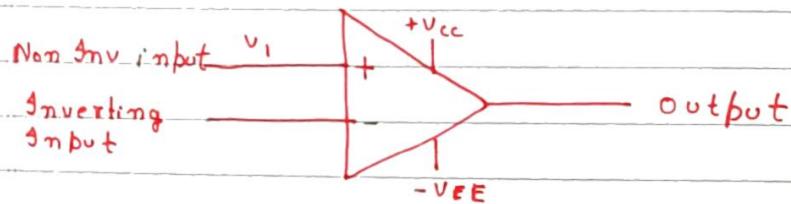
Terminology

* **Bandwidth** - Range of freq over which gain of OPAMP is almost const. (∞)

* **V_{oo} (output offset)** = V_{out} when input voltage are zero

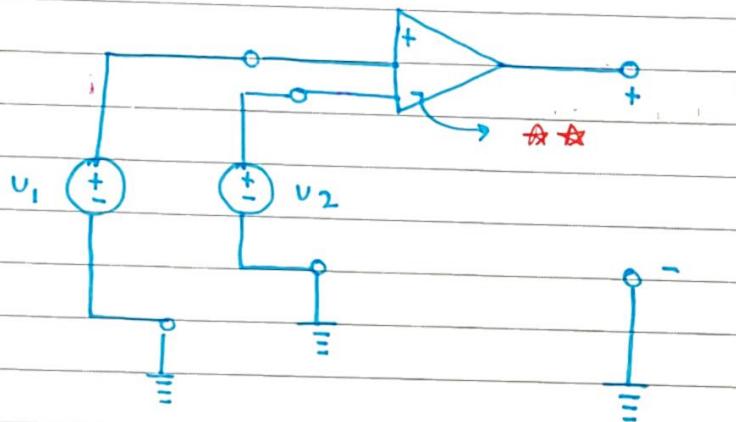
* **V_{io} (input offset)** = Difference in V_{in} when $V_o = 0$

Op - Amp



$A = \text{Large Signal Voltage Gain}$

Open - Loop Configuration



$$A_{OL} = \frac{V_o}{V_i}$$

- * Input offset current - It is difference between input current when both input voltages are 0.
 - (I_{io})
 - (o)

$$I_{io} = |I_1 - I_2|$$

- * Input bias current (I_{ib}) - It is the avg of current when both input voltages are zero.

$$I_{ib} = \frac{(I_1 + I_2)}{2}$$

- * Slope rate - Maximum rate of change of output voltage wrt to time.

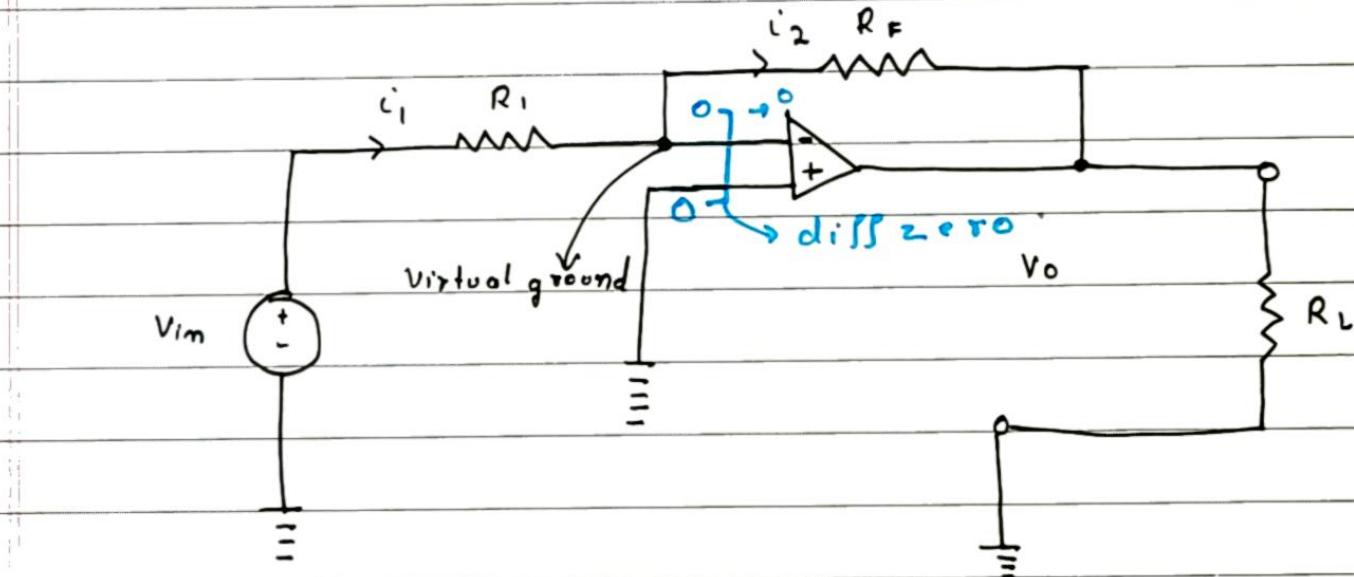
- * SVRR - Maximum rate at which Input offset voltage of OPAMP changes with change in supply voltage

* Voltage difference b/w input terminal is 0

* Current Entering into OPAMP through its terminal is zero

Always Valid.

Inverting Amplifier

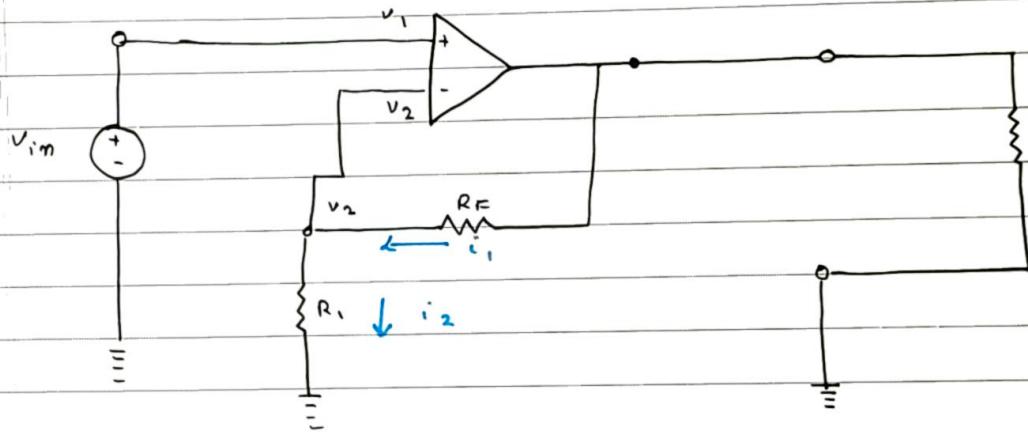


$$i_1 = i_2$$

$$V_o = - V_{in} \frac{R_F}{R_i} \quad \left. \right\} \rightarrow \text{Source.}$$

$$A_v = \frac{V_o}{V_{in}} = - \frac{R_F}{R_i}$$

Non Inverting Amplifier

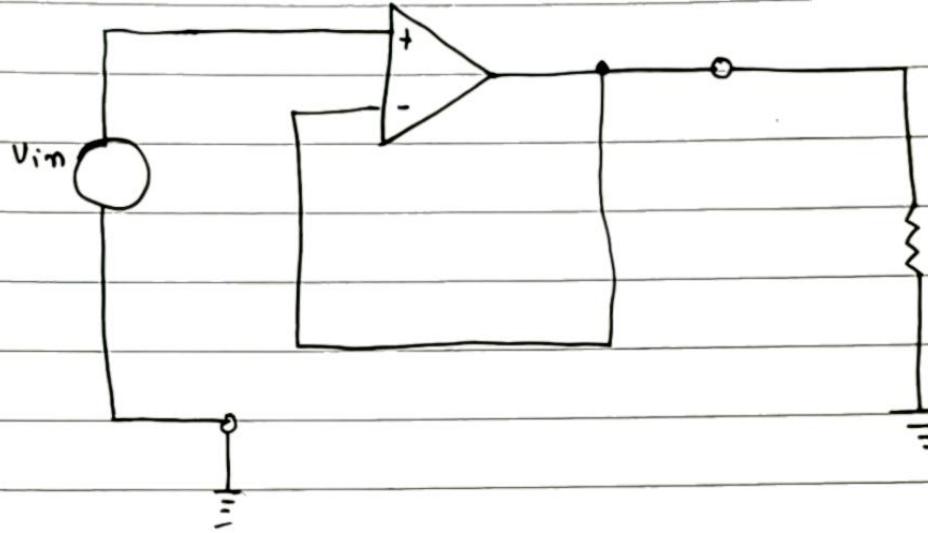


$$V_1 = V_2 = V_{in}$$

$$i_1 = i_2$$

$$\frac{V_o - V_{in}}{R_F} = \frac{V_2}{R_i} \quad \left. \right\} \rightarrow s$$

$$V_o = V_{in} \left(1 + \frac{R_F}{R_i} \right) \rightarrow \text{Ans.}$$

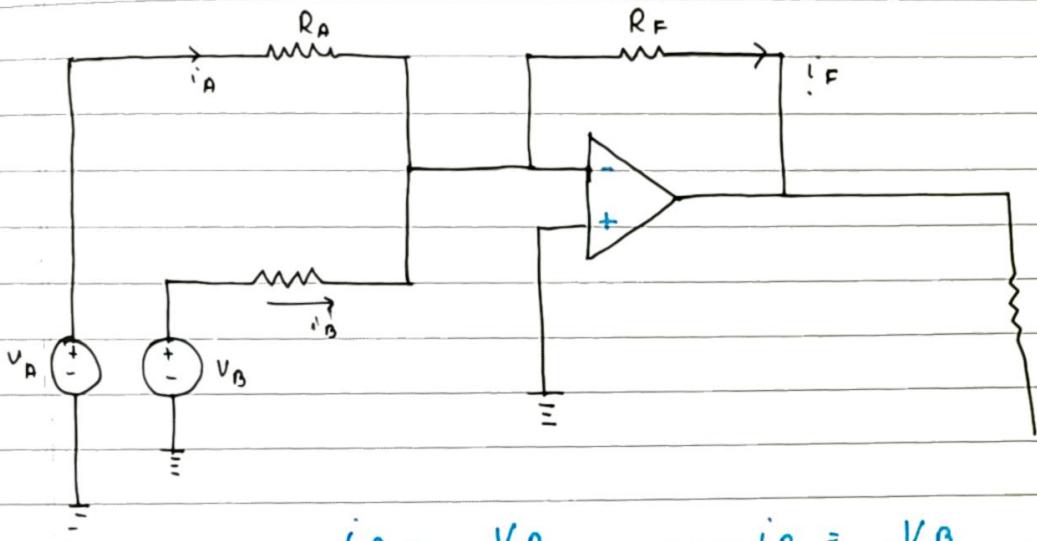


$$V_o = V_{in}$$

used as buffer for impedance matching

Voltage gain = 1

Summing Amplifier



$$i_A = \frac{V_A}{R_A}, \quad i_B = \frac{V_B}{R_B}$$

$$i_F = i_A + i_B$$

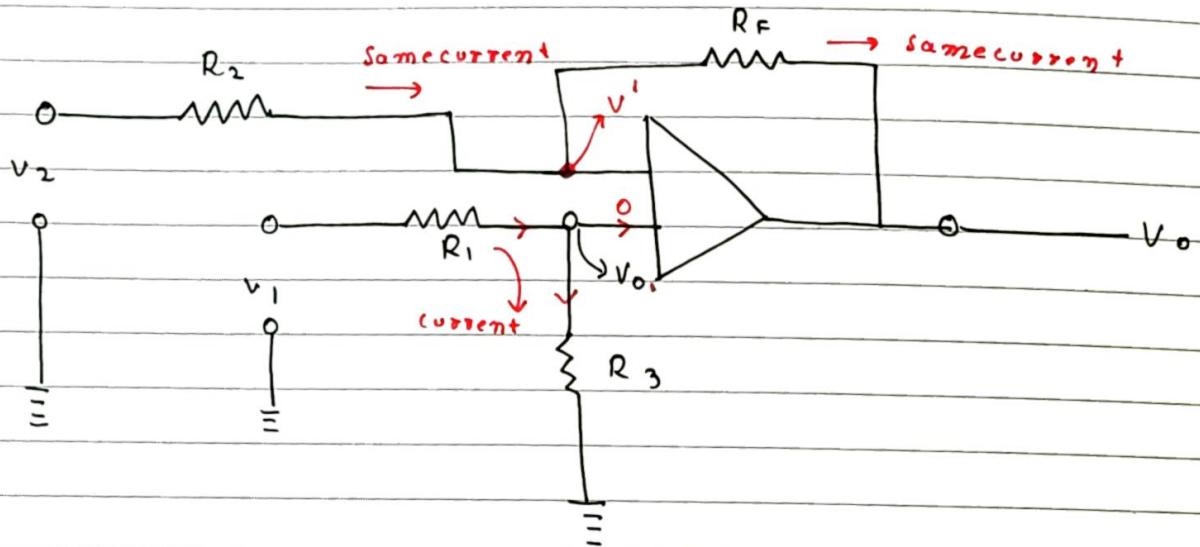
$$-\frac{V_o}{R_F} = \frac{V_A}{R_A} + \frac{V_B}{R_B}$$

$$V_o = - \left[V_A \frac{R_F}{R_A} + V_B \frac{R_F}{R_B} \right] \rightarrow \star$$

$$R_F = R_A = R_B$$

$$V_o = - [V_A + V_B]$$

Difference Amplifier



$$I = \frac{V_1}{R_1 + R_3} = V_{o1} = \frac{V_1 R_3}{R_1 + R_3}$$

$$[V_{o1} = V']$$

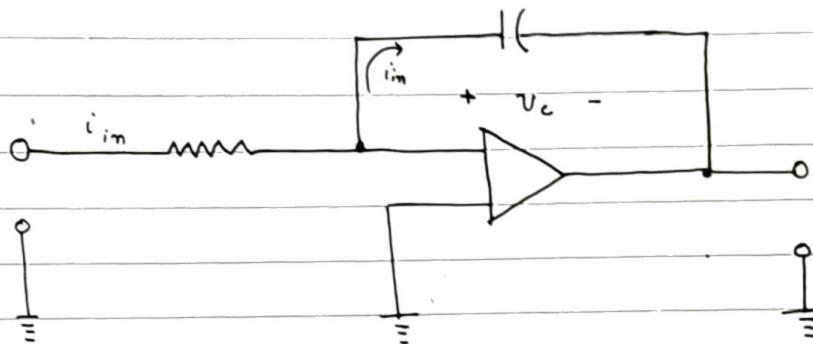
$$\frac{V_2 - V'}{R_2} = + \frac{V' - V_o}{R_F}$$

$$\frac{V_2}{R_2} - V' \left[\frac{1}{R_2} + \frac{1}{R_F} \right] = - \frac{V_o}{R_F}$$

$$V' \left[\frac{R_F + 1}{R_2} \right] - \frac{V_2 R_F}{R_2} = V_o$$

$$V_o = \left(\frac{V_1 R_3}{R_1 + R_3} \right) \left(1 + \frac{R_F}{R_2} \right) - V_2 \frac{R_F}{R_2}$$

Integrator

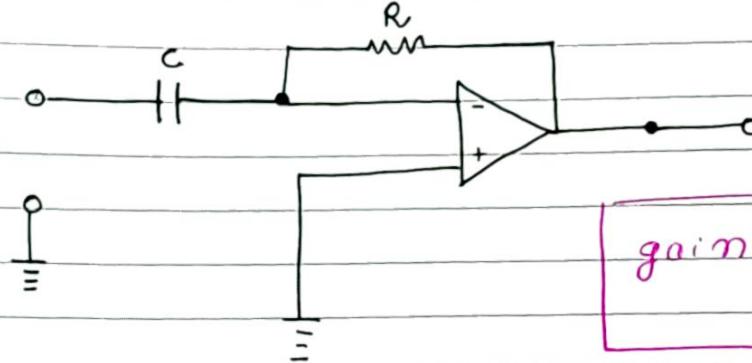


$$i_m = i_{in}$$

$$\frac{v_{in}}{R} = -C \frac{dv_o}{dt}$$

$$v_o = -\frac{1}{RC} \int_0^t v_{in} dt$$

Differentiator



low freq - less gain

high freq - More gain

$$\boxed{\text{gain} = \frac{R_f}{X_C}}$$

$\Rightarrow DC \rightarrow 0$

$$C \frac{dV_{in}}{dt} = - \frac{V_o}{R}$$

$$V_o = - RC \frac{dV_{in}}{dt}$$

] *gives*

Capacitance has $X_C = \frac{1}{2\pi f C}$

$f \gg$ high $\rightarrow X_C \rightarrow$ low.

Easy flow

DC content 0

capacitor only allows AC type
input voltage to pass through
whose freq is dependent on
rate of input sign.

Robta Bai