Pulse Multiplication in AC–DC Converters for Harmonic Mitigation in Vector-Controlled Induction Motor Drives

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***Abstract*—In this paper, an autotransformer with reduced kilovoltampere rating for 24-pulse ac-dc converter fed vector controlled induction motor drives (VCIMDs) is presented for harmonic current reduction. The 24-pulse operation is achieved using dc ripple reinjection technique in 12-pulse ac–dc converters. The proposed novel harmonic mitigator is found capable of suppressing up to 21st harmonic in the supply current. The procedure for the design of autotransformer for proposed ac–dc converter is presented to show the flexibility in the design for making it a cost-effective replacement suitable for retrofit applications, where presently a 6-pulse diode bridge rectifier is used. The effect of load variation on VCIMD is also studied to demonstrate the effectiveness of the proposed ac–dc converter. A set of power quality indices on input ac mains and on dc bus for a VCIMD fed from other 24-pulse ac–dc converters are also given to compare their performance. The laboratory prototypes of proposed autotransformers based 12-pulse and 24-pulse ac–dc converters are developed and test results are presented to validate the developed design procedure and the simulation models of these ac–dc converters under varying loads.**

***Index Terms*—Autotransformer, multipulse ac–dc converter, pulse multiplication, vector controlled induction motor drives (VCIMD).**

I. Introduction

THE rapid development of power electronics controllers in recent years has attracted the attention of researchers for making use of flexible characteristics of an induction motor in variable frequency drives. For this, the vector control [1] of induction motor drives has been widely used in high performance control systems like fans in heating, ventilating, and air conditioning (HVAC) systems, blowers, pumps for waste water treatment plants, etc. These VCIMD employ a 6-pulse diode bridge rectifier, (for rectifying the input ac voltage) which results in injection of current harmonics in the ac mains. These current harmonics while propagating through the finite source impedance result in voltage distortion at the point of common coupling, thereby affecting the nearby consumers. The widespread use of variable frequency drives has sharpened the focus on harmonics distortion generated by them. To have a control of these harmonics, an IEEE Std. 519 [2] has been reissued in 1992, giving the limits on current and voltage distortion.

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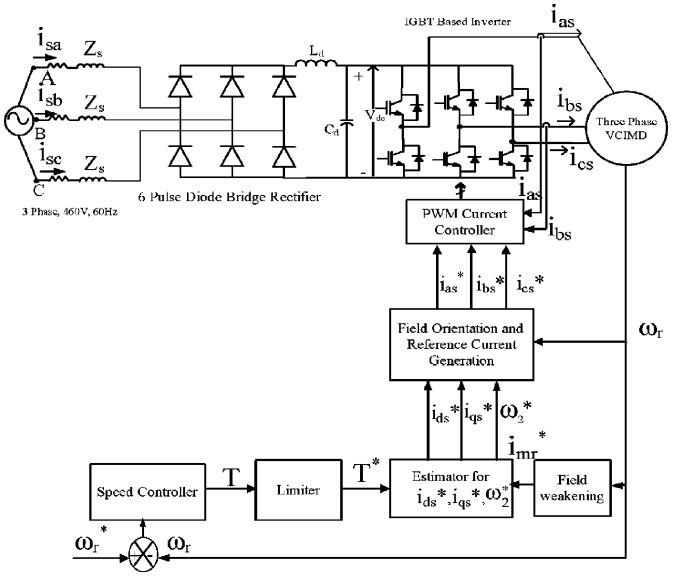

Fig. 1. Six-pulse diode bridge rectifier fed vector-controlled induction motor drive.

The mitigation of harmonics has been reported in the literature, using different techniques of increasing the number of rectification pulses [3]. These methods use two or more converters, where the harmonics generated by one converter are cancelled by other converter by appropriate phase shift. The autotransformer-based configurations provide the reduction in magnetics rating, as the transformer magnetic coupling transfers only a small portion of the total kilovoltampere of the induction motor drive. Various 12-pulse based rectification schemes [4]–[9] have been reported and used in practice for the purpose of line current harmonic reduction. It is known that increasing the number of pulses further results in reduction in current harmonics, but this is accompanied by an increase in cost as well as complexity. To increase the number of pulses without increasing the cost and complexity, dc ripple reinjection has been used [10], [11] for harmonic current reduction. One such configuration has been reported in [12], but the dc link voltage is higher than that of a 6-pulse diode bridge rectifier, thus making the scheme nonapplicable for retrofit applications. Paice [7] has reported 12-pulse based autotransformer fed ac–dc converter suitable for retrofit applications, but the rating of the magnetics is high.

This paper presents an autotransformer-based 24-pulse ac–dc converter with reduced magnetics rating and suitable for retrofit

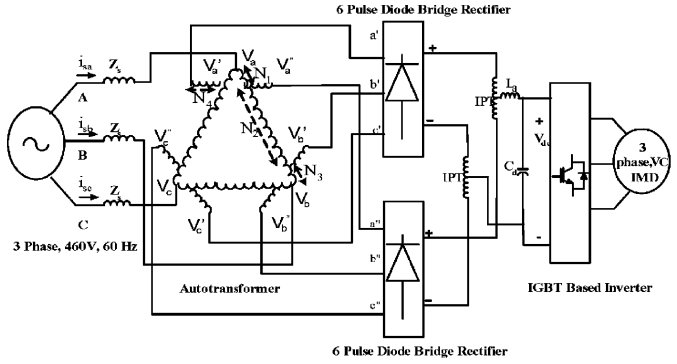

Fig. 2. Differential delta autotransformer-based 12-pulse converter (with phase shift of $+15^\circ$ and -15°) fed VCIMD. (Topology B.)

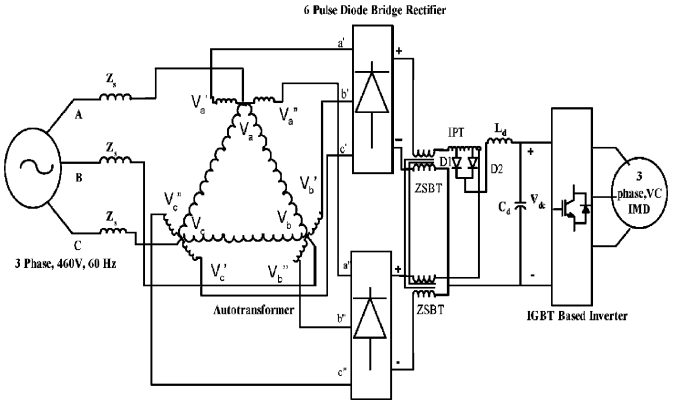

Fig. 3. Extended delta autotransformer-based 24-pulse converter fed VCIMD. (Topology C.)

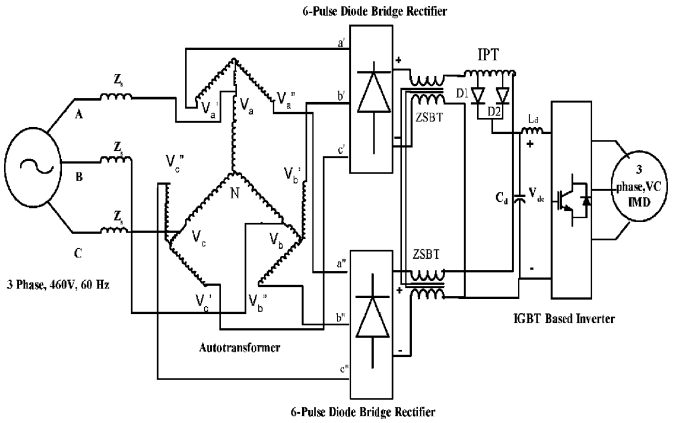

Fig. 4. Fork autotransformer-based 24-pulse converter fed VCIMD. (Topology D.)

applications (where presently 6-pulse converter is being used, as shown in Fig. 1 referred as Topology A). The presented technique for design of autotransformer provides flexibility in design to vary the output voltage to make it suitable for retrofit applications without much alteration in the system layout. This arrangement results in elimination up to 21st harmonic in the input line current. Further, a comparison of existing topologies has been made to demonstrate the effectiveness and the advantages of the proposed configuration. The proposed converter is able to achieve almost unity power factor in wide operating range of the drive. A set of tabulated results giving the comparison of different power quality parameters such as total harmonic distortion (THD) and crest factor of ac mains current (CF), power factor (PF), displacement factor (DPF) and distortion factor (DF), THD of supply voltage at PCC is presented for a VCIMD fed from an existing 6-pulse ac–dc converter, 12-pulse converter, various derived topologies of 24-pulse ac–dc converters, and proposed 24-pulse ac–dc converter. Moreover, various tests are conducted on the prototype autotransformers developed in the laboratory alongwith the interphase reactors and the zero sequence blocking transformer (ZSBT). The experimental results validate the simulation results for both 12-pulse and proposed 24-pulse ac–dc converters.

II. Circuit Configurations of 12-Pulse AC–DC Converters

For harmonic elimination, the required minimum phase shift is given by [3]

$$\text{Phase shift} = 60^\circ/\text{Number of six-pulse converters.}$$

For achieving 12-pulse rectification, the phase shift between the two sets of voltages may be either of 0° and 30° or $\pm 15^\circ$ with respect to the supply voltages. In this work various topologies based on $+15^\circ$ and -15° have been studied to reduce the size of the magnetics.

Fig. 2 shows the schematic diagram of the proposed differential delta autotransformer-based 12-pulse ac–dc converter with a phase shift of $+15^\circ$ and -15°, referred as Topology B. Similarly Fig. 3 shows the schematic diagram of an extended delta autotransformer [5] based 12-pulse ac–dc converter with a phase shift of $+15^\circ$ and -15° alongwith the pulse multiplication circuit, resulting in 24-pulse ac–dc converter, referred as Topology C.

Fig. 4 shows the schematic diagram of a fork autotransformer based 12-pulse ac–dc converter [7] with a phase shift of $+15^\circ$ and -15° alongwith the pulse multiplication circuit, referred as Topology D.

III. DC Ripple Reinjection in 12-Pulse AC–DC Converters

Fig. 5 shows the proposed reduced rating differential delta autotransformer-based 24-pulse ac–dc converter fed VCIMD. This configuration needs one ZSBT to ensure independent operation of the two diode rectifier bridges. It exhibits high impedance to zero sequence currents, resulting in 120° conduction for each diode and also results in equal current sharing in the output. An interphase reactor tapped suitably to achieve pulse doubling [12] has been connected at the output of the ZSBT. The two rectifier output voltages $V_{\rm d1}$ and $V_{\rm d2}$ shown in Fig. 5 are identical except for a phase shift of 30° (required for achieving 12-pulse operation) and these voltages contain ripple of six times the source frequency. The rectifier output voltage

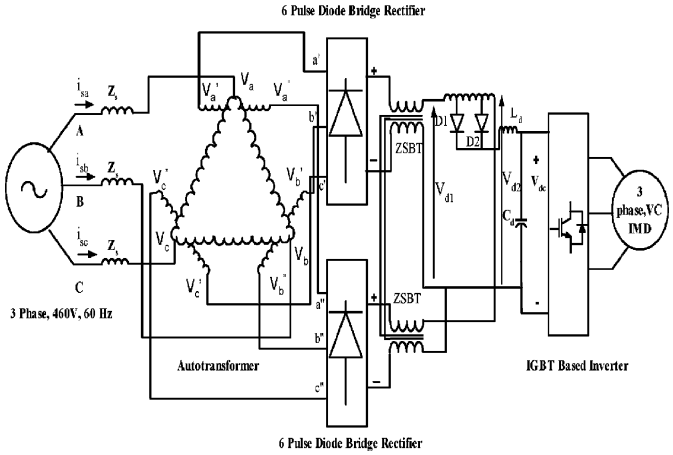

Fig. 5. Proposed autotransformer-based proposed 24-pulse converter fed VCIMD. (Topology E.)

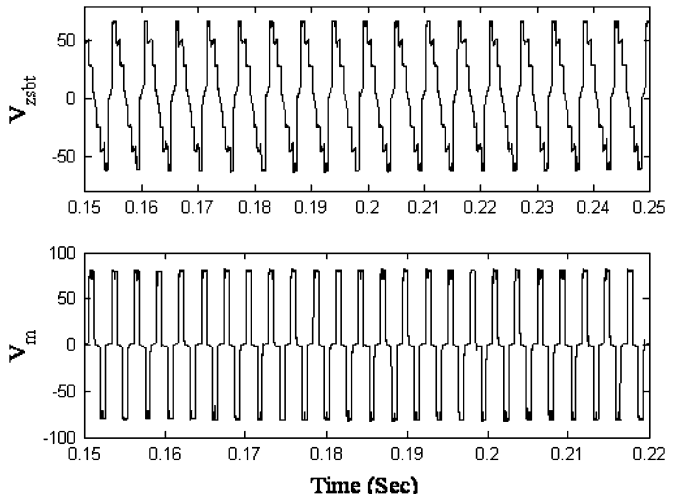

Fig. 6. Voltage waveforms across the ZSBT and tapped interphase reactor.

$V_{\rm d}$ is given by

$$V_{\rm d} = \frac{1}{2}(V_{\rm d1} + V_{\rm d2}). \tag{1}$$

Similarly, the voltage across interphase reactor is given by

$$V_{\rm m} = V_{\rm d1} - V_{\rm d2} \tag{2}$$

$V_{\rm m}$ is an ac voltage ripple of six times source frequency appearing across the tapped interphase reactor as shown in Fig. 6.

A. Design of Interphase Reactor

Pulse multiplication has been achieved [10], [11] for controlled converters with a tapped interphase reactor and two additional diodes. Choi *et al.* [12] give the details of pulse multiplication arrangement for diode bridge rectifiers, as shown in Fig. 7. The same concept has been used here for achieving the desired pulse doubling for line current harmonic reduction. The voltage appearing across the interphase reactor $V_{\rm m}$ is an ac voltage ripple of 6 times the source frequency, resulting in smaller size, weight, and volume of the transformer. Thus, depending upon the polarity of the impressed voltage across the interphase reactor, diodes D_1 or D_2 conduct. Fig. 8 shows the waveforms of the diode currents showing the changeover of currents through the diodes and this results in achieving the 24-pulse characteristics. The turns ratio of the interphase reactor is given by [12]

$$N_{\rm A}/N_{\rm o} = 0.2457 \tag{3}$$

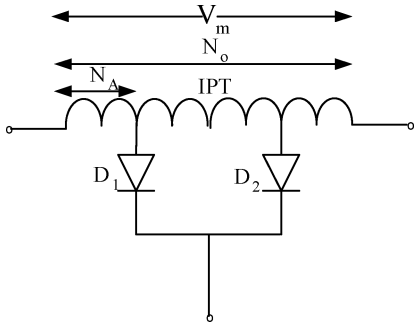

Fig. 7. Tapped interphase reactor alongwith diodes.

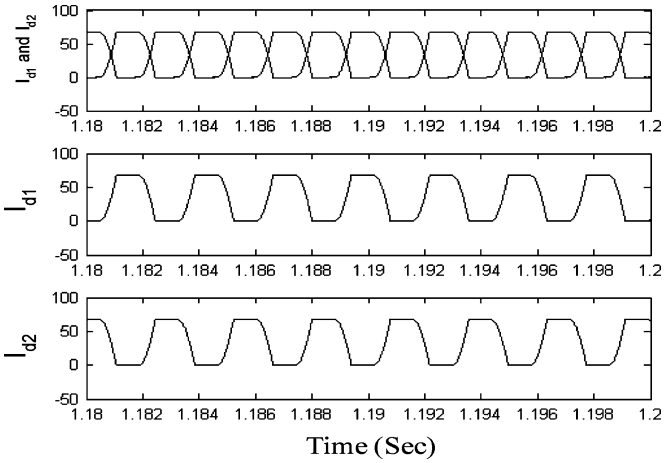

Fig. 8. Diodes D_1 and D_2 current waveforms.

B. Design of Zero Sequence Blocking Transformer (ZSBT)

The ZSBT helps in achieving independent operation of the two rectifier bridges, thus eliminating the unwanted conducting sequence of the rectifier diodes. ZSBT offers very high impedance for zero sequence current components. The voltage waveform across ZSBT, shown in Fig. 6, contains only triplen frequency components resulting in smaller size, weight, and volume of the transformer. However, the detailed design of the interphase reactor and ZSBT has been given in [12] and same procedure is used in this work.

IV. Design of Proposed 24-Pulse AC–DC Converter

This section presents the design technique for achieving 12-pulse rectification in the proposed harmonic mitigator.

Further, this technique can be used to design the transformer for retrofit applications by varying the transformer output voltages.

A. Design of Autotransformer for 12-Pulse Converter

To achieve the 12-pulse rectification, the necessary requirement is the generation of two sets of line voltages of equal magnitude and which are 30° out of phase with respect to each other (either ±15° or 0° and 30°).

From the supply voltages, two sets of three-phase voltages (phase shifted through +15° and −15°) are produced. The number of turns required for +15° and −15° phase shift are calculated as follows. Consider phase "a" voltages in Fig. 5 as

$$V'_{\rm a} = V_{\rm a}\angle 0^\circ + K_1 V_{\rm ca}\angle -30^\circ - K_2 V_{\rm bc}\angle 90^\circ \quad (4)$$

$$V''_{\rm a} = V_{\rm a}\angle 0^\circ + K_1 V_{\rm ab}\angle 30^\circ + K_2 V_{\rm bc}\angle 90^\circ. \quad (5)$$

Assume the following set of voltages:

$$V_{\rm a} = V\angle 0^\circ, \quad V_{\rm b} = V\angle -120^\circ, \quad V_{\rm c} = V\angle 120^\circ. \quad (6)$$

Similarly

$$V'_{\rm a} = V\angle +15^0, \quad V'_{\rm b} = V\angle -105^\circ, \quad V'_{\rm c} = V\angle 135^\circ \quad (7)$$

$$V''_{\rm a} = V\angle -15^\circ, \quad V''_{\rm b} = V\angle -135^\circ, \quad V''_{\rm c} = V\angle 105^\circ \quad (8)$$

where V is the rms value of phase voltage.

Using above equations K_1 and K_2 can be calculated. These equations result in $K_1 = 0.0227$ and $K_2 = 0.138$ for the desired phase shift in autotransformer. The phase shifted voltages for phase "a" are

$$V'_{\rm a} = V_{\rm a} + 0.0227 V_{\rm ca} + 0.138 V_{\rm bc} \quad (9)$$

$$V''_{\rm a} = V_{\rm a} + 0.0227 V_{\rm ab} + 0.138 V_{\rm bc}. \quad (10)$$

A phase-shifted voltage (e.g., $V'_{\rm a}$) is obtained by tapping a portion (0.0227) of line voltage $V_{\rm ca}$ and connecting one end of an approximately (0.138) of line voltage (e.g., $V_{\rm bc}$) to this tap.

With this transformer arrangement the dc link voltage obtained is slightly higher than that of a six-pulse diode bridge rectifier output voltage, similar to given in [12]. To make the proposed harmonic mitigator suitable for retrofit applications, the transformer design has been modified to make the dc link voltage same as that of six-pulse diode bridge rectifier. By following the above procedure, for same dc link voltage as that of six-pulse diode bridge rectifier, the values of K'_1 and K'_2 are as $K'_1 = 0.0195$ and $K'_2 = 0.1402$, where K'_1 and K'_2 are the new constants for achieving same dc link voltage as that of six-pulse diode bridge rectifier. Now, the phase shifted voltages for phase "a" are as

$$V'_{\rm a} = V_{\rm a} + 0.0195 V_{\rm ca} + 0.1402 V_{\rm bc} \quad (11)$$

$$V''_{\rm a} = V_{\rm a} + 0.0195 V_{\rm ab} + 0.1402 V_{\rm bc}. \quad (12)$$

Thus, by simply changing the transformer winding tapping, the same dc link voltage as that of 6-pulse diode bridge rectifier is obtained. The kVA rating of the autotransformer is calculated as [3]

$$\text{kVA} = 0.5 \sum V_{\rm winding} I_{\rm winding}. \quad (13)$$

The kVA rating of the interphase transformer and ZSBT is also calculated using this relationship.

V. Vector-Controlled Induction Motor Drive

Fig. 1 shows the schematic diagram of an indirect VCIMD. In the rotor-flux-oriented reference frame the x-component of the stator current reference vector i^*_{sx} is obtained as

$$i^*_{\rm sx} = i_{\rm mr} + \tau_{\rm r}(\Delta i_{\rm mr}/\Delta T). \quad (14)$$

The closed loop PI speed controller compares the reference speed ($\omega^*_{\rm r}$) with motor speed ($\omega_{\rm r}$) and generates reference torque T^* (after limiting it to a suitable value) as

$$T^*_{(n)} = T^*_{(n-1)} + K_{\rm p}\left\{\omega_{{\rm e}(n)} - \omega_{{\rm e}(n-1)}\right\} + K_{\rm I}\omega_{{\rm e}(n)} \quad (15)$$

where $T^*_{(n)}$ and $T^*_{(n-1)}$ are the output of the PI controller (after limiting it to a suitable value) and $\omega_{{\rm e}(n)}$ and $\omega_{{\rm e}(n-1)}$ refer to speed error at the nth and $(n-1)$th instants. $K_{\rm p}$ and $K_{\rm I}$ are the proportional and integral gain constants. The y-component of the stator current reference vector i^*_{sy} is obtained from the output of the PI controller as

$$i^*_{\rm sy} = T^*/(k\, i_{\rm mr}) \quad (16)$$

The x-component i^*_{sx} and y-component i^*_{sy} of the stator current form the inverter current reference vector in rotor-flux-oriented reference frame, which is then converted to stationary reference frame using rotor flux angle calculated as sum of the rotor angle and the value of slip angle as

$$\omega^*_2 = i^*_{sy}/(\tau_{\rm r} i_{\rm mr}) \quad (17)$$

$$\Psi_{(n)} = \Psi_{(n-1)} + (\omega^*_2 + \omega_{\rm r})\Delta T \quad (18)$$

$$k = (3/2)(P/2)\{{\rm M}/(1+\sigma_{\rm r})\} \quad (19)$$

$i_{\rm mr}$ is the magnetizing current, ω^*_2 is the slip speed of rotor, $\omega_{\rm r}$ is the angular velocity of rotor, P, M, and $\sigma_{\rm r}$ are the number of poles, mutual inductance, and rotor leakage factor, respectively, $\Psi_{(n)}$ and $\Psi_{(n-1)}$ are the value of rotor flux angles at nth and $(n-1)$th instants, respectively, and ΔT is the sampling time taken as 100 μs.

These currents (i^*_{sx}, i^*_{sy}) are in synchronously rotating reference frame and these are converted into stationary reference frame three-phase currents $(i^*_{\rm as}, i^*_{\rm bs}, i^*_{\rm cs})$ as

$$i^*_{\rm as} = -i^*_{sy}\sin\Psi + i^*_{sx}\cos\Psi \quad (20)$$

$$i^*_{\rm bs} = [-\cos\Psi + \sqrt{3}\sin\Psi]i^*_{sx}(1/2) + [{\rm Sin}\Psi + \sqrt{3}\cos\Psi]i^*_{sy}(1/2) \quad (21)$$

$$i^*_{\rm cs} = -(i^*_{\rm as} + i^*_{\rm bs}) \quad (22)$$

$i^*_{\rm as}, i^*_{\rm bs}$, and $i^*_{\rm cs}$ are the three-phase reference currents. These three-phase reference currents generated by the vector controller are compared with the sensed motor currents ($i_{\rm as}, i_{\rm bs}$, and $i_{\rm cs}$). The calculated current errors are

$$i_{\rm ke} = i^*_{\rm ks} - i_{\rm ks}, \quad \text{where } k = a, b, c. \quad (23)$$

These current errors are amplified and fed to the pulse width modulation (PWM) current controller, which controls the on and off periods of different switches in VSI. The VSI generates

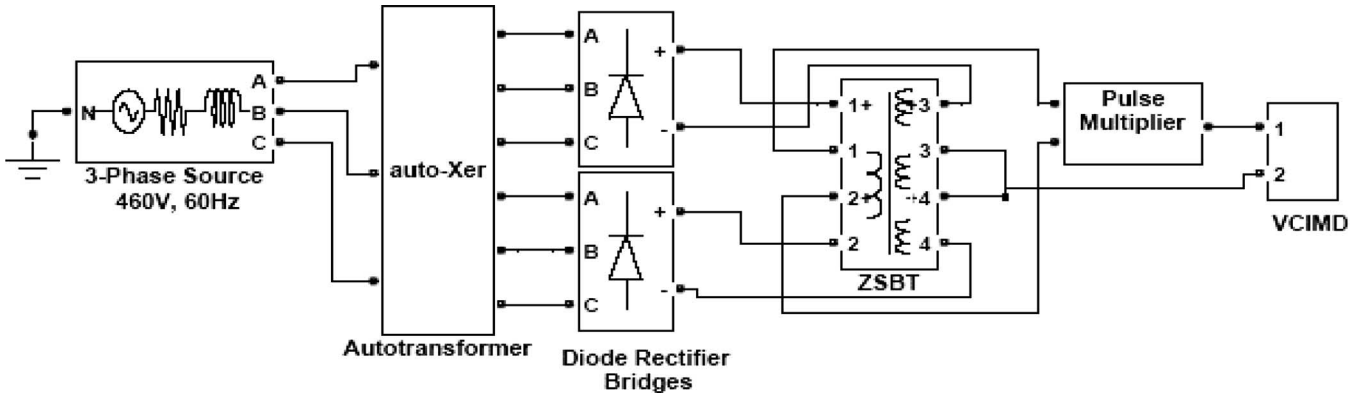

Fig. 9. MATLAB block diagram of proposed harmonic mitigator fed VCIMD (Topology E.)

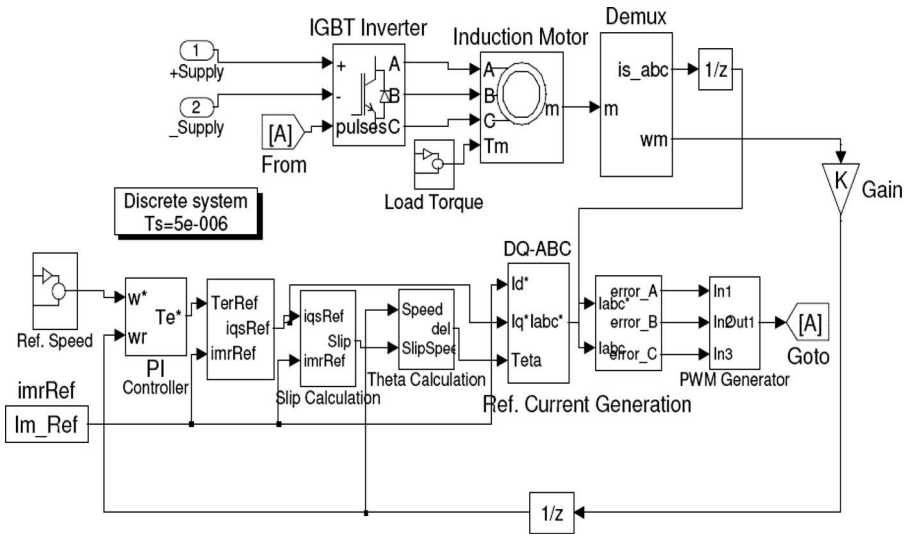

Fig. 10. MATLAB block diagram of VCIMD.

the PWM voltages being fed to the motor to develop the torque for running the motor at a desired speed under required loading conditions.

VI. MATLAB-Based Simulation

The proposed harmonic mitigator alongwith the VCIMD is simulated in MATLAB environment alongwith SIMULINK and power system blockset (PSB) toolboxes. Fig. 9 shows the MATLAB model of the proposed harmonic mitigator based on 12-pulse rectification alongwith the pulse multiplication circuit connected on the dc side to improve further various power quality indices. It eliminates upto 21st harmonics in ac mains current. Fig. 10 shows the MATLAB model of a VCIMD.

VII. Experimentation

The simulated results have been verified on a test bench consisting of the newly designed and developed autotransformer alongwith small rating interphase reactor and a ZSBT, as shown in Fig. 5. Three single-phase autotransformers have been designed and wound in the laboratory as per the design details:

TABLE I
Autotransformer Winding Details

Winding	Number of turns	Gauge of wire
N_1	17	13
N_2	561	21
N_3	17	13
N_4	79	13

Flux density $= 0.8$ Tesla, Current density $= 2.3$ A/m^2, Core Size $= 8$ No., Area of cross section of core $= 32.25$ cm^2 (5.08 cm $\times$ 6.35 cm). E-Laminations: Length $= 18.41$ cm, width $= 17.14$ cm, I-lamination: Length $= 17.14$ cm, width $= 5.08$ cm. The number of turns of different windings (shown in Fig. 2) and conductor cross section are given in Table I. Similarly, the interphase transformers of small ratings have been designed and fabricated. Various tests have been carried out at three-phase line voltage of 230 V ac input and with an equivalent resistive load and these test results are given in Figs. 25–28 and in Tables IV–V. The test results have been recorded using Fluke make power analyzer model 43B on the developed prototype.

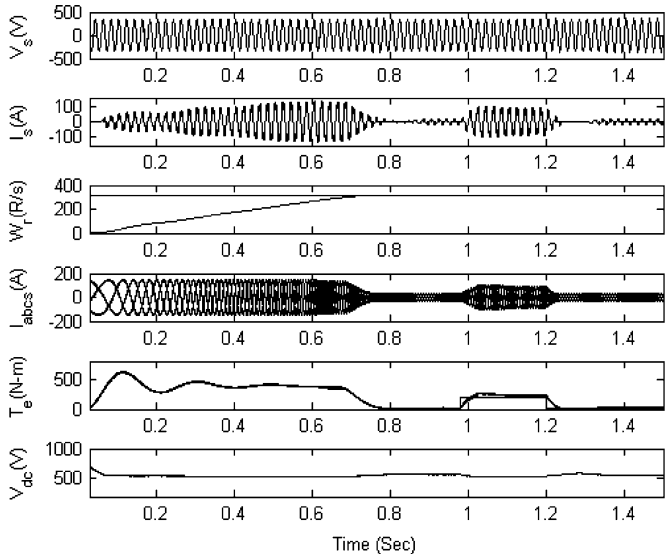

Fig. 11. Dynamic response of six-pulse diode rectifier fed VCIMD with load perturbation.

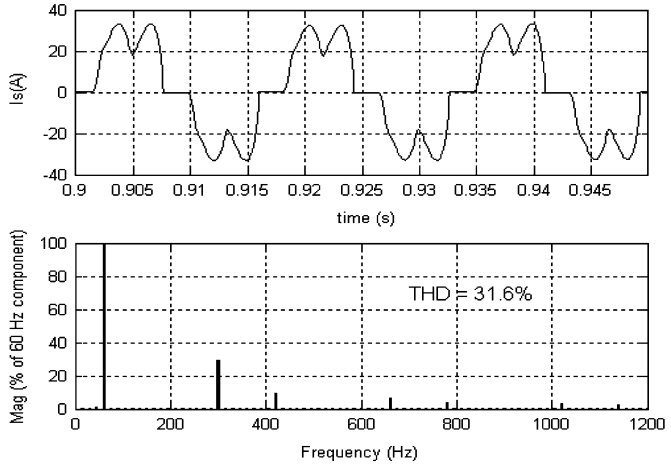

Fig. 12. AC mains current waveform of VCIMD fed by six-pulse diode rectifier along with its harmonic spectrum at full load.

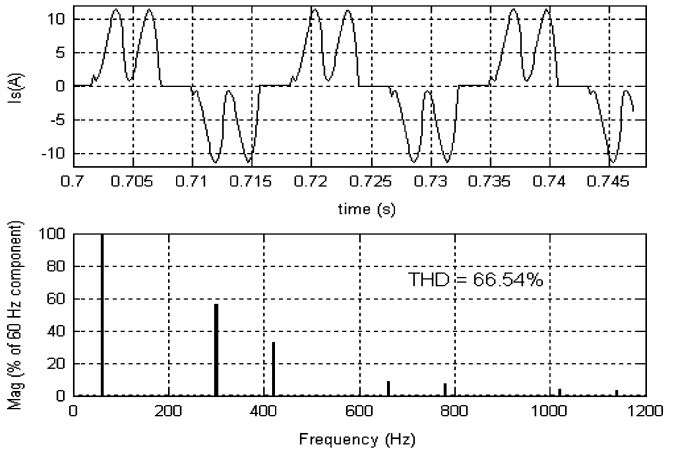

Fig. 13. AC mains current waveform of VCIMD fed by 6-pulse diode rectifier along with its harmonic spectrum at light load (20%).

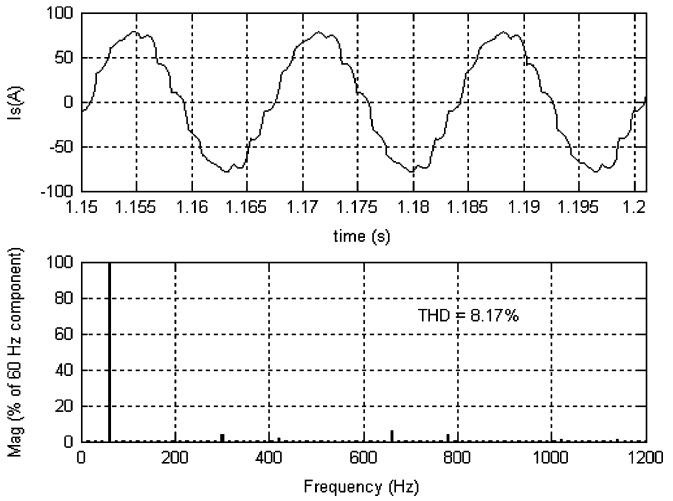

Fig. 14. AC mains current waveform alongwith its harmonic spectrum at full load for Topology B.

VIII. Results and Discussion

The proposed harmonic mitigator alongwith the VCIMD has been designed for retrofit applications. Fig. 11 shows the dynamic performance alongwith load perturbation on the VCIMD fed by a six-pulse diode bridge rectifier. It consists of supply voltage $V_{\rm s}$, supply current $i_{\rm s}$, rotor speed '$\omega_{\rm r}$' (in electrical rad/sec), three-phase motor currents $i_{\rm abcs}$, motor developed torque '$T_{\rm e}$' (in N·m), and dc link voltage $V_{\rm dc}$ (V). Fig. 12 shows the supply current waveform alongwith its harmonic spectrum at full load, showing THD of ac mains current as 31.6%, which deteriorates to 66.54% at light load (20%) as shown in Fig. 13.

Moreover, the power factor at full load is 0.937, which deteriorates to 0.848 as the load is reduced to 20%. These results show that there is a need for improving the power quality at ac mains using some harmonic mitigators, which can easily replace the existing six-pulse converter.

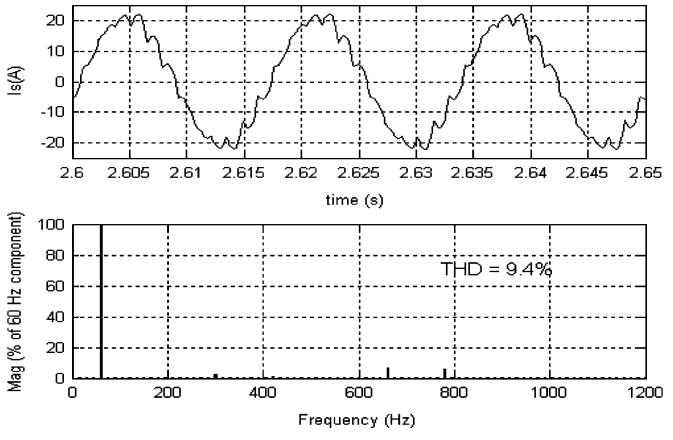

Fig. 15. AC mains current waveform alongwith its harmonic spectrum at light load (20%) for Topology B.

TABLE II
COMPARISON OF POWER QUALITY PARAMETERS OF A VCIMD FED FROM DIFFERENT CONVERTERS

Sr. No.	Topology	THD V_s (%)		AC Mains Current I_s (A)		THD of I_s (%)		DF		DPF		PF		DC Link Voltage(V) Average	
		FL	LL (20 %)	FL	LL (20%)	FL	LL (20%)	FL	LL (20 %)	FL	LL (20%)	FL	LL (20%)	FL	LL (20%)
1.	A	6.76	3.31	56.9	17.26	31.2	57.7	.955	.866	.982	0.979	.938	0.848	612	621
2.	B	3.38	1.22	55.5	14.65	8.17	9.40	.996	.995	.978	0.973	.975	0.969	612	622
3.	C	2.75	1.25	53.4	13.5	4.69	5.75	.999	.998	.995	.9976	.994	0.996	637	649
4.	D	3.17	1.38	52.9	13.54	4.1	5.7	.999	.998	.9968	.998	.996	.9967	623	631
5.	E	3.18	1.36	53.4	13.42	4.00	5.68	.999	.998	.9967	.998	.996	.9968	612	622

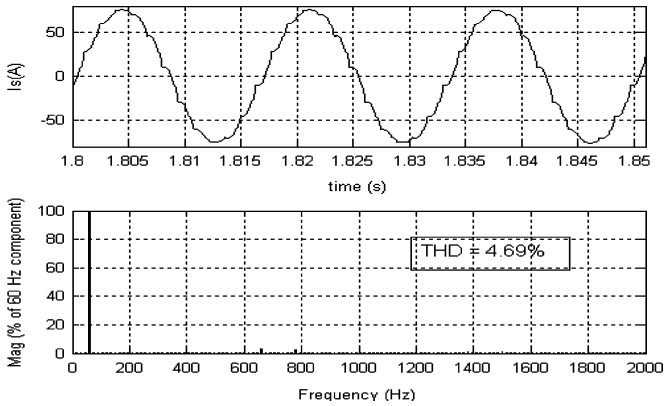

Fig. 16. AC mains current waveform alongwith its harmonic spectrum at full load for Topology C.

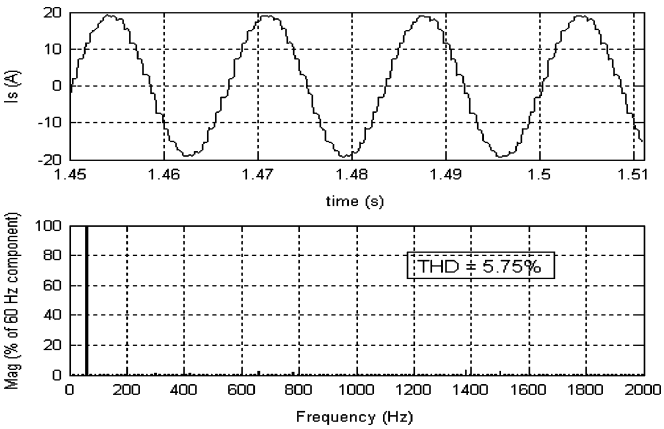

Fig. 17. AC mains current waveform alongwith its harmonic spectrum at light load (20%) for Topology C.

A. Performance of 12-Pulse Rectification Based Harmonic Mitigator (Topology B)

To improve the power quality indices, a 12-pulse ac–dc converter fed VCIMD has been modeled and simulated. Fig. 14 shows the waveform of the supply current alongwith its harmonic spectrum at full load and Fig. 15 shows these parameters at light load (20%). The THD of supply current at full load is 8.17% and that at light load is 9.4%, whereas the power factor under these conditions is 0.975 and 0.969, respectively, as given in Table II.

B. Performance of 24-Pulse Rectification Based Harmonic Mitigators (Topology C and D)

To improve the power quality indices further, DC ripple reinjection technique has been incorporated in existing twelve-pulse based ac–dc converters. The simulation results are shown in Figs. 16–19 and these have been tabulated in Table II. It is observed from the results that the THD of ac mains current at full load in Topology C is 4.69, shown in Fig. 16, and that at light load (20%) is 5.75%, as shown in Fig. 17. Similarly, Fig. 18 shows the THD of ac mains current at full load in Topology D as 4.1% and at light load as 5.7%, shown in Fig. 19.

In Topology C, the dc link voltage is higher than that of a 6-pulse diode bridge rectifier. So, it cannot be used in retrofit applications. Topology D can be used for retrofit applications, as the dc link voltage is almost the same as that of a 6-pulse diode

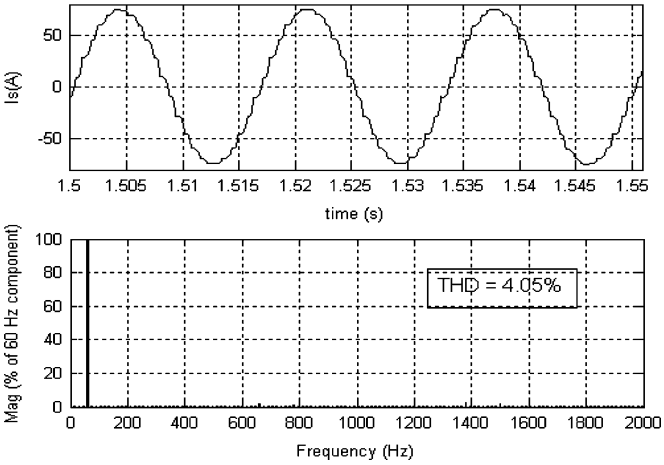

Fig. 18. AC mains current waveform alongwith its harmonic spectrum at full load for Topology D.

rectifier, but the rating of magnetics is high, causing hindrance in using this topology.

C. Performance of Proposed Harmonic Mitigator (Topology E)

Fig. 20 shows the dynamic performance of the proposed harmonic mitigator at starting and load perturbation. The supply current waveform at full load alongwith its harmonic spectrum is shown in Fig. 21, which shows that the THD of ac mains current

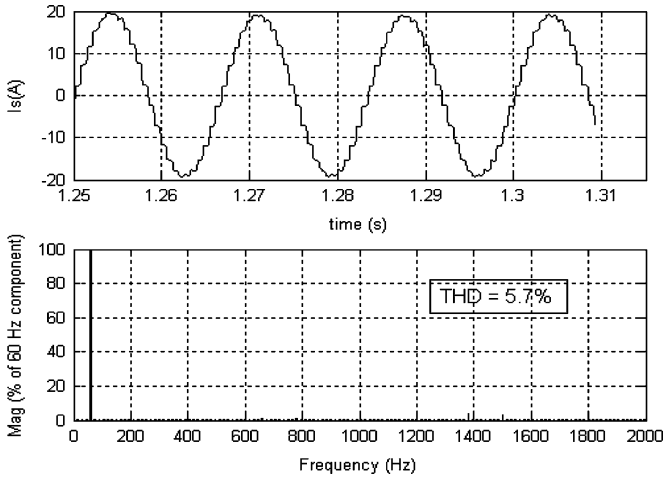

Fig. 19. AC mains current waveform alongwith its harmonic spectrum at light load (20%) for Topology D.

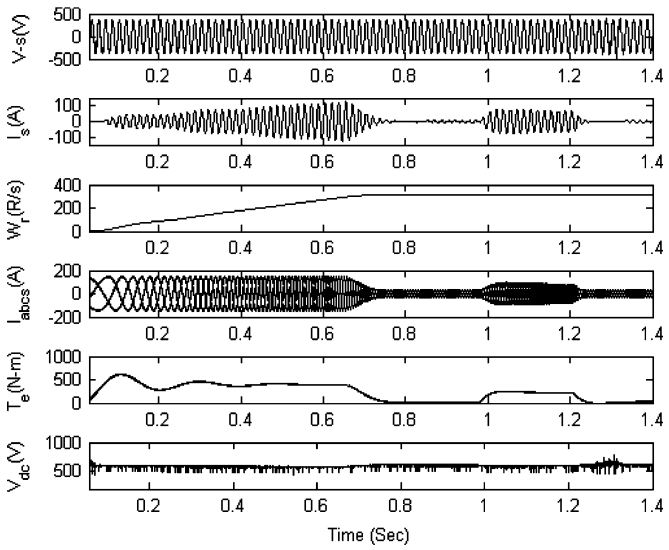

Fig. 20. Dynamic response of proposed harmonic mitigator (Topology E) fed VCIMD with load perturbation.

is 4.00% and the power factor obtained is 0.996. Fig. 22 shows the supply current waveform alongwith its harmonic spectrum under light load condition (20%).

At light load condition, the THD of ac mains current is 5.68% and the power factor is 0.9968.

Table III shows the effect of load variation on the VCIMD to study various power quality indices. It shows that the proposed harmonic mitigator is able to perform satisfactorily under load variation on VCIMD with almost unity power factor in the wide operating range of the drive and THD of supply current always less than 8%. This is within the IEEE Standard 519 [2] limits for SCR > 20.

The variation of THD of ac mains current and power factor with load on VCIMD fed from a 6-pulse, 12-pulse, and the proposed 24-pulse ac-dc converter is shown in Figs. 23 and 24, respectively, showing a remarkable improvement in these power quality indices.

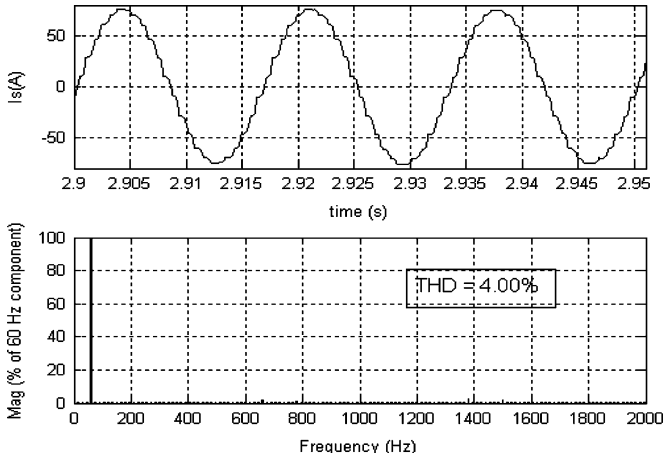

Fig. 21. AC mains current waveform alongwith its harmonic spectrum at full load for Topology E.

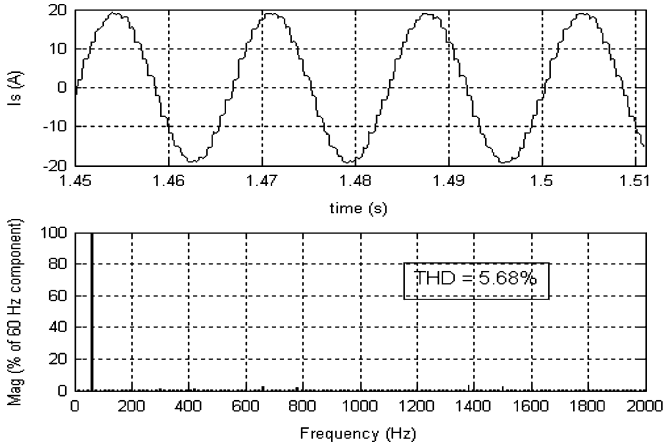

Fig. 22. AC mains current waveform alongwith its harmonic spectrum at light load (20%) for Topology E.

TABLE III
COMPARISON OF POWER QUALITY INDICES OF PROPOSED 24-PULSE HARMONIC MITIGATOR FED VCIMD UNDER VARYING LOADS IN SIMULATION

Load (%)	THD (%)		CF	DF	DPF	PF	RF	V_{dc} (V)
	I_s	V_t						
20	5.68	1.37	1.410	.998	.998	.9968	0.28	622
40	5.16	1.94	1.410	.998	.998	.9967	0.27	619
50	4.93	2.21	1.408	.998	.997	.9964	0.25	618
60	4.72	2.43	1.408	.998	.997	.9964	0.25	617
80	4.37	2.84	1.405	.999	.997	.9963	0.24	614
100	4.00	3.18	1.400	.999	.996	.9960	0.22	612

D. Experimental Performance of Proposed Harmonic Mitigators (Topology B and E)

Various tests have been carried out on the developed prototypes for Topologies B and E, shown in Figs. 2 and 5, respectively. The harmonic spectrum of ac mains current alongwith the waveform of supply voltage $(V_{\rm AB})$ and current $(I_{\rm C})$ at full load in Topology B is shown in Fig. 25, and at light load (20%) is shown in Fig. 26. The effect of load variation on different power quality indices in Topology B is shown in Table IV. It

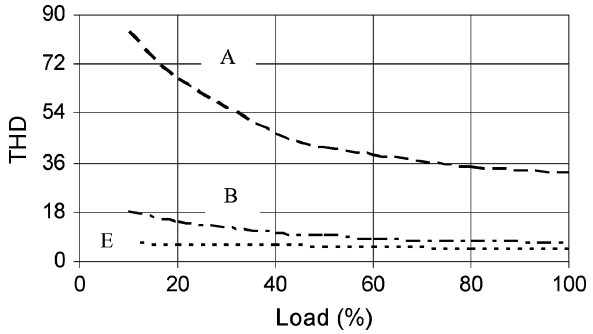

Fig. 23. Variation of THD of supply current with load on VCIMD in 6-pulse (Topology A), 12-pulse (Topology B), and proposed 24-pulse ac–dc converter (Topology E) fed VCIMD.

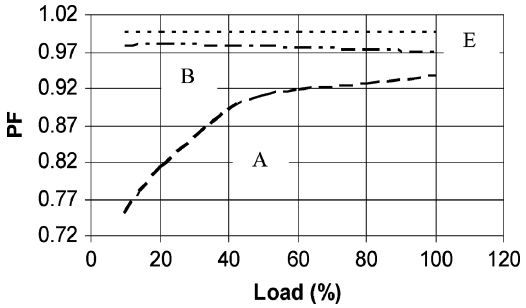

Fig. 24. Variation of power factor with load on VCIMD in 6-pulse (Topology A), 12-pulse (Topology B), and proposed 24-pulse ac–dc converter (Topology E) fed VCIMD.

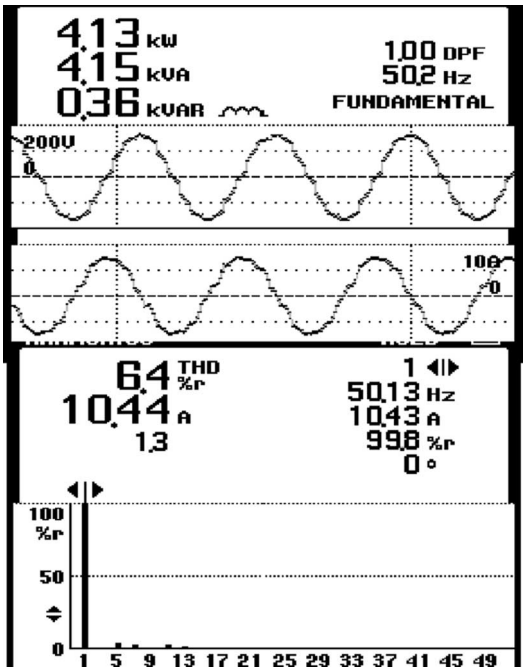

Fig. 25. Experimental results of ac mains voltage and current waveforms alongwith harmonic spectrum of ac mains current at full load for Topology B.

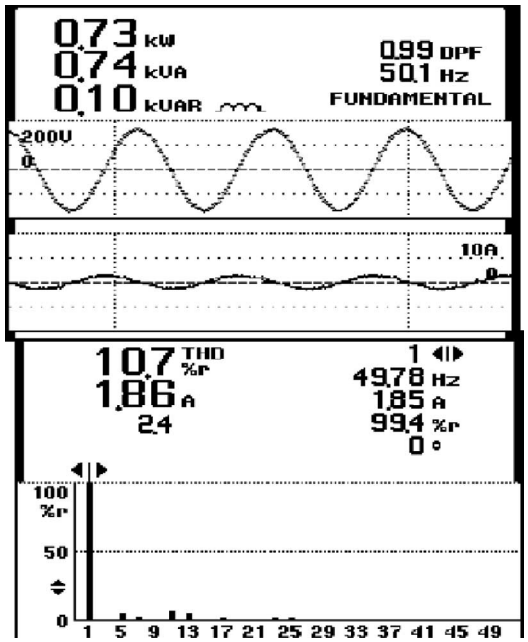

Fig. 26. Experimental results of ac mains voltage and current waveforms alongwith harmonic spectrum of ac mains current at light load (20%) for Topology B.

TABLE IV
COMPARISON OF POWER QUALITY INDICES WITH 12-PULSE HARMONIC MITIGATOR UNDER VARYING LOADS IN EXPERIMENTATION

AC Mains Current I_s (A)	THD (%)		CF of I_s	DF	DPF	PF	V_{dc} (V)
	I_s	V_s					
1.88	10.7	2.3	1.4	.994	0.99	0.984	308
3.9	10.1	3.5	1.4	.995	1.00	0.995	304
5.95	9.0	4.6	1.4	.996	1.00	0.996	301
7.00	8.3	4.9	1.4	.996	1.00	0.996	299
9.00	7.3	5.4	1.4	.997	1.00	0.997	296
10.5	6.8	5.6	1.4	.997	1.00	0.997	293

can be observed from Table IV that under light load condition the power quality indices start deteriorating, thus not qualifying the IEEE Standard 519 [2].

Similarly, tests have been conducted for the proposed 24-pulse ac–dc converter on the laboratory prototype. Fig. 27 shows the line voltage $(V_{\rm AB})$ and current through the other line $(I_{\rm C})$ along with the harmonic spectrum of the line current at full load in Topology E. Fig. 28 shows these waveforms at light load. Again the effect of load variation is shown in Table V. It is observed from Table V, that in the proposed 24-ac–dc converter, the power quality indices are always within IEEE Standard 519 [2] limits, even under light load conditions. The power factor is near unity in wide variation of the load. The recorded results are in close agreement with the simulated results for both the configurations.

IX. SUITABILITY FOR RETROFIT APPLICATIONS

The converters in Topologies A and B result in poor power quality indices, which needs improvement. The 24-pulse converter in Topology C results in a higher dc link voltage than a 6-pulse diode bridge rectifier. Therefore, this topology

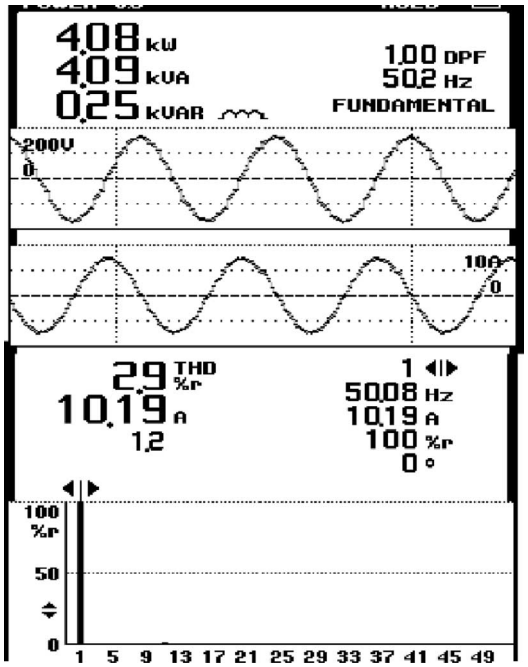

Fig. 27. Experimental results of ac mains voltage and current waveforms alongwith harmonic spectrum of ac mains current at full load for Topology E.

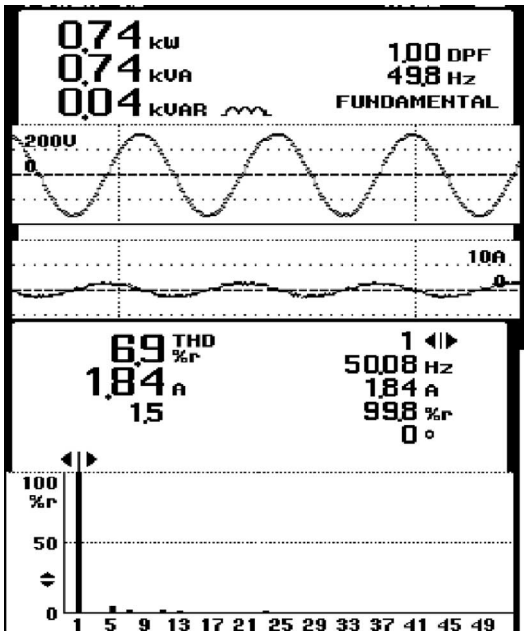

Fig. 28. Experimental results of ac mains voltage and current waveforms alongwith harmonic spectrum of ac mains current at light load (20%) for Topology E.

cannot be used in retrofit applications. The autotransformers in Topologies D and E result in a dc link voltage same as that of a 6-pulse diode bridge rectifier. So these topologies may be used for retrofit applications. Again, the converter in Topology D needs magnetics of 31.84% of the drive rating, as shown in Table VI. The proposed 24-pulse harmonic mitigator (Topology E) has been designed to give same dc link voltage as that of a six-pulse diode bridge rectifier. This topology needs an autotransformer of 9.19 kVA, an interphase transformer of 0.433 kVA and ZSBT of 2.33 kVA, totaling all these require magnetics of 11.95 kVA, i.e., only 25% of the drive rating. The proposed autotransformer-based 24-pulse ac–dc converter results in a cost-effective replacement for retrofit applications, where presently a six-pulse diode bridge rectifier is being used.

TABLE V
COMPARISON OF POWER QUALITY INDICES IN PROPOSED 24-PULSE HARMONIC MITIGATOR UNDER VARYING LOADS IN EXPERIMENTATION

Supply Current I_s (A)	THD (%)		CF of I_s	DF	DPF	PF	V_{dc} (V)
	I_s	V_s					
1.84	6.9	1.6	1.4	.997	0.99	0.987	306
4.13	4.6	2.6	1.4	.998	1.00	0.988	304
6.28	3.5	3.2	1.4	.999	1.00	0.999	302
7.5	3.2	3.4	1.4	.999	1.00	0.999	300
8.5	3.1	3.6	1.4	.999	1.00	0.999	299
10.23	2.9	3.8	1.4	.999	1.00	0.999	296

TABLE VI
COMPARISON OF RATING OF MAGNETICS IN DIFFERENT CONVERTER FED VCIMD

Sr. No	Topology	Transformer Rating (kVA)	Interphase Transformer rating (kVA)	ZSBT Rating (kVA)	Rating of magnetics % of drive rating
1	A	0	0.0	0.0	0.0
2.	B	9.3	1.38	0.0	22.34
3.	C	9.01	0.53	2.99	26.22
4.	D	12.22	0.628	3.0	31.84
5.	E	9.19	0.433	2.33	25.01

X. CONCLUSION

A novel autotransformer-based 24-pulse ac–dc converter has been designed and modeled with a VCIMD load. Pulse multiplication has been achieved using dc ripple reinjection technique in existing twelve-pulse based ac–dc converters, which needs only two additional diodes alongwith a suitably tapped inductor. The design technique of the proposed converter has shown the flexibility to design the transformer suitable for retrofit applications with variable frequency induction motor drives operating under varying load conditions. The proposed harmonic mitigator has resulted in reduction in rating of the magnetics, leading to the saving in overall cost of the drive. The proposed harmonic mitigator is able to achieve close to unity power factor in the wide operating range of the drive. The performance of the proposed harmonic mitigator has demonstrated the capability of this converter resulting in improved power quality indices at ac mains in terms of THD and crest factor of supply current, THD of supply voltage, and power factor.

APPENDIX

Motor and Controller Specifications.

Three-Phase Squirrel Cage Induction Motor -50 HP (37.3 kW), 3-Phase, 4 Pole, Y- connected, 460 V, 60 Hz, $R_s = 0.087\ \Omega$, $R_R = 0.228\ \Omega$, $X_{ls} = 0.3016\ \Omega$, $X_{lr} = 0.3016\ \Omega$, $L_m = 0.034.7$ Henry, $J = 1.662$ kg·m^2.

Controller Parameters:

PI Controller: $K_p = 45.0, K_I = 0.1$

DC link parameters: $L_d = 0.6$ mH, $C_d = 3200\ \mu$F.

Magnetics ratings:

24-pulse based converter: Autotransformer Rating 9.19 kVA, Interphase Transformer 0.433 kVA, ZSBT 2.33 kVA.

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