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Fully Resonant Adaptive Gate Driver Scheme for GaN FETs

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Abstract

Silicon carbide (SiC) and Gallium Nitride (GaN) metal–oxide–semiconductor field-effect transistors (MOSFETs) are capable of processing high power at high switching frequencies with less switching losses and conduction losses. The gate driver circuit power consumption is directly proportional to the switching frequency. The power taken from the gate supply is dissipated in the gate resistance of the conventional gate driver (CGD) circuit. Instead of dissipating all the gate driver energy, some energy can be recovered or recycled by utilizing the principle of resonance. This reduces the net power being taken from the gate supply. This project aims to propose a new resonant gate driver (RGD) circuit which consumes less power compared to the CGD circuit at high switching frequencies. The performance of the proposed circuit is simulated in LTSpice environment.

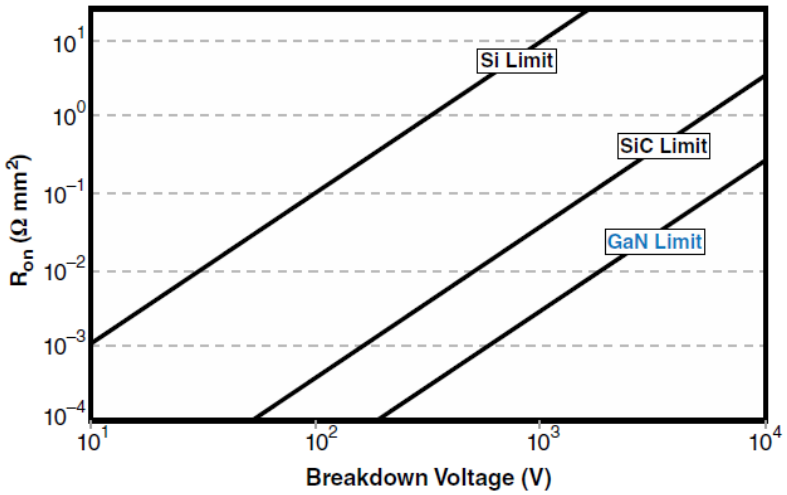
Introduction

The increasing demand for high power density, high performance, compactness, better transient response, etc., inspires the pursuit of high switching frequency operation. Silicon (Si) devices have reached their physical limits. Wide band gap materials, such as silicon carbide (SiC) and gallium nitride (GaN) are now being recognized as an alternative to silicon because of their superior properties.

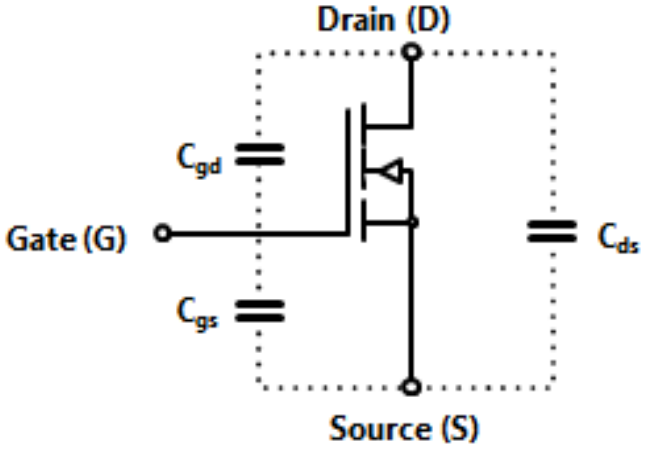
Parameter		Silicon	GaN	SiC
Band Gap E_g	eV	1.12	3.39	3.26
Critical Field E_{Crit}	MV/cm	0.23	3.3	2.2
Electron Mobility μ_n	$cm^2/V{\cdot}s$	1400	1500	950
Permittivity ε_r		11.8	9	9.7
Thermal Conductivity λ	W/cm·K	1.5	1.3	3.8

Advantages of GaN

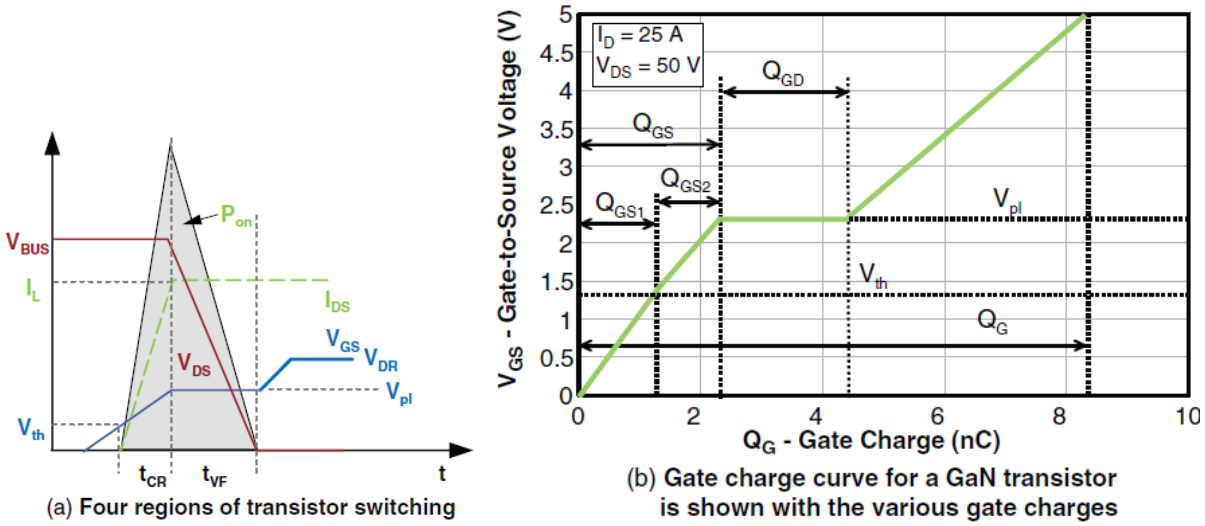
- Lower leakage currents, higher operating temperatures
- Higher Breakdown Voltage/ Smaller width
- Lower losses/ Higher Switching Frequencies



MOSFETs and IGBTs have a metal–oxide structure between the gate and the source or the emitter. It can be represented by an input capacitance (*C*iss) which is not constant due to the miller effect.



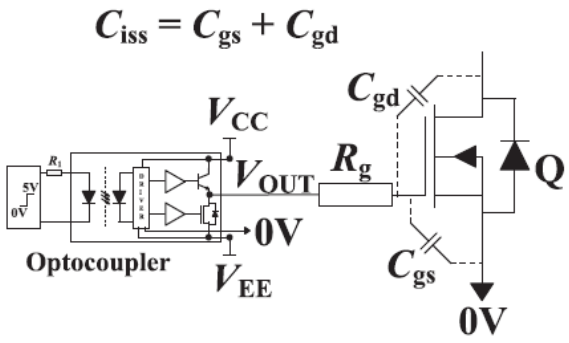
Any gate driver circuit supplies energy in the form of charge (*Q*g) to *C*iss for the switching transitions.



(a) Four regions of transistor switching

(b) Gate charge curve for a GaN transistor is shown with the various gate charges

This energy is dissipated in the gate resistance of the conventional gate driver (CGD) circuit.



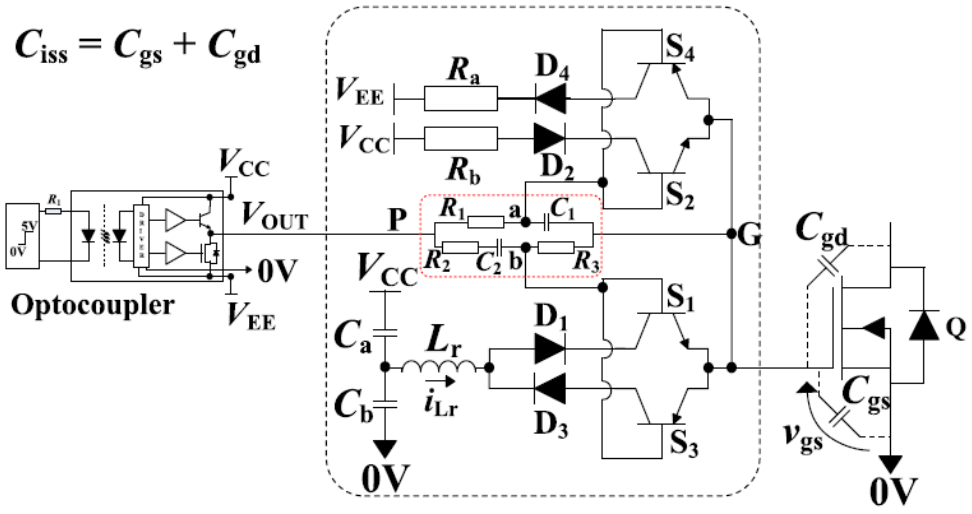
(a)

Conventional Gate Drive Circuit

If the switching frequency increases, the power consumption of the gate driver circuit increases. One way to reduce the power consumption is by either recovering or recycling the energy supplied by the gate power supply. To achieve this, the gate resistance is replaced with an inductor (*L*r) in the gate driver circuit. This inductor with the input capacitance *C*iss forms a resonance circuit, which can recover or recycle the energy. In order to have efficient recovery or recycling, a gate driver circuit comprising of small signal bipolar junction transistors (BJTs), small signal diodes, low power resistances, and capacitances is proposed. The proposed resonant gate driver (RGD) circuit recycles the energy instead of dissipating it. This reduces the energy being taken from the supply, which in turn reduces the gate driver power consumption. The evolution of SiC, GaN, and other devices makes power switches operating near MHz range available in the near future. The gate driver power consumption which becomes a considerable portion of the total loss can be reduced by the proposed RGD circuit. By using the state-of-the-art very large-scale integration technologies, the proposed RGD circuit can be fabricated into a low power consuming gate driver IC along with optocoupler functionality. This new IC can consume much less power than the present-day gate driver ICs.

Proposed RGD Circuit

The proposed RGD circuit is designed to operate a GaN MOSFET, which requires –5 and + 20 V as gate voltages for its switching. Therefore, it is chosen that V_{CC} = +20 V and V_{EE} = −5 V. For analysis and simplicity, it is assumed that the input capacitance C_{iss} remains constant.

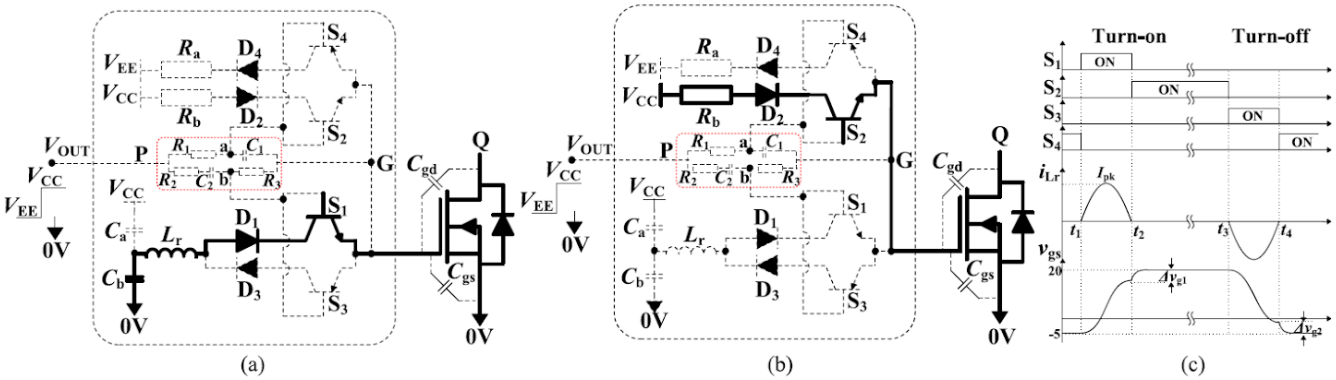


Although, it is similar to the RGD proposed in [3], the following are the differentiating features:

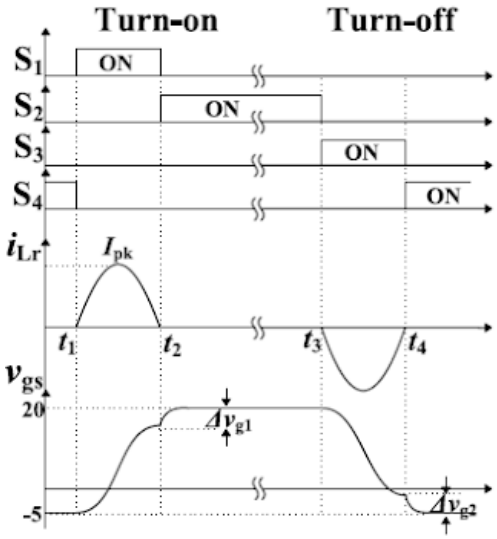
1) It works on series resonance principle as the resonant inductor, the gate–source capacitance, and a voltage source are connected in series during the resonance period.
2) It is a universal RGD circuit which is used to produce gate voltage transition between any voltage levels whereas the RGD in [3] can produce either unipolar or bipolar voltages with equal magnitude only.

In addition, other main features of the proposed RGD circuit are given as follows:

3) Gate terminal is clamped after each switching transition to avoid false triggering.
4) Influence of resistance in the resonance path is negligible on the gate voltage levels.
5) Timing tolerances in switching any auxiliary devices do not affect the gate voltage levels.
6) Simple control of the gate driver circuit.



3. Turn-ON transition (a) resonance stage, (b) clamping stage, and (c) switching states of BJTs and waveforms of i_{Lr} and v_{gs}.



Turn-On Transition

Each switching transition consists of two stages: resonance and clamping. During the resonance stage, energy is recycled and during the clamping stage, lost energy if any, is supplied by the gate supply. Thus, the power is consumed only during the clamping stage.
It is assumed that initially the main switch "Q" is in OFF-state, i.e., $v_{gs} = -5$ V, S_4 is in ON-state, and $v(C_b) = 7.5$ V due to the self-balancing feature which will be explained later. Since the value of C_b is chosen to be greater than C_{iss}. Therefore, the voltage ripple across C_b is very small and C_b acts as a voltage source. The voltage across C_b is denoted by V_g.

1) **Resonance Stage ($t_1 < t < t_2$):** Turn-On transition is initiated by turning ON the small signal BJT "S_1" at t_1. This enables energy transfer between C_b, L_r, and C_{iss} resulting in voltage (v_{gs}) transitioning across C_{iss} from –5 to +20 V. During this stage, the voltage across gate-source and the inductor current are given by

$$v_{\mathrm{gs}}(t) = V_{\mathrm{i}} + (V_{\mathrm{g}} - V_{\mathrm{i}})(1 - \cos\omega_{\mathrm{r}} t)$$
$$i_{\mathrm{Lr}}(t) = \frac{(V_{\mathrm{g}} - V_{\mathrm{i}})}{L_{\mathrm{r}}\omega_{\mathrm{r}}} \sin\omega_{\mathrm{r}} t$$

where V_{i} is the initial voltage across C_{iss} which is –5 V, L_{r} is the resonant inductance, and ω_{r} is the resonant frequency. The relation between t_1 and t_2 is given by

$$t_2 - t_1 = \pi\sqrt{L_{\mathrm{r}} C_{\mathrm{iss}}}$$

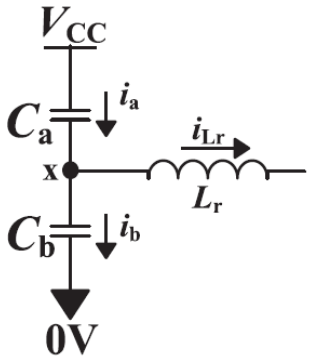
Practically, the gate voltage (v_{gs}) after the resonance is less than 20 V. This loss in voltage (Δv_{g1}) is a result of energy loss due to parasitic resistance, diode, and BJT forward drop.

2) **Clamping Stage (t > t_2):** MOSFET's desired on state gate voltage is 20 V. To compensate the loss Δv_{g1}, the gate–source terminals should be clamped after the switching transition. This is achieved by turning OFF S_1 and turning ON S_2 at t_2. The current path is shown by a solid line. This stage is similar to the CGD circuit but only the energy required to compensate Δv_{g1} is supplied by V_{CC}. After charging is done, v_{gs} is clamped to 20 V through R_{b}, D_2, and S_2. Now the BJT S_2 is on the verge of being in OFF-state since the voltage across the base and emitter is approximately zero. Due to some reasons external to the gate circuit; if v_{gs} falls below 20 V, S_2 will come into ON-state followed by the clamping stage. Thus, the proposed RGD circuit avoids false triggering by immediately charging and clamping the gate terminal to 20 V.

Turn-Off Transition

Turn-off transition is very similar to turn-on transition. It also consists of resonance stage and clamping stage. S_3 is turned ON at t_3 for resonance, and S_4 is turned ON and S_3 is turned OFF at t_4 for clamping during turn-off transition. During resonance, v_{gs} transition should be from 20 to –5 V according to (2) with V_{i} = 20 V. Because of the losses associated with parasitic resistances, BJT and diode forward voltage drop, v_{gs} is greater than –5 V. Therefore, there is also a voltage loss Δv_{g2} in v_{gs} which is supplied by V_{EE} during the clamping stage.

Self-Balancing of the Voltage Across C_b



Consider the turn-on transition where the initial voltage (v_{gs}) across C_{iss} is V_{EE}. It is desired that v_{gs} after resonance be V_{CC}. Substituting the initial and final voltages of v_{gs} gives

$$V_g = \frac{|V_{CC}| - |V_{EE}|}{2}$$

But, the initial value of $v(C_b)$ may not be the same. Consider Fig. 5 which is a part of the proposed RGD circuit.

$$i_a = -C_a \frac{dv(C_b)}{dt}$$

$$i_b = C_b \frac{dv(C_b)}{dt}.$$

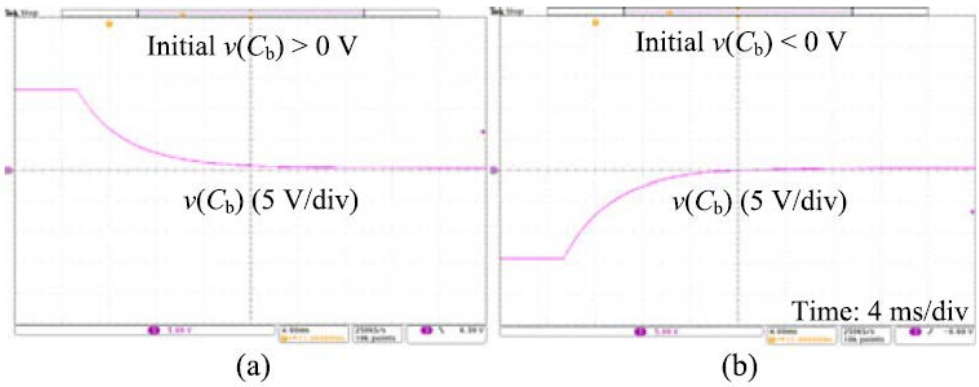
Applying KCL at 'x' gives the following equation:

$$i_{Lr} = -(C_a + C_b)\frac{dv(C_b)}{dt}$$

It is known that the node voltage remains constant when the average current flowing through that node is zero. The voltage at the node "x" i.e. $v(C_b)$ remains constant if the current averaged over a switching period $< i_{Lr} >_{Ts}$ flowing away from node "x" is zero. The expression for $< i_{Lr} >_{Ts}$ from (2) is given by

$$\langle i_{Lr} \rangle_{Ts} = \frac{2}{T_s}\left(\frac{(V_g - |V_{CC}|)}{L_r \omega_r^2} + 2\frac{(V_g + |V_{EE}|)}{L_r \omega_r^2}\right).$$

Equating this to zero gives the same expression as before. This proves that the voltage across C_b, i.e., V_g or $v(C_b)$ is maintained at a constant value given by in the steady state irrespective of the initial value. In addition, it does not depend on the values of C_a and C_b. It proves that irrespective of C_a, C_b values, average value of $v(C_b)$ is maintained according to the above equation assuming ideal conditions.



LTSpice Simulation showing the self-balancing nature of capacitor voltage.

Conclusion

A universal RGD circuit which works on the series resonance principle was proposed. The proposed circuit was able to generate unipolar gate voltages as well as bipolar gate voltages with equal and unequal magnitudes. It used two series connected capacitors across one of its supply, where the common point was connected to the resonant inductor. This common point which served as a voltage source in the series resonance needed to be balanced. However, the circuit was designed in a way that the voltage of the capacitor between the common point and the ground was self-balanced due to the operation of the circuit. It was also proved mathematically that the proposed RGD consumed less power compared to the CGD. **The saving in the power consumption was found to be 44.5% with the proposed RGD**. The dominant part of the power consumption was the optocoupler IC power. If an optocoupler IC with low power consumption is selected, the saving could be increased. Excluding the optocoupler's power consumption, the saving was found to be near 71%.

References

[1] A. Lidow, J. Strydom, M. D. Rooij, and Y. Ma, GaN Transistors for Efficient Power Conversion. EI Segundo, CA, USA: Power Conversion Publications, 2012.

[2] J. V. P. S. Chennu, R. Maheshwari and H. Li, "New Resonant Gate Driver Circuit for High-Frequency Application of Silicon Carbide MOSFETs," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8277-8287, Oct. 2017.

[3] M. M. Swamy, T. Kume, and N. Takada, "An efficient resonant gate-drive scheme for high-frequency applications," *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1418–1431, Jul./Aug. 2012.