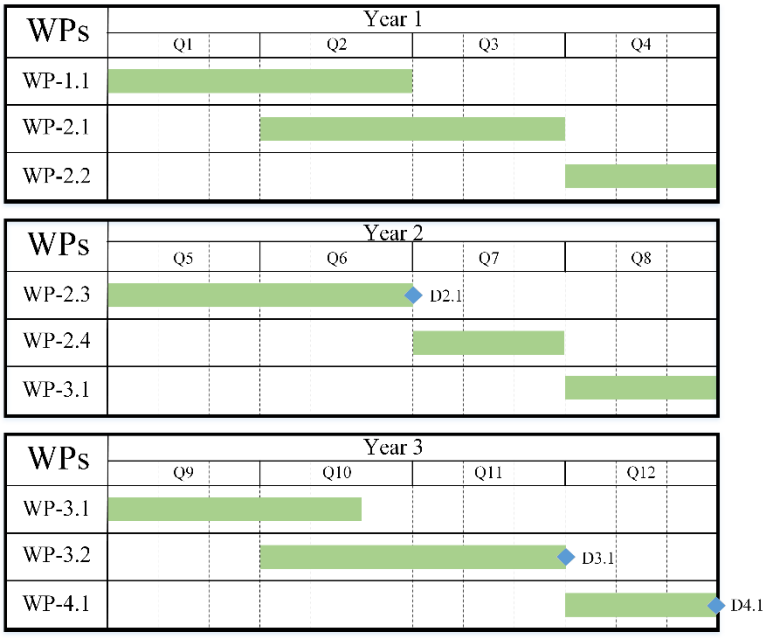
Performa for submitting project proposal for seeking financial support under
NaMPET Phase-III Programme
SUMMARY SHEET

1. Title of Project	**Smart gate driver and real time health monitoring of GaN HEMT**
2. Organization a) Name b) Address c) Legal status (indicate if Government Department, Statutory, Corporate Body, Registered Society, Private Company with recognized R&D unit etc.)	Indian Institute of Technology Kanpur Kalyanpur, Kanpur, Uttar Pradesh 208016 Government Educational Institute
3. Chief Investigator a) Name b) Designation c) Department d) Address e) Email, Fax, Tel, Mobile	Sandeep Anand Assistant Professor Department of Electrical Engineering ACES - 103 A, Dept. of Elec. Engg., IIT Kanpur - 208016 asandeep@iitk.ac.in Tel: (91) 512 259 7131
4. Nature of Project (Check one)	a) Research, Development & Engineering (R,D & E) leading to production capability b) ✓**Application oriented Research, Design and Development (R, D&D) having production potential** c) Basic R&D
5. Objective of the Project	1. Study the equivalent circuit model of GaN HEMT its modes of failures 2. Design and Development of Smart Gate Driver for GaN HEMT Devices 3. Integration of GaN parameter measurement circuit in the gate driver. 4. Technique for online health monitoring of GaN HEMT Devices employed in power electronics circuits using the smart gate driver.
6. Brief outline of the project with specific technology fall-outs	This project would focus on smart gate driver design with integrated electrical measurements. The key challenges related to gate driver design will be analyzed and solved. The measurement circuit for different electrical parameters for reliability

	assessment will be integrated with the gate driver. The measured electrical parameters using the gate driver, would be used for improving the reliability of GaN devices, by developing the real time health monitoring solution. (more details are included in Appendix-1)
7. Expected Deliverables	1. Developed smart gate driver for GaN HEMT with online parameter measurement 2. Online health monitoring technique for GaN HEMT 3. Report on experimental validation of online health monitoring technique
8. Expected Outcome in physical terms (as applicable)	Smart gate driver with integrated electrical parameter measurement for health monitoring of GaN HEMT
9. Agency with which link up is (Details may be given as applicable) established/ proposed	N/A
10. Duration of Project	3 Years
11. Month-wise break-up of physical activities with specific intermediate milestones on Quarterly basis	 WP-1.1 Study of existing gate driver circuits and modes of failures in GaN HEMT WP-2.1 Identification of measurement parameters of Smart gate driver WP-2.2 Design of smart gate driver WP-2.3 Fabrication of smart gate driver and testing WP-2.4 Fabrication of revised smart gate driver

	WP-3.1 Scheme development of online health monitoring of GaN HEMT with simulation WP-3.2 Experimental validation of online health monitoring scheme WP-4.1 Documentation and possibility of technology transfer **Deliverables:** D2.1 Developed smart gate driver for GaN HEMT with online parameter measurement D3.1 Online health monitoring technique for GaN HEMT D4.1 Report on experimental validation of online health monitoring technique
12. Likely End User(s)	Solar inverter manufacturers, aeronautical industry, space applications, telecommunication power supplies, wireless charging
13. Name of other organizations jointly participating in the project	IITD, IITM, IISc

14. Total Budget outlay
(details provided in Part III of this proposal)

Head	1st Year (in Lakhs INR)	IInd Year (in Lakhs INR)	IIIrd Year (in Lakhs INR)	Total (in Lakhs INR)
Capital Equipment	37.14	0	0	37.14
Consumable stores	10	10	10	30
Manpower	12.72	12.72	12.72	38.16
Travel & Training	3	3	3	9
Contingencies	1	1	1	3
Overheads (@20%)	12.772	5.344	5.344	23.46
Grand Total	**76.632**	**32.064**	**32.064**	**140.76**

14. a) Contribution of Project Implementing & other Organization in Total Budget Outlay b)NaMPET-III, MeitY Contribution	Rs. 0 Rs. 140.76 (in Lakhs)

Signature of Chief Investigator

Designation :

Date :

Signature of Head of the Department

Designation :

Date :

Signature of Head of the Institution/Organization

Designation :

Date :

Additional Information Required

1. Wherever applicable, Under S.No.13, share of the industry, collaborating agency, any other assistance and DIT's support required in the total cost of the Project may be provided under various budget heads.
2. Brief history of the electronics company including products being made, capacities, related collaborators, achievements, capabilities etc. may be provided (including recent annual reports and company brochure)
3. Please indicate recent major achievements of in-house R&D Unit of the electronics company in development of new products/processes, technology export, patent taken etc. and whether in-house R&D unit of the firm is recognized by DSIR.
4. Any other information in support of the proposal.

DETAILS OF THE PROPOSAL

PART 1: BACKGROUND INFORMATION

1. Title of Project	**Smart gate driver and real time health monitoring of GaN HEMT**
2. (i) Chief Investigator (ii) Co-Investigator	Sandeep Anand
3. Other Investigators of the Project with their designations	
4. Brief Bio-data of Chief Investigator and other Investigators (including publications/ patents) (Please attach separate sheets)	Attached CV
5. Competence of Investigator in Project Area (Including Industry interaction/ Technology transfer)	We have been working on **reliability of power electronic converters** from the last six years. In one of the projects sponsored by Artificial Limbs Manufacturing Corporation of India (ALIMCO), reliability study of flyback converter based battery charger was carried out. A comprehensive test regime was designed to test the charger under various input and environmental conditions. Modifications in the specification of the charger for improved reliability were suggested based on the test results. The research and development on **reliability of Insulated Gate Bipolar Transistor (IGBT) and Aluminum Electrolytic Capacitors (AECs)** are also under progress. In one of the projects, scheme is developed for on-line condition monitoring of bond wires present in IGBT package. The proposed method detects bond wire degradation using on-state collector emitter voltage (V_{on}) at the inflection point. Previously reported condition monitoring methods based on V_{on} as a precursor of aging require an accurate knowledge of junction temperature which is difficult to measure online during an inverter operation. The key advantage of the developed

	scheme is that it monitors the bond wire degradation irrespective of the junction temperature. The challenges in the V_{on} measurement are also addressed. The fast, accurate and online V_{on} measurement circuit is developed and integrated with the driver circuit of the IGBT. In reliability of AEC, the techniques for the online estimation of its capacitance and equivalent series resistance were proposed to determine the real time health. The reliability of AEC banks was analyzed and **health of individual capacitors** in the bank was estimated. The method for the accelerated aging of the AEC was also proposed. We are also working on GaN based power electronic converters. In a project sponsored by Indian Space Research Organization (ISRO), the viability of GaN HEMT for dc-dc converter applications for satellite application is explored. Two multioutput flyback converter prototypes with Si and GaN switches were developed for the same specifications to observe the direct benefits and challenges of using GaN switches. Flyback converter was designed to meet the transient and steady state performance using GaN HEMT. The developed converter was tested for thermal and electrical performance. It is observed that for same efficiency, GaN converter can have upto 10 times the switching frequency as compared to a Si converter. This results in significant reduction in capacitor and inductor size, resulting in a twofold improvement in overall power density. Our group is also working on **other aspects of power electronics**, including solar PV inverters, microgrids and power quality. A project on design and development of smart solar inverter with battery energy storage system is being carried out in collaboration

	with National Thermal Power Corporation (NTPC). The smart solar inverter includes the features like Low Voltage Ride Through (LVRT), High Voltage Ride Through (HVRT), Voltage Regulation System (VRS) and power ramp rate. A project on Voltage and Current Harmonic Compensation using Static Voltage Regulator was sponsored by Emerson Network Power (I) Pvt. Ltd.
6. Indicate the percentage of time the Chief Investigator and Co-Investigator would devote to the project.	35%
7. Whether similar project proposals (submitted by any of the Investigators) have been submitted elsewhere and awaiting consideration of MeitY and other funding agencies like DST, DRDO, DSIR, MHRD, ICICI, IDBI etc.	NO
8. Infrastructure and other facilities available at the institute for undertaking this project. a) List of major equipment along with model numbers, specifications etc.	o Solar Energy Research Enclave (SERE) o Real Time Digital Simulator (RTDS) o OPAL-RT o Typhoon Simulator o Chroma Model 61830 Regenerative Grid Simulator (30kVA, 0-300V, 0-100Hz) o 62050H-600S Programmable DC Power Supply (600V, 8.5A, 5000W) o Agilent E4360A Modular Solar Array Simulator Mainframe (1200W) o Omicron-Lab BODE 100 Frequency Response Analyser with all accessories o Fluke 434 Series II 3-Phase Energy Analyzer o Aplab Model-LD3210 Dual Output Power Supply o Fluke-62 Max Handheld Thermometer o Keysight U1733C Handheld LCR Meter (100Hz/120Hz/1kHz/10kHz/100kHz) o Tektronix PA1000 Single-Phase Power Analyzer o Fluke TiX520-9Hz Infrared Camera o Weller WR3000M Solder Rework Station o Yokogawa DL850E ScopeCorder

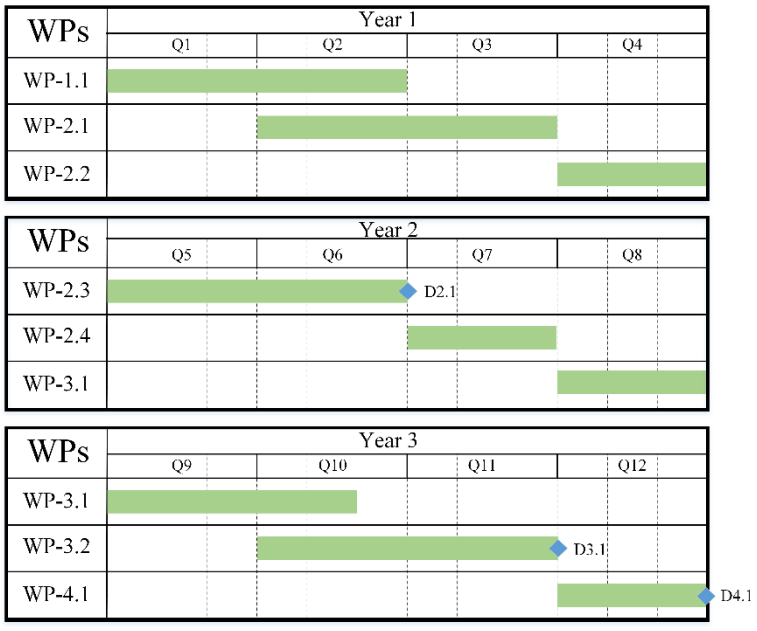
	o Tektronix Oscilloscope (500 MHz, 2.5 GS/s) o Industrial Oven with PID Temperature Control
b) Existing manpower and other personnel with names available for the project on full-time basis.	1. Paramahans Kumar Yadav (Project Technician) 2. Ph.D. Students
9. Expensive Equipment /facilities available elsewhere which could be made use of for the project.	o Power Device Analyzer / Curve tracer other measurement instruments for characterization of GaN HEMT, available at IISc Bangalore would be used for this project.
10. Details of collaborating agencies (As this would vary from project to project, necessary details may be given as appropriate)	IITD, IISc, IITM
11. Additional information, if any.	

PART II: TECHNICAL INFORMATION

1. Aim and Scope of the project (in terms of specific physical achievement)	This project would focus on smart gate driver design for GaN HEMT with integrated parameter measurements. The key challenges related to gate driver design will be analyzed and solved. The measurement circuit for different electrical parameters for reliability assessment will be integrated with the gate driver. The measured electrical parameters using the gate driver, would be used for improving the reliability of GaN devices, by developing the real time health monitoring solution.
2. Detailed description of the Project	Motivation, Literature Review, Methodology and Work Plan are included as Appendix – 1
3. Expected deliverables from the project	1. Developed smart gate driver for GaN HEMT with online parameter measurement 2. Online health monitoring technique for GaN HEMT 3. Report on experimental validation of online health monitoring technique
4. Need, forecast and urgency for the technology proposed to be developed with justification such as importance of know-how, import substitution role, pay off w.r.t. purchase of know-how or development of technology competitiveness, technology exports, international alliances possibilities etc.	There is significant potential for use of GaN HEMT in power electronic circuits. These devices are gaining popularity in space, aeronautical, telecom, solar inverters etc. However, there also are many challenges related to gate driver and reliable operation of the device, which need to be addressed before this potential can be fully accomplished. This project is centered around identifying these challenges and addressing them to ensure the reliable operation of the GaN devices in power electronic converters.
5. Specific manner in which know-how generated here is envisaged to be translated into production, details regarding a) The end product (with specifications to be attained etc.) b) Availability of pilot production facility in the organization	Smart gate driver with integrated measurement circuit. The real time electrical parameter measurement for health monitoring of GaN HEMT is also integrated with the gate driver.

6. a) Name of production agencies willing to productionise /use and market surveys if any made by them regarding demand for the product b) Alternative production/user agencies.	
7. Period required for completing the project	3 years
8. Details of work already done by present investigators/ R&D team in the proposed areas	We have been working on **reliability of power electronic converters** from the last six years. In one of the projects sponsored by Artificial Limbs Manufacturing Corporation of India (ALIMCO), reliability study of flyback converter-based battery charger was carried out. A comprehensive test regime was designed to test the charger under various input and environmental conditions. Modifications in the specification of the charger for improved reliability were suggested based on the test results. The research and development on **reliability of Insulated Gate Bipolar Transistor (IGBT) and Aluminum Electrolytic Capacitors (AECs)** are also under progress. In one of the projects, scheme is developed for on-line condition monitoring of bond wires present in IGBT package. The proposed method detects bond wire degradation using on-state collector emitter voltage (V_{on}) at the inflection point. Previously reported condition monitoring methods based on V_{on} as a precursor of aging require an accurate knowledge of junction temperature which is difficult to measure online during an inverter operation. The key advantage of the developed scheme is that it monitors the bond wire degradation irrespective of the junction temperature. The challenges in the V_{on} measurement are also addressed. The fast, accurate and online V_{on} measurement circuit is developed and integrated with the driver circuit of the IGBT. In reliability of AEC, the techniques for the online estimation of its capacitance and equivalent series resistance were proposed to determine the real time health. The reliability of AEC banks was analyzed and **health of individual**

	capacitors in the bank was estimated. The method for the accelerated aging of the AEC was also proposed. We are also working on GaN based power electronic converters. In a project sponsored by Indian Space Research Organization (ISRO), the viability of GaN HEMT for dc-dc converter applications for satellite application is explored. Two multioutput flyback converter prototypes with Si and GaN switches were developed for the same specifications to observe the direct benefits and challenges of using GaN switches. Flyback converter was designed to meet the transient and steady state performance using GaN HEMT. The developed converter was tested for thermal and electrical performance. It is observed that for same efficiency, GaN converter can have upto 10 times the switching frequency as compared to a Si converter. This results in significant reduction in capacitor and inductor size, resulting in a twofold improvement in overall power density. Our group is also working on **other aspects of power electronics**, including solar PV inverters, microgrids and power quality. A project on design and development of smart solar inverter with battery energy storage system is being carried out in collaboration with National Thermal Power Corporation (NTPC). The smart solar inverter includes the features like Low Voltage Ride Through (LVRT), High Voltage Ride Through (HVRT), Voltage Regulation System (VRS) and power ramp rate. A project on Voltage and Current Harmonic Compensation using Static Voltage Regulator was sponsored by Emerson Network Power (I) Pvt. Ltd.
9. Summary of similar work being done elsewhere in the country	A team of researchers at IISc Banglore are working on design, process and fabrication of GaN HEMT on silicon platform. GaN based circuits are also being explored at IITB. In IITD and IITM, the work on Silicon Carbide (SiC) based converters and its gate driver design is under process. However, there is limited focus on package level reliability and online health monitoring techniques for GaN, which is being proposed in this project.

10. a) Specific problems, hold-ups and difficulties foreseen in the implementation of the project. b) If the answer is not Nil to 10(a), how does Chief Investigator propose to overcome them?	1) One of the practical difficulties in using GaN HEMT would be its soldering and mounting for power electronic application. Soldering of GaN HEMTs in surface mount package having a very small footprint is a challenge. Manufacturers like EPC make GaN HEMTs in passivated die form with ball grid array (BGA) or land grid array (LGA) packaging. There is a possibility of the solder balls melting and creating a short circuit among themselves if the soldering process is not done precisely. If the drain and source of the GaN HEMT are shorted then it might lead to destruction of the device when a voltage is applied across them. IIT Kanpur has recently acquired a state-of-the-art rework soldering station for soldering BGA package chips properly. 2) Heat evacuation from small GaN HEMT packages adds complexity to the prototype design. Proper thermal design must be done such that the heat generated from losses in the switch gets evacuated to the environment quickly. The most effective way to improve vertical heat transfer through a PCB is to add plated through-hole thermal vias between conductive layers. Since the PCB material has very low thermal conductivity, thermal via design is one of the predominating factors for total PCB thermal resistance. PCB thickness also has an impact on the thermal via performance.
11. Detailed PERT/BAR Chart with activities broken in to sub-activities on monthly basis and specific intermediate milestones on Quarterly basis	

	WP-1.1 Study of existing gate driver circuits and modes of failures in GaN HEMT WP-2.1 Identification of measurement parameters of Smart gate driver WP-2.2 Design of smart gate driver WP-2.3 Fabrication of smart gate driver and testing WP-2.4 Fabrication of revised smart gate driver WP-3.1 Scheme development of online health monitoring of GaN HEMT with simulation WP-3.2 Experimental validation of online health monitoring scheme WP-4.1 Documentation and possibility of technology transfer **Deliverables** D2.1 Developed smart gate driver for GaN HEMT with online parameter measurement D3.1 Online health monitoring technique for GaN HEMT D4.1 Report on experimental validation of online health monitoring technique
12. Details of possible alternative arrangements if the Chief Investigator leaves institution or is unable for any other reason to continue on this project.	
13. Name of other organizations in India or Abroad jointly participating in this effort, extent of their involvement, specific division of responsibility, accountability etc.	
14. List the personnel already working in the organization who would be transferred to work full time on this project.	1. Paramahans Kumar Yadav (Project Technician) 2. Ph.D Student
15. Name of experts whom the CI would invite to join the project team as full time/part time member.	

PART III - FINANCIAL DETAILS

Table – 1(a) Yearly Break-up (Year -1)

Budget requirements for the Year -1 (Please provide separate breakup for each year of the project duration)

(Rs.in lakhs)

Sl. No (1)	Head (2)	Local expenses (3)	Foreign Exchan-ge (FE) (4)	Duty (5)	Total (6)	Part of 6 to be borne by participating/ other organization (*7)	Amt. Payable by NaMPET, DIT (8)
1	Capital Equipment	26.24	10.9	0	37.14	0	37.14
2	Consumable stores	10	0	0	10	0	10
3	Manpower	12.72	0	0	12.72	0	12.72
4	Travel/ Training	3	0	0	3	0	3
5	Contingencies other expenditure debitable to this project	1	0	0	1	0	1
6	Overhead, if any	12.772	0	0	12.772	0	12.772
Total: Rs.76.632				**Others: Rs.0**		**MeitY. Rs.**	**76.632**

*Total cost of the project and contribution to be made by the organization/other organization should be shown separately.

Table – 1(b) Yearly Break-up (Year -2)

Budget requirements for the Year -1 (Please provide separate breakup for each year of the project duration)

(Rs.in lakhs)

Sl. No (1)	Head (2)	Local expenses (3)	Foreign Exchange (FE) (4)	Duty (5)	Total (6)	Part of 6 to be borne by participating/ other organization (*7)	Amt. Payable by NaMPET, DIT (8)
1	Capital Equipment	0	0	0	0	0	0
2	Consumable stores	10	0	0	10	0	10
3	Manpower	12.72	0	0	12.72	0	12.72
4	Travel/ Training	3	0	0	3	0	3
5	Contingencies other expenditure debitable to this project	1	0	0	1	0	1
6	Overhead, if any	5.344	0	0	5.344	0	5.344
		Total: Rs.32.064		**Others: Rs.0**		**MeitY. Rs.**	**32.064**

*Total cost of the project and contribution to be made by the organization/other organization should be shown separately.

Table – 1(c) Yearly Break-up (Year -3)

Budget requirements for the Year -1 (Please provide separate breakup for each year of the project duration)

(Rs.in lakhs)

Sl. No (1)	Head (2)	Local expenses (3)	Foreign Exchange (FE) (4)	Duty (5)	Total (6)	Part of 6 to be borne by participating/ other organization (*7)	Amt. Payable by NaMPET, DIT (8)
1	Capital Equipment	0	0	0	0	0	0
2	Consumable stores	10	0	0	10	0	10
3	Manpower	12.72	0	0	12.72	0	12.72
4	Travel/ Training	3	0	0	3	0	3
5	Contingencies other expenditure debitable to this project	1	0	0	1	0	1
6	Overhead, if any	5.344	0	0	5.344	0	5.344
		Total: Rs. 32.064		**Others: Rs.0**		**MeitY. Rs. 32.064**	
		Grand Total				**Rs. (in lakhs) 140.76**	

*Total cost of the project and contribution to be made by the organization/other organization should be shown separately.

Table II: Capital Equipment			
Sl. No	**Equipment**	**Description**	**Estimated Cost (Rs. in Lakhs)**
1	Optically Isolated voltage probe	Galvanically isolated measurement solution specialized for GaN measurements. As the switching frequency of GaN HEMTs is very high compared to Si MOSFETs, proper measurement of its various waveforms is essential. For example, normal differential probes will induce unwanted noise in the measured waveform of a gate to source voltage. Unlike all other commercially available probes, optically isolated probes use an electro-optic sensor to convert the input signal to optical modulation, which electrically isolates the device-under-test from the oscilloscope giving much accurate results.	14.2
2	Differential voltage and current probes (4 no)	For measuring various voltages and currents in the gate driver and converter.	7.64
3	DC Power Supplies (2 nos)	Programmable and reliable DC sources which can provide high currents. High amount of currents will be flown through GaN HEMT devices for inducing stress in it. This is essential for reliability testing of GaN HEMT.	10.9
4	Computer (3 nos)	Computers will be required for running software, carrying out simulation and various design suites. Out of total 3 systems, one system will be dedicated for gate driver design, one system for GaN HEMT reliability studies, and one for experimentation.	2.4
5	Humidity Chamber (1 no)	Humidity testing will be done to determine the behavior of the GaN HEMT in severe test conditions and environments that involve fluctuating environment, high temperature, and different relative humidity. The tests will be done in a dynamic state where the moisture is used to induce a failure of the GaN HEMT switches.	2
Total			**37.14**

Table III: Consumable Stores			
Sl. No	**Major Components**	**Description**	**Estimated Cost (Rs. in Lakhs)**
1.	GaN Devices	GaN HEMT switches are being manufactured by various companies. Different voltage and current rated GaN HEMT from different manufacturers would be required for failure analysis. As modes of failure of GaN HEMTs would be tested, a large number of switches are bound to get destroyed.	7
2.	Inductors, cores, Capacitors, Resistors, coils, rheostats	These would be used for developing the laboratory prototype.	5
3.	Multilayered PCB Fabrication Costs	Printed circuit boards would be designed and fabricated to validate the proposed schemes experimentally. Multilayered PCBs will be used for proper thermal design as well as EMI shielding through careful placement of power and ground layers.	5
4.	Heat sink and cooling solutions, fans and blowers	Custom made heatsinks / cooling solution suited for the application will be used.	5
5.	Current Sensors, Gate driver ICs, voltage isolators, connectors, surge protectors, relays, DSPs, LEDs, batteries, temperature sensors, transformers, wire and cables, solder paste, flux paste	These would be used for developing smart gate drive and converter laboratory prototype.	8
			30

Table IV: Manpower details						
Sl. No	Designation of Post	Monthly Salary (Rs.)	Year I			Role of the Member
			No of post	MM	Expenditure (Rs. in Lakhs)	
1.	Post Doc Fellow / Senior Project Scientist	55000	1	12	6.6	To work on the reliability of GaN HEMT. Understanding failure mechanism, analyzing the problems and identifying suitable solutions.
2.	Project Engineering / Project Associate	31000	1	12	3.72	Simulations using suitable tools / packages would be carried out. Would also be designing the printed circuit boards (PCBs).
3.	Project Technician	20000	1	12	2.4	Procurement, assembling components, and testing etc.
TOTAL = 3 x 12.72/year = 38.16 Lakhs						

Part IV

Endorsement by the Head of the Institution

1. I have read the terms & conditions (including special terms & conditions for co-financing) governing the grant-in-aid and I agree to abide by them.

2. I certify that I have no objection to the submission of this research proposal for consideration by the NaMPET, Department of Information Technology

3. In case the project is approved, I undertake to make available facilities to carry it out, to arrange for the submission of periodic progress reports and other information that may be required by the NaMPET, Department of Information Technology and In general to ensure that the conditions attached to the award of such grant are fulfilled by my institution/organization.

4. I certify that in case present chief investigator is not available for any reason to continue work on this project, the following persons will be available to carry it throughout to completion:

Sl. No.	Name	Designation
1		
2		

5. I certify that the facilities mentioned in the body of this report are available at my institution.

6. I certify that I shall ensure that accounts will be kept of the funds received and spent and made available on demand, as specified and required by the NaMPET/ Department of Information Technology.

7. I certify that I am the competent authority, the virtue of the administrative and financial powers vested in me by to undertake the above stated commitments on behalf of my institution.

Signature of the
Head of the Institution
Designation
Date:

Appendix-1
(Project Description)

1.1 Motivation and Literature Review

An underlying advantage of the Gallium Nitride (GaN) high electron mobility transistor (HEMT) over similarly rated silicon (Si) MOSFETs is that it can switch faster, thereby allowing higher switching frequency and/or reduced switching losses [1]. The higher switching speeds and lower on-state resistances enable power electronic converters with smaller form factor and higher efficiency. Some of the other benefits of GaN HEMTs are low gate and output capacitance, absence of reverse recovery charge, and small footprint.

Although, there is significant potential for GaN technology for application to power electronic circuits, it suffers from challenges related to gate driver design and reliable operation of the device. These issues need to be addressed before this potential can be fully accomplished. E-mode GaN HEMTs have unique gate driver requirements, which are different from those for Si MOSFETs. The threshold voltage of an enhancement mode GaN HEMT is approximately 1.6 V, and the recommended voltage for its on-state is typically around 5 V. This only allows a few volts of oscillation (due to parasitic RLC elements) before any unintended turn-on event occurs. Also, even a small gate voltage overshoot may destroy the device completely. A few gate driver ICs available in the market are designed for the requirements of GaN devices. For example, the LM5113 from Texas Instruments is designed to drive both the high-side and the low-side enhancement mode GaN HEMTs in a synchronous buck or a half bridge configuration. However, this driver is not well suited for high voltage applications, as this can isolate the high-side driver only up to 100 V [2]. One of the methods to prevent unintended turn on events is to provide a negative gate voltage during the OFF period. However, this is an imperfect solution for GaN devices, because it makes reverse conduction losses during dead time considerably higher. One solution proposed in [3] is to provide a three-level gate voltage (positive, zero and negative) to the primary switch in a resonant SEPIC converter. However little research has been conducted for other converter configurations.

The high frequency operation of wide bandgap devices (e.g. GaN, SiC) result in significant gate driver losses with conventional resistive gate driver circuits. Resonant gate driving techniques help in reducing these gate drivers related losses. A resonant gate driver circuit based on series

resonance was proposed in [4] and applied to Silicon Carbide (SiC) devices. Compared to a conventional resistive gate driver circuit, it has been reported to be able to reduce driver losses by 50%. High speed switching transients increase the influence of parasitic inductances in device packaging and printed circuit board (PCB) traces, thereby worsening the ringing that occurs during the switching transient, which limits the switching speed and may cause damage to the device. Minimizing the high frequency loop inductance results in lower voltage overshoot, improved input voltage capability, and reduced electromagnetic interference (EMI). The impact of circuit parasitics on converter efficiency has been assessed in [5]. It suggests methods for improved PCB design, which decreases the value of parasitic inductance by 40%. Overall parasitics can be reduced by integrating the gate driver into the module, i.e. a single device and gate driver combined in a surface-mount package [6].

Besides the challenges related to gate driver design, the GaN HEMT also suffers from reliability issues. Enhancement mode (e-mode) GaN HEMTs are normally-off (by using schottky gate) and are preferred over depletion mode (d-mode) GaN HEMTs [7]. GaN HEMTs are generally fabricated on epitaxial layers that are grown on Si, SiC or GaN substrates. Among them, Si is the least expensive material and there is a large and well-developed infrastructure to process GaN HEMT on silicon substrates [8]. This leads to high concentration of defects due to lattice mismatch between GaN and substrate. With the improvement in fabrication process, these defects are minimised. However, in actual application, the device undergoes different stresses such as thermal, electrical and mechanical. The prolonged operation of the device under stressful environment may cause potential reliability issues in different regions of the device, according to the operating conditions.
GaN is a high-temperature-tolerant material. But for a Schottky gate device, the semiconductor–metal contact degrades due to high temperature. Also, defects in the crystal lattice will be accelerated at high temperatures [8]. Also, due to aging, the current collapse effect significantly limits the current performance. Current collapse is mainly caused by trapped charges in the device. Majorly, the traps are formed under the gate or in the channel between gate and drain [9]. If the trapping exists under the gate, there would be a dynamical shift in the gate threshold voltage. In the semi-on-state (at lower gate voltage), the trapping of negative charge may dominate. In the off-state, the charge

trapping may be promoted by the high reverse gate voltage and high gate leakage current levels [10]. This is shown in Fig. 1(a) and 1(b).

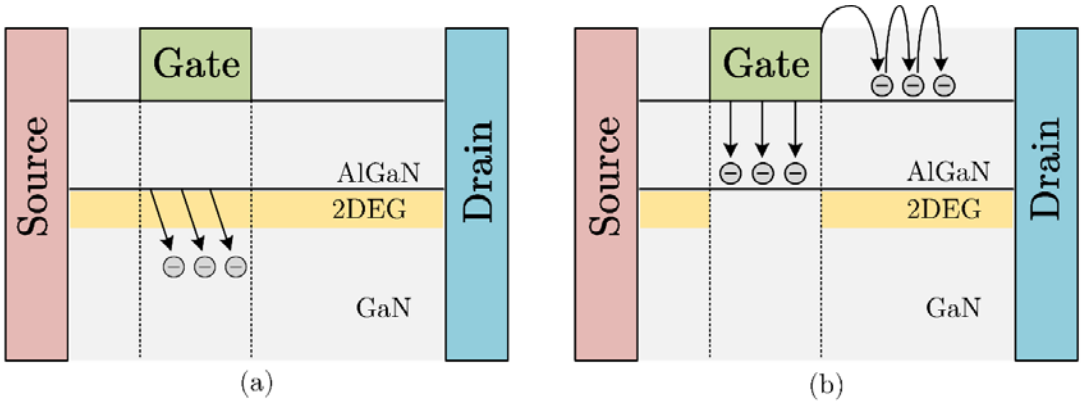


Figure 1: Possible trapping mechanisms in (a) semi-on-state and (b) off- state bias operating points.

The trapped charges would significantly affect the performance of the device such as increase/decrease in gate threshold voltage, change in drain-source voltage and current characteristics, variation in transconductance etc. The reliability of GaN HEMTs are also affected under the reverse-bias condition, where the electric field of a GaN HEMT is not uniformly distributed along the channel between gate and drain. It is very high at the drain side of the gate. When the electric field at this location reaches the breakdown electric field, it leads to the increase in tunneling leakage [11]. Also, the crystal structure of GaN acquires the piezoelectric properties. The electric field stress generates the mechanical strain, that can lead to lattice damage [8, 12]. Furthermore, for GaN HEMT on Si substrate, the lattice mismatch between Si and GaN results in severe cracks. Defects originated from cracking can reduce the insulation performance of the GaN buffer layer and the Si substrate. This may lead to severe leakage current and a low vertical breakdown voltage [13].

All the above-mentioned device degradation/failure mechanisms would affect its reliable operation. The crystal defects and trapped charges would turn-on/off the device unwillingly. This would lead to the loss of control over the gate driving of the device. It is required to make the gate driver smarter enough to adapt the operating conditions and health of the device. Furthermore, to employ the GaN HEMT in applications successfully and to ensure the reliable operation, real time health monitoring of the device is essential. This would prevent the catastrophic failure of the device/system.

1.2 Methodology

The methodology for research and development of smart gate driver with online health monitoring of GaN HEMT, to be followed in this project is described below:

1.2.1 Effect of circuit parasitics

Due to the high operating frequency, GaN HEMTs are exposed to remarkably higher voltage and current slew rates, which can affect the performance of the transistor. Fig. 2 shows an example of a synchronous buck converter with GaN HEMTs showing all the parasitic elements. The common source inductance consists of the common source inductance in the device package and the parasitic inductance of the PCB trace.

When Q2 is turned off and after a dead time Q1 is turned on, the sudden change of current through Q2 will induce a voltage across LS2. With insufficient damping of the OFF state gate loop LCR resonant tank, this voltage could induce ringing and may cause an unintended turn on of Q2. Similarly, LS1 may also lead to unintended turn on of Q1. It is possible to prevent this type of turn on by sufficiently damping the gate turn off loop; however, this is not a viable solution because it will lead to additional gate driver losses. The best way to improve di/dt immunity is to minimize LS1 and LS2 by improving package and PCB layout. Ways to reduce common source inductance by careful design of the PCB, possibly utilizing several layers would be explored in this project. Based on the study of the circuit parasitics, the gate driver will be designed with optimized PCB.

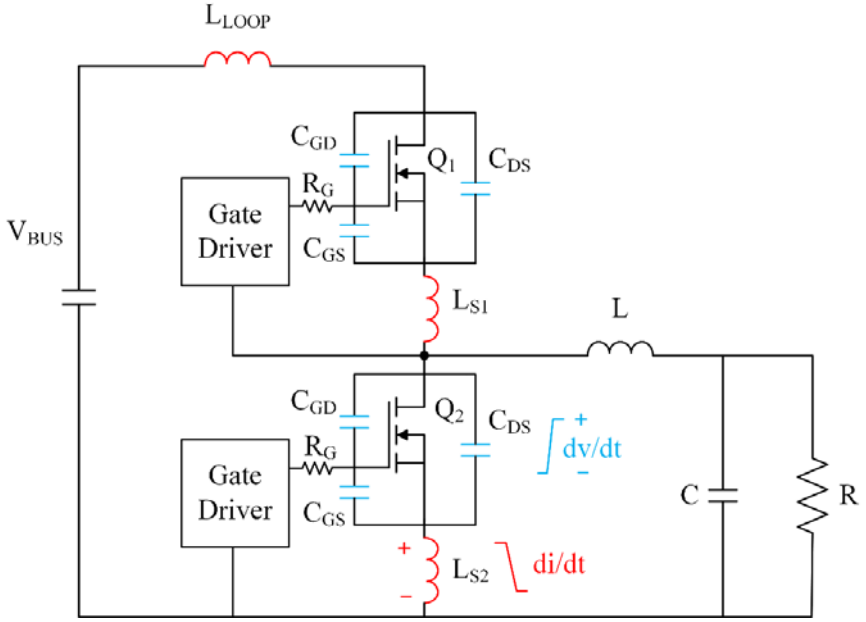
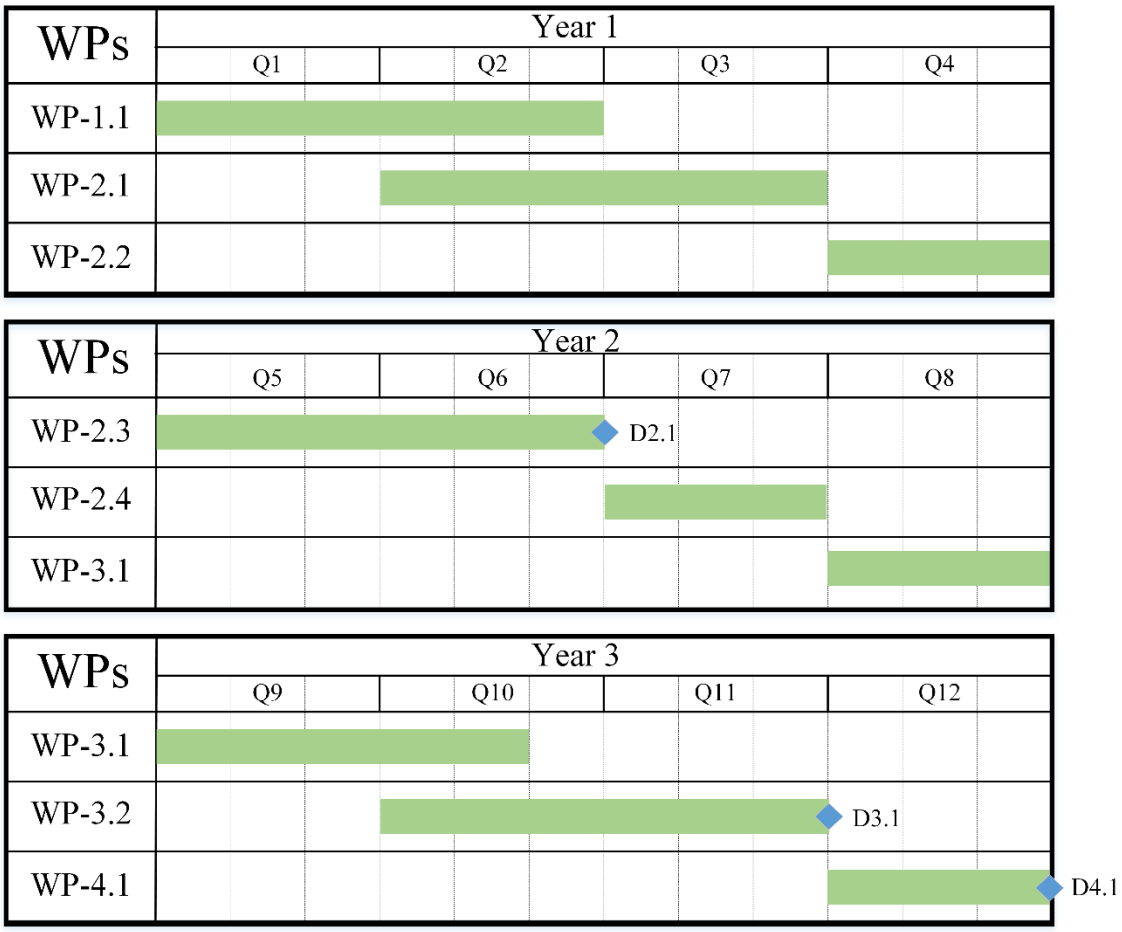


Figure 2: Circuit parasitics in a half bridge configuration.

1.2.2 Identification of electrical parameters for measurement

The reliability of GaN HEMT suffers due to thermal, electrical and mechanical stresses, which it undergoes during actual converter operation. The thermal performance of GaN devices is limited due to poor quality of material, change of surface charge distribution etc. The device operation at high temperature would degrade the metal-semiconductor interface in a GaN HEMT [3]. The prolonged operation of the device at high temperature would also affect the performances such as maximum drain current, transconductance and threshold voltage. Also, during reverse bias, high gate–drain electric field is responsible for degradation of the device due to inverse piezoelectric effect [8]. The thermal and electrical stresses would also result in charge trapping in different regions of the device crystal lattice. This would result in increase/decrease in gate threshold voltage, change in drain-source voltage and current characteristics, variation in transconductance etc. It is necessary to identify the electrical parameter(s) which could be utilized to determine the deterioration in performance of the device. In this project, study will be done to find the measurable electrical parameter(s), which could lead to the health status of the device. The measurement circuit of the chosen electrical parameter(s) would be integrated with the gate driver. This will make the gate driver adaptive to the operating conditions and health of the device – smart gate driver. The measured electrical parameter will also be utilised in developing the real time health monitoring of the GaN HEMT. This will provide the health status of the device online, which would reduce the downtime of the system and prevent catastrophic failure.

1.3 Work Plan



The work packages are listed below

WP-1.1 Study of existing gate driver circuits and modes of failures in GaN HEMT

WP-2.1 Identification of measurement parameters of Smart gate driver

WP-2.2 Design of smart gate driver

WP-2.3 Fabrication of smart gate driver and testing

WP-2.4 Fabrication of revised smart gate driver

WP-3.1 Scheme development of online health monitoring of GaN HEMT with simulation

WP-3.2 Experimental validation of online health monitoring scheme

WP-4.1 Documentation and possibility of technology transfer

1.4 Deliverables

D2.1 Developed smart gate driver for GaN HEMT with online parameter measurement
D3.1 Online health monitoring technique for GaN HEMT
D4.1 Report on experimental validation of online health monitoring technique

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