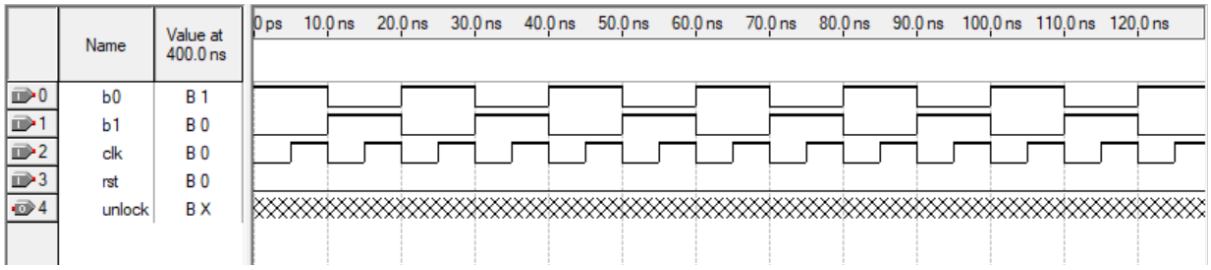
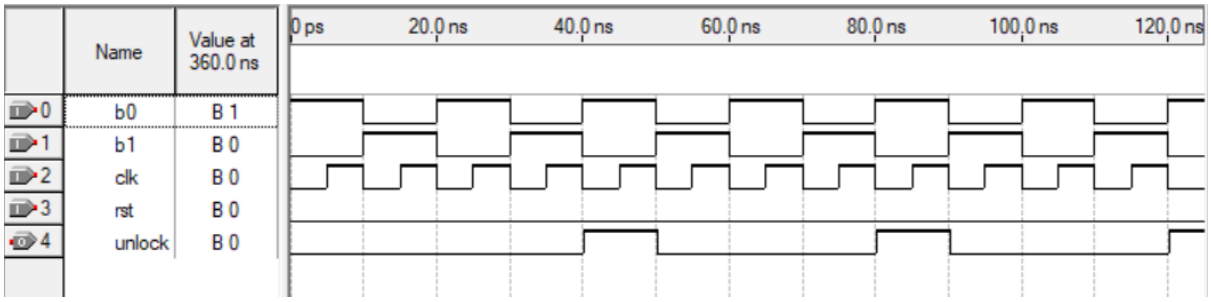
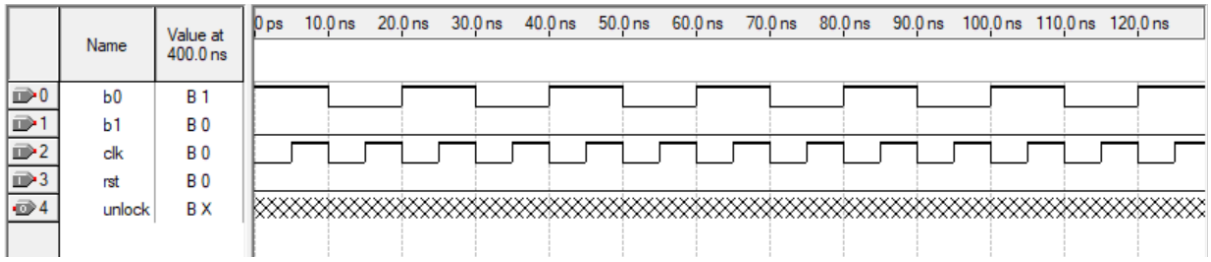
```
module electronic_lock(clk,rst,b0,b1,unlock);
 output reg unlock;
 input clk,rst;
 input b0,b1;

 reg [2:0] state;
 reg [2:0] next_state;

 parameter [2:0] s_rst=3'b000;
 parameter [2:0] s1=3'b001;
 parameter [2:0] s2=3'b010;
 parameter [2:0] s3=3'b011;
 parameter [2:0] s4=3'b100;

always @(posedge clk)
        begin
                if (rst)
                        state=s_rst;
                else
                        state=next_state;
        end

always @(state,b0,b1)
        begin
                case(state)
                  s_rst: next_state = b0 ? s1 : b1 ? s_rst : state;
                  s1: next_state = b0 ? s1 : b1 ? s2 : state;
                  s2: next_state = b0 ? s3 : b1 ? s_rst : state;
                  s3: next_state = b0 ? s1 : b1 ? s4 : state;
                  s4: next_state = b0 ? s1 : b1 ? s_rst : state;
                  default: next_state = s_rst;
                endcase
        end
```

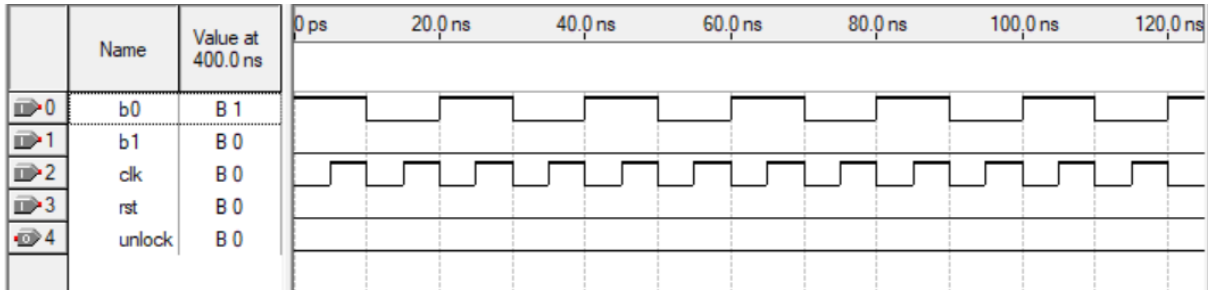
```
always @(state)
        begin
                case(state)
                  s_rst : unlock<=1'b0;
                  s1 : unlock<=1'b0;
                  s2 : unlock<=1'b0;
                  s3 : unlock<=1'b0;
                  s4 : unlock<=1'b1;
                  default : unlock<=1'b0;
                endcase
        end

endmodule
```

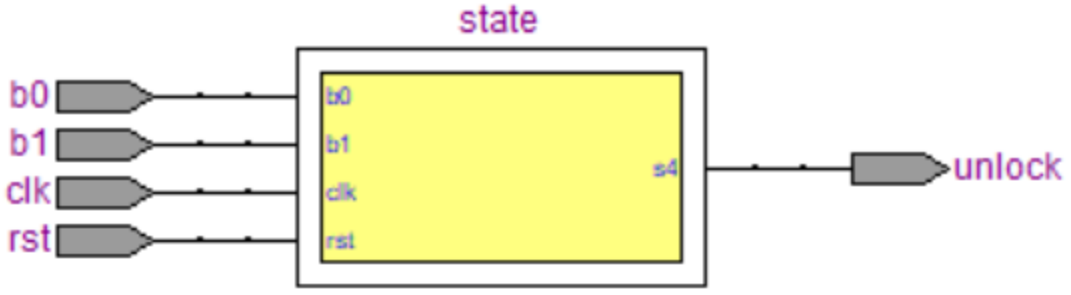
Flow Status	Successful - Tue Sep 24 20:24:47 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	electronic_lock
Top-level Entity Name	electronic_lock
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	7 / 12,480 (< 1 %)
Dedicated logic registers	6 / 12,480 (< 1 %)
Total registers	6
Total pins	5 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final


Name
Value at 400.0 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
120.0 ns
0 b0 B 1
1 b1 B 0
2 clk B 0
3 rst B 0
4 unlock B X


Name
Value at 360.0 ns
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
0 b0 B 1
1 b1 B 0
2 clk B 0
3 rst B 0
4 unlock B 0


Name
Value at 400.0 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
120.0 ns
0 b0 B 1
1 b1 B 0
2 clk B 0
3 rst B 0
4 unlock B X


Name
Value at 400.0 ns
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
0 b0 B 1
1 b1 B 0
2 clk B 0
3 rst B 0
4 unlock B 0


state
b0
b1
clk
rst
b0
b1
clk
rst
s4
unlock