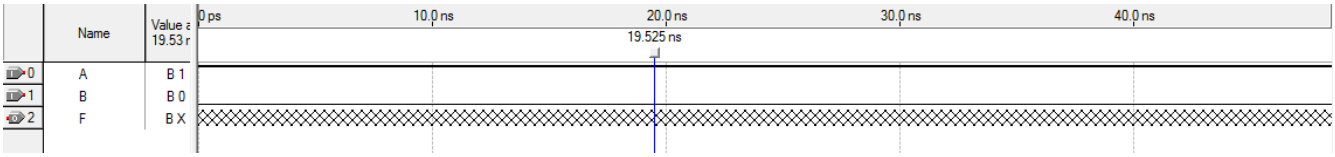
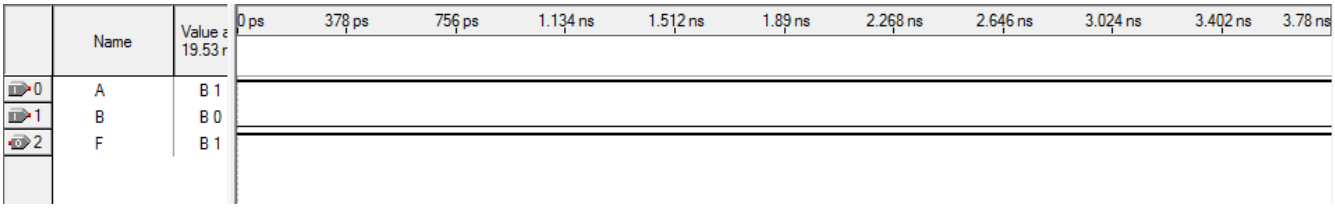
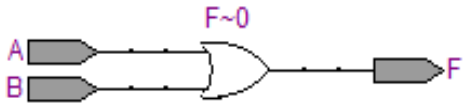
OR Gate

```
module my_OR(A, B, F);
input A, B;
output F;
assign F= A|B;
endmodule
```

Flow Status	Successful - Mon Sep 16 11:14:42 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_OR
Top-level Entity Name	my_OR
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	3 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



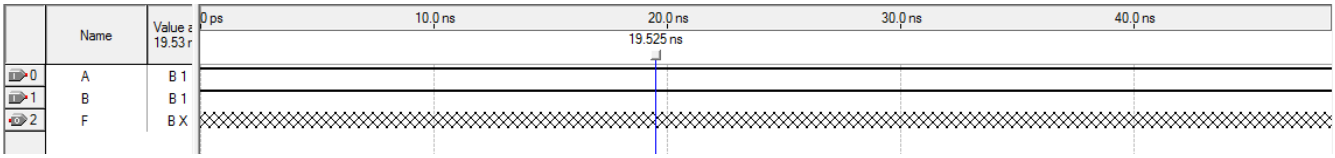


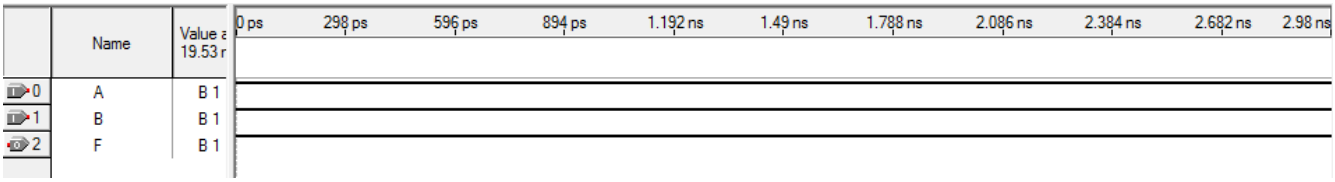


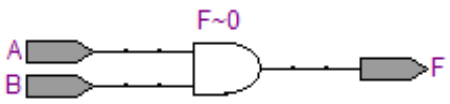
AND Gate

```
module my_AND(A, B, F);
input A, B;
output F;
assign F= A&B;
endmodule
```

Flow Status	Successful - Mon Sep 16 11:18:19 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_AND
Top-level Entity Name	my_AND
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	3 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



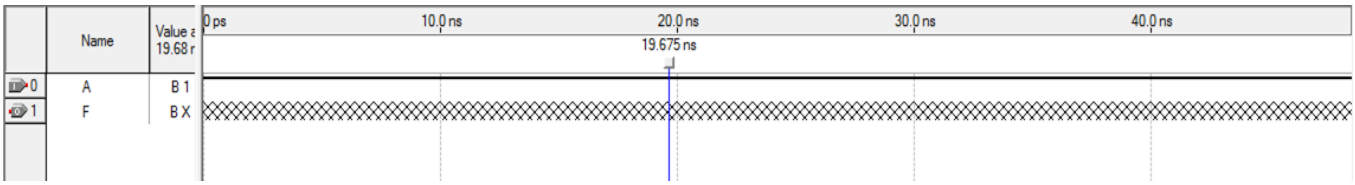


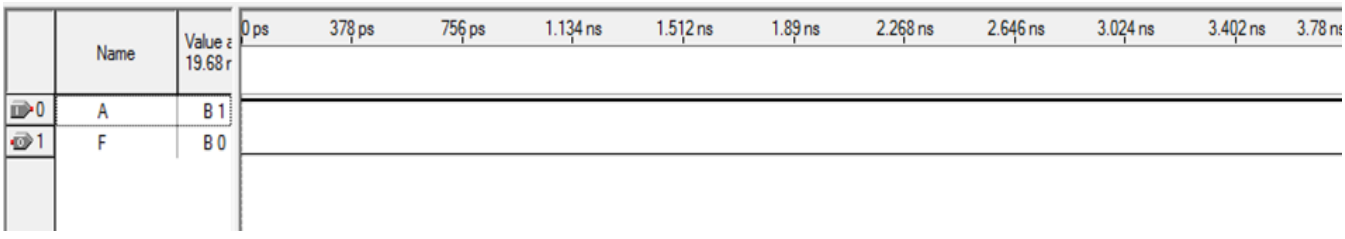


NOT:

```
module my_NOT(A, F);
input A;
output F;
assign F= ~A;
endmodule
```

Flow Status	Successful - Mon Sep 16 10:37:33 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_NOT
Top-level Entity Name	my_NOT
Family	Stratix II
Met timing requirements	Yes
Logic utilization	0 %
Combinational ALUTs	0 / 12,480 (0 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	2 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

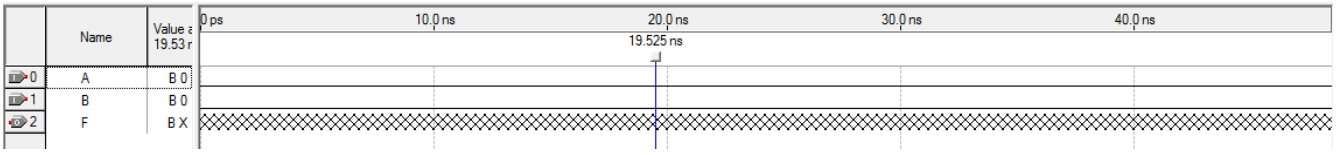


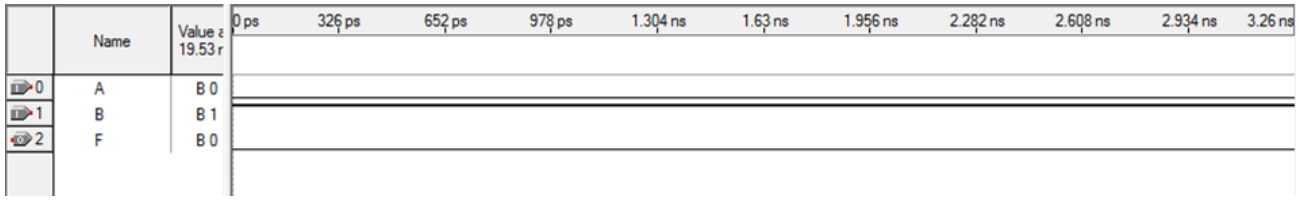


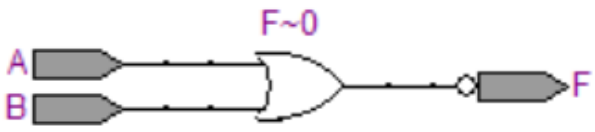
NOR:

```
module my_NOR(A, B, F);
input A, B;
output F;
assign F= ~(A|B);
endmodule
```

Flow Status	Successful - Mon Sep 16 10:54:29 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_NOR
Top-level Entity Name	my_NOR
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	3 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



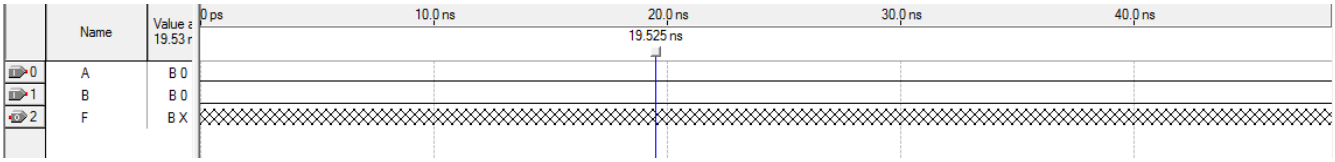


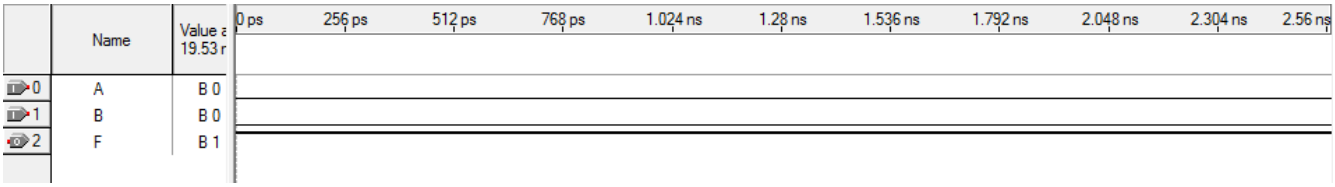


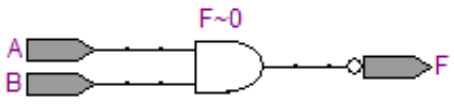
NAND:

```
module my_NAND(A, B, F);
input A, B;
output F;
assign F= ~(A&B);
endmodule
```

Flow Status	Successful - Mon Sep 16 10:59:53 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_NAND
Top-level Entity Name	my_NAND
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	3 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



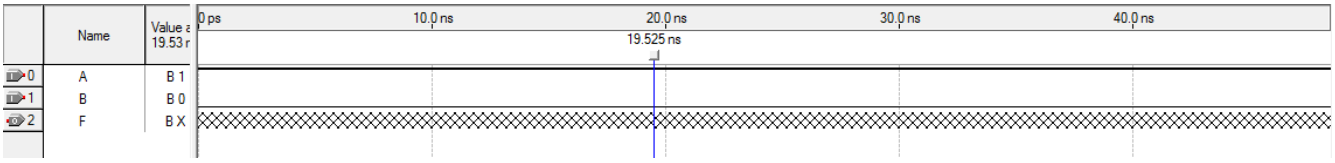


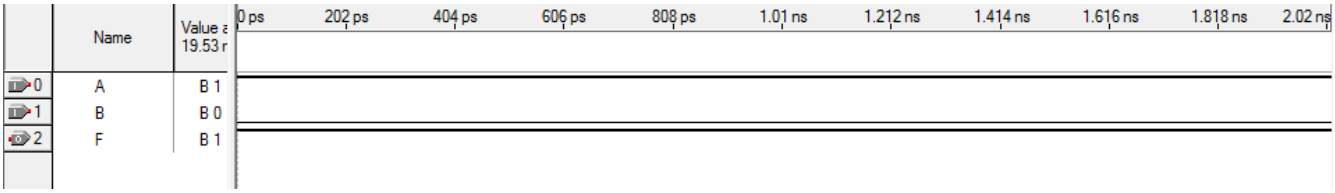


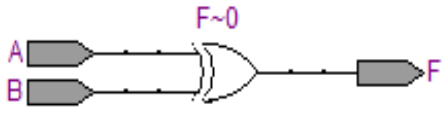
EX-OR:

```
module my_XOR(A, B, F);
input A, B;
output F;
assign F= A^B;
endmodule
```

Flow Status	Successful - Mon Sep 16 11:03:36 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_XOR
Top-level Entity Name	my_XOR
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	3 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



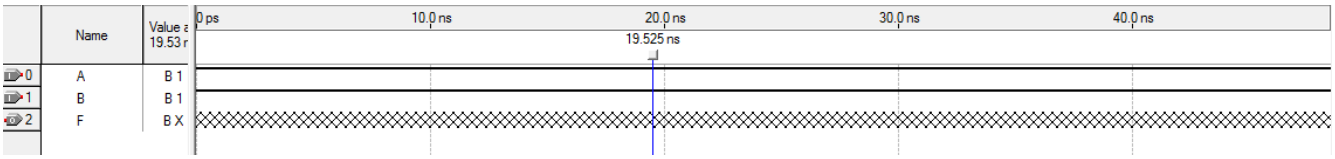


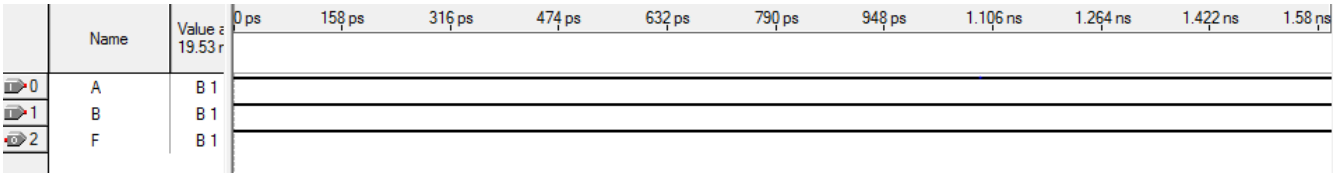


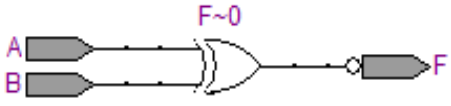
EX-NOR:

```
module my_XNOR(A, B, F);
input A, B;
output F;
assign F= ~(A^B);
endmodule
```

Flow Status	Successful - Mon Sep 16 11:07:26 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_XNOR
Top-level Entity Name	my_XNOR
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	3 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



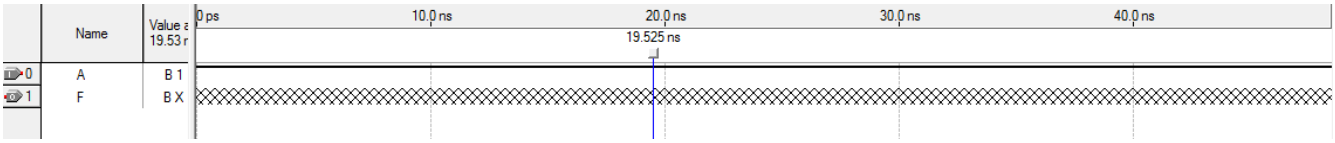


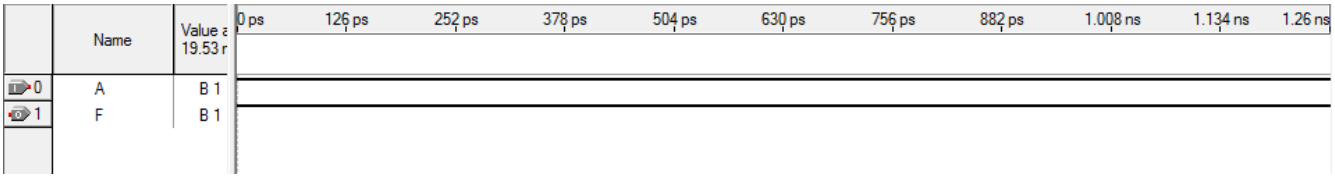


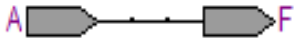
BUFFER:

```
module my_BUF(A, F);
input A;
output F;
assign F= A;
endmodule
```

Flow Status	Successful - Mon Sep 16 11:11:06 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	my_BUF
Top-level Entity Name	my_BUF
Family	Stratix II
Met timing requirements	Yes
Logic utilization	0 %
Combinational ALUTs	0 / 12,480 (0 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	2 / 343 (< 1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



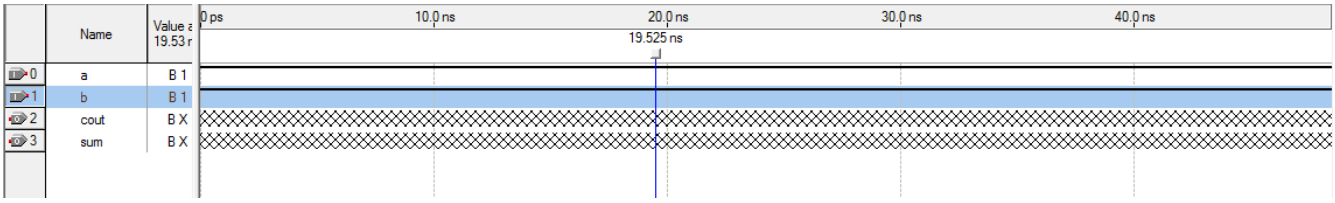


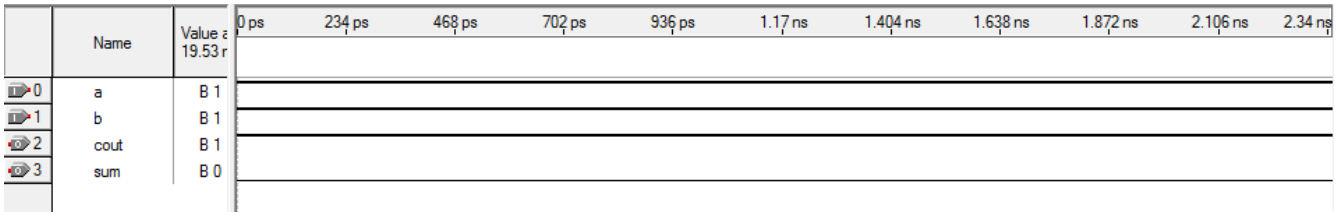


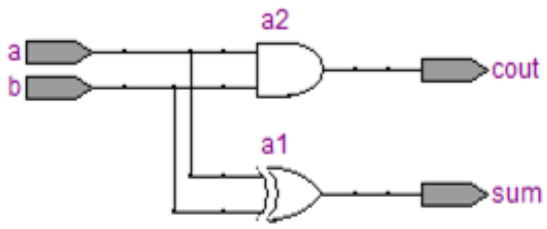
HALF ADDER:

```
module HalfAdder(a, b, sum, cout);
input a, b;
output sum, cout;
xor a1(sum, a, b);
and a2(cout, a, b);
endmodule
```

Flow Status	Successful - Mon Sep 16 11:25:44 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	HalfAdder
Top-level Entity Name	HalfAdder
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	2 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	4 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



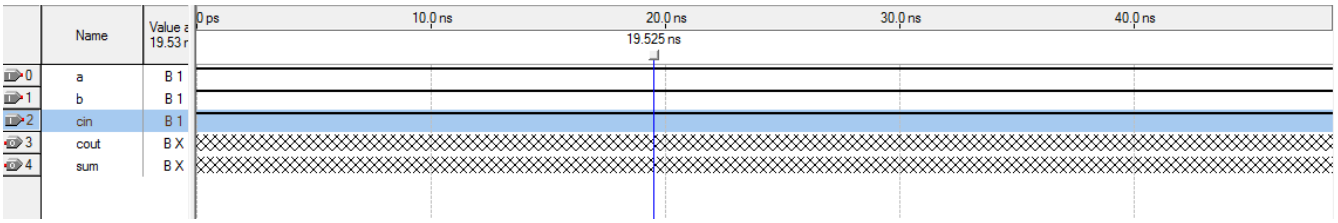


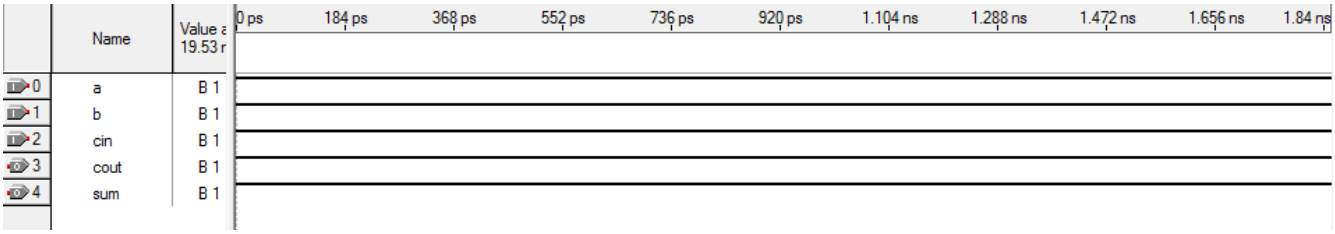


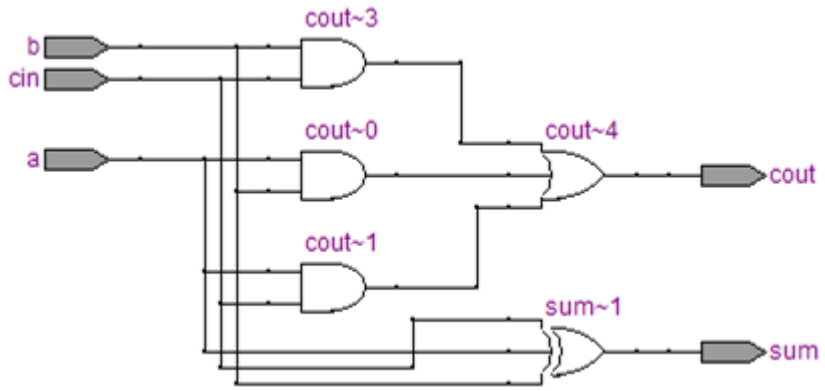
FULL ADDER:

```
module FullAdder(a,b,cin,sum,cout);
input a,b,cin;
output sum, cout;
reg sum, cout; // registers retain value
always @ (a or b or cin) // Anytime a or b or cin CHANGE, run the process
begin sum <= a ^ b ^ cin;
        cout <= (a & b) | (a & cin) | (b & cin);
        end
endmodule
```

Flow Status	Successful - Mon Sep 16 11:29:21 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	FullAdder
Top-level Entity Name	FullAdder
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	2 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	5 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



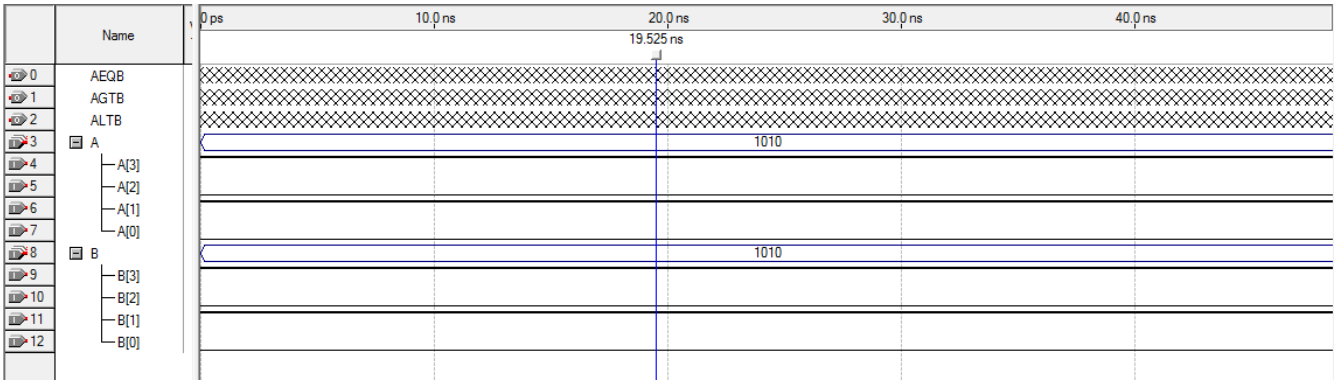


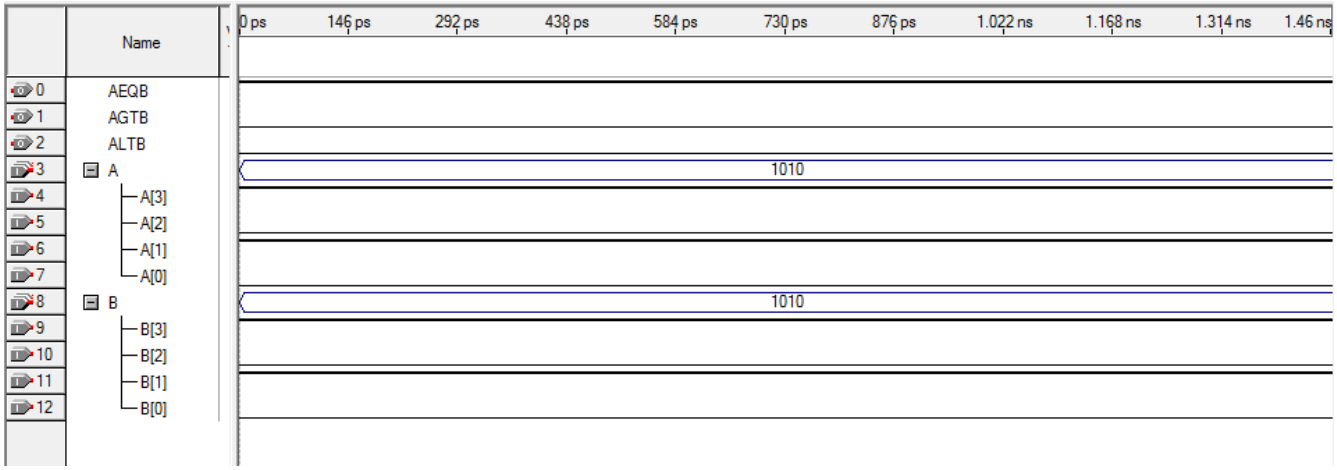


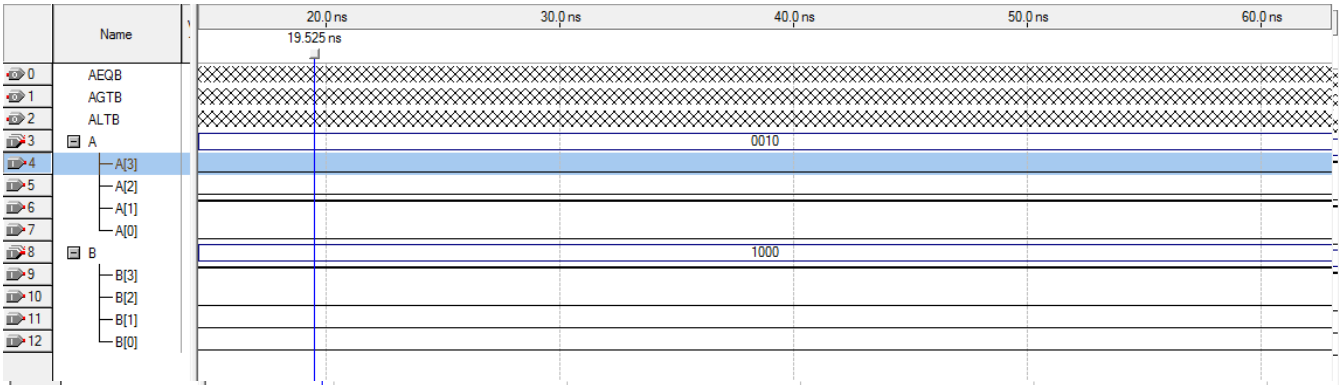
4 bit Magnitude Comparator :

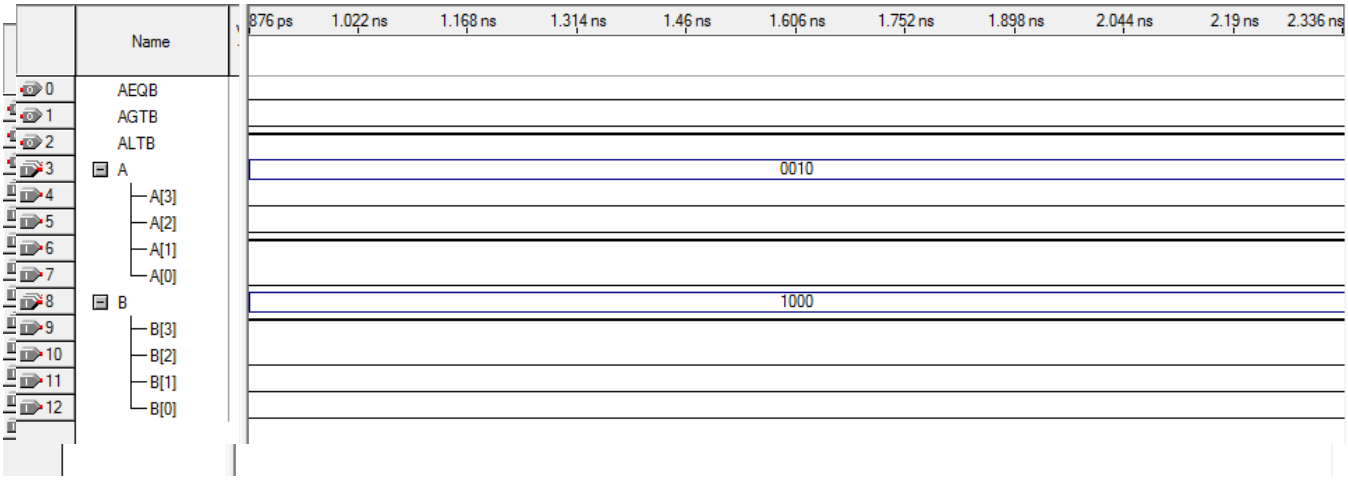
```
module mag_comp (A,B,ALTB,AGTB,AEQB);
input [3:0] A,B;
output ALTB,AGTB,AEQB;
assign ALTB = (A < B),
       AGTB = (A > B),
       AEQB = (A == B);
endmodule
```

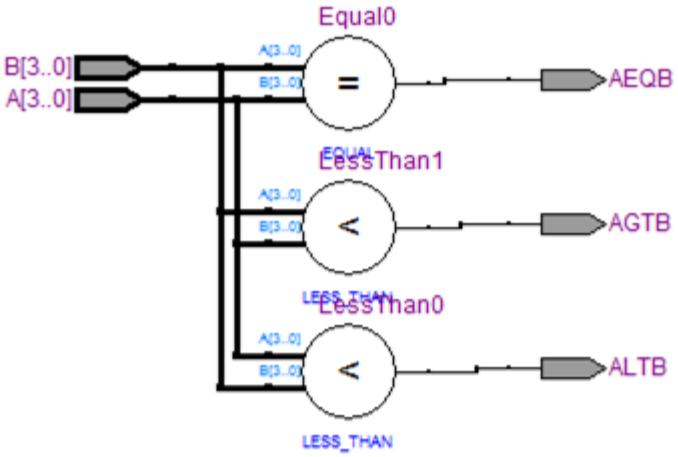
Flow Status	Successful - Mon Sep 16 11:32:22 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	mag_comp
Top-level Entity Name	mag_comp
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	6 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	11 / 343 (3 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final


Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
19.525 ns
0 AEQB
1 AGTB
2 ALTB
3 A
4 A[3]
5 A[2]
6 A[1]
7 A[0]
8 B
9 B[3]
10 B[2]
11 B[1]
12 B[0]
1010
1010


Name
0 ps
146 ps
292 ps
438 ps
584 ps
730 ps
876 ps
1.022 ns
1.168 ns
1.314 ns
1.46 ns
0 AEQB
1 AGTB
2 ALTB
3 A
4 A[3]
5 A[2]
6 A[1]
7 A[0]
8 B
9 B[3]
10 B[2]
11 B[1]
12 B[0]
1010
1010


Name
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
19.525 ns
0 AEQB
1 AGTB
2 ALTB
3 A
4 A[3]
5 A[2]
6 A[1]
7 A[0]
8 B
9 B[3]
10 B[2]
11 B[1]
12 B[0]
0010
1000

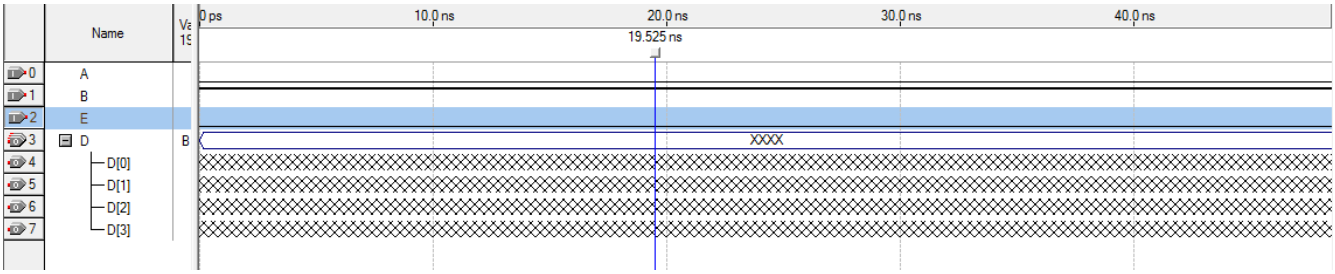

Name
876 ps
1.022 ns
1.168 ns
1.314 ns
1.46 ns
1.606 ns
1.752 ns
1.898 ns
2.044 ns
2.19 ns
2.336 ns
0 AEQB
1 AGTB
2 ALTB
3 A
4 A[3]
5 A[2]
6 A[1]
7 A[0]
8 B
9 B[3]
10 B[2]
11 B[1]
12 B[0]
0010
1000

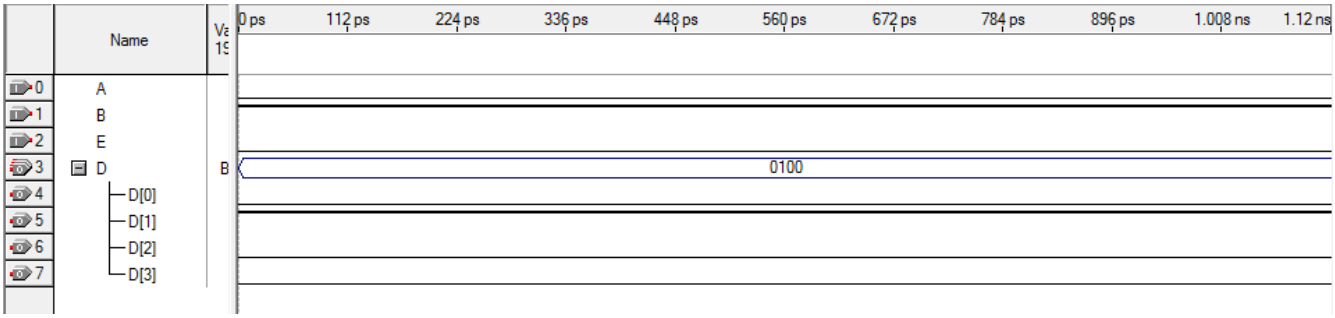


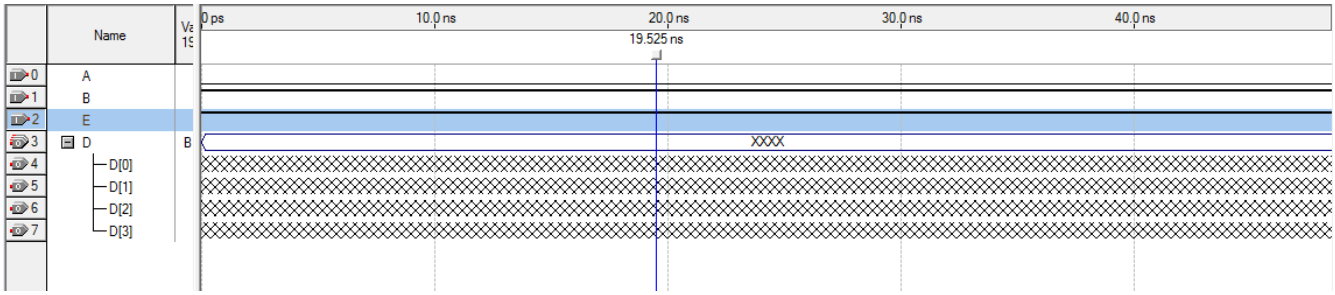
2:4 Decoder

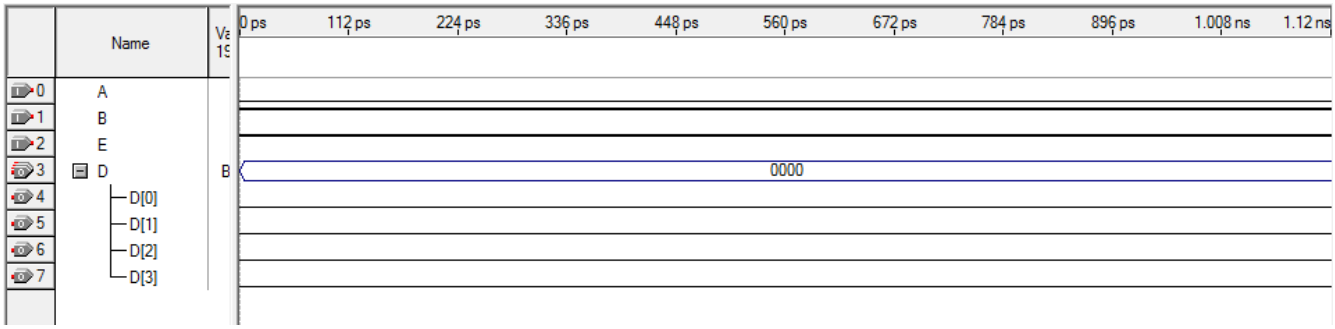
```
module DECODER2_4 (A,B,E,D);
input A,B,E;
output [0:3] D;
assign D[0] = ~(~A & ~B & ~E),
       D[1] = ~(~A & B & ~E),
       D[2] = ~(A & ~B & ~E),
       D[3] = ~(A & B & ~E);
endmodule
```

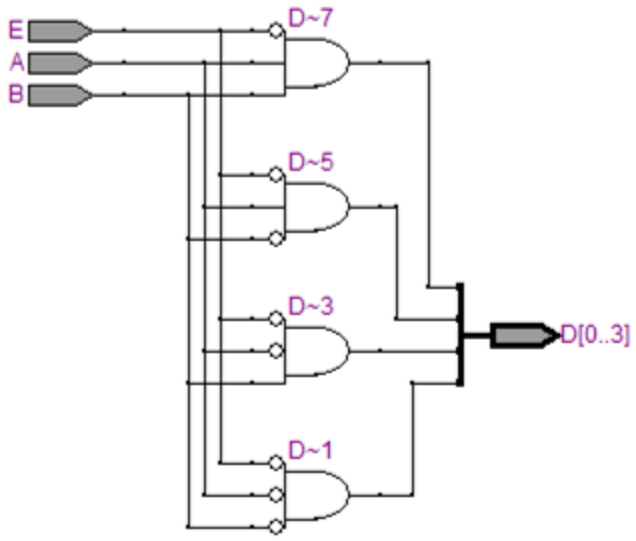
Flow Status	Successful - Mon Sep 16 11:40:40 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DECODER2_4
Top-level Entity Name	DECODER2_4
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	4 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	7 / 343 (2 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final


Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
19.525 ns
A
B
E
D
D[0]
D[1]
D[2]
D[3]
XXXX


Name
0 ps
112 ps
224 ps
336 ps
448 ps
560 ps
672 ps
784 ps
896 ps
1.008 ns
1.12 ns
A
B
E
D
D[0]
D[1]
D[2]
D[3]
0100


Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
19.525 ns
A
B
E
D
D[0]
D[1]
D[2]
D[3]
XXXX

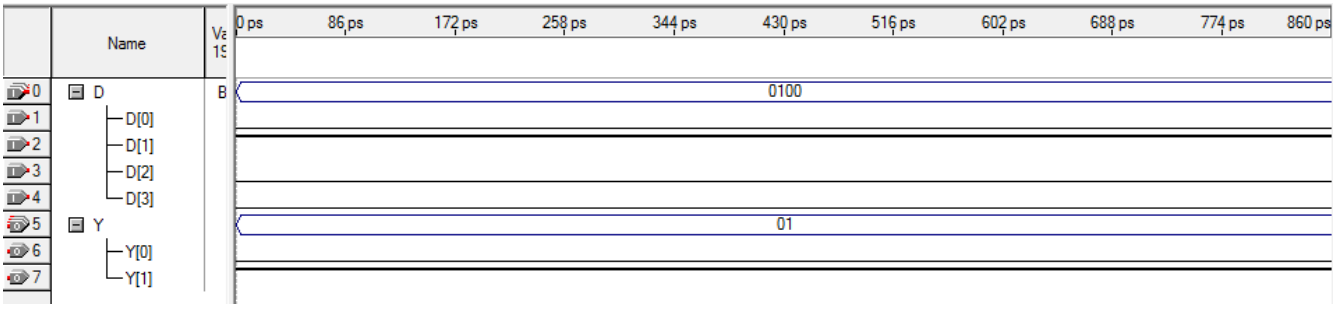

Name
0 ps
112 ps
224 ps
336 ps
448 ps
560 ps
672 ps
784 ps
896 ps
1.008 ns
1.12 ns
A
B
E
D
D[0]
D[1]
D[2]
D[3]
0000

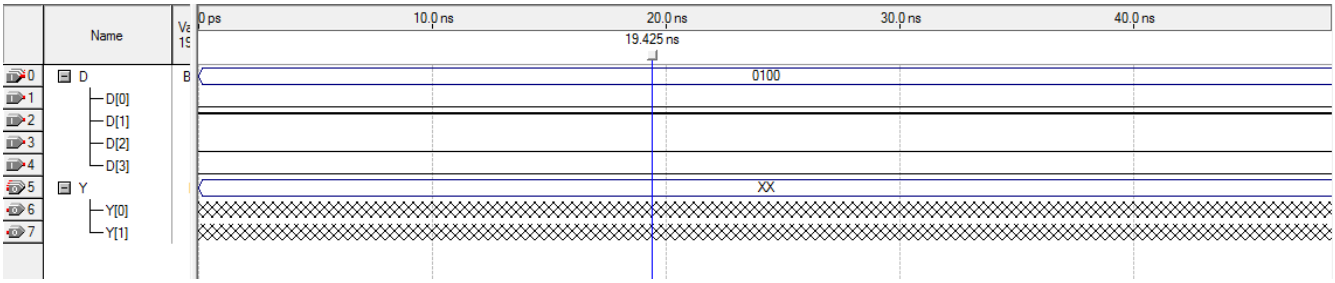

E
A
B
D~7
D~5
D~3
D~1
D[0..3]

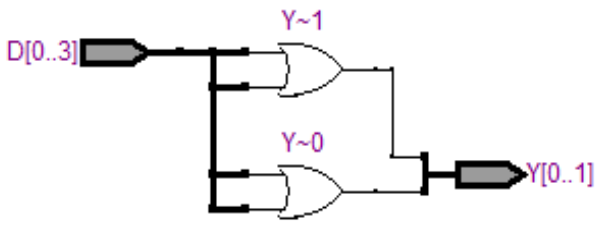
ENCODER 4:2:

```
module ENCODER4_2 (D, Y);
input [0:3] D;
output [0:1] Y;
assign Y[0] = (D[2]|D[3]),
 Y[1] = ( D[1]|D[3]);
endmodule
```

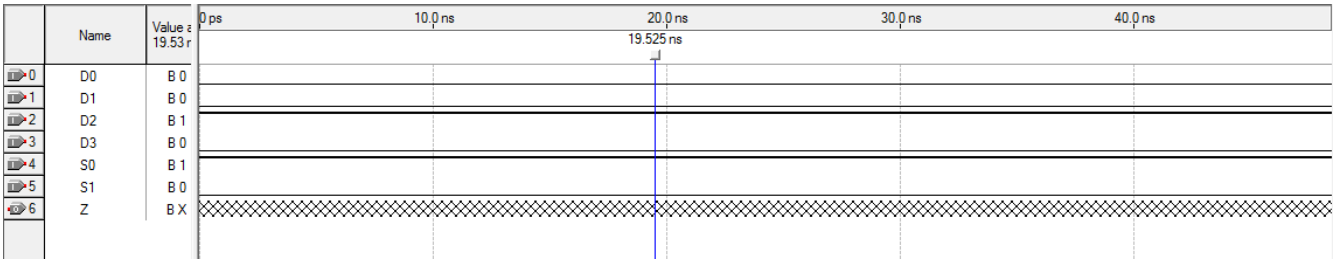
Flow Status	Successful - Mon Sep 16 11:49:46 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	ENCODER4_2
Top-level Entity Name	ENCODER4_2
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	2 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	6 / 343 (2 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

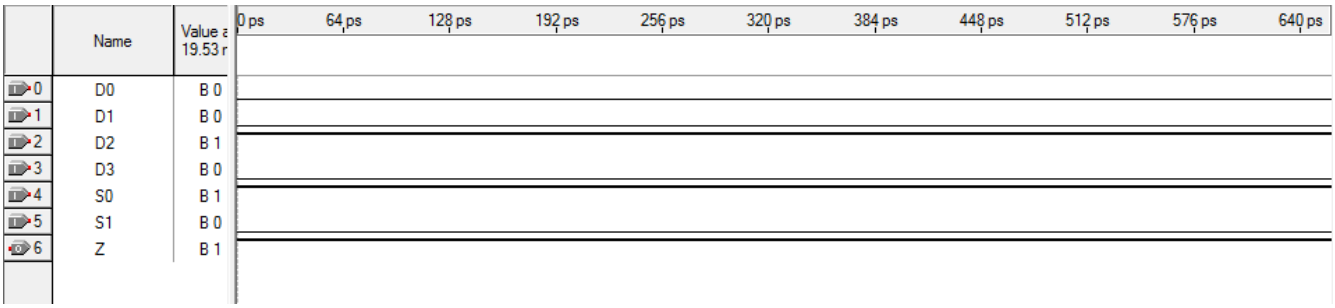


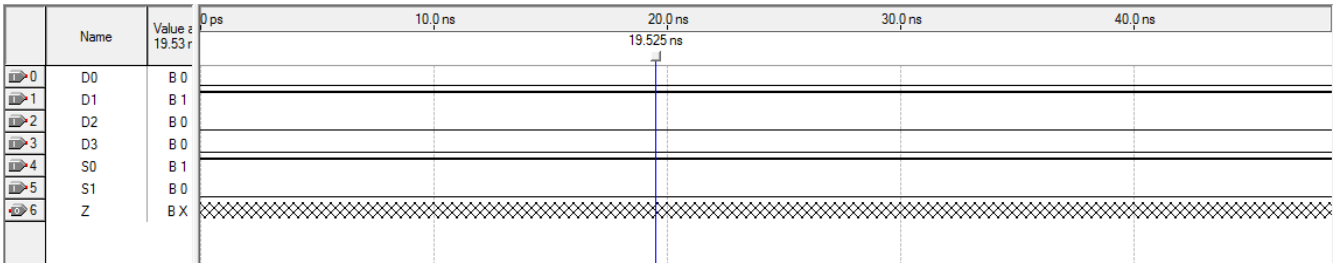


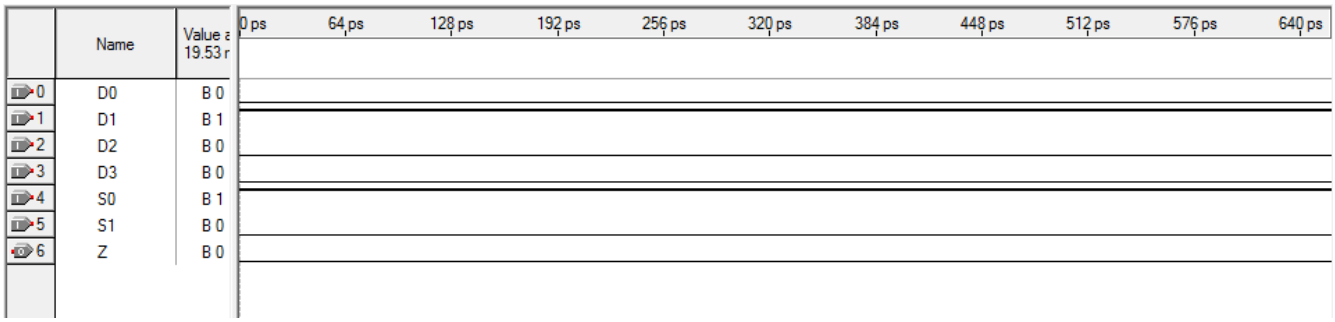


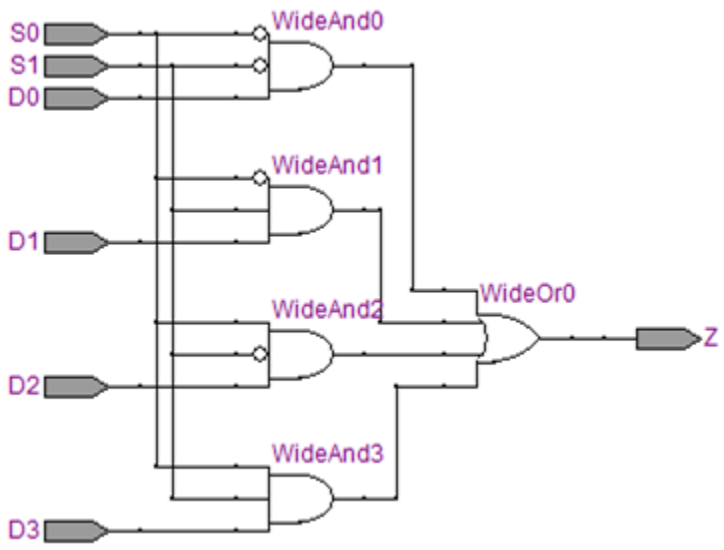
```
module MUX4x1(Z, D0, D1, D2, D3, S0, S1);
output Z;
input D0, D1, D2, D3, S0, S1;
and (T0, D0, S0BAR, S1BAR),
      (T1, D1, S0BAR, S1),
      (T2, D2, S0, S1BAR),
      (T3, D3, S0, S1);
not (S0BAR, S0),
     (S1BAR, S1);
nor(Z, T0, T1, T2, T3);
endmodule
```





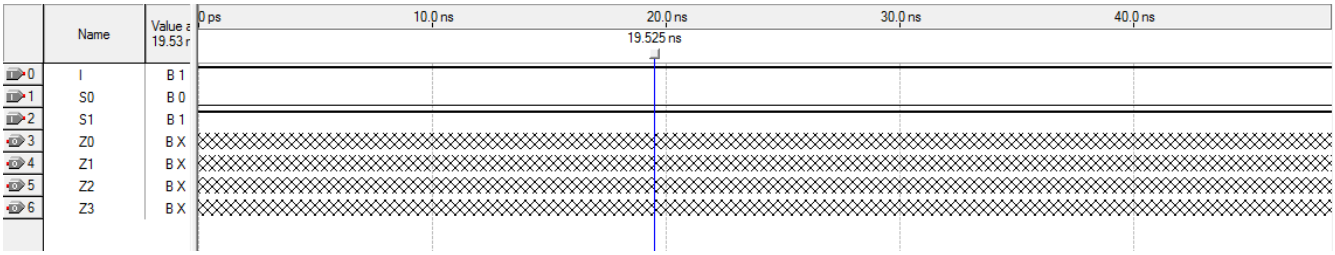


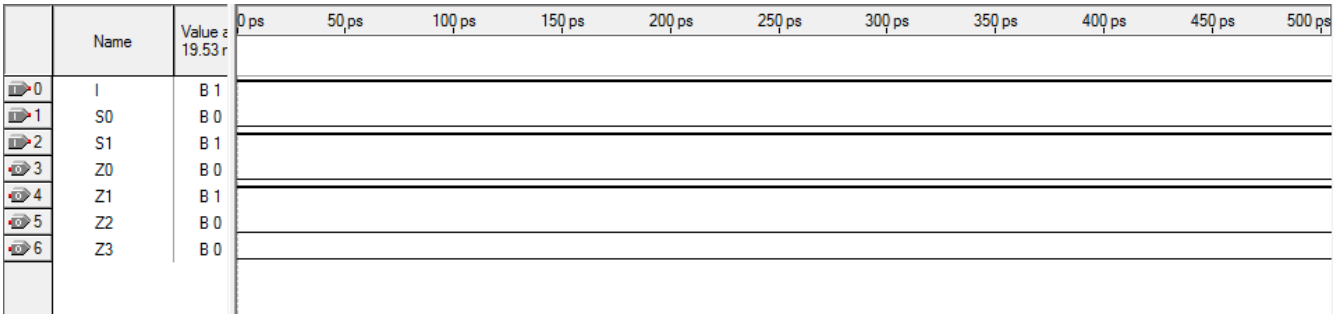


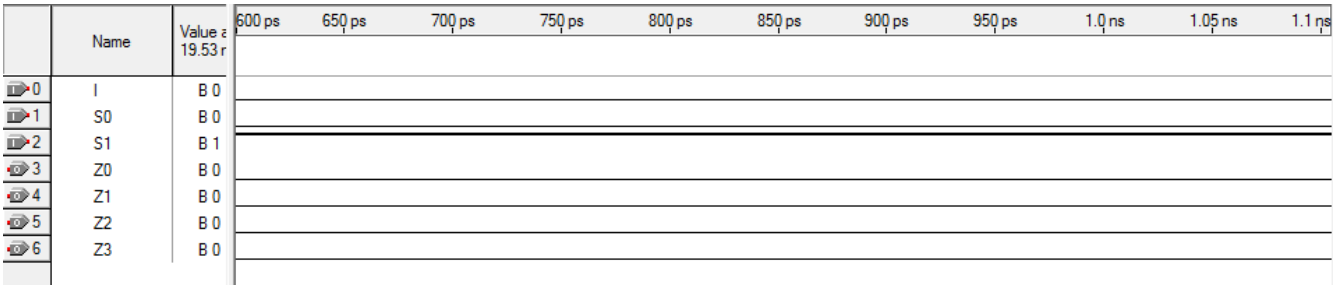


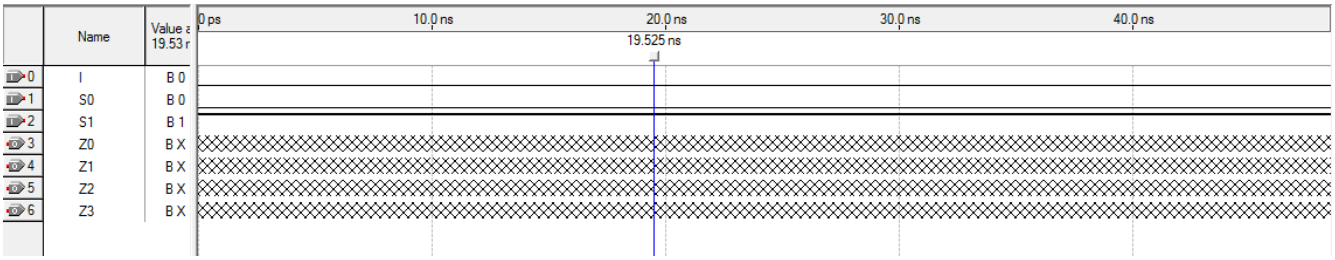

```
module DEMUX1x4(Z0, Z1, Z2, Z3, I, S0, S1);
output Z0, Z1, Z2, Z3;
input I, S0, S1;
and (Z0, I, S0BAR, S1BAR),
      (Z1, I, S0BAR, S1),
      (Z2, I, S0, S1BAR),
      (Z3, I, S0, S1);
not (S0BAR, S0),
     (S1BAR, S1);
endmodule
```

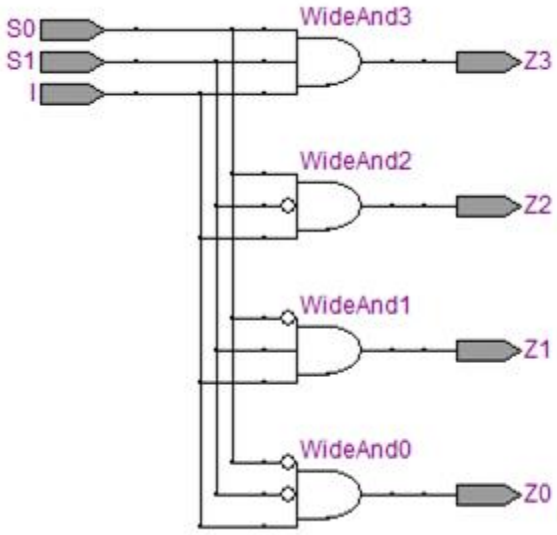
Flow Status	Successful - Mon Sep 16 12:02:00 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DEMUX1x4
Top-level Entity Name	DEMUX1x4
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	4 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	7 / 343 (2 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final


Name
Value a
19.53 r
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
19.525 ns
0 I B 1
1 S0 B 0
2 S1 B 1
3 Z0 B X
4 Z1 B X
5 Z2 B X
6 Z3 B X


Name
Value a
19.53 r
0 ps
50 ps
100 ps
150 ps
200 ps
250 ps
300 ps
350 ps
400 ps
450 ps
500 ps
0 I B 1
1 S0 B 0
2 S1 B 1
3 Z0 B 0
4 Z1 B 1
5 Z2 B 0
6 Z3 B 0


Name
Value a
19.53 r
600 ps
650 ps
700 ps
750 ps
800 ps
850 ps
900 ps
950 ps
1.0 ns
1.05 ns
1.1 ns
0 I B 0
1 S0 B 0
2 S1 B 1
3 Z0 B 0
4 Z1 B 0
5 Z2 B 0
6 Z3 B 0

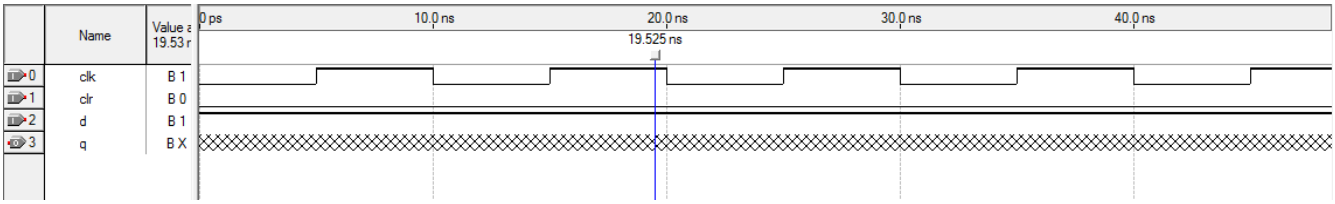

Name
Value a
19.53 r
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
19.525 ns
0 I B 0
1 S0 B 0
2 S1 B 1
3 Z0 B X
4 Z1 B X
5 Z2 B X
6 Z3 B X

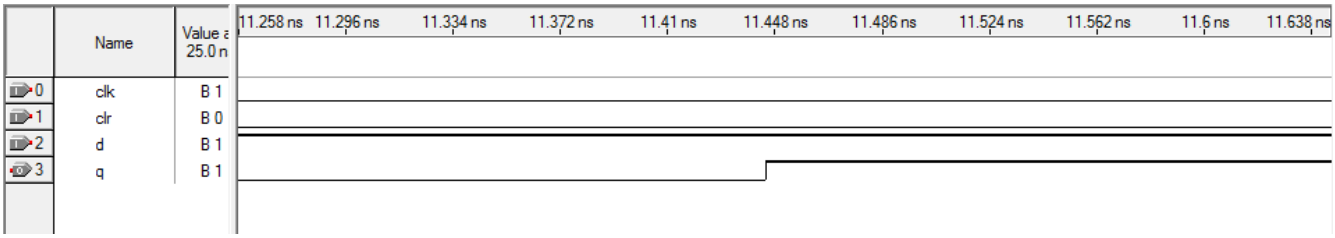

S0
S1
I
WideAnd3
Z3
WideAnd2
Z2
WideAnd1
Z1
WideAnd0
Z0

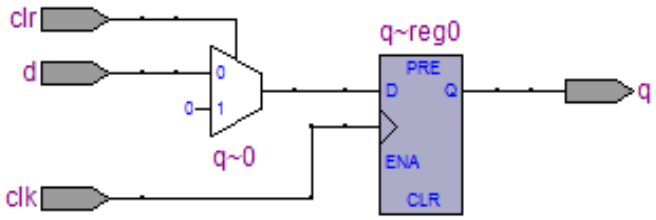
Dflipflop:

```
module Dflipflop (d, clk, clr, q);
input d, clk, clr;
output q;
reg q;
always @(posedge clk)
begin
        if(clr==1)
                q=0;
        else
                q=d;
end
endmodule
```

Flow Status	Successful - Fri Sep 20 08:15:05 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	Dflipflop
Top-level Entity Name	Dflipflop
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	1 / 12,480 (< 1 %)
Total registers	1
Total pins	4 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



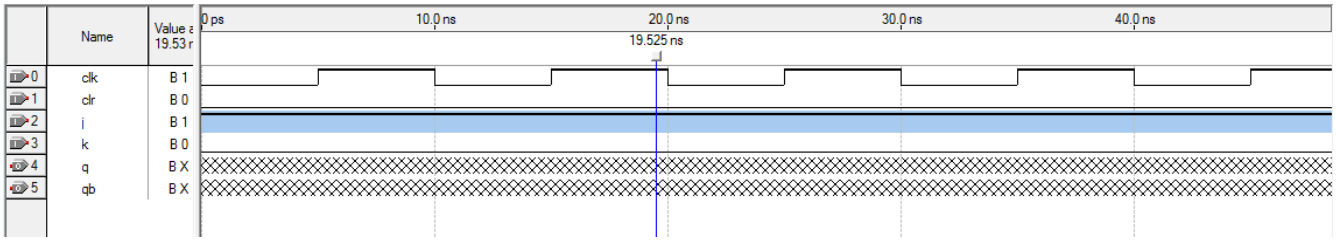


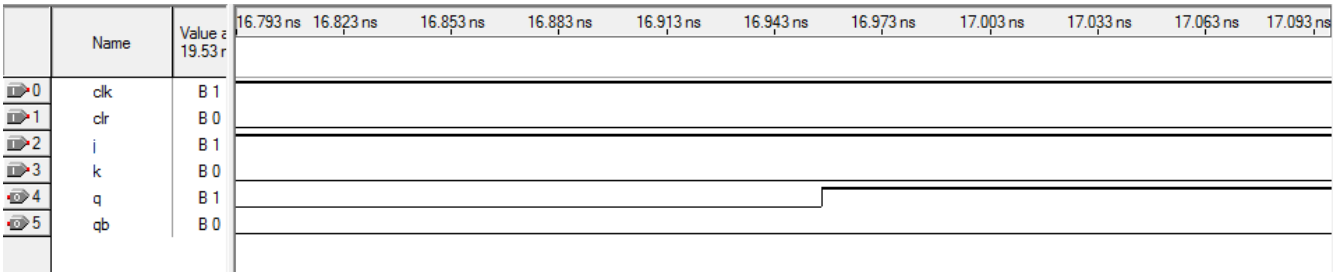


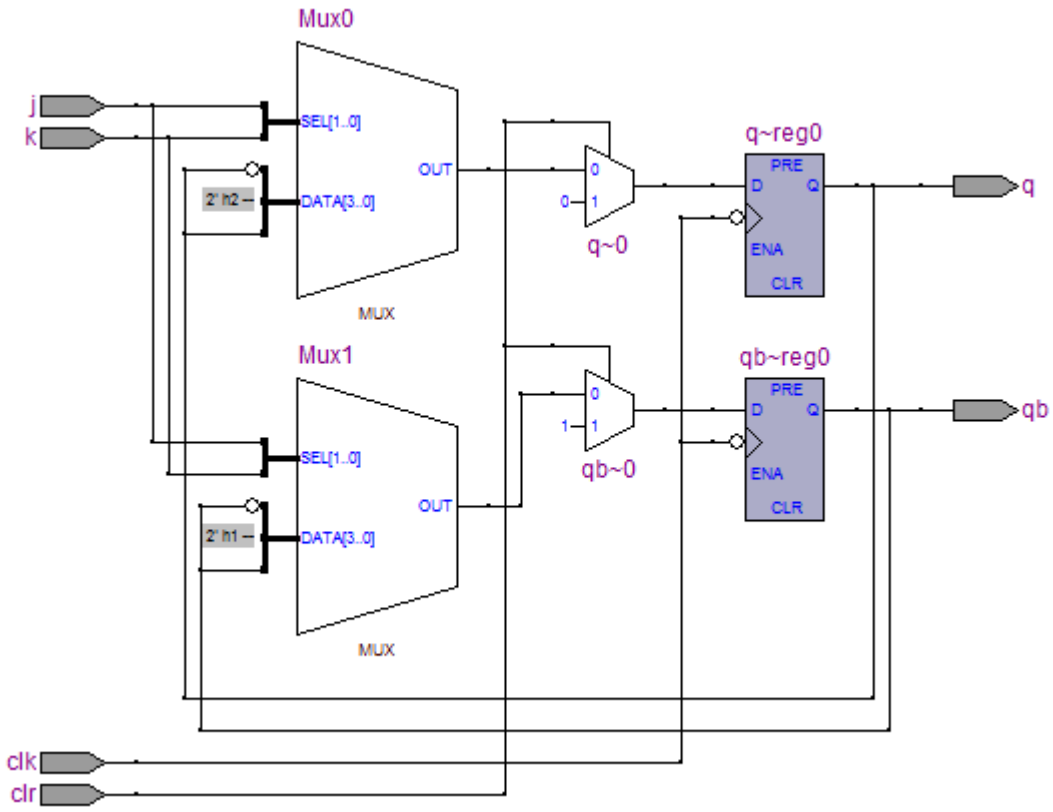
JKflipflop:

```
module JKflipflop (j, k, clk, clr, q, qb);
input j, k, clk, clr;
output q, qb;
reg q, qb;
always@(negedge clk)
begin
        if(clr==1)
                begin
                        q<=0;
                        qb<=1;
                end
        else
                begin
                        case({j, k})
                                2'b00:      begin   q<=q;    qb<=qb;    end
                                2'b01:      begin   q<=0;    qb<=1;     end
                                2'b10:      begin   q<=1;    qb<=0;     end
                                2'b11:      begin   q<=~q;   qb<=~qb;   end
                        endcase
                end
end
endmodule
```

Flow Status	Successful - Fri Sep 20 08:25:46 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	JKflipflop
Top-level Entity Name	JKflipflop
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	2 / 12,480 (< 1 %)
Dedicated logic registers	2 / 12,480 (< 1 %)
Total registers	2
Total pins	6 / 343 (2 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



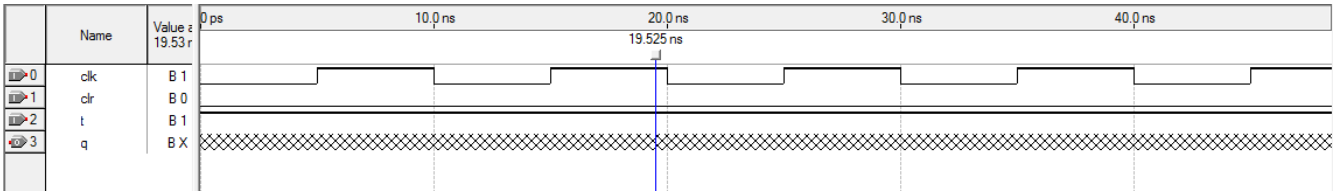


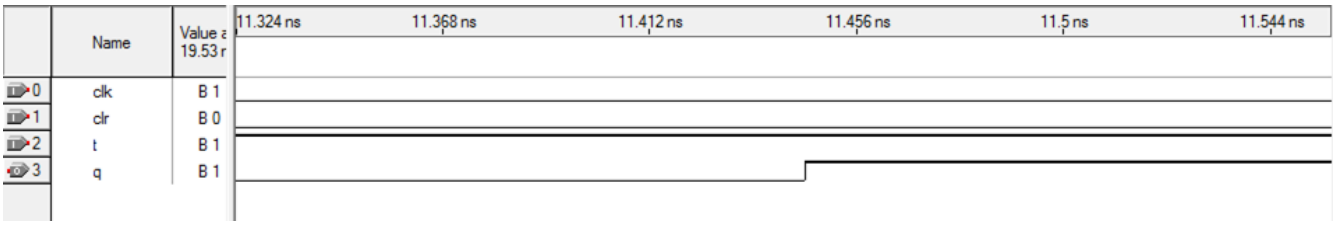


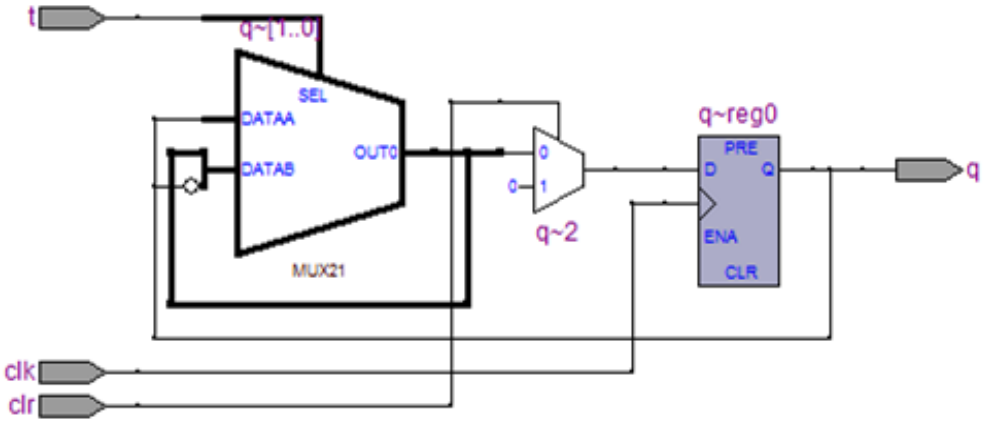
Tflipflop:

```
module Tflipflop (t, clk, clr, q);
input t, clk, clr;
output q;
reg q;
always@(posedge clk)
begin
        if(clr==1)
                q=0;
        else
                begin
                        if(t==0)
                                q=q;
                        else if(t==1)
                                q=~q;

                end
end
endmodule
```

Flow Status	Successful - Fri Sep 20 08:32:24 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	Tflipflop
Top-level Entity Name	Tflipflop
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	1 / 12,480 (< 1 %)
Total registers	1
Total pins	4 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final



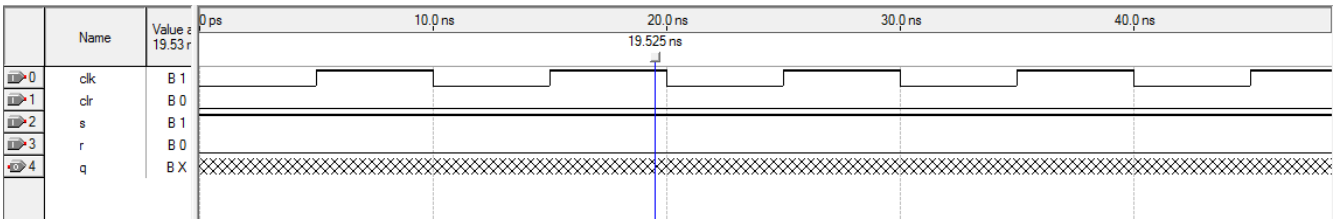


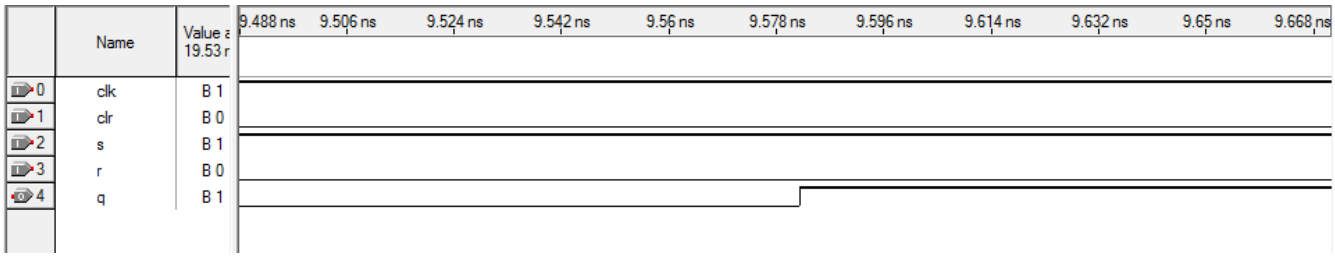


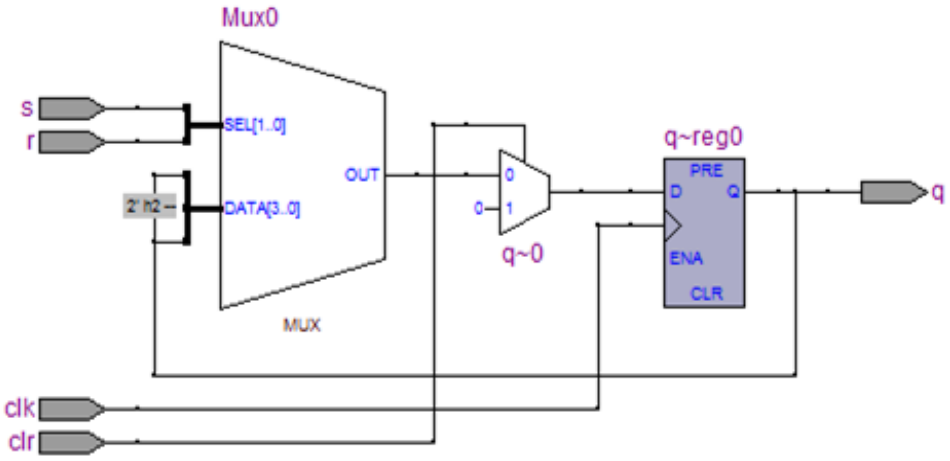
SRflipflop:

```
module SRflipflop (s, r, clk, clr, q);
input s, r, clk, clr;
output q;
reg q;
always@(posedge clk)
begin
        if(clr==1)
                q=0;
        else
                begin
                        case({s, r})
                                2'b00:          q=q;
                                2'b01:          q=0;
                                2'b10:          q=1;
                        endcase
                end
end
endmodule
```

Flow Status	Successful - Fri Sep 20 08:42:13 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	SRflipflop
Top-level Entity Name	SRflipflop
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	1 / 12,480 (< 1 %)
Total registers	1
Total pins	5 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final





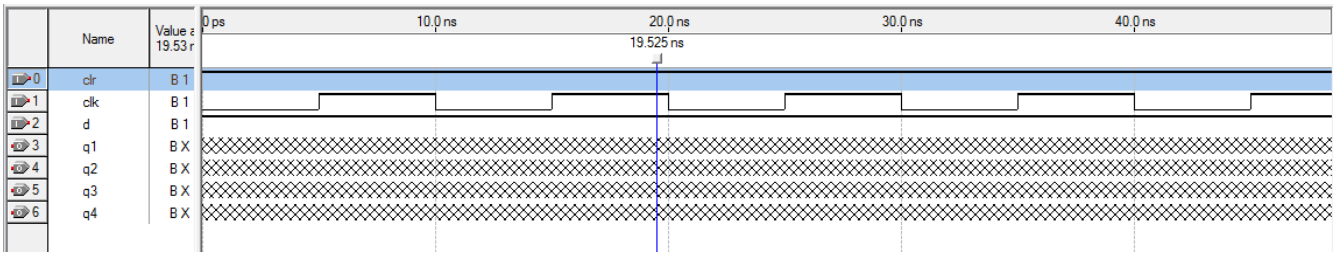


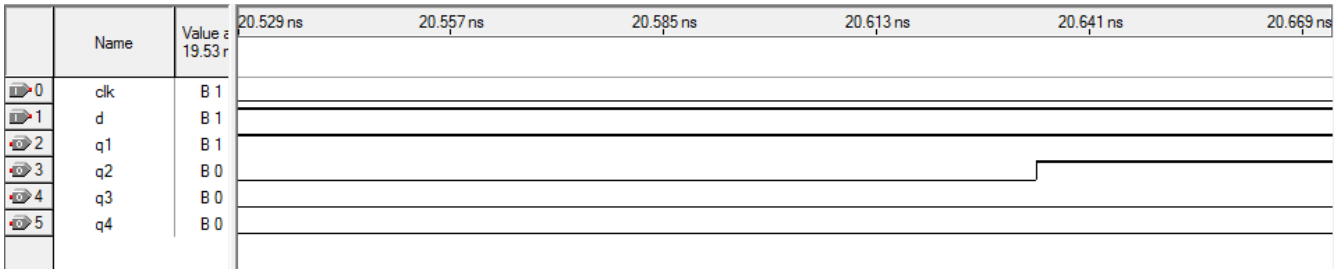
sipo:

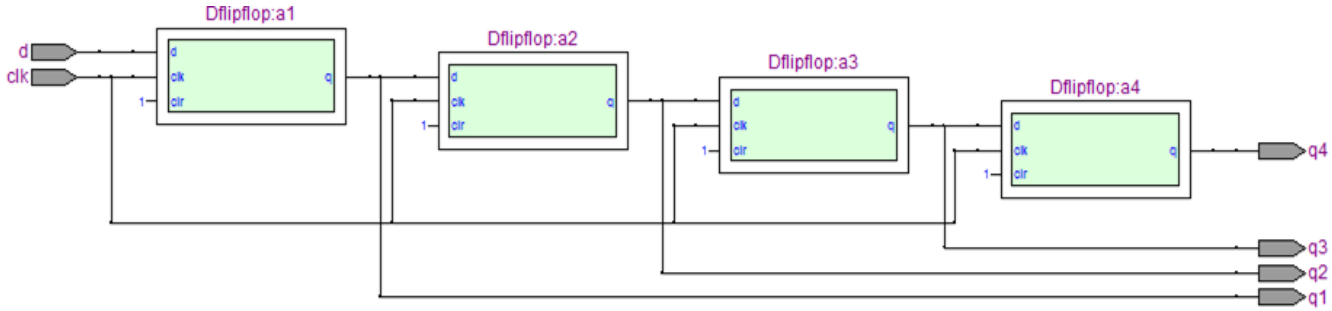
```
module Dflipflop (d, clk, clr, q);
input d, clk, clr;
output q;
reg q;
always @(posedge clk)
begin
        if(clr==1)
                q=0;
        else
                q=d;
end
endmodule
```

```
module sipo(q1, q2, q3, q4, clk, d);
input d, clk;
output q1, q2, q3, q4;
Dflipflop a1(d, clk, clr, q1);
Dflipflop a2(q1, clk, clr, q2);
Dflipflop a3(q2, clk, clr, q3);
Dflipflop a4(q3, clk, clr, q4);
endmodule
```

Flow Status	Successful - Fri Sep 20 09:35:18 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	sipo
Top-level Entity Name	sipo
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	0 / 12,480 (0 %)
Dedicated logic registers	4 / 12,480 (< 1 %)
Total registers	4
Total pins	6 / 343 (2 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

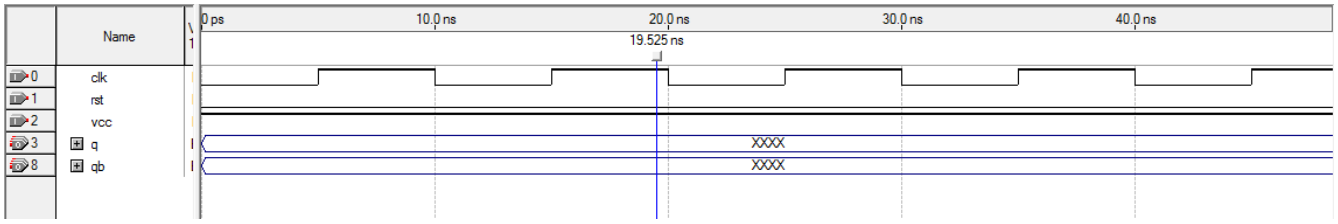


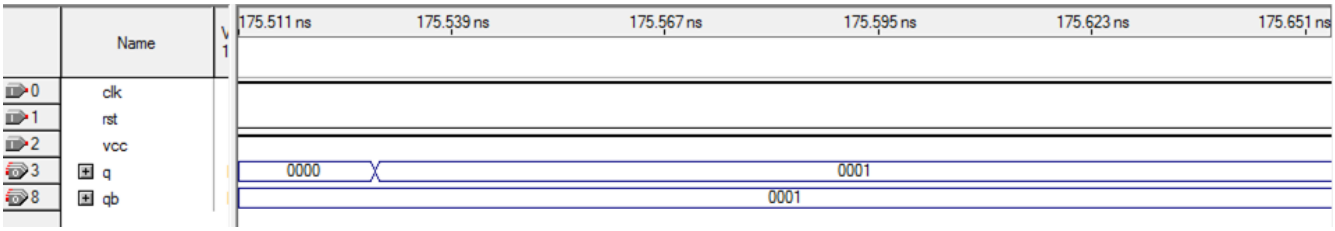


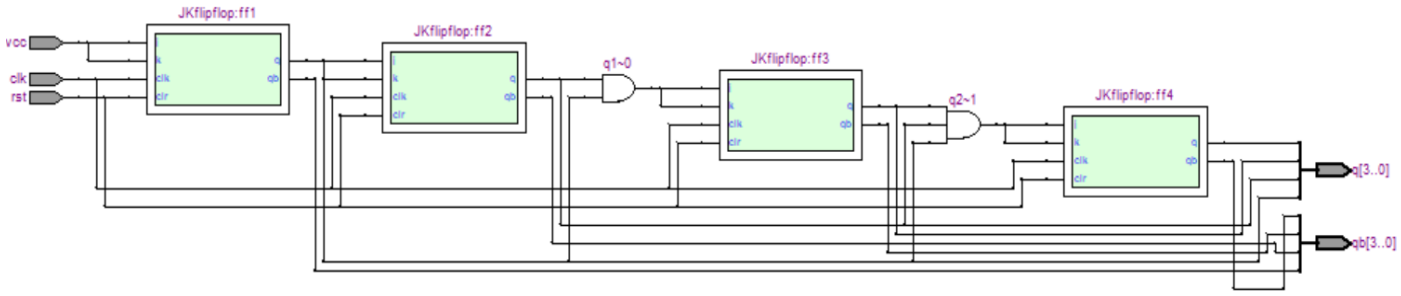



```
module JKflipflop (j, k, clk, clr, q, qb);
input j, k, clk, clr;
output q, qb;
reg q, qb;
always@(negedge clk)
begin
        if(clr==1)
                begin
                        q<=0;
                        qb<=1;
                end
        else
                begin
                        case({j, k})
                                2'b00:      begin   q<=q;    qb<=qb;    end
                                2'b01:      begin   q<=0;    qb<=1;     end
                                2'b10:      begin   q<=1;    qb<=0;     end
                                2'b11:      begin   q<=~q;  qb<=~qb;   end
                        endcase
                end
end
endmodule

module sync_UP(clk, rst, vcc, q, qb);
input clk, rst, vcc;
output [3:0]q, qb;
wire q1, q2;
JKflipflop ff1(vcc, vcc, clk, rst, q[0], qb[0]);
JKflipflop ff2(q[0], q[0], clk, rst, q[1], qb[1]);
assign q1=q[0] & q[1];
JKflipflop ff3(q1, q1, clk, rst, q[2], qb[2]);
assign q2=q[0] & q[1] & q[2];
JKflipflop ff4(q2, q2, clk, rst, q[3], qb[3]);
endmodule
```

Flow Status	Successful - Fri Sep 20 09:14:15 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	sync_UP
Top-level Entity Name	sync_UP
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	11 / 12,480 (< 1 %)
Dedicated logic registers	11 / 12,480 (< 1 %)
Total registers	11
Total pins	11 / 343 (3 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

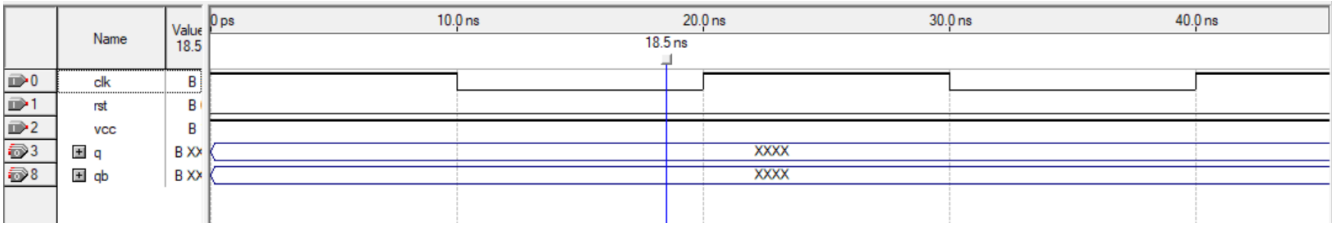


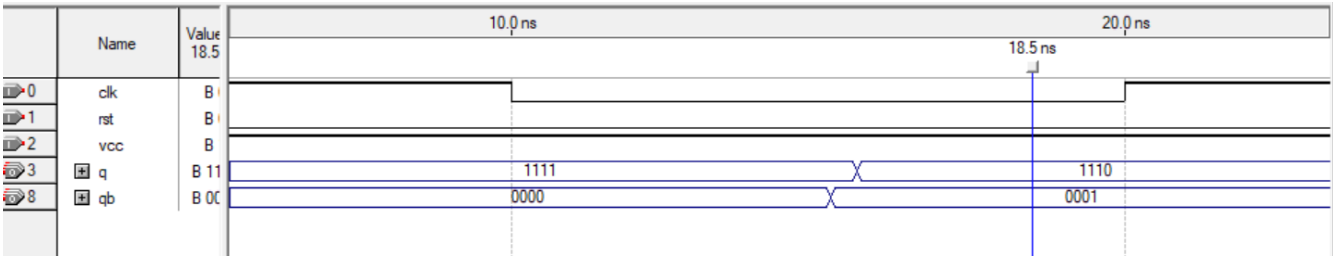


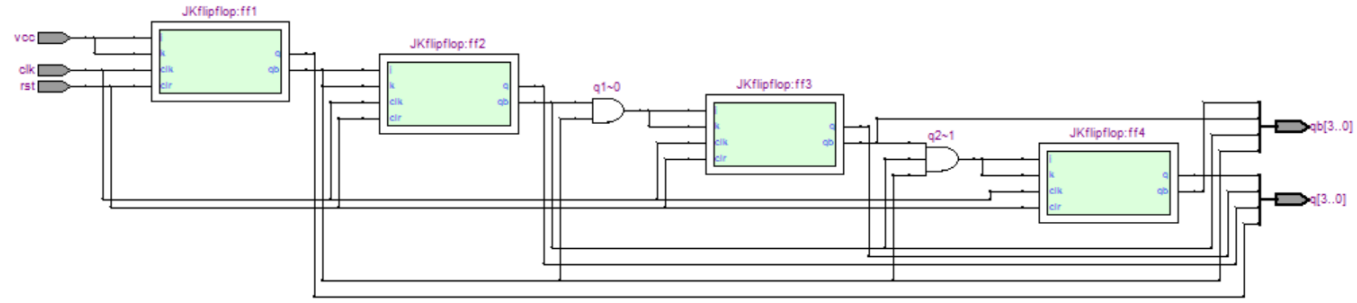


```
module JKflipflop (j, k, clk, clr, q, qb);
input j, k, clk, clr;
output q, qb;
reg q=1, qb=0;

always@(negedge clk)
begin
	if(clr==1)
		begin
			q=0;
			qb=1;
		end
	else
		begin
			case({j, k})
				2'b00:	begin	q=q;	qb=qb;	end
				2'b01:	begin	q=0;		qb=1;	end
				2'b10:	begin	q=1;	qb=0;	end
				2'b11:	begin	q=~q;	qb=~qb;	end
			endcase
		end
end
endmodule

module sync_DOWN(clk, rst, vcc, q, qb);
input clk, rst, vcc;
output [3:0]q, qb;
wire q1, q2;
JKflipflop ff1(vcc, vcc, clk, rst, q[0], qb[0]);
JKflipflop ff2(qb[0], qb[0], clk, rst, q[1], qb[1]);
assign q1=qb[0] & qb[1];
JKflipflop ff3(q1, q1, clk, rst, q[2], qb[2]);
assign q2=qb[0] & qb[1] & qb[2];
JKflipflop ff4(q2, q2, clk, rst, q[3], qb[3]);
endmodule
```

Flow Status	Successful - Sat Sep 21 20:29:37 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	sync_DOWN
Top-level Entity Name	sync_DOWN
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	10 / 12,480 (< 1 %)
Dedicated logic registers	10 / 12,480 (< 1 %)
Total registers	10
Total pins	11 / 343 (3 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final







Flow Status	Successful - Sun Sep 22 12:38:07 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	MUX4x1
Top-level Entity Name	MUX4x1
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	7 / 343 (2 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final