GATE

January 18, 2024

1. A counter is constructed with three D flip-flops. The input-output pairs are named (D_0, Q_0), (D_1, Q_1), and (D_2, Q_2), where the subscript 0 denotes the least significant bit. The output sequence is desired to be the Gray-code sequence $000, 001, 011, 010, 110, 111, 101$, and 100, repeating periodically. Note that the bits are listed in the $Q_2\ Q_1\ Q_0$ format. The combinational logic expression for D_1 is (GATE-EE2021,37)

   (a) $Q_2Q_1Q_0$

   (b) $Q_2Q_0 + Q_1\bar{Q}_0$

   (c) $\bar{Q}_2Q_0 + Q_1\bar{Q}_0$

   (d) $Q_2Q_1 + \bar{Q}_2\bar{Q}_1$