Design and Analysis of a 4-Bit Carry Look-Ahead Adder Using Static CMOS and TSPC Logic

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***Abstract*—This report presents the design and implementation of a 4-bit Carry Look-Ahead (CLA) adder using Static CMOS logic for the adder and True Single Phase Clock (TSPC) logic for the D flip-flops. The design is simulated and analyzed for performance metrics such as setup time, hold time, and delay. The following sections outline the structure, design, simulation, and experimental validation of the system.**

I. Introduction

Addition is one of the fundamental operations in digital systems, with wide applications in arithmetic units, processors, and digital signal processing. Among various adder designs, the Carry Look-Ahead (CLA) adder is preferred for its fast computation, as it minimizes the delay associated with carry propagation.

In this project, a 4-bit CLA adder is designed and implemented using Static CMOS logic for the adder blocks and True Single Phase Clock (TSPC) logic for the D flip-flops. The CLA adder operates by generating carry signals in advance, leveraging the propagate (p_i) and generate (g_i) signals for each bit position. This approach significantly reduces delay compared to ripple-carry adders.

The choice of Static CMOS logic ensures robust operation, low power consumption, and excellent noise margins. Additionally, TSPC logic is selected for the D flip-flops due to its energy efficiency and capability to achieve high-speed operation, making it suitable for modern digital circuits.

This document provides a comprehensive analysis of the design process, starting from circuit topology and simulation to layout generation and FPGA implementation. The goal is to achieve an efficient and reliable adder design while adhering to timing constraints and minimizing layout area. The subsequent sections detail the methodology, results, and performance evaluation.

II. Proposed Structure

The 4-bit Carry Look-Ahead (CLA) adder is designed using a combination of **Static CMOS logic** and **True Single Phase Clock (TSPC) logic** to optimize speed, power consumption, and reliability.

A. Logic Choices

- **TSPC D Flip-Flops**:
  - Each D flip-flop is implemented with **12 transistors** using TSPC logic.
  - This design ensures low power consumption and high-speed operation due to its clocking efficiency.
  - The flip-flops are used to synchronize the input and output of the CLA adder.
- **XOR Gate**:
  - The XOR gate is implemented using **8 transistors**.
  - It is used to calculate the propagate signals ($p_i = a_i \oplus b_i$) in the CLA logic and for generating the sum ($sum_i = p_i \oplus c_i$).
- **AND Gate**:
  - The AND gate is designed with **4 transistors**, consisting of a combination of a **2-transistor inverter** and a basic PMOS-NMOS configuration.
  - It is used to compute the generate signals ($g_i = a_i \cdot b_i$) in the CLA logic.
- **OR Gate**:
  - The OR gate is implemented by combining a **4-transistor NOR gate** and a **2-transistor inverter**.
  - It is used in the carry computation logic for combining carry propagate and generate terms.

B. Adder Design

The CLA adder consists of three main blocks:

1) **Propagate and Generate Block**:
   - Calculates the propagate (p_i) and generate (g_i) signals for each bit position.
   - These signals are the basis for fast carry computation.
2) **Carry Look-Ahead Logic**:
   - Computes the carry signals (c_{i+1}) for each bit position using the pre-computed p_i and g_i signals.
   - The carry logic eliminates ripple propagation by generating all carry signals simultaneously.
3) **Sum Block**:
   - Computes the sum bits ($sum_i = p_i \oplus c_i$) using XOR gates for each bit position.

C. Implementation Style

The adder is designed entirely using **Static CMOS logic**, which provides:

- High noise margins.
- Low static power dissipation.
- Robust operation across varying supply voltages.

The combination of Static CMOS logic for the adder and TSPC logic for flip-flops ensures an optimal tradeoff between speed, power, and area, making the design suitable for high-performance applications.

III. Design Details

A. Topology and Sizing

The circuit diagram used is given in Figures 1.

The size of inverter used is W_n = $1.8\,\mu\mathrm{m}$ W_p = 2W and L = $0.18\,\mu\mathrm{m}$. The length is the same for all blocks.

The width of PMOS and NMOS for D Flip Flop is the same as that of the inverter(2W and W), The width of PMOS is 4W and the width of NMOS is 2W for XOR gate, The width of PMOS is 2W and the width of NMOS is 2W for NAND part of AND GATE (the inverter part has the same length as that of the previously defined inverter) and The width of PMOS is 4W and width of NMOS is W for NOR part of OR GATE (the inverter part has the same length as that of the previously defined inverter).

B. Simulation Results

The NGSpice Simulation results of each block are given in Figure 2.

IV. Flip-Flop Timing Analysis

Setup Time = 130 pico seconds and Hold Time = 150 pico seconds and Clock-to-Q delay = 300 pico seconds

V. Stick Diagrams

Stick Diagrams of all unique gates is given in Figure 3.

VI. Layout and Post-Layout Simulation

post-layout simulation results are given in Figure 4.

VII. Integration and Netlist

simulation results are given in Figure 5.

VIII. Floor Plan

the horizontal pitch = $93.69\,\mu\mathrm{m}$and vertical pitch = $122.22\,\mu\mathrm{m}$

IX. Complete Circuit Layout

The screenshot of layout is given in Figure 6. Post Layout Simulation is given in Figure 7.

X. Performance Analysis

delay of the CLA adder = 180 pico seconds and the maximum clock frequency = 1739.13043 MHz .

XI. HDL Description

waveforms are given in figure 8.

XII. FPGA Implementation

The experimental results, including oscilloscope waveforms given in Figure 9.

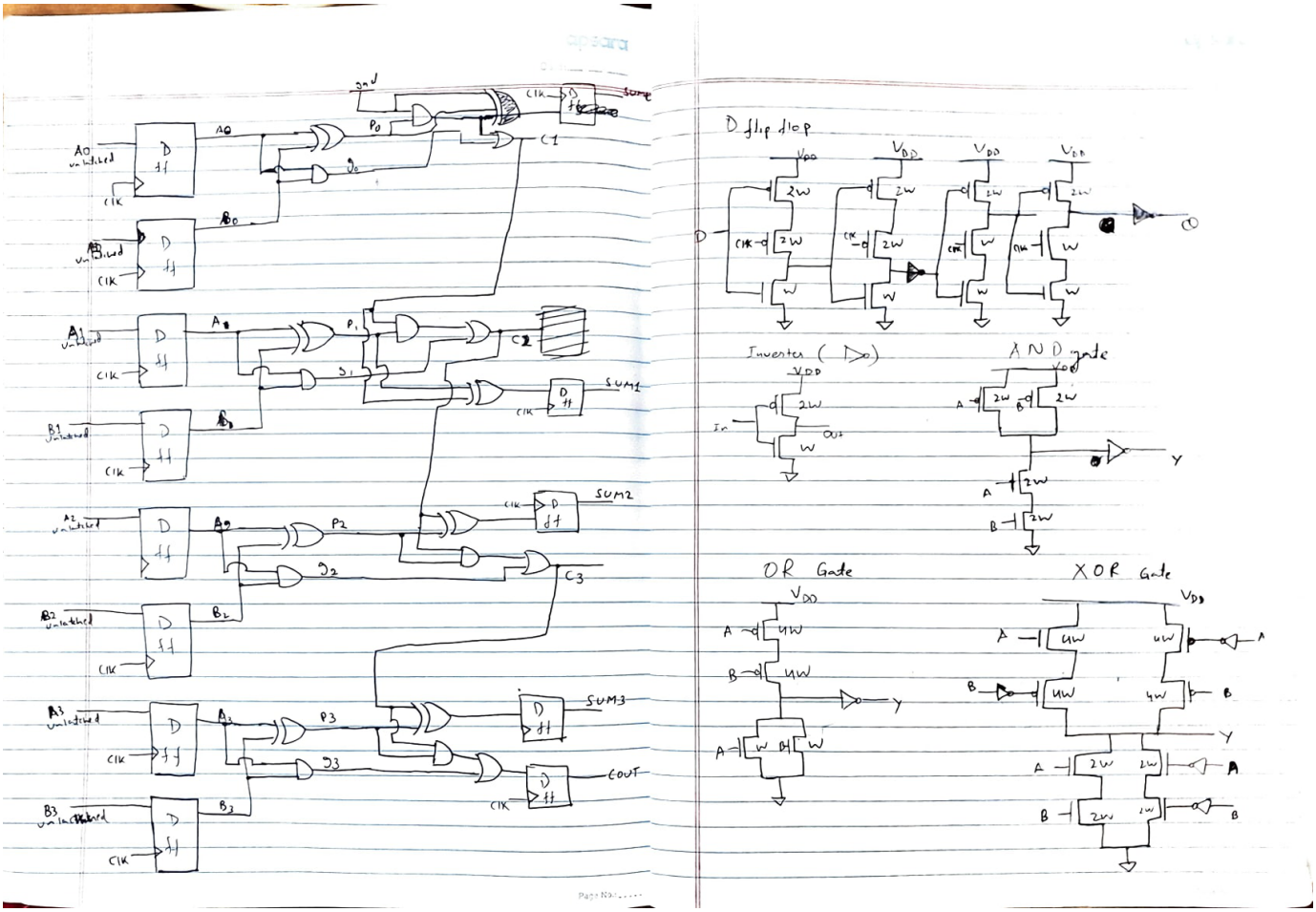


Fig. 1: Circuit Diagrams

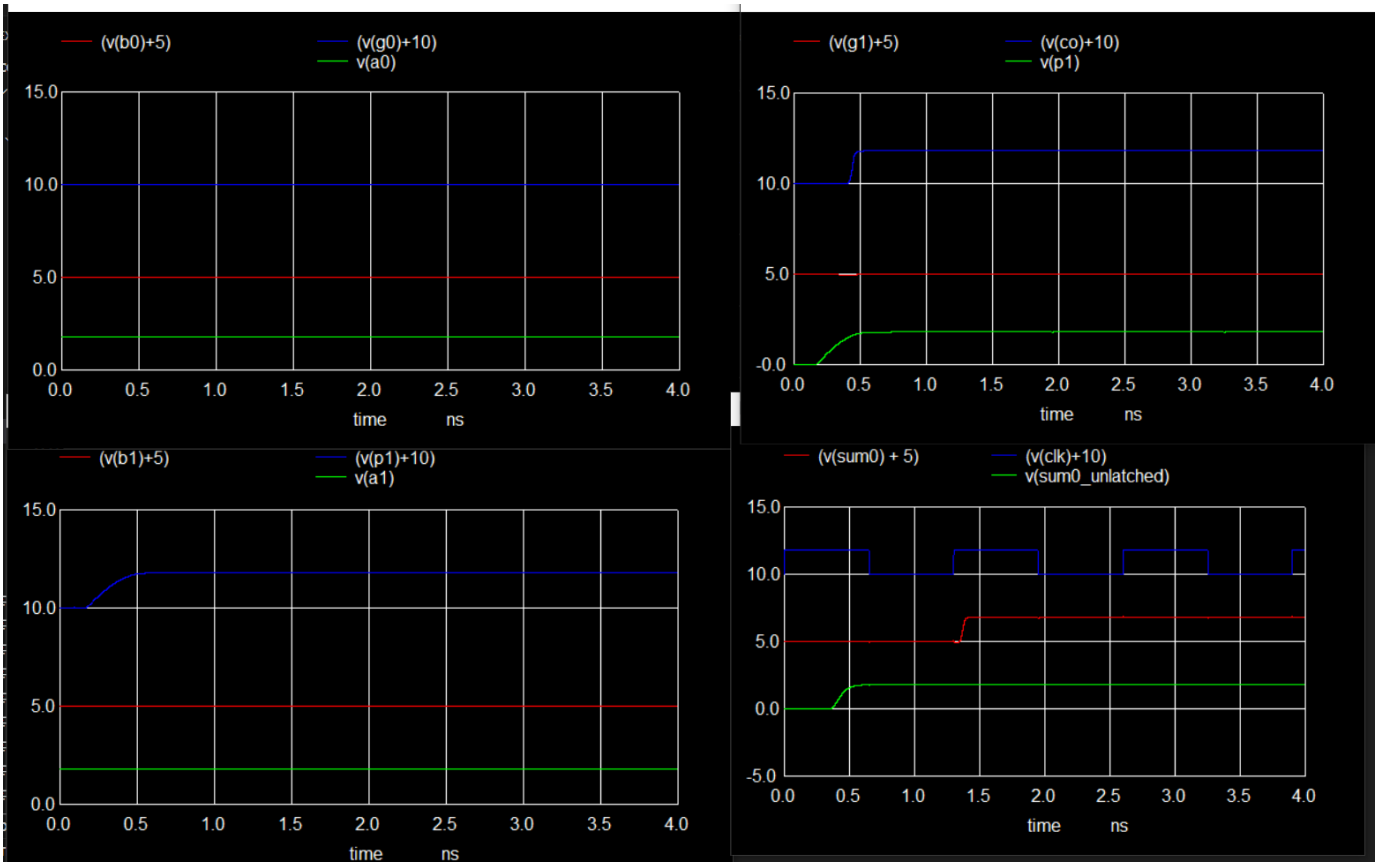
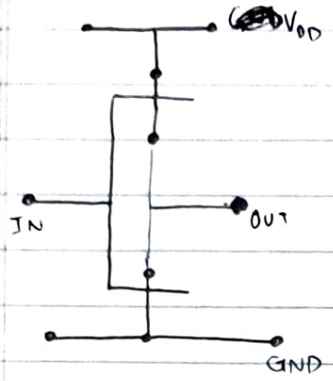
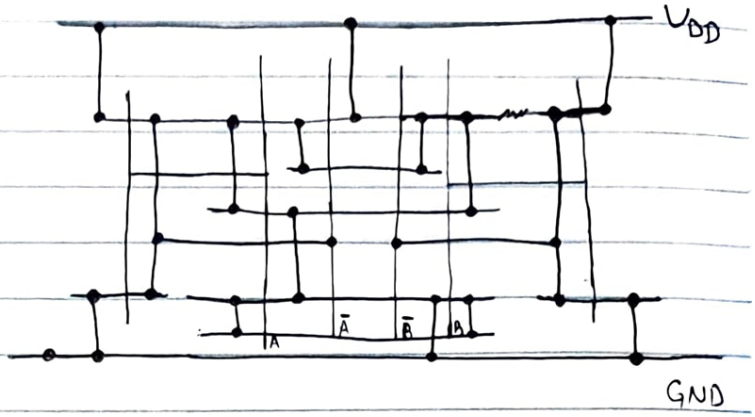


Fig. 2: Pre Layout NGSPICE Plots of Blocks

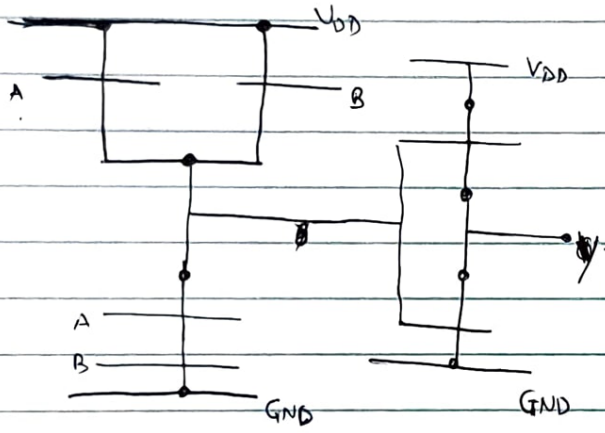
Inverter



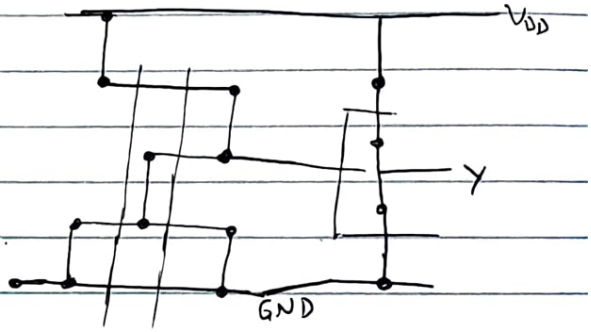
XOR Gate



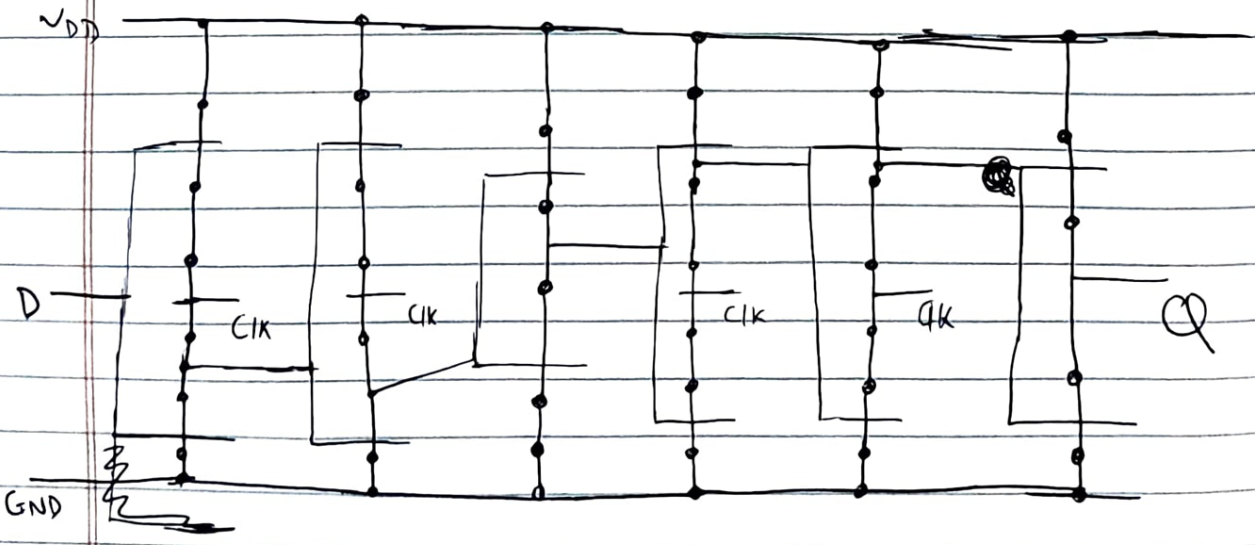
AND Gate



OR GATE



D flip flop



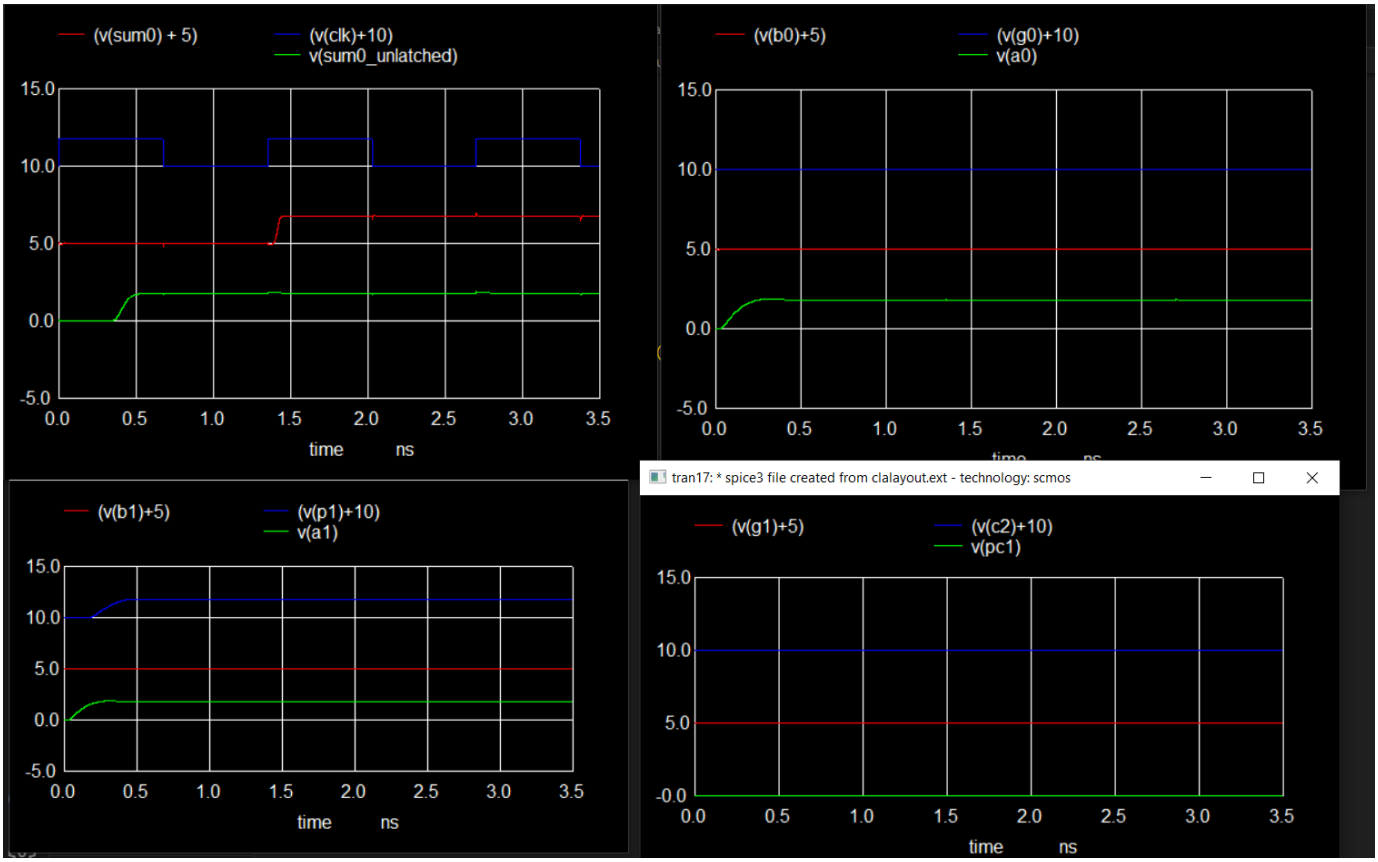


Fig. 4: Post Layout Simulation of Blocks

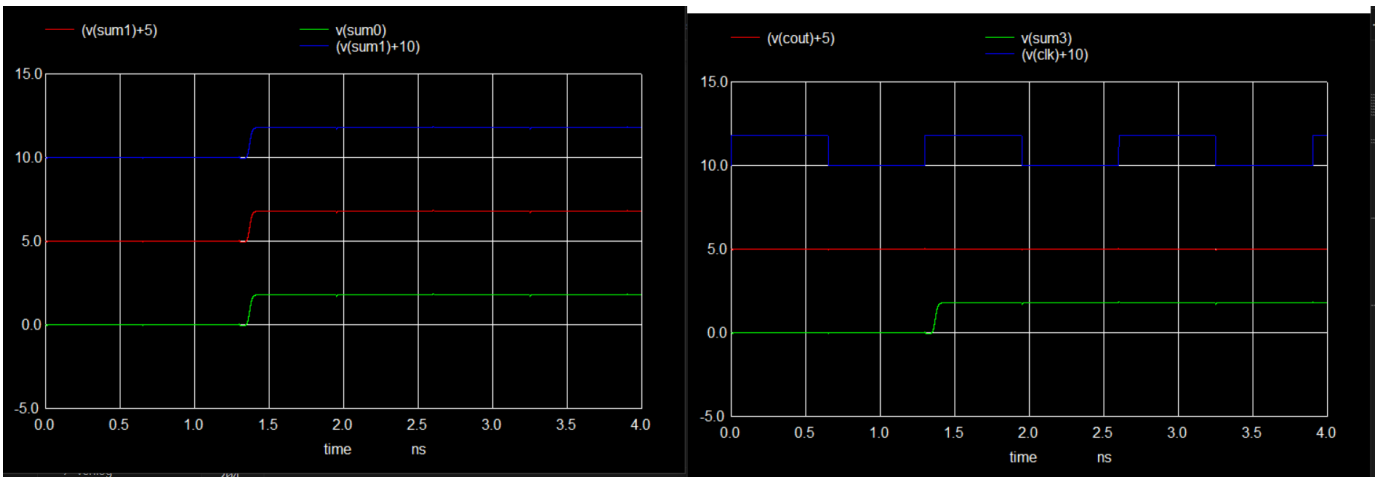


Fig. 5: Pre Layout Simulation Results

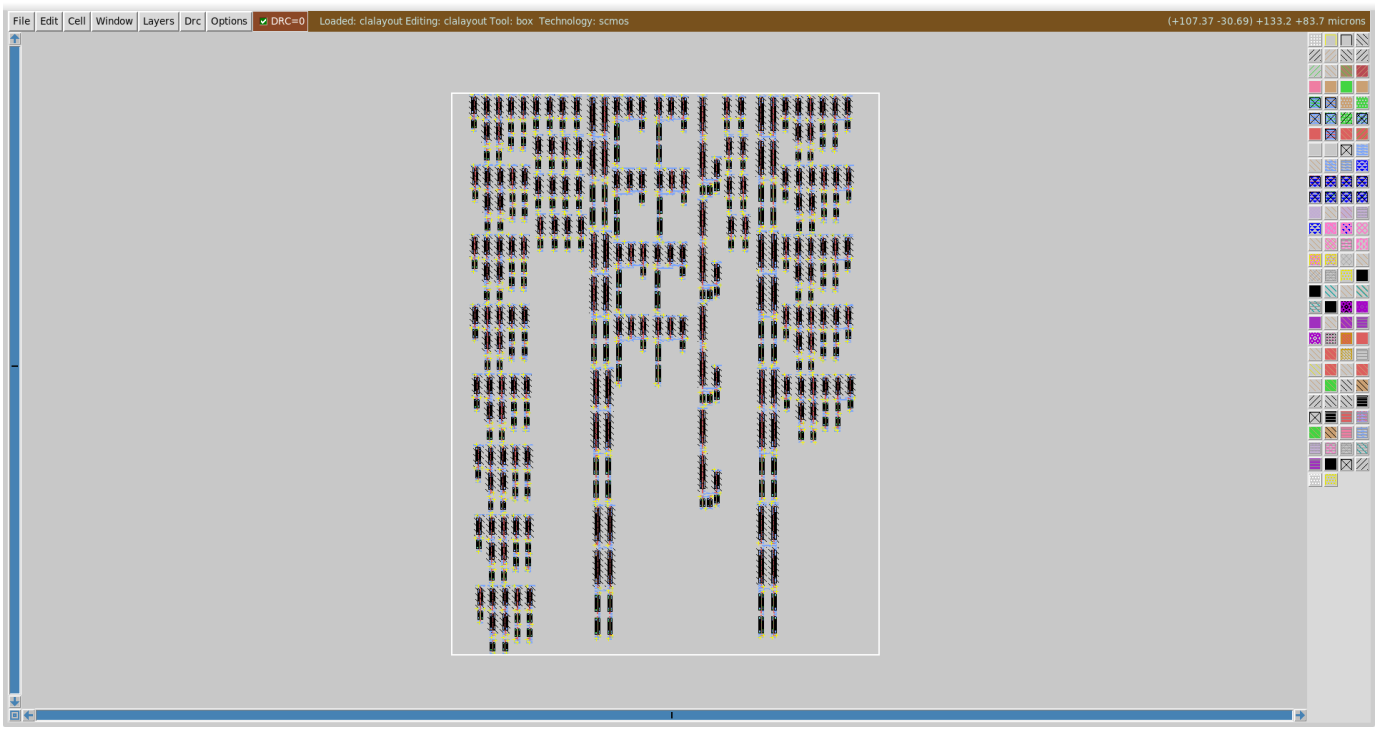


Fig. 6: Complete Layout

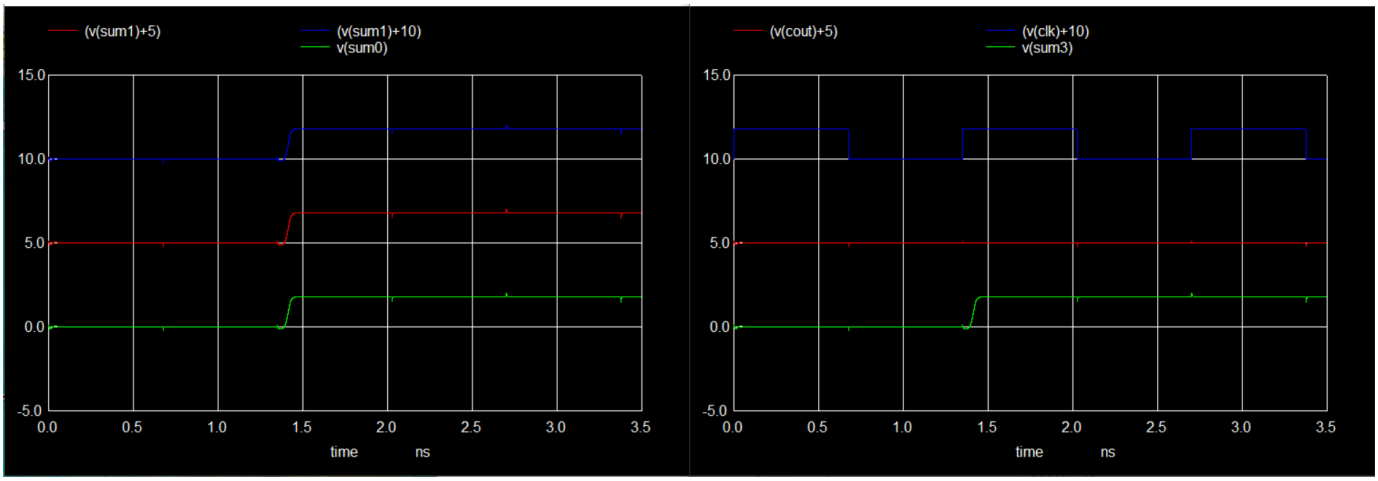


Fig. 7: Post Layout Simulation Results

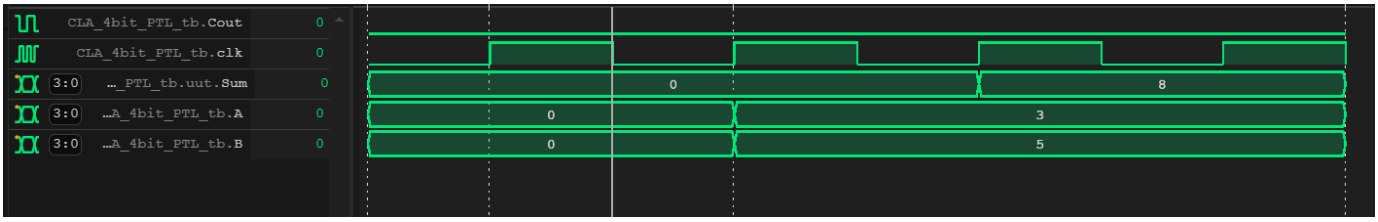


Fig. 8: Verilog Waveforms Results

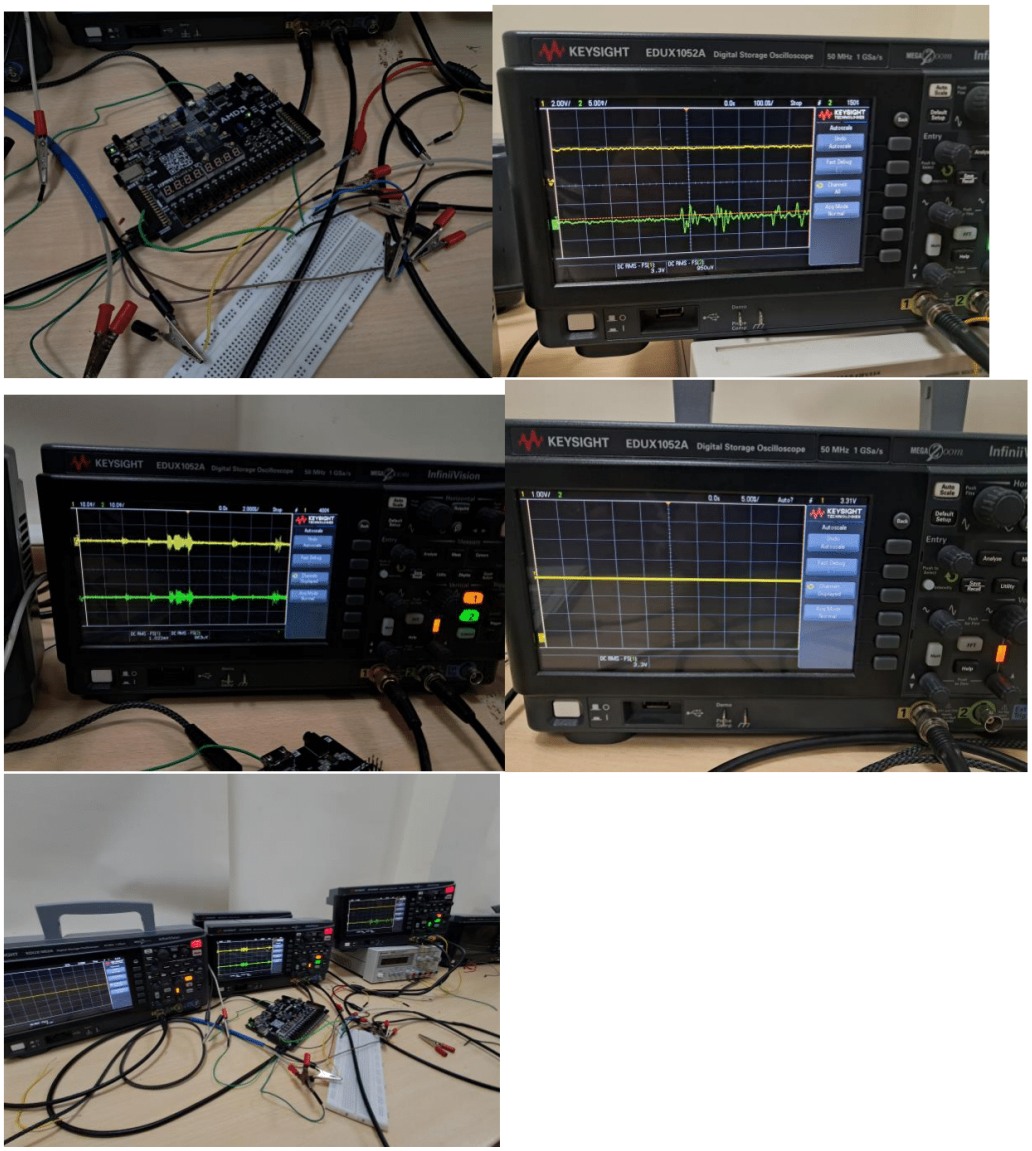


Fig. 9: FPGA Results