14IS32

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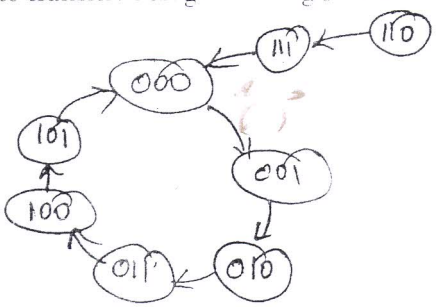
Third Semester B.E. Degree Examination, December 2015
Information Science and Engineering
Principles of analog and Digital Design (14IS32)

Time:3Hrs

Max. Marks: 100

Instructions: 1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.

				Course Outcome, Blooms Level
		UNIT-I		
1.	a.	Draw the transconductance curve and drain curves for E-MOSFET. How inversion layer in E-MOSFET helps in conduction? Explain	10 Marks	CO2,L2
	b.	Given Vgs(off)=-2V. I_{dss}=6mA. Find the values of Ids for the following values of Vgs of D-MOSFET a) Vgs= - 4V b) Vgs= - 6V c) Vgs= +3V	06 Marks	CO1, CO2,L3
	c.	What is active load switching? Explain	04 Marks	CO1, L1
2.	a.	With necessary circuit diagram. drain curves and trans conductance curves brief the operation of D-MOSFET	10 Marks	CO2, L3
	b.	What is passive load switching? Explain with necessary diagram.	05 Marks	CO1, L2
	c.	Write a short note on CMOS and its applications.	05 Marks	CO1,L1
		UNIT-II		
3.	a.	What is universal gate? Implement the basic gates using universal gates.	05 Marks	CO1,L3
	b.	Minimize the expressions, using K-map $Y=A\bar{B}C+\bar{A}\bar{B}C+\bar{A}BC+A\bar{B}\bar{C}+\bar{A}\bar{B}\bar{C}$ $Y=\bar{A}BC\bar{D}+\bar{A}BC\bar{D}+ABC\bar{D}+ABC\bar{D}+A\bar{B}C\bar{D}+\bar{A}\bar{B}C\bar{D}$	08 Marks	CO2,L5
	c.	Explain parity generator and checker in detail	07 Marks	CO2,L4
4.	a.	Simplify the expression using boolean laws and theory i. $X=(\bar{A}+B)(A+B+C)\bar{D}$ ii. $Z=(\bar{A}+B)(A+\bar{B})$	05 Marks	CO1,CO2,L5
	b.	Using graphical procedure, obtain a NOR-gate realization of the boolean expression. $f(a,b,c,d)=\bar{a}d+a\bar{d}(b+\bar{c})$	05 Marks	CO2,L5
	c.	What is K-map? Explain in detail how to simplify the expression using K-map by grouping the minterms. Also simplify $f(x,y,z)=\sum m(0,1,4)+\sum dc(3,7)$	10 Marks	CO1,L5
		UNIT-III		
5.	a.	List and Explain the different types of Flip-Flops with truth table and excitation table.	09 Marks	CO3, L1
	b.	Explain the working of NAND gate latch circuit.	06 Marks	CO3,L1
	c.	Discuss the effect of propagation delay in a Flip-Flop circuit.	05 Marks	CO3,L2
6.	a.	Explain any two application of Flip-Flops in detail.	10 Marks	CO3, L2
	b.	Briefly discuss the working of JK master-Slave Flip Flop.	05 Marks	CO3, L2
	c.	What is switch contact Bounce problem? How it is overcome by S-R Flip-Flop? Explain.	05 Marks	CO3,L3
		UNIT-IV		
7.	a.	Differentiate between synchronous counters and Asynchronous counter.	05 Marks	CO3,L3

	b.	Explain four bit ripple counter along with the circuit diagram and waveform	10 Marks	CO3,L4
	c.	What is presentable counters? Explain	05 Marks	CO3,L1
8.	a.	Explain the advantages of synchronous counter over Asynchronous counter.	05 Marks	CO3,L4
	b.	Design the following state transition diagram using JKFF  Show the design and circuit diagram	10 Marks	CO3, L5
	c.	Explain 3-bit binary Asynchronous up-down counter, along with the waveforms	05 Marks	CO3,L3

UNIT-V

9.	a.	Find out voltages caused by the following a) Each bit in a5 bit ladder b) Output voltage for digital input 10111 Assume 0=0V and 1 = +10V	10 Marks	CO4,L4
	b.	Illustrate the working of R-ZR ladder for the digital input 0010	05 Marks	CO2, L2
	c.	Discuss the process of successive approximation.	05 Marks	CO4,L2
10.	a.	Differentiate between Resistive divider method and R-ZR method.	06 Marks	CO4,L4
	b.	Write a neat diagram explain the conversion of analog to digital using counter method.	10 Marks	CO4,L2
	c.	Throw light on the different testing methods involved in a simple DAC machine.	04 Marks	CO4,L3