14IS32 USN

Third Semester B.E Degree Examination, Dec 2016/Jan 2017
Information Science and Engineering
Principles of Analog and Digital Design (14IS32)

Time:3Hrs Max. Marks:100

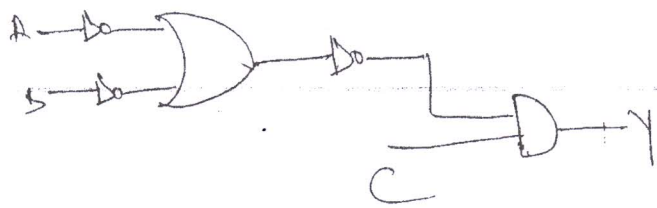
Instructions: 1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.

UNIT-I

				CO; BL
1.	a.	Explain series clipper and parallel clipper with bias in detail.	06 Marks	1;2
	b.	With short notes on following i. Active load switching. ii. Passive load switching	06 Marks	1;2
	c.	What is an ideal positive clamber? Differentiate positive clamper and negative clamper with necessary circuits and waveforms along with its working.	08 Marks	1;4
2.	a.	Describe the enhancement type MOSFET with circuit diagram and necessary graphs.	10 Marks	1;2
	b.	Explain CMOS Inverter in detail and show how power consumption is reduced with CMOS devices.	10 Marks	1;3

UNIT-II

3.	a.	Simplify the Boolean expression $Y=\bar{A}B+AB\bar{C}+\bar{A}C+\bar{A}B\bar{C}+ABC$ Using Boolean algebra	04 Marks	2;3
	b.	Use K-map and simplify the expressions i) $Y(A,B,C,D)=\varepsilon m(0,1,4,7,13,15)+ d(2,5,8)$ ii) $Y(A,B,C)= \varepsilon m(2,5,7) +d(0,1)$ iii) $Y(A,B,C,D)=\varepsilon m(2,5,8) +d(0,1,4,7,13,15)$	12 Marks	2;3
	c.	How NOT, OR, AND Gates can also Obtained using only NOR Gates? Explain.	04 Marks	2;4
4.	a.	Using Q-M method simplify $Y(A,B,C,D)= \varepsilon m(4,8,9,10,11,12,14,15)$	10 Marks	2;3
	b.	Use Demorgan's theorem to convert $Y=\overline{\overline{A+\overline{B+\overline{CD}}}}$ to an expression containing only single variable inversions.	05 Marks	2;3
	c.	Convert the following circuit to one using only NAND gates.	05 Marks	2;3



UNIT-III

5.	a.	With a neat block diagram. explain the working of a Master-Slave JK Flip-Flop. Also write its truth table.	10 Marks	3;2
	b.	Write the characteristics of clock	04 Marks	3;2
	c.	Show how a SR Flip-Flop can be converted to JK Flip-Flop	06 Marks	3;2
6.	a.	Explain the different types of Flip-Flops along with truth table and excitation tables	10 marks	3;2
	b.	Explain a 4 bit shift Register in detail and give its timing diagrams	10 Marks	3;2

UNIT-IV

7.	a.	Explain a 4-bit ripple counter with necessary circuit diagram and waveforms	06 Marks	3;2
	b.	Show how to wire the IC 74LS293 as decade counter	06 Marks	3;2
	c.	Analyze the working of Synchronous mod-16 counter.	08 Marks	3;2

8. a. Design a Synchronous counter that has the following Sequence:- 000,010,101,110 and repeat. The Undesired states 001,011,100 and 111 must always go to 000 on the next clock pulse. **10 Marks** 3;3

   b. Write short notes on **10 Marks** 3;2
   i) Cascading BCD counter
   ii) Frequency division and counting.

UNIT-V

9. a. Calculate the output-voltage of a 6-bit binary ladders for the following input using 0=0 volt and 1=10volt. **06 Marks** 4;3
   i) 100100
   ii) 110011
   iii) 000111

   b. Give the working details of ADC using Counters method. **06 Marks** 4;3

   c. Write short notes on the following. **08 Marks** 4;2
   i) Resolution
   ii) Accuracy
   iii) Monotonocity
   iv) Register Networks

10. a. With the help of a neat block diagram explain the working of successive Approximation ADC. **10 Marks** 4;2

    b. In a 8 bit counter type ADC driven by 1000KHZ. Find **06 Marks** 4;3
    i) Conversion time
    ii) Average Conversion time
    iii) Maximum conversion time

    c. Write a short note on 2-bit Simultaneous A/D converter. **04 Marks** 4;2