Date: October 28, 2011 9:49 AM
Topic: cis501 hw3: paper review

Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers by Norm Jouppi

Q1: Briefly describe the experiment and/or analysis Jouppi might have performed to generate the data for the graph in figure 2-2.

And: The author first ran the benchmark in their baseline system with the miss rate in Table 2-2, and the result is the solid line. And then, the author removes the L1 I-cahce misses, i.e. making every instruction hit in the L1 I-cache, therefore the bottom dotted line is there. Afterwards, the author removes the L1 D-cache misses, i.e. making every data access hit in the L1 D-cache, and this produces the top dotted line. Finally, the author concludes that if L2 cache misses are removed, there will be no performance loss in all the benchmarks.

Q2: Using what you've learned in class and from the textbook readings, briefly discuss a few interesting similarities and/or differences in the memory hierarchy described by Jouppi and a typical memory hierarchy for today's processors.

And: Similarities: 1) The L1 cache is separated into I-cache and D-cache. Differences 1) In Jouppi's paper, L2 cache was off-chip, which is on chip right now. 2) L1 cache was all direct-mapped in Jouppi's paper, but now L1 cache is mostly set-associative cache.

Q3: Assume that you must choose between adding either a victim cache or a multi-stream buffer to a modern microprocessor. Discuss which one you would choose and why.

And: I will choose multi-stream buffer. Because modern microprocessors have L1 cache set associative which reduce the improvement brought by victim cache, but introduce more vector-like operations, which need more data to be brought in at one time of data fetch. Therefore, I think multi-stream buffer will benefit the vector-like operations, and this benefit will be more than the one brought by victim cache to L1 cache misses.