CIS501 Homework 4

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Question 1

a The number of bits in the block offset is 6.

b The number of "sets" in the cache is 256

c The total number of block frames in the cache is $256 \times 2 = 512$.

d The number of index bits is 8.

e The number of tag bits is $32 - 6 - 8 = 18$.

Question 2

a The number of bits in the block offset is $\log_2 B$.

b The number of "sets" in the cache is $\frac{S}{B \times A}$.

c The total number of block frames in the cache is $\frac{S}{B}$.

d The number of index bits is $\log_2 \frac{S}{B \times A}$.

e The number of tag bits is $32 - \log_2 B - \log_2 \frac{S}{B \times A}$.

Question 3

a tag = (address>>(num_index_bits+num_offset_bits))&((1<<num_tag_bits)−1).

b index = (address>>(num_offset_bits))&((1<<num_index_bits)−1).

Question 4

a When the cache size is 2^{13} = 8K bytes, the miss rate is less than 10%. When the cache size is 2^{15} = 32K bytes, the miss rate is less than 5%.

b The ratio is $\frac{0.2343}{0.1533} = 1.528$.

Question 5

a When the cache size is 2^{12} = 4K bytes, the miss rate is less than 10%. When the cache size is 2^{13} = 8K bytes, the miss rate is less than 5%.

b The direct-mapped cache must be at most 32KB before it equals or exceeds the performance of the 16KB two-way set-associative cache.

c Because direct-mapped cache has more conflict misses than set-associative cache, the gap is mainly caused by conflict misses, and the increasing cache sizes can reduce the conflict misses, therefore the gap narrows as the cache size increases.

Question 6

a When cache size is 2^{13} = 8K bytes, two write policies generate approximately the same amount of traffic.

b Because at large cache sizes cache misses are reduced, and write-back of dirty blocks is also reduced, but write-through traffic does not change, therefore write-back traffic is less than write-through.

c Because at small cache sizes write-back of dirty block is a lot due to the high cache misses rate, therefore write-back traffic is more than write-through.

Question 7

a 64-byte block has the lowest miss rate.

b 8-byte block has the lowest traffic.

c

- As block size increases, each write-back has to write more bytes back to lower-level memory.
- As block size increases, the set number decreases, therefore more conflict misses cause more write-back.

d Today's caches are designed to minimize miss rate, because reducing the miss rate can also reduce the traffic, and there is enough bandwidth for current cache traffic.

Question 8

a The accuracy of a single-entry way predictor is 65.83%. It was more accurate than I anticipated. Because 1) the way is either 0 or 1, thus the accuracy should be around 50%, 2) all cache way information is squeezed into one predictor, then the predictor actually does not learn and record information about any access, therefore the predictor works no better than simply always predicting way 0 or way 1.

b When the predictor size is 2^{10} = 1K bytes, the two-way set associative cache is certainly better than a direct-mapped cache.

c There are $32 \times 1024 \div 64 = 512$block frames. The number of tag bits is $64 - 6 - 8 = 50$. The overhead is $2^{10} \times 1 + 512 \times 50 = 26624$bits = 3328bytes, and it is $3328 \div 32K = 10.16\%$ (including predictors and tags).

Appendix: Data

Question 4:

Direct-mapped cache

Cache size (bit)	Miss rate (%)	Misses
8	48.06	1299371
9	38.54	1042167
10	29.34	793218
11	19.60	529838
12	10.86	293507
13	7.78	210431
14	5.56	150254
15	2.34	63350
16	1.53	41449
17	0.91	24635
18	0.74	20091
19	0.19	5011
20	0.13	3541
21	0.12	3165
22	0.12	3143

Question 5:

Two-way set associative cache

Cache size (bit)	Miss rate (%)
8	44.59
9	33.36
10	23.64
11	13.89
12	7.22
13	3.49
14	1.95
15	1.26
16	0.49
17	0.23
18	0.13
19	0.12
20	0.12
21	0.12
22	0.12

Question 6:

Traffic

Cache size (bit)	Write-thr (bytes/op)	Write-bck (bytes/op)
8	29.56	37.77
9	22.37	28.81
10	16.15	20.64
11	9.91	11.94
12	5.65	6.18
13	3.25	3.00
14	2.27	1.76
15	1.83	1.17
16	1.34	0.46
17	1.17	0.20
18	1.11	0.10
19	1.10	0.08
20	1.10	0.08
21	1.10	0.07
22	1.10	0.07

Question 7:

Block size varies

Block size (bit)	Miss rate (%)	Traffic (bytes/op)
3	1.94	0.26
4	1.50	0.39
5	1.27	0.62
6	1.26	1.17
7	1.47	2.61
8	1.81	6.21
9	2.52	17.19

Question 8:

Way Prediction

Predictor size (bit)	Mis-prediction rate (%)	Mis-pred+cache misses
0	34.16	946051
1	27.34	764040
2	22.00	621390
3	18.27	521758
4	14.28	415296
5	9.72	293532
6	6.13	197754
7	4.86	163861
8	4.36	150254
9	1.33	69401
10	0.89	57783
11	0.50	47268
12	0.43	45514
13	0.03	34861
14	0.0032	34060
15	0.0005	33988
16	0.0002	33980