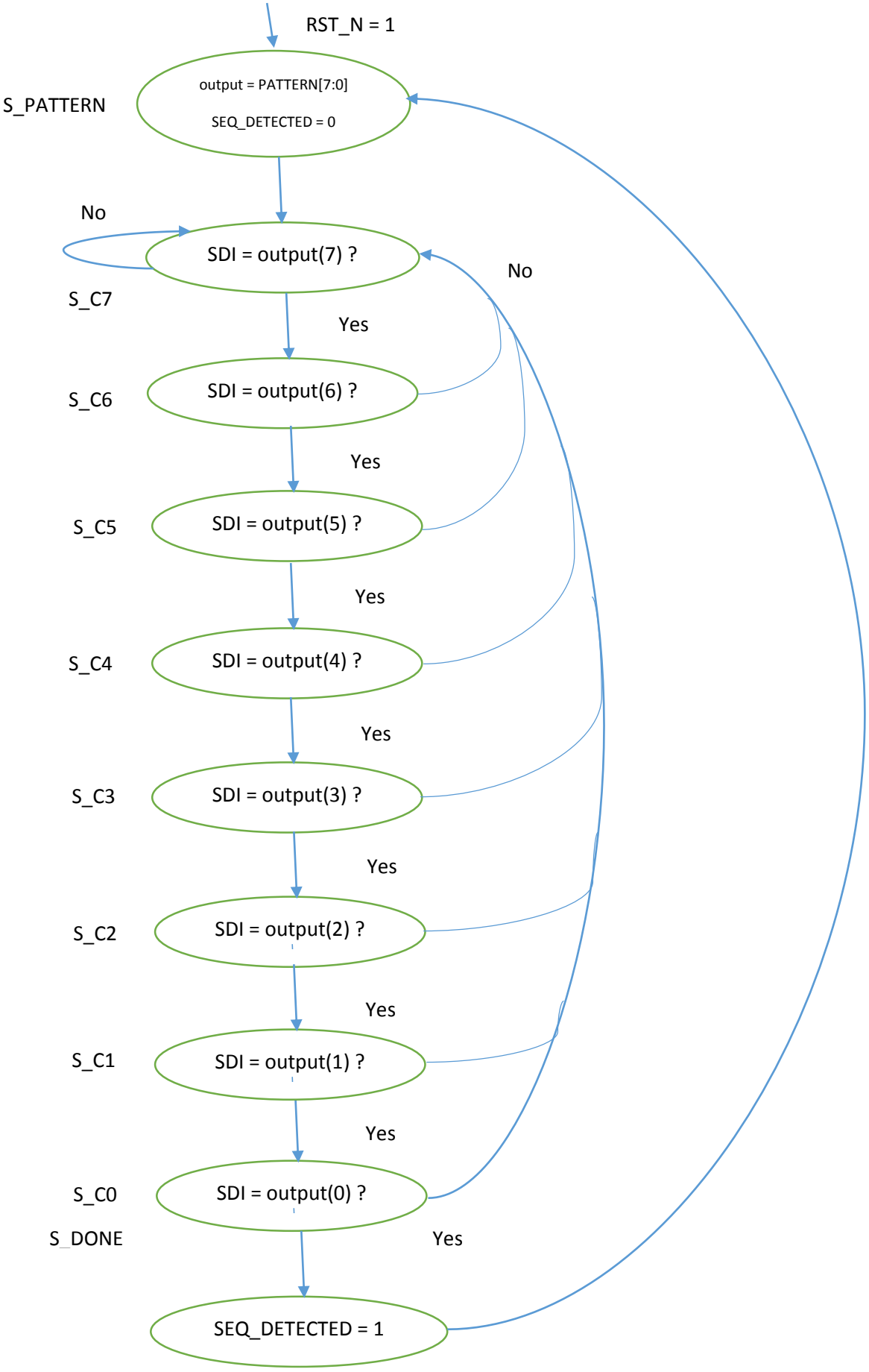
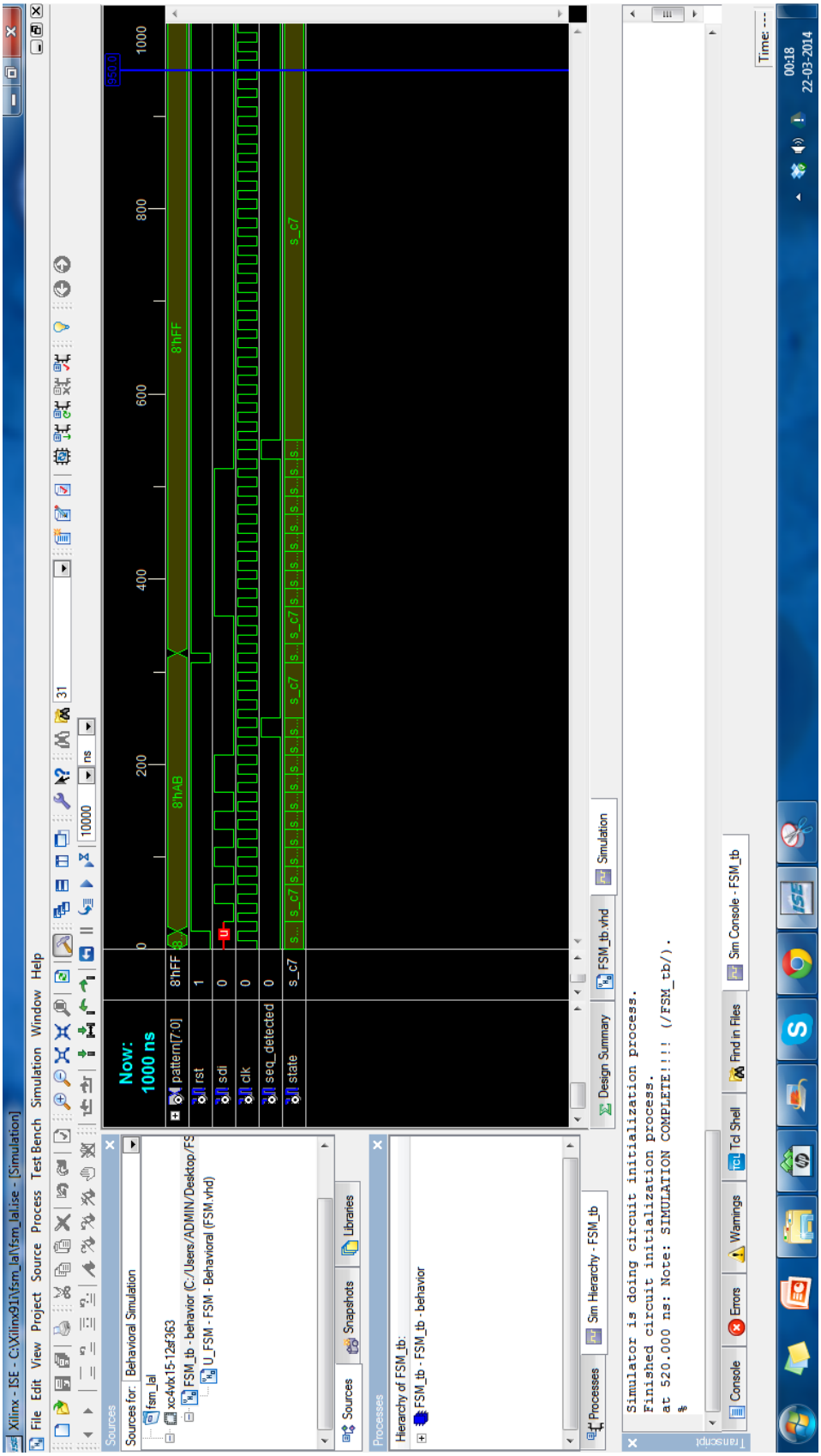
8-BIT SEQUENCE DETECTOR

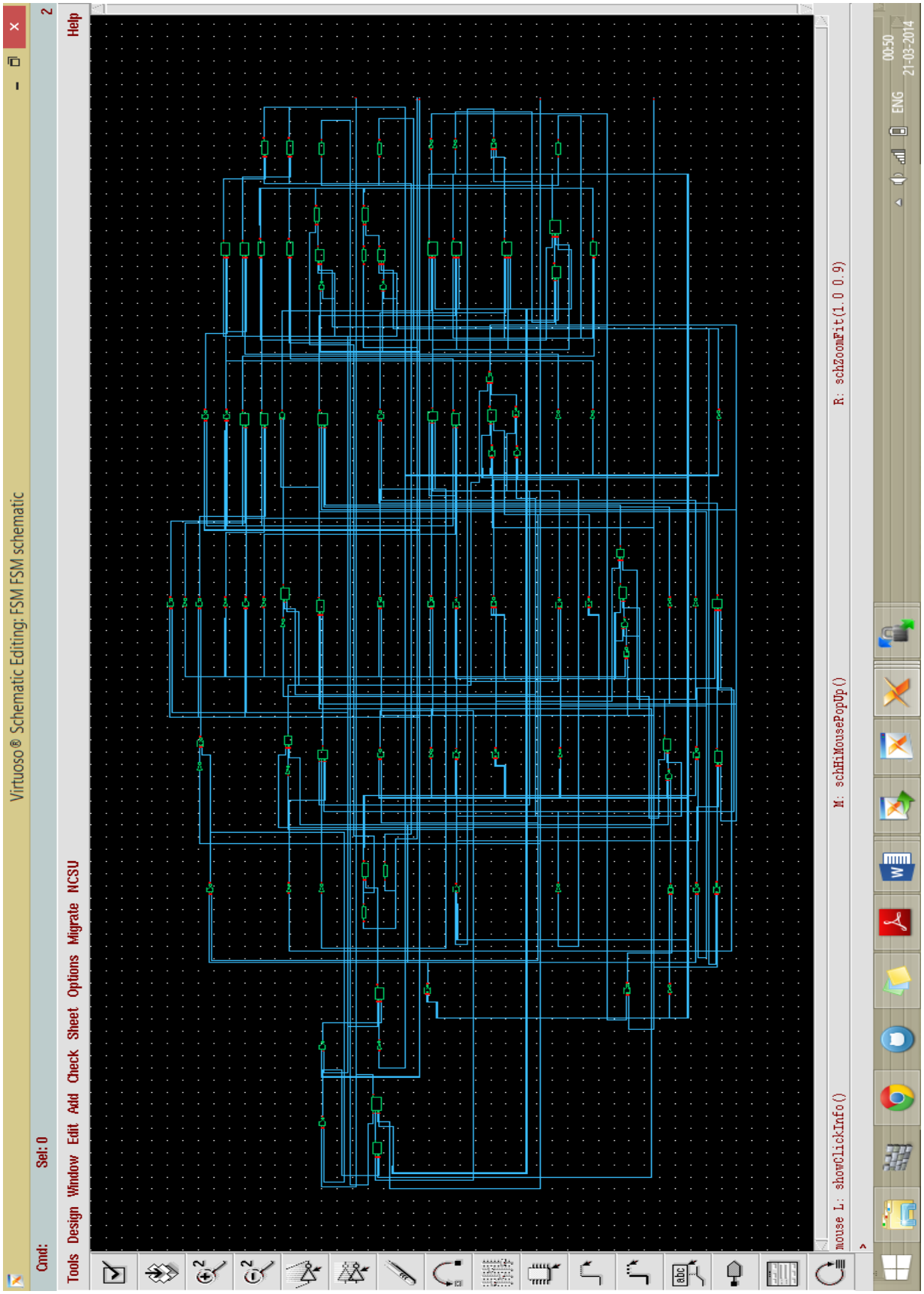
Block diagram or Finite State Machine diagram and corresponding brief description



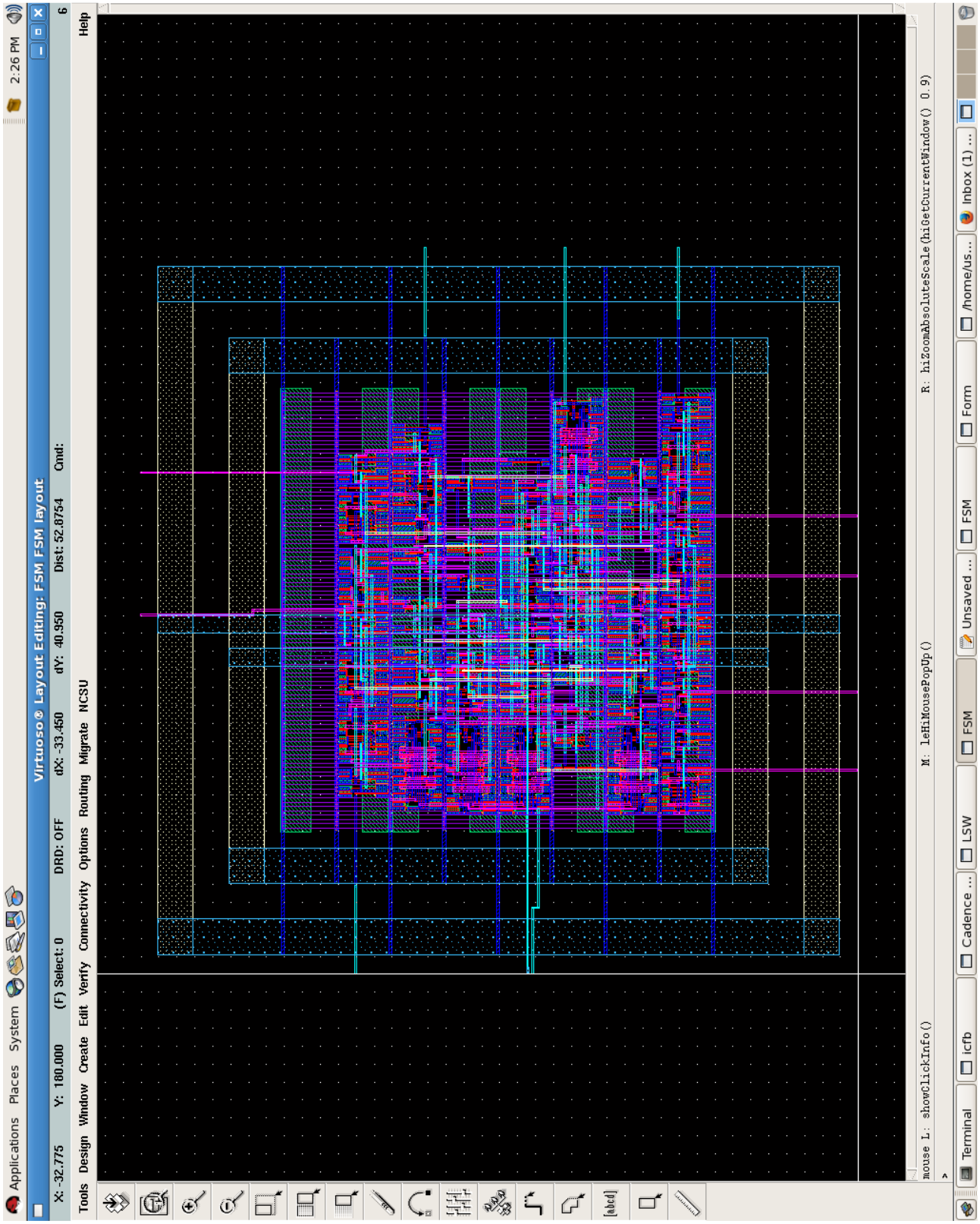
SIMULATON


Xilinx - ISE - C:\Xilinx91i\fsm_lal\fsm_lal.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Now: 1000 ns
pattern[7:0]
rst
sdi
clk
seq_detected
state
8'hFF
8'hAB
8'hFF
s_c7
Simulator is doing circuit initialization process.
Finished circuit initialization process.
at 520.000 ns: Note: SIMULATION COMPLETE!!!! (/FSM_tb/).
Time: ---
00:18
22-03-2014

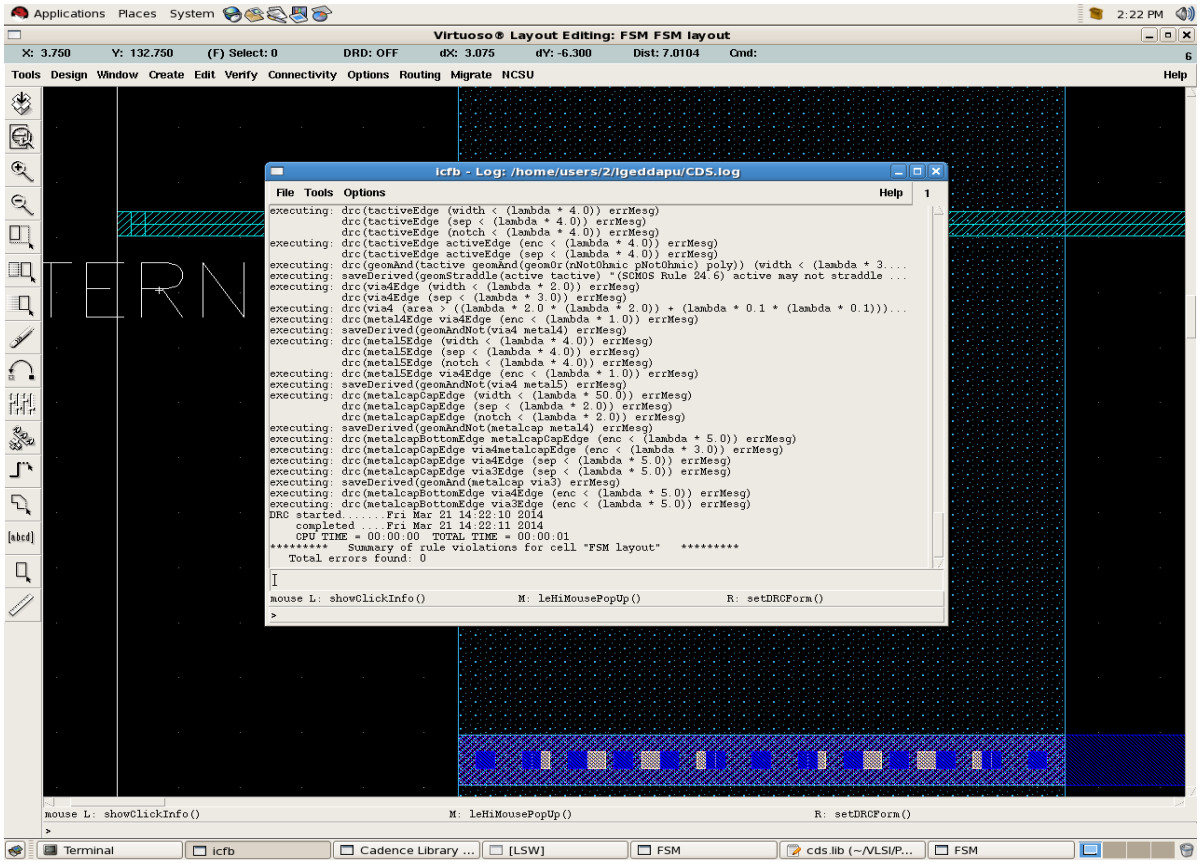
Gate-Level schematic after synthesis



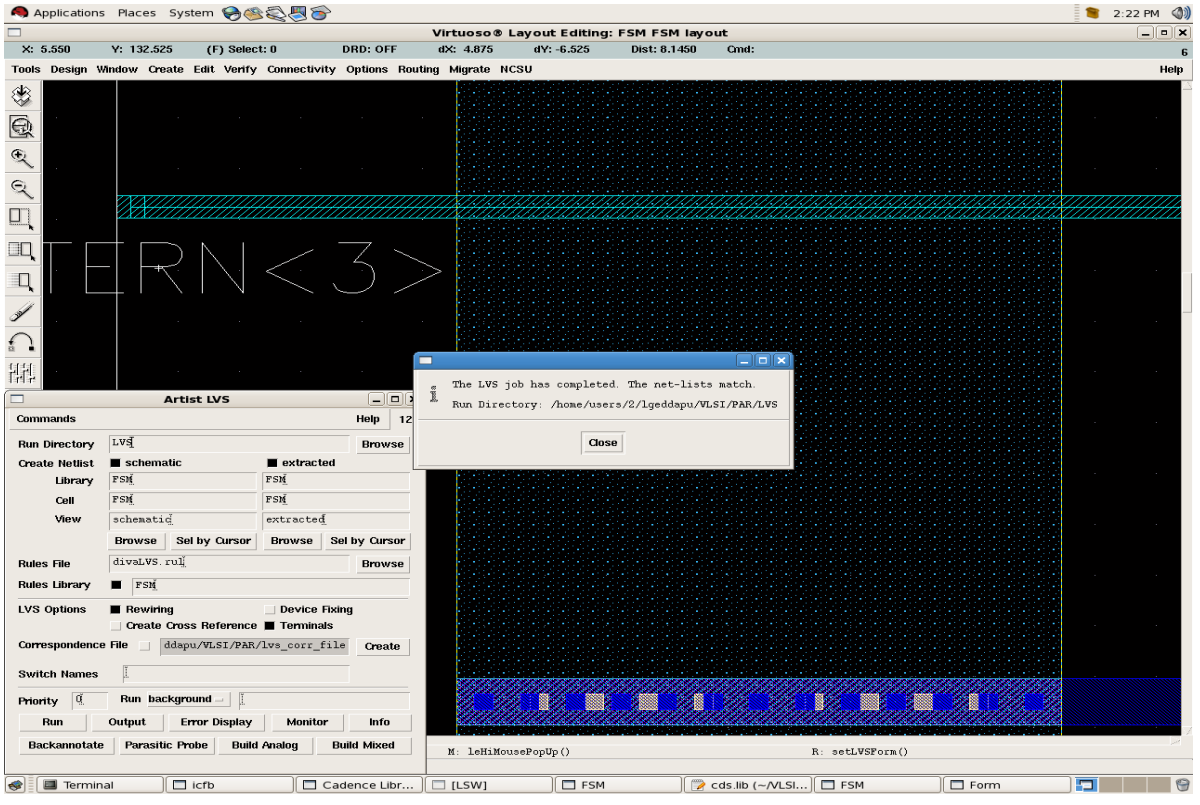
Layout


Applications Places System
2:26 PM
Virtuoso® Layout Editing: FSM FSM layout
X: -32.775 Y: 180.000 (F) Select: 0 DRD: OFF dX: -33.450 dY: 40.950 Dist: 52.8754 Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate NCSU Help
mouse L: showClickInfo()
M: leHiMousePopUp()
R: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)
Terminal
icfb
Cadence ...
LSW
FSM
Unsaved ...
FSM
Form
/home/us...
Inbox (1) ...

DRC clean report



LVS report



The Gate-Level netlist after synthesis final.v

```
/*
##############################################################
#
#  Generated by:      Cadence Encounter 10.13-s292_1
#  OS:                Linux x86_64(Host ID lnx19.ecel.ufl.edu)
#  Generated on:      Thu Mar 20 13:24:36 2014
#  Design:            FSM
#  Command:           saveNetlist -excludeLeafCell final.v
##############################################################
#
*/
module FSM (
        PATTERN,
        RST_N,
        SDI,
        SCK,
        SEQ_DETECTED);
   input [7:0] PATTERN;
   input RST_N;
   input SDI;
   input SCK;
   output SEQ_DETECTED;

   // Internal wires
   wire SCK__L1_N5;
   wire SCK__L1_N4;
   wire SCK__L1_N3;
   wire SCK__L1_N2;
   wire SCK__L1_N1;
   wire SCK__L1_N0;
   wire n1;
   wire n2;
   wire n3;
   wire n4;
   wire n5;
   wire n6;
   wire n7;
   wire n8;
   wire n9;
   wire n10;
   wire n11;
   wire n12;
   wire n13;
   wire n14;
   wire n15;
   wire n16;
   wire n17;
   wire n18;
   wire n19;
   wire n20;
```

```
wire n21;
wire n22;
wire n23;
wire n24;
wire n25;
wire n26;
wire n27;
wire n28;
wire n29;
wire n30;
wire n31;
wire n32;
wire n33;
wire n34;
wire n35;
wire n36;
wire n37;
wire n38;
wire n39;
wire n40;
wire n41;
wire n42;
wire n43;
wire n44;
wire n45;
wire n46;
wire n47;
wire n48;
wire n49;
wire n50;
wire n51;
wire n52;
wire n53;
wire n54;
wire n55;
wire n56;
wire n57;
wire n58;
wire n59;
wire n60;
wire n61;
wire n62;
wire n63;
wire n64;
wire n65;
wire n66;
wire n67;
wire n68;
wire n69;
wire n70;
wire n71;
```

```
wire n72;
wire n73;
wire n74;
wire n80;
wire n81;
wire n82;
wire n83;
wire n84;
wire [3:0] state;
wire [7:0] \output ;

BUFX4 SCK__L1_I5 (.Y(SCK__L1_N5),
     .A(SCK));
BUFX4 SCK__L1_I4 (.Y(SCK__L1_N4),
     .A(SCK));
BUFX4 SCK__L1_I3 (.Y(SCK__L1_N3),
     .A(SCK));
BUFX4 SCK__L1_I2 (.Y(SCK__L1_N2),
     .A(SCK));
BUFX4 SCK__L1_I1 (.Y(SCK__L1_N1),
     .A(SCK));
BUFX4 SCK__L1_I0 (.Y(SCK__L1_N0),
     .A(SCK));
DFFSR \state_reg[0]  (.S(1'b1),
     .R(RST_N),
     .Q(state[0]),
     .D(n84),
     .CLK(SCK__L1_N2));
DFFSR \state_reg[3]  (.S(1'b1),
     .R(RST_N),
     .Q(state[3]),
     .D(n83),
     .CLK(SCK__L1_N2));
DFFSR \state_reg[1]  (.S(1'b1),
     .R(RST_N),
     .Q(state[1]),
     .D(n81),
     .CLK(SCK__L1_N0));
DFFSR \state_reg[2]  (.S(1'b1),
     .R(RST_N),
     .Q(state[2]),
     .D(n82),
     .CLK(SCK__L1_N0));
DFFSR SEQ_DETECTED_reg (.S(1'b1),
     .R(RST_N),
     .Q(SEQ_DETECTED),
     .D(n80),
     .CLK(SCK__L1_N4));
DFFPOSX1 \output_reg[0]  (.Q(\output [0]),
     .D(n74),
     .CLK(SCK__L1_N2));
```

```
DFFPOSX1 \output_reg[1]  (.Q(\output [1]),
     .D(n73),
     .CLK(SCK__L1_N4));
DFFPOSX1 \output_reg[2]  (.Q(\output [2]),
     .D(n72),
     .CLK(SCK__L1_N5));
DFFPOSX1 \output_reg[3]  (.Q(\output [3]),
     .D(n71),
     .CLK(SCK__L1_N0));
DFFPOSX1 \output_reg[4]  (.Q(\output [4]),
     .D(n70),
     .CLK(SCK__L1_N3));
DFFPOSX1 \output_reg[5]  (.Q(\output [5]),
     .D(n69),
     .CLK(SCK__L1_N1));
DFFPOSX1 \output_reg[6]  (.Q(\output [6]),
     .D(n68),
     .CLK(SCK__L1_N1));
DFFPOSX1 \output_reg[7]  (.Q(\output [7]),
     .D(n67),
     .CLK(SCK__L1_N5));
OAI21X1 U3 (.Y(n67),
     .C(n3),
     .B(n2),
     .A(n1));
NAND2X1 U4 (.Y(n3),
     .B(n1),
     .A(PATTERN[7]));
INVX1 U5 (.Y(n2),
     .A(\output [7]));
OAI21X1 U6 (.Y(n68),
     .C(n5),
     .B(n4),
     .A(n1));
NAND2X1 U7 (.Y(n5),
     .B(n1),
     .A(PATTERN[6]));
INVX1 U8 (.Y(n4),
     .A(\output [6]));
OAI21X1 U9 (.Y(n69),
     .C(n7),
     .B(n6),
     .A(n1));
NAND2X1 U10 (.Y(n7),
     .B(n1),
     .A(PATTERN[5]));
INVX1 U11 (.Y(n6),
     .A(\output [5]));
OAI21X1 U12 (.Y(n70),
     .C(n9),
     .B(n8),
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```
     .A(n1));
NAND2X1 U13 (.Y(n9),
     .B(n1),
     .A(PATTERN[4]));
OAI21X1 U14 (.Y(n71),
     .C(n11),
     .B(n10),
     .A(n1));
NAND2X1 U15 (.Y(n11),
     .B(n1),
     .A(PATTERN[3]));
INVX1 U16 (.Y(n10),
     .A(\output [3]));
OAI21X1 U17 (.Y(n72),
     .C(n13),
     .B(n12),
     .A(n1));
NAND2X1 U18 (.Y(n13),
     .B(n1),
     .A(PATTERN[2]));
OAI21X1 U19 (.Y(n73),
     .C(n15),
     .B(n14),
     .A(n1));
NAND2X1 U20 (.Y(n15),
     .B(n1),
     .A(PATTERN[1]));
INVX1 U21 (.Y(n14),
     .A(\output [1]));
OAI21X1 U22 (.Y(n74),
     .C(n17),
     .B(n16),
     .A(n1));
NAND2X1 U23 (.Y(n17),
     .B(n1),
     .A(PATTERN[0]));
INVX1 U24 (.Y(n16),
     .A(\output [0]));
NOR2X1 U25 (.Y(n1),
     .B(n19),
     .A(n18));
INVX1 U26 (.Y(n18),
     .A(RST_N));
OAI21X1 U27 (.Y(n80),
     .C(n22),
     .B(n21),
     .A(n20));
NAND2X1 U28 (.Y(n22),
     .B(n19),
     .A(SEQ_DETECTED));
NAND2X1 U29 (.Y(n19),
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     .B(n24),
     .A(n23));
OAI22X1 U30 (.Y(n81),
     .D(n28),
     .C(n27),
     .B(n26),
     .A(n25));
AOI21X1 U31 (.Y(n28),
     .C(n31),
     .B(n30),
     .A(n29));
OAI21X1 U32 (.Y(n30),
     .C(n32),
     .B(n21),
     .A(state[1]));
NAND3X1 U33 (.Y(n32),
     .C(n33),
     .B(n21),
     .A(state[1]));
XNOR2X1 U34 (.Y(n33),
     .B(SDI),
     .A(\output [6]));
INVX1 U35 (.Y(n27),
     .A(n26));
NAND2X1 U36 (.Y(n82),
     .B(n35),
     .A(n34));
INVX1 U37 (.Y(n35),
     .A(n31));
OAI21X1 U38 (.Y(n31),
     .C(n38),
     .B(n37),
     .A(n36));
NAND3X1 U39 (.Y(n38),
     .C(n39),
     .B(n23),
     .A(state[1]));
NOR2X1 U40 (.Y(n39),
     .B(n41),
     .A(n40));
XNOR2X1 U41 (.Y(n41),
     .B(SDI),
     .A(n12));
INVX1 U42 (.Y(n12),
     .A(\output [2]));
INVX1 U43 (.Y(n40),
     .A(state[2]));
AOI22X1 U44 (.Y(n34),
     .D(n44),
     .C(n43),
     .B(n42),
```

```
     .A(state[2]));
OAI21X1 U45 (.Y(n42),
     .C(n26),
     .B(n46),
     .A(n45));
NAND2X1 U46 (.Y(n46),
     .B(n25),
     .A(n23));
XNOR2X1 U47 (.Y(n45),
     .B(SDI),
     .A(n8));
INVX1 U48 (.Y(n8),
     .A(\output [4]));
OAI21X1 U49 (.Y(n83),
     .C(n48),
     .B(n26),
     .A(n47));
AOI22X1 U50 (.Y(n48),
     .D(n52),
     .C(n51),
     .B(n50),
     .A(n49));
XNOR2X1 U51 (.Y(n50),
     .B(SDI),
     .A(\output [0]));
NOR2X1 U52 (.Y(n49),
     .B(n20),
     .A(state[0]));
OR2X1 U53 (.Y(n84),
     .B(n54),
     .A(n53));
OAI21X1 U54 (.Y(n54),
     .C(n56),
     .B(n37),
     .A(n55));
INVX1 U55 (.Y(n55),
     .A(n36));
XOR2X1 U56 (.Y(n36),
     .B(SDI),
     .A(\output [3]));
OAI21X1 U57 (.Y(n53),
     .C(n57),
     .B(n26),
     .A(n21));
AOI22X1 U58 (.Y(n57),
     .D(n59),
     .C(n43),
     .B(n58),
     .A(n51));
INVX1 U59 (.Y(n59),
     .A(n44));
```

```
XNOR2X1 U60 (.Y(n44),
     .B(SDI),
     .A(\output [5]));
INVX1 U61 (.Y(n43),
     .A(n60));
INVX1 U62 (.Y(n58),
     .A(n52));
XNOR2X1 U63 (.Y(n52),
     .B(SDI),
     .A(\output [1]));
NAND3X1 U64 (.Y(n26),
     .C(n62),
     .B(n61),
     .A(n56));
NOR2X1 U65 (.Y(n62),
     .B(n63),
     .A(n51));
NAND2X1 U66 (.Y(n63),
     .B(n60),
     .A(n37));
NAND3X1 U67 (.Y(n60),
     .C(n29),
     .B(state[0]),
     .A(state[1]));
NOR2X1 U68 (.Y(n29),
     .B(state[2]),
     .A(state[3]));
OR2X1 U69 (.Y(n37),
     .B(state[1]),
     .A(n64));
NOR2X1 U70 (.Y(n51),
     .B(n25),
     .A(n64));
INVX1 U71 (.Y(n25),
     .A(state[1]));
NAND3X1 U72 (.Y(n64),
     .C(state[2]),
     .B(n47),
     .A(state[0]));
INVX1 U73 (.Y(n47),
     .A(state[3]));
OAI21X1 U74 (.Y(n61),
     .C(n24),
     .B(n65),
     .A(state[3]));
XNOR2X1 U75 (.Y(n65),
     .B(SDI),
     .A(\output [7]));
AOI21X1 U76 (.Y(n56),
     .C(n23),
     .B(n66),
```

```
        .A(n21));
    NOR2X1 U77 (.Y(n23),
        .B(state[3]),
        .A(state[0]));
    INVX1 U78 (.Y(n66),
        .A(n20));
    NAND2X1 U79 (.Y(n20),
        .B(n24),
        .A(state[3]));
    NOR2X1 U80 (.Y(n24),
        .B(state[1]),
        .A(state[2]));
    INVX1 U81 (.Y(n21),
        .A(state[0]));
endmodule
```