4x1 SRAM Design Project Report

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***Abstract*—This project report represents a design of a 4x1 SRAM. Each SRAM cell has 6 transistors. The design is completed using CADENCE tool, and includes schematic, layout, and simulations. Then, several critical parameters, cell area, read/write access time, static noise margins, will be evaluated respectively.**

***Index Terms*—SRAM, simulation, noise margin, area**

I. Introduction

Static Random-Access Memory (SRAM) is widely used in electronic applications. Compared to dynamic random-access memory, SRAM does not require reentering periodically when store the binary values. But it still a volatile form of memory and needs incessant power supply to keep the values. SRAM uses memory cells to store data. There are many way to implement SRAM memory cell, the way we use in this project is using 6 transistors, known as 6T cell. In some other design, more transistors may be used. To minimize the size of cell, six is a better number for this project. Each cell stores one variable bit and its complement. One memory cell requires 6 transistors per bit. In each cell, word line can enable the access to the SRAM, and the two bit lines transfer the stored signal and its inverse respectively. The cell support read and write operations, namely, the bit that stored in the cell can be output to a terminal and new bit can be stored in cell as an input. A sense amplifier is used to improve the accuracy of reading data, since environment noise decreases the quality of input signal and increases the probability of errors. Two clocks are used to control the two operations.

In other parts of the report, we are going to illustrate our idea with schematic and layout and analysis the modifications we made on the parameters in part II. In part III, show the simulation figures, and analysis the result in details. In part IV, make some evaluations about key parameters, such as overall SRAM area, read/write access time, and hold/read/write cell stability.

II. SRAM Schematic and Layout

In this project, as we described above, we use 6T (6 transistors in a cell) cell as a memory cell. The whole design can be divided into three main part. The first part is memory core, which consists of four 6T memory cells (Fig.1a and Fig.1b). Each cell can store one bit data and its complement. The whole memory core could store four bits in total. The word line is used to make selections of which cell to be read from or written to.

The sense amplifier is the second part. There are two kinds of sensing amplifiers generally. One is basic single-ended sensing amplifier, and the other one is differential sensing amplifier. In our project, we use the second kind of differential amplifier sense because it has numerous advantages over the first one, such being the common-mode rejection (such an amplifier rejects noise that is equally injected to both inputs). It is especially attractive in memories where the exact value of the bit line signal varies from die to die and even for different locations on a single die.

The third part is a tri-state transistor switch. The function of this switch is to control the word line to read or not.

Schematic and layout of the whole design is shown in Fig.2a and Fig.2b. And the DRC result in Fig 2c shows the correctness of layout design.

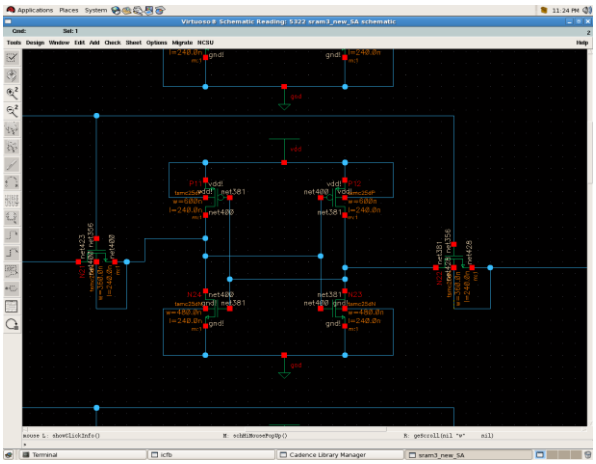

Fig.1a Schematic of 6T cell

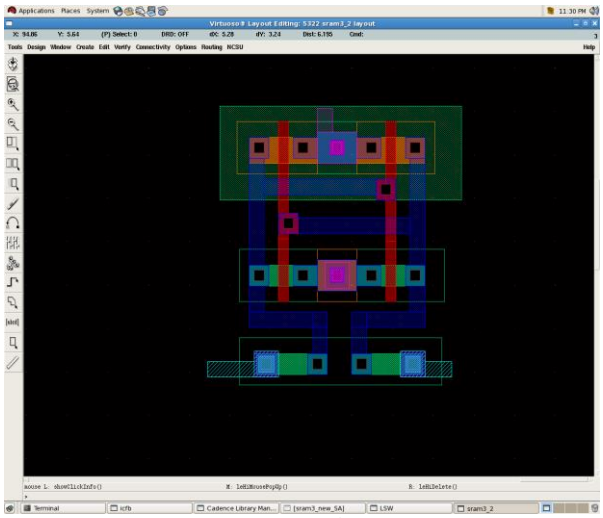

Fig.1b Layout of 6T cell

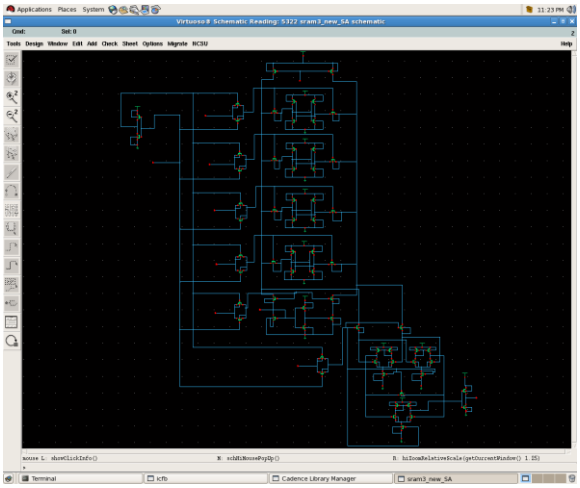

Fig.2a Schematic of SRAM

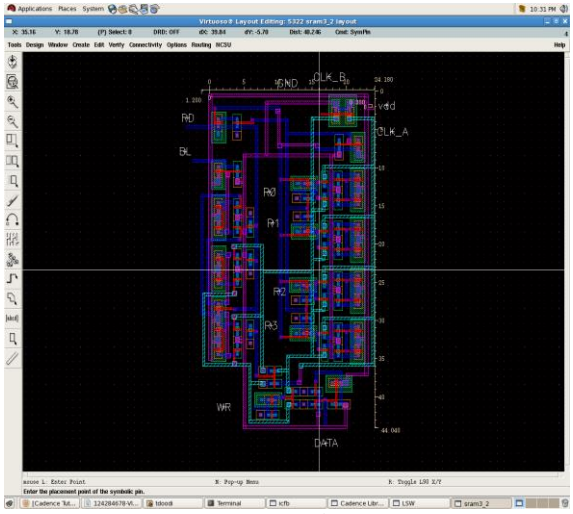

Fig.2b Layout of SRAM

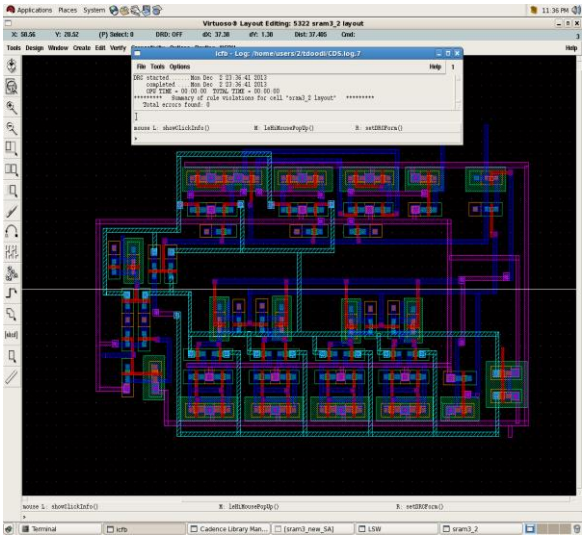

Fig.2c DRC result

III. SIMULATION

In reading operation, former outputs the variable stored in the memory cell, and later outputs the complement of variable. When the word line of the memory cell to be read has a higher voltage, the NMOS transistor will conduct the current and stored variable will be output to the corresponding line.

The simulation result of static noise margin of reading operation is shown in Fig.3

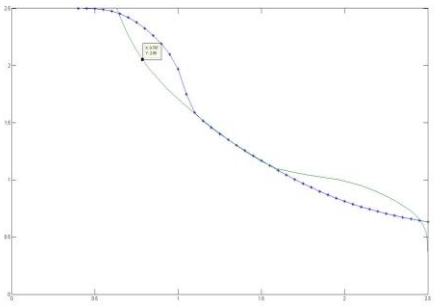

Fig.3 SNM of reading operation
(0.787, 2.05)(0.9,2.189) L = 0.113 W = .139

Writing operation is performed by changing the values stored in Q and Q bar in memory cells. It is done by setting the input to a high or low depending on whether to store a 1 or 0 for Q, respectively. When the write line is set to high for a memory cell, then writing operation is initialed and data stored on BL will be transferred to Q, so is data stored on bit bar line, it will be transferred to Q bar.

Fig. 4 shows the static noise margin of writing operation. And the static noise margin of holding operation(not reading and writing) is shown in Fig.5. The reading and writing access time simulation are shown in Fig.6 and Fig.7.

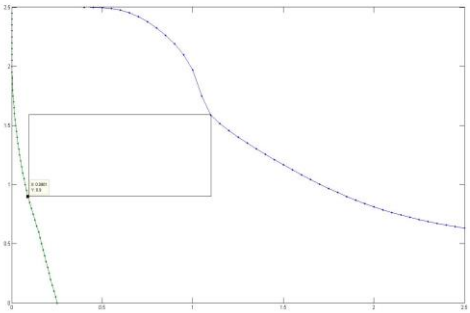

Fig.4 SNM of writing operation.
(0.0901, 0.9)(1.1,1.59) L = 1.0099 W = 0.69

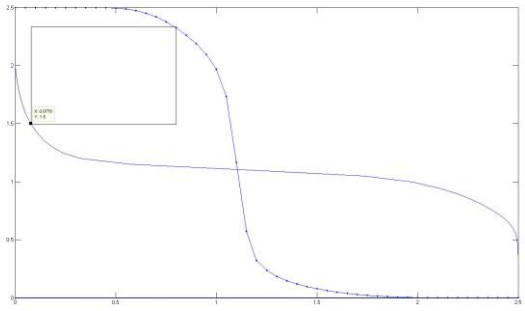

Fig.5 SNM of holding operation.
(0.0778,1.5)(0.8, 2.325) L = 0.7222 W = 0.825

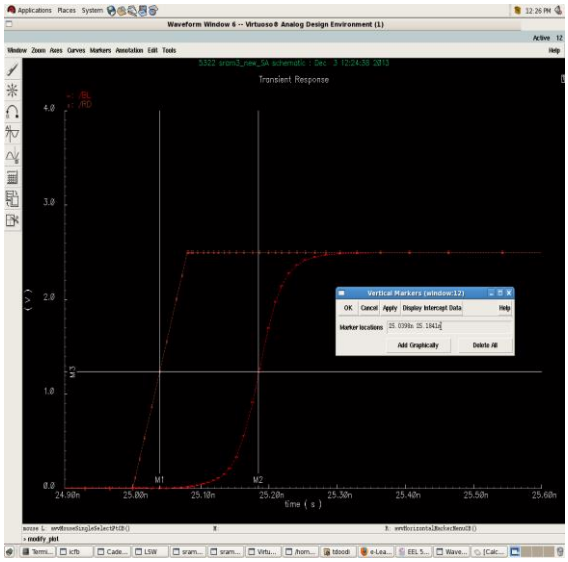

Fig.6 Reading access time

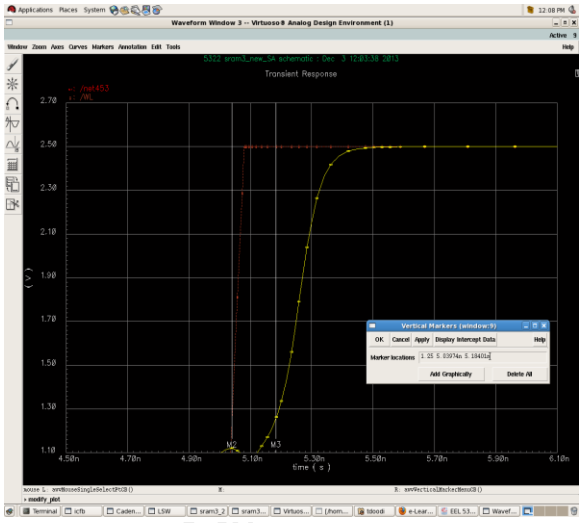

Fig.7 Writing assess time

IV. PARAMETERS EVALUATION

a. Area

After calculation, the area of 6T cell is 36.1348 and the area of the whole design is 1050.76. It is easy to find that our whole design area result is larger than usual. There are two reasons that lead to the larger result. First, in this project, we use differential amplifier sensing(shown in Fig.8 and Fig.9), which is bigger than the simple amplifier. So our design inevitably becomes bigger in area. The second reason is since the implementation of λ rule is complicated, we didn't strictly follow the λ rule everywhere in the design. It is something we can improve in the future.

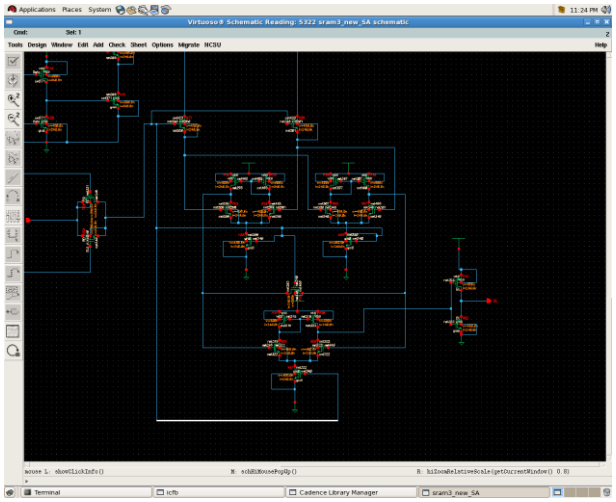

Fig.8 schematic of sensing amplifier

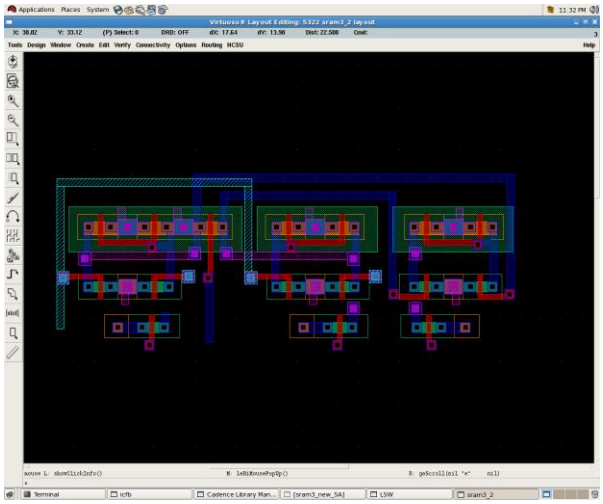

Fig.9 Layout of sensing amplifier

In practice, the values on bit and bit bar line are in the middle of 0 or 1 because of the noise and some other interference factors. In that way, it cannot ensure that the operations could get the correct values. By using differential sensing amplifier, it can help to output a voltage which is close to 0 or 1 as required. The differential sensing amplifier has a better performance of improving the operation accuracy because it uses the difference instead of the exact values. As long as the quantity relationship

of two values doesn't go wrong, the differential sensing amplifier is able to output the correct value.

b. Static noise margin

According to the simulation result, we can calculate the value of SNM for reading, writing and holding operations.
Reading operation: SNM = sqrt(0.113*0.139*2) = 0.117
Writing operation: SNM = sqrt(1.393662) = 1.18
Holding operation: SNM = sqrt(1.19163) = 1.09

c. Reading/writing access time

According to the simulation, Fig.6 and Fig.7 shows the results of the simulation. The reading access time is 144.3ps and writing access time is 144.27ps.

d. Capacitance

For 0.24um design rule, the capacities of our design are calculated as following:
Cox = 6fF/um2
Co = 0.31fF/um
Cj = 2fF/um2
Cjsw = 0.28fF/um

V. CONCLUSION

In this project, we design a 4x1 SRAM as required in the instruction. And completed the simulation, calculated the corresponding parameters and gave the analysis. We used 0.24um design rule in this design. At the beginning we didn't follow the design rule properly and got a very large area. After times of modifications, we finally achieved a relative small area.

REFERENCES

[1] Jan M. Rabaey, *Digital Integrated Circuits A Design Perspective*. International Edition: PHI, 2003, pp. 658–681.