

Learning large systems using peer-to-peer gossip

#### Policy Against Harassment at ACM Activities

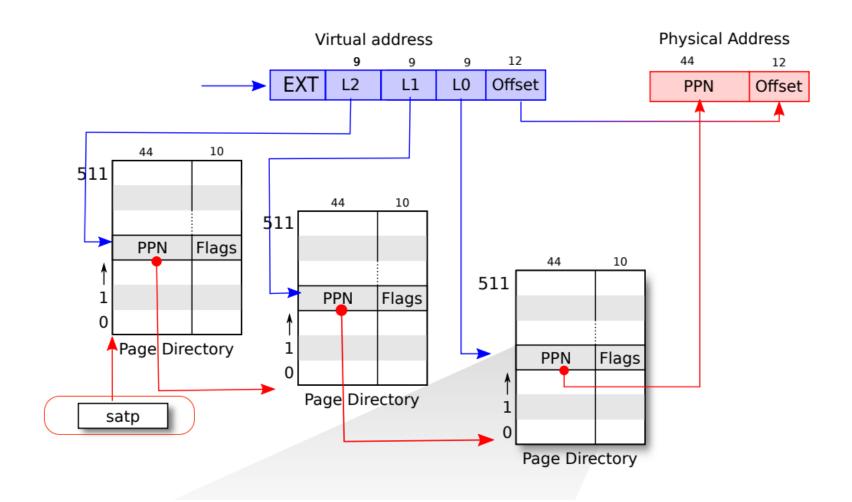
OS Meetup wants to encourage and preserve this open exchange of ideas, which requires an environment that enables all to participate without fear of personal harassment. We define harassment to include specific unacceptable factors and behaviors listed in the ACM's policy against harassment. Unacceptable behavior will not be tolerated.

https://www.acm.org/about-acm/policy-against-harassment

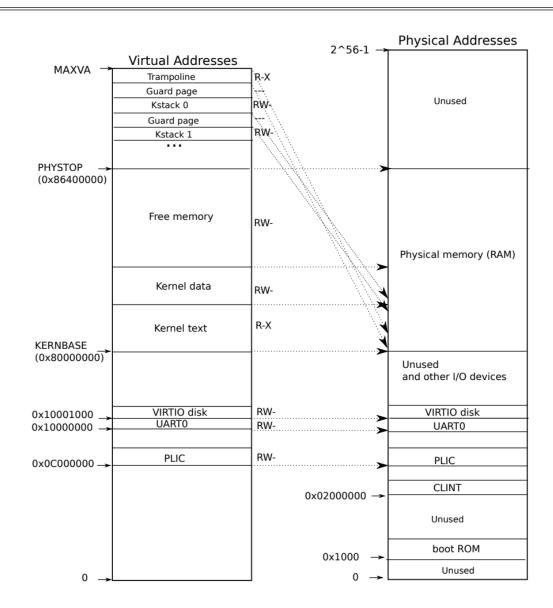
### Syscall Preparation: Registers & Memory

- o Recall:
  - Page table
- o Page table contents
  - Trampoline & Trapframe
- o Registers in Risc-V
  - Supervisor Registers
  - General Purpose Registers
- System Calls (User -> Kernel)
  - What CPU does for us?
  - What OS does for us?

# Recall: Page Table



# Recall: Page Table



### Recall: Page Table

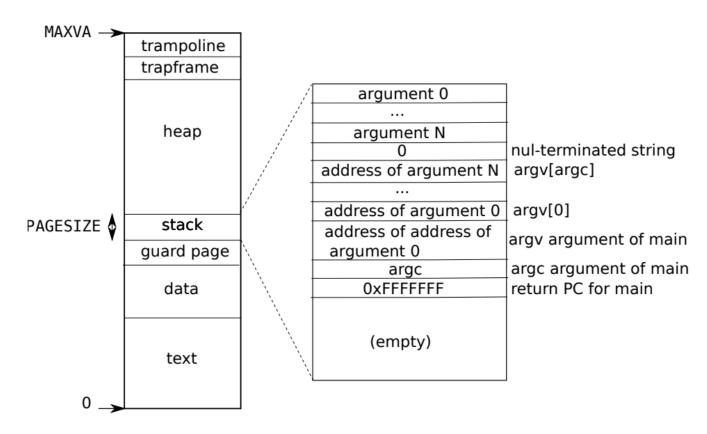
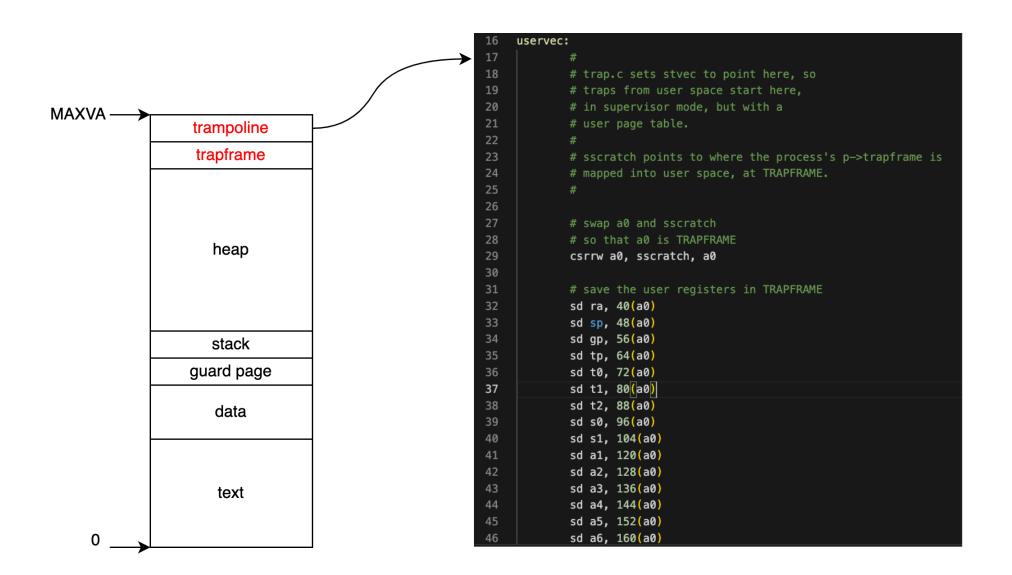
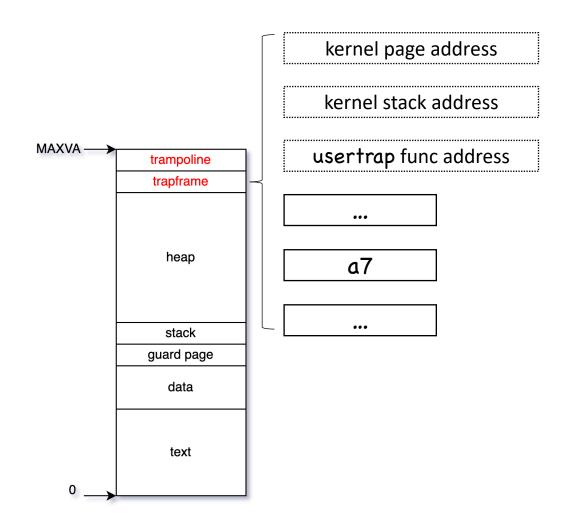


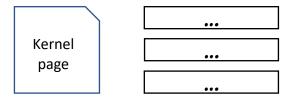
Figure 3.4: A process's user address space, with its initial stack.

#### Page: Trampoline



### Page: Trapframe





```
usertrap(void)
      int which_dev = 0;
       if((r_sstatus() & SSTATUS_SPP) != 0)
        panic("usertrap: not from user mode");
      // send interrupts and exceptions to kerneltrap(),
       w_stvec((uint64)kernelvec);
       struct proc *p = myproc();
       p->trapframe->epc = r_sepc();
       if(r_scause() == 8){\{}
         if(p->killed)
           exit(-1);
         // but we want to return to the next instruction.
         p->trapframe->epc += 4;
65
         intr_on();
       } else if((which_dev = devintr()) != 0){
```

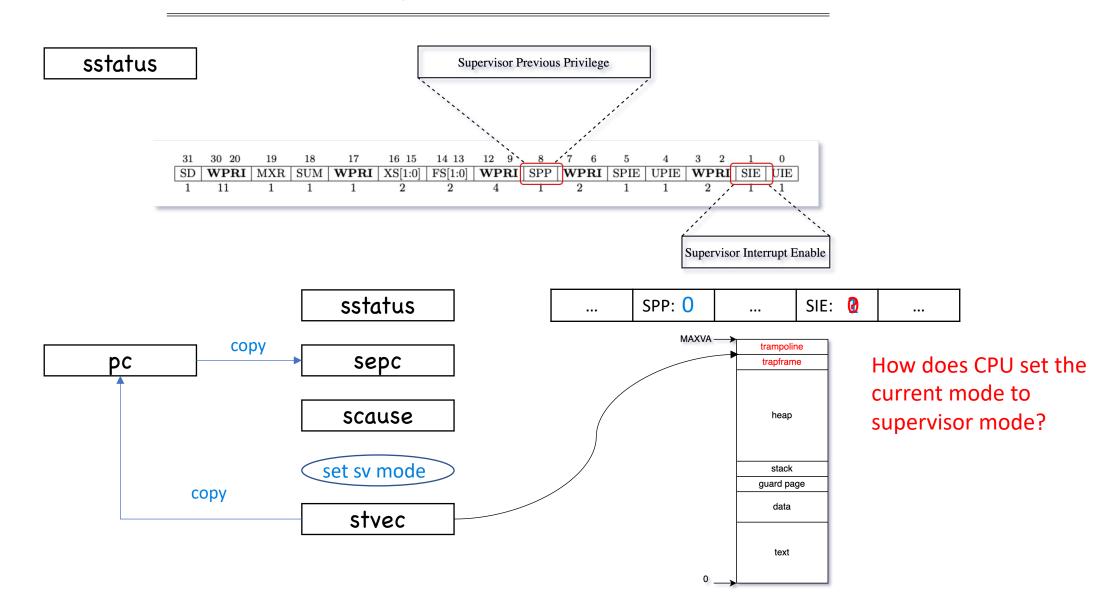
## **Risc-V Registers**

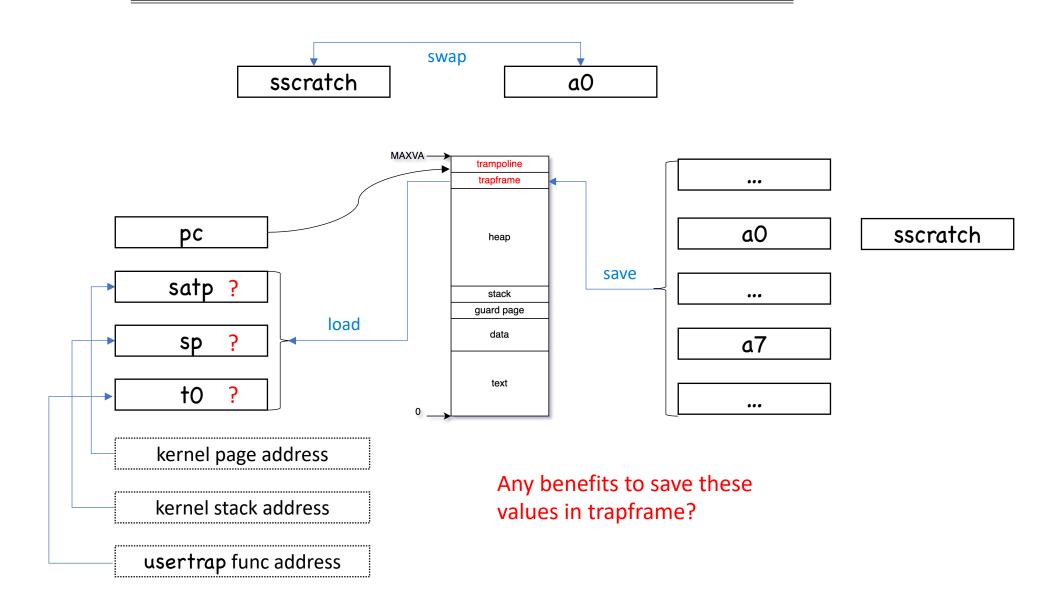
- o Supervisor control and status registers
- o General purpose registers

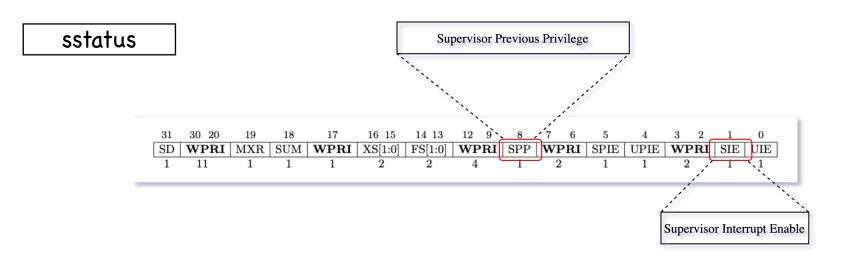
4	Supervisor-Level ISA, Version 1.10				
	4.1	Superv	risor CSRs		
		4.1.1	Supervisor Status Register (sstatus)		
		4.1.2	Base ISA Control in sstatus Register		
		4.1.3	Memory Privilege in sstatus Register		
		4.1.4	Supervisor Trap Vector Base Address Register (stvec)		
		4.1.5	Supervisor Interrupt Registers (sip and sie)		
		4.1.6	Supervisor Timers and Performance Counters		
		4.1.7	Counter-Enable Register (scounteren)		
		4.1.8	Supervisor Scratch Register (sscratch)		
		4.1.9	Supervisor Exception Program Counter (sepc)		
		4.1.10	Supervisor Cause Register (scause)		
		4.1.11	Supervisor Trap Value (stval) Register		
		4.1.12	Supervisor Address Translation and Protection (satp) Register .		

Register	ABI Name	Description
x0	zero	hardwired zero
x1	ra	return address
x2	sp	stack pointer
x3	gp	global pointer
x4	tp	thread pointer
x5	t0	temporary register 0
х6	t1	temporary register 1
х7	t2	temporary register 2
х8	s0 / fp	saved register 0 / frame pointer
x9	s1	saved register 1
x10	a0	function argument 0 / return value 0
x11	a1	function argument 1 / return value 1
x12	a2	function argument 2
x13	a3	function argument 3
x14	a4	function argument 4
x15	a5	function argument 5
x16	a6	function argument 6
x17	a7	function argument 7
x18	s2	saved register 2
x19	s3	saved register 3
x20	s4	saved register 4
x21	s5	saved register 5
x22	s6	saved register 6
x23	s7	saved register 7
x24	s8	saved register 8
x25	s9	saved register 9
x26	s10	saved register 10
x27	s11	saved register 11
x28	t3	temporary register 3
x29	t4	temporary register 4
x30	t5	temporary register 5
x31	t6	temporary register 6
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### System Calls: CPU



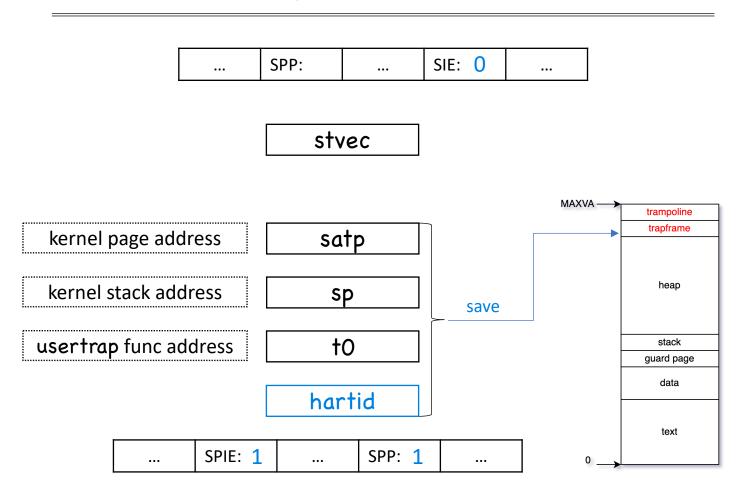


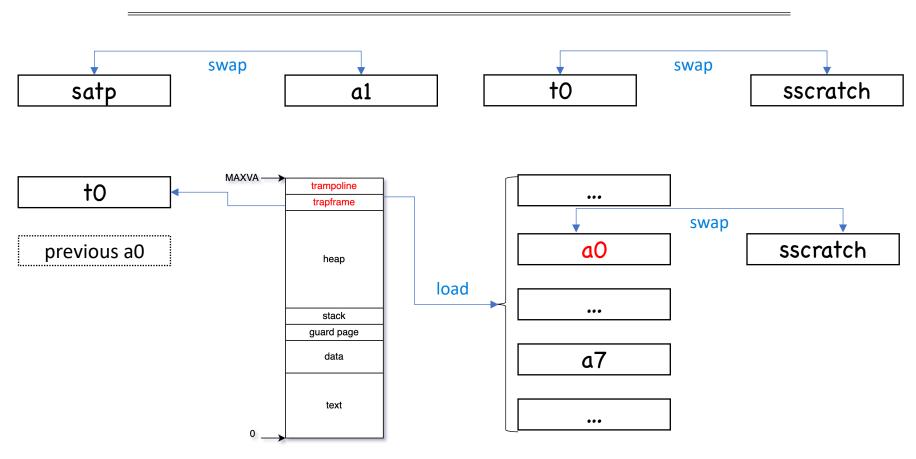


Which part will enable SIE again?

... SPP: 1 ... SIE: 0 ...

```
132
      void
      syscall(void)
133
134
135
        int num;
        struct proc *p = myproc();
136
137
138
        num = p->trapframe->a7;
139
        if(num > 0 && num < NELEM(syscalls) && syscalls[num]) {</pre>
140
          p->trapframe->a0 = syscalls[num]();
        } else {
141
142
          printf("%d %s: unknown sys call %d\n",
143
                  p->pid, p->name, num);
          p->trapframe->a0 = -1;
144
        }
145
146
147
```





## Summary

- o Trampoline & Trapframe
- o Registers in Risc-V
- CPU preparation for system calls
- OS preparation for system calls
- Next
  - Hongwang Li