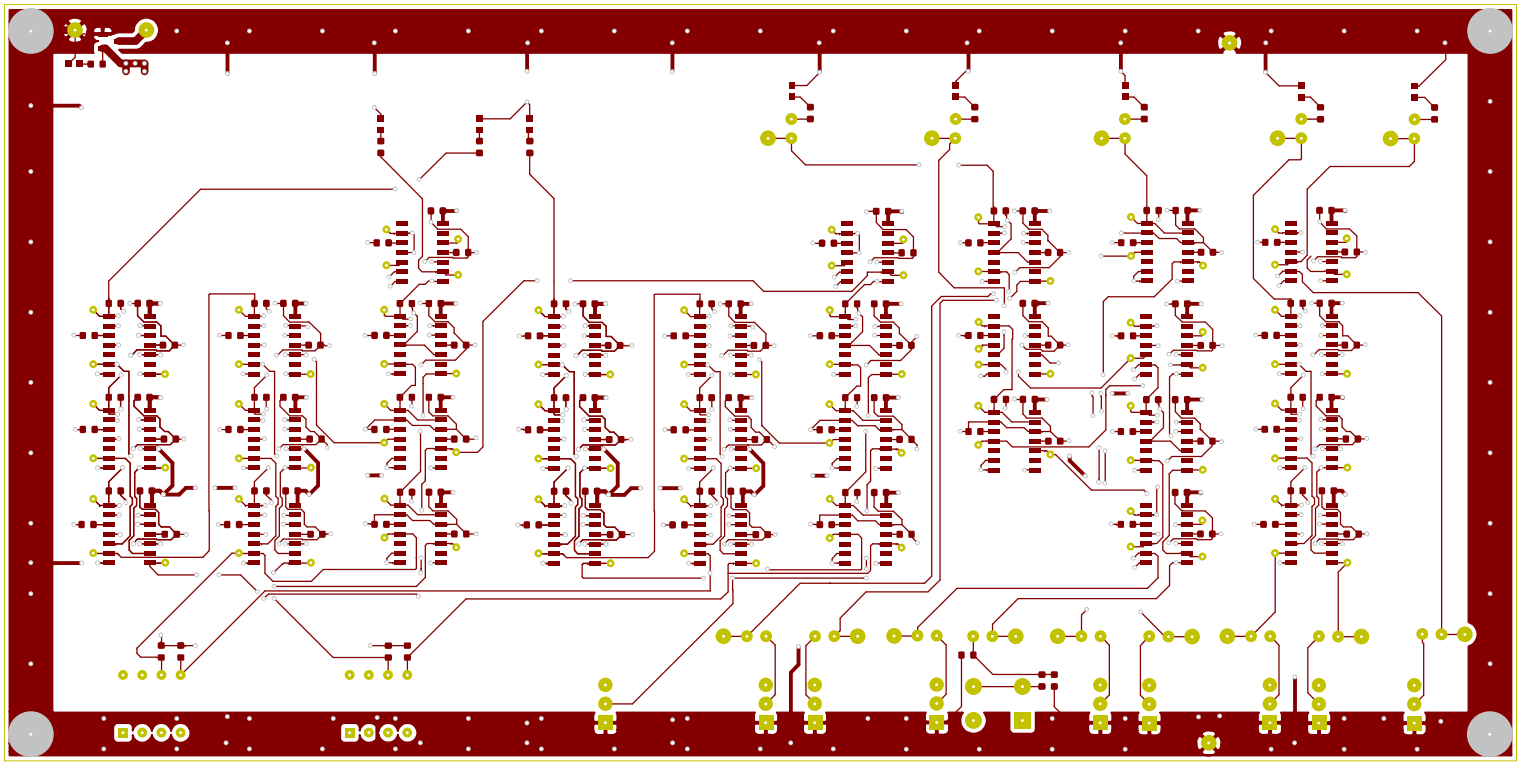

Design by Lambda Wolf Labs.

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Lambda Wolf Labs (Lorne Chrones)		
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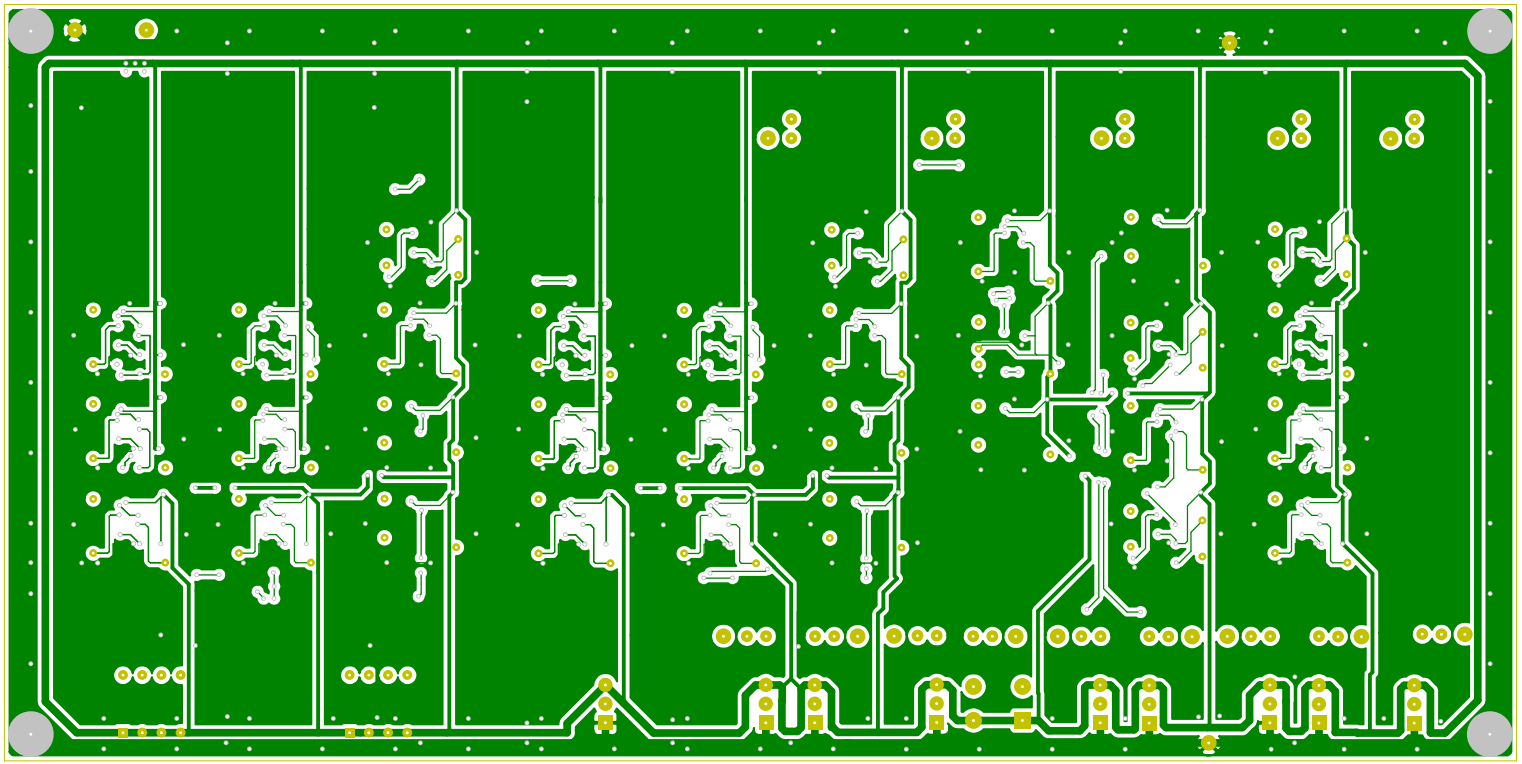
Title: 555 Timer Functional & Turing Complete Project		
Size: A4	Date: 2021-12-24	Rev: A
KiCad E.D.A. kicad (5.1.2)-2		Id: 1/1



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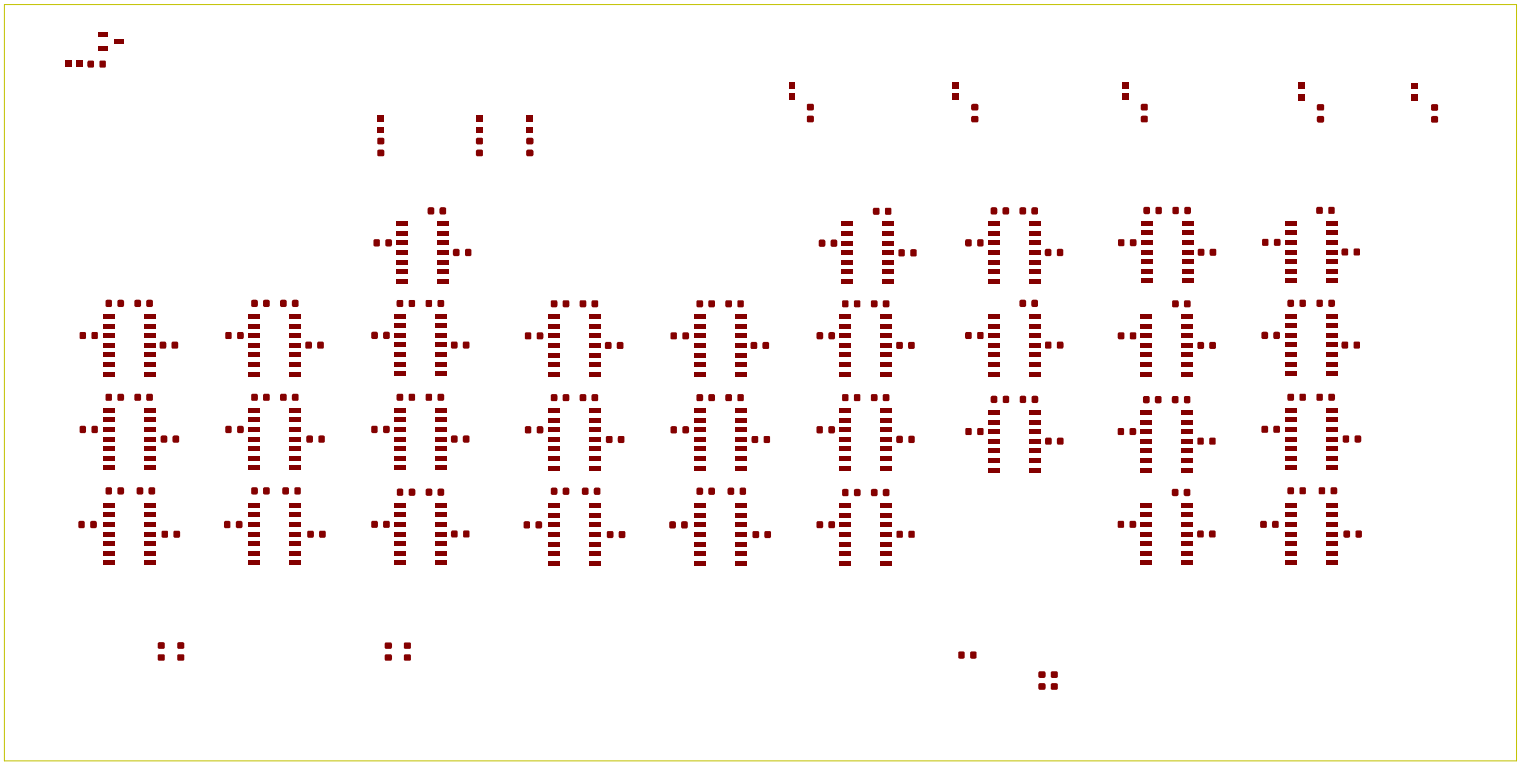

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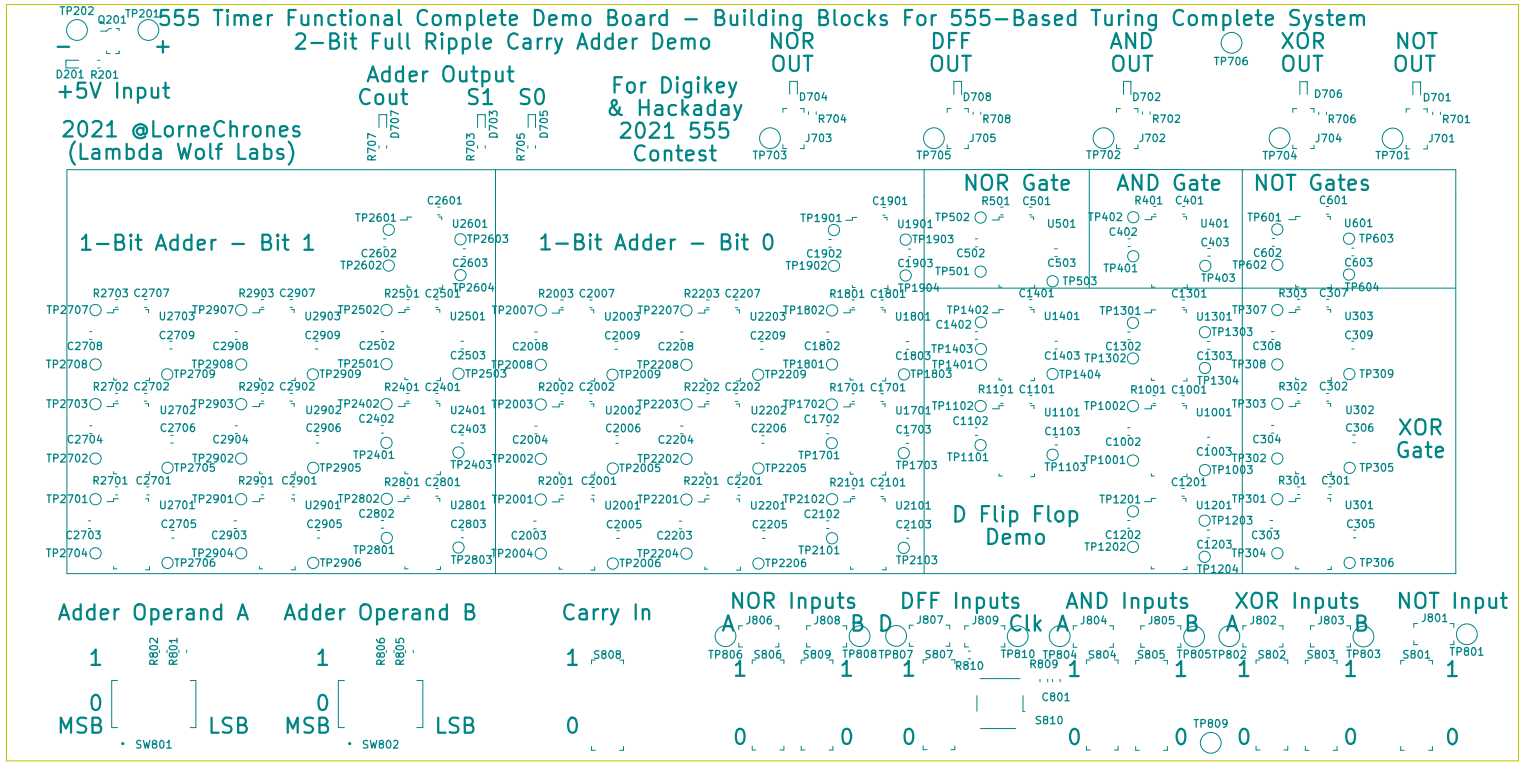
555 Timer Functional Complete Demo Board – Building Blocks For 555-Based Turing Complete System
2-Bit Full Ripple Carry Adder Demo
+5V Input
2021 @LorneChrones
(Lambda Wolf Labs)
Adder Output
Cout S1 S0
For Digikey
& Hackaday
2021 555
Contest
NOR OUT
DFF OUT
AND OUT
XOR OUT
NOT OUT
1-Bit Adder – Bit 1
1-Bit Adder – Bit 0
NOR Gate
AND Gate
NOT Gates
XOR Gate
D Flip Flop
Demo
Adder Operand A
Adder Operand B
Carry In
MSB
LSB
NOR Inputs
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Clk
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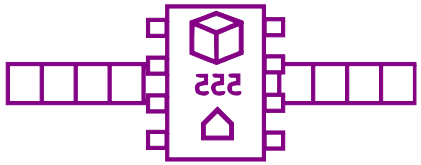

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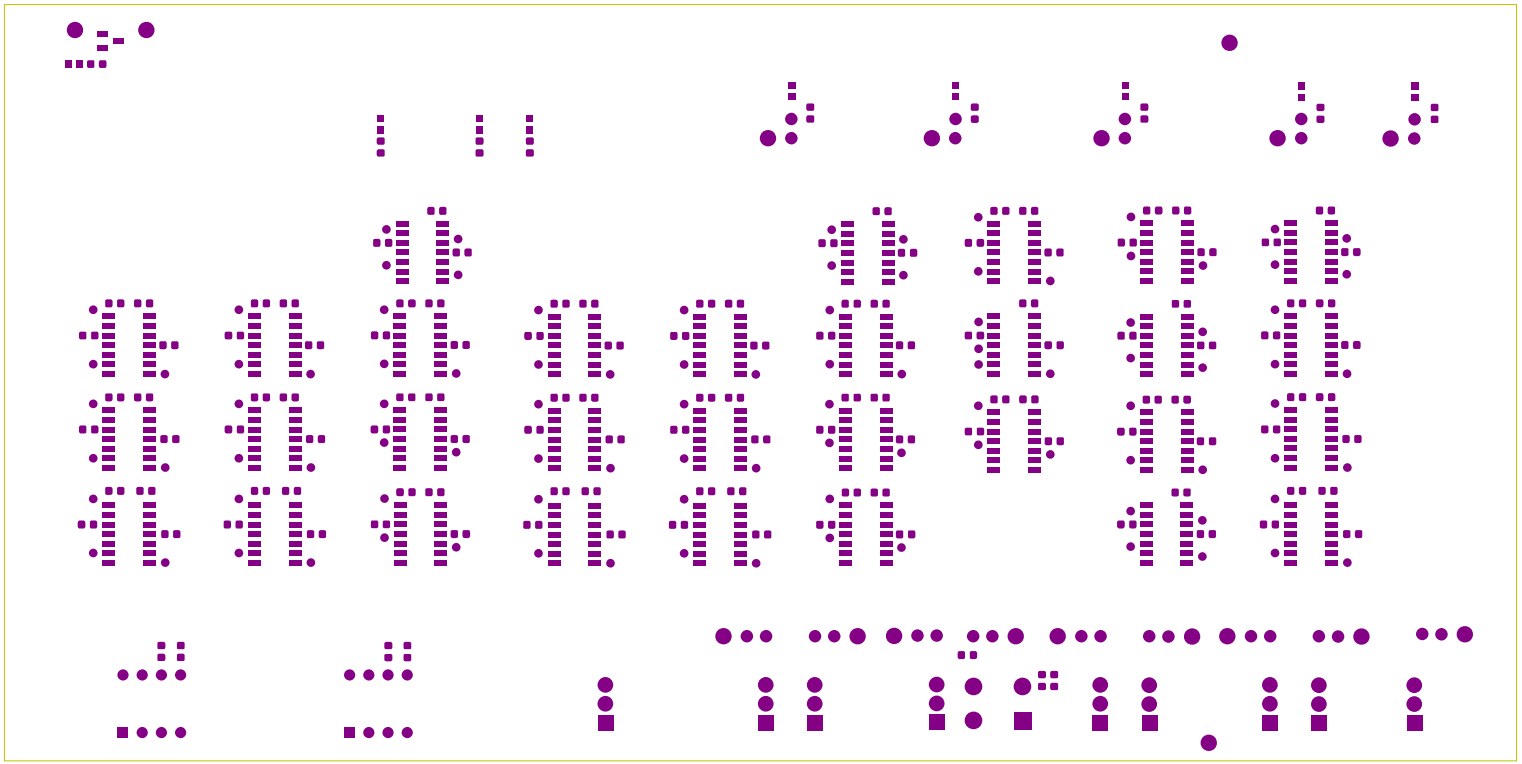

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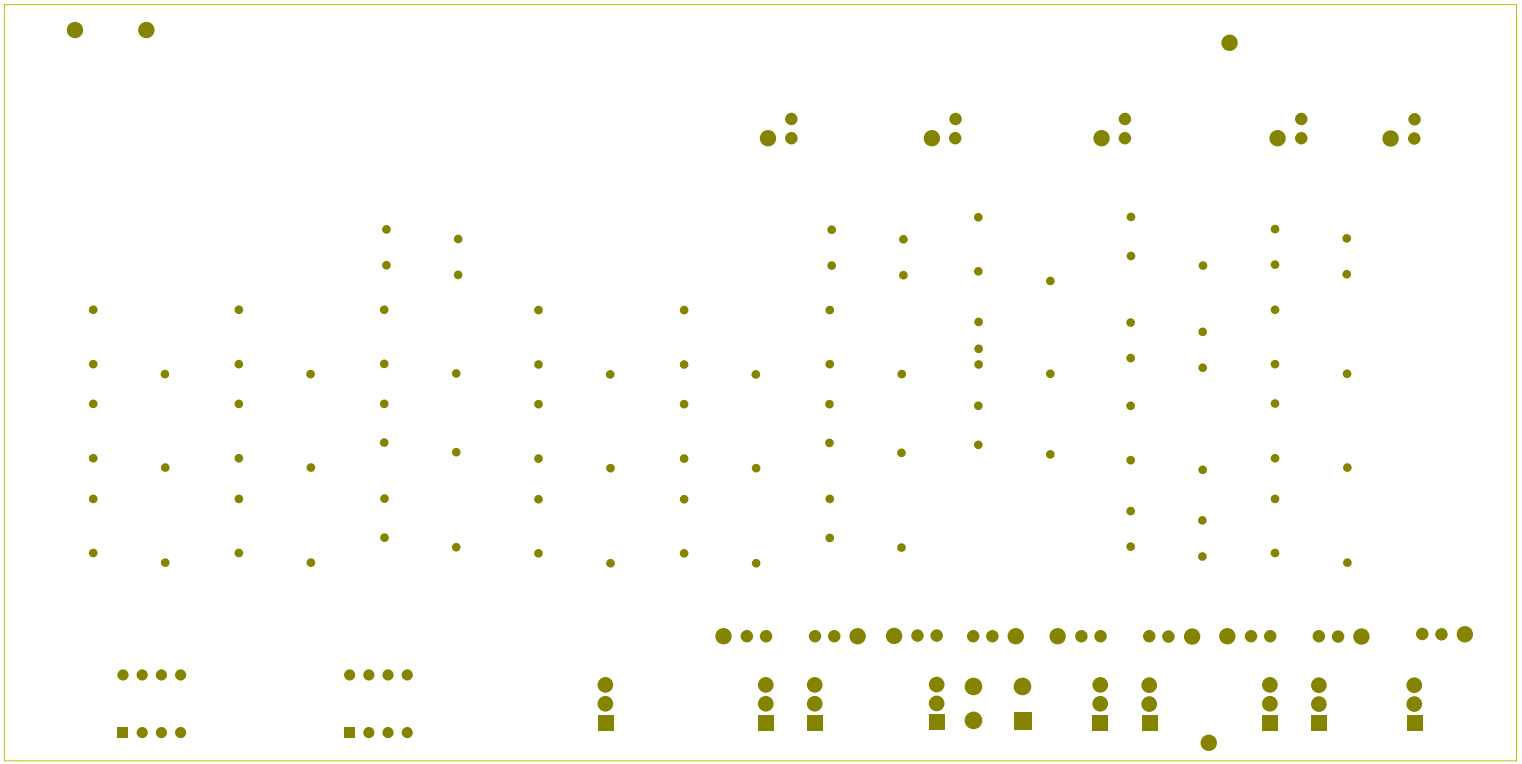

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General Notes

1. Fabricate per IPC-610-A Class 2, ANSI/IPC-A-600, IPC-QE-605, IPC-4101, IPC-4552 and IPC-SM-840 Specifications.
Use of EU ROHS-Compliant materials required. EU REACH compliance preferred but not required.

2. Material: Base material laminated epoxy glass FR-4, nominal core thickness 0.062" / 1.54mm, color natural,
nominal 1oz copper weight.
Thickness 0.07" / 1.62mm max after plating and finishing. ROHS compliant per IPC-4101 slash sheets #26
or #83 or #98 with minimum Tg 135 Degree C or Higher, Td 300 Degree C or Higher & Flame Rated UL 94V-0.

3. Soldermask both sides of board over bare copper with material per ANSI/IPC-SM-840. Color shall be green.

4. Apply solder plating (HASL) with hot-air leveling to exposed copper both sides. Lead-free HASL required.

5. Bottom side silkscreen available to apply markings such as manufacturer, UL marking, date-code, etc.
Avoid modifying top side silkscreen.

6. Apply silkscreen to top side of board using non-conductive white epoxy ink.

7. See fabrication files with same title or drawing number and revision as this drawing.

8. Dimensional tolerances are: 0.XX" = +/- 0.01", 0.XXX = +/- 0.005, angles = +/- 2 degrees.

9. Outline defined in separate gerber file with ".GM1" file extension.

10. See separate drill file with ".DRL" file extension for hole locations.
Selected hole locations in this drawing are for reference only.

11. Hole locations specified in the separate drill file take precedence over this drawing and artwork.
Contact purchaser / engineer to resolve dimension conflicts between drawing and artwork, if any.

12. Hole sizes are specified as final dimensions after plating and finishing unless otherwise specified.

13. Vendor to plate holes and exposed pads.

14. After assembly, trim solder fillets and component leads to 0.06" (Max) beyond board surface on bottom side.

15. Design geometry minimum feature sizes & design rules:
Trace Width: 6mils
Hole-Hole: 25mils
Silkscreen Line Width: 6mils
Minimum Hole Size (Plated): 10mils
Board Edge-Copper: 15mils
Trace-Trace / Trace-Pad: 6mils
Pad-Pad: 6mils
Silkscreen-Bare Copper: 6mils
Maximum Hole Size (Unplated): 250mils

Stackup:

F.SilkS – Top Silkscreen
F.Mask – Top Mask – 1mil thick max
F.Cu – Top Layer – 1oz Copper

FR-4 Dielectric 62mils

B.Cu – Bottom Layer – 1oz Copper
B.Mask – Bottom Mask – 1mil thick max
B.SilkS – Bottom Silkscreen

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Power In

Adder Output LEDs

Misc Output LEDs

555 Adder Logic

Misc 555 Gates

Adder User Input

Misc User Input

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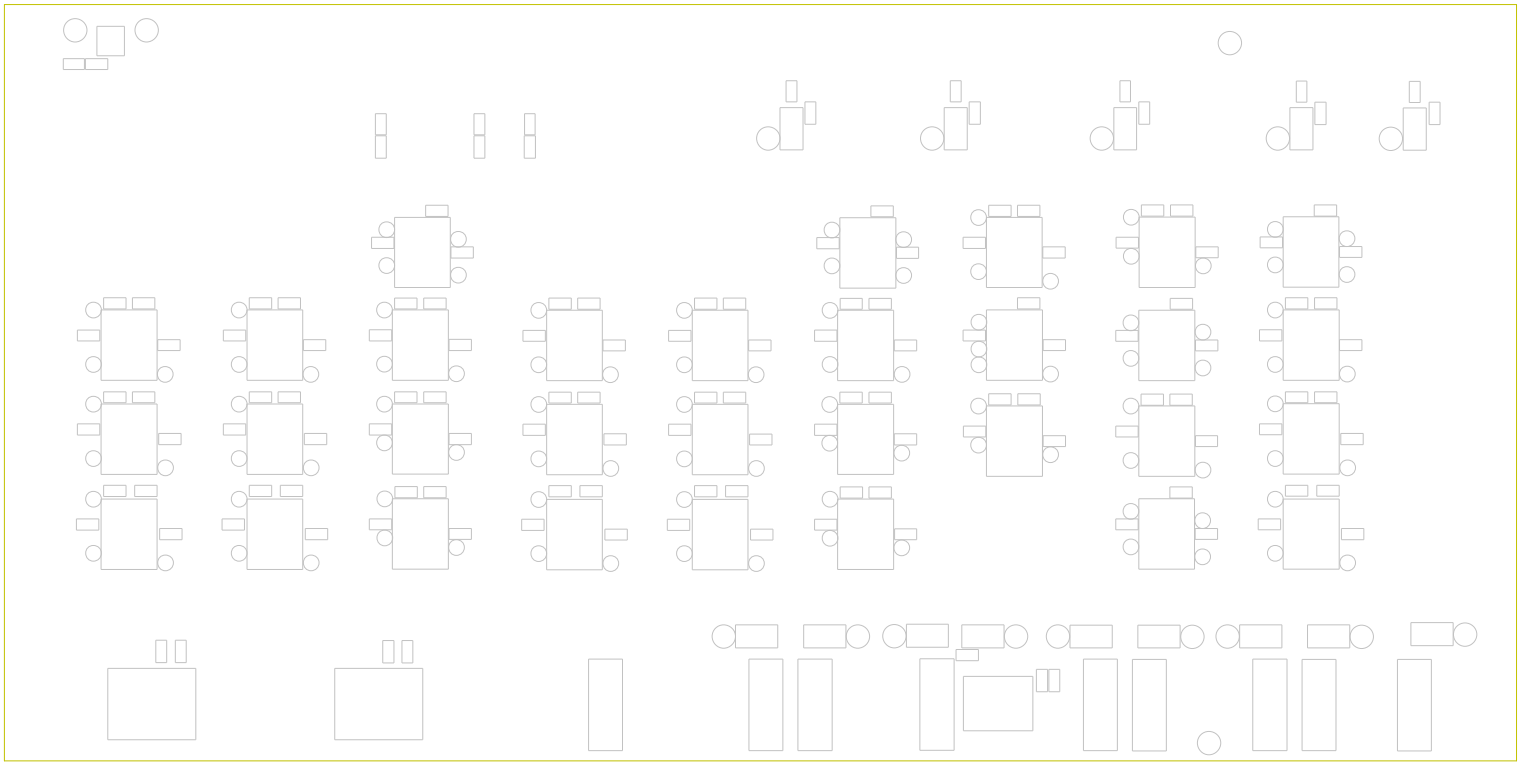

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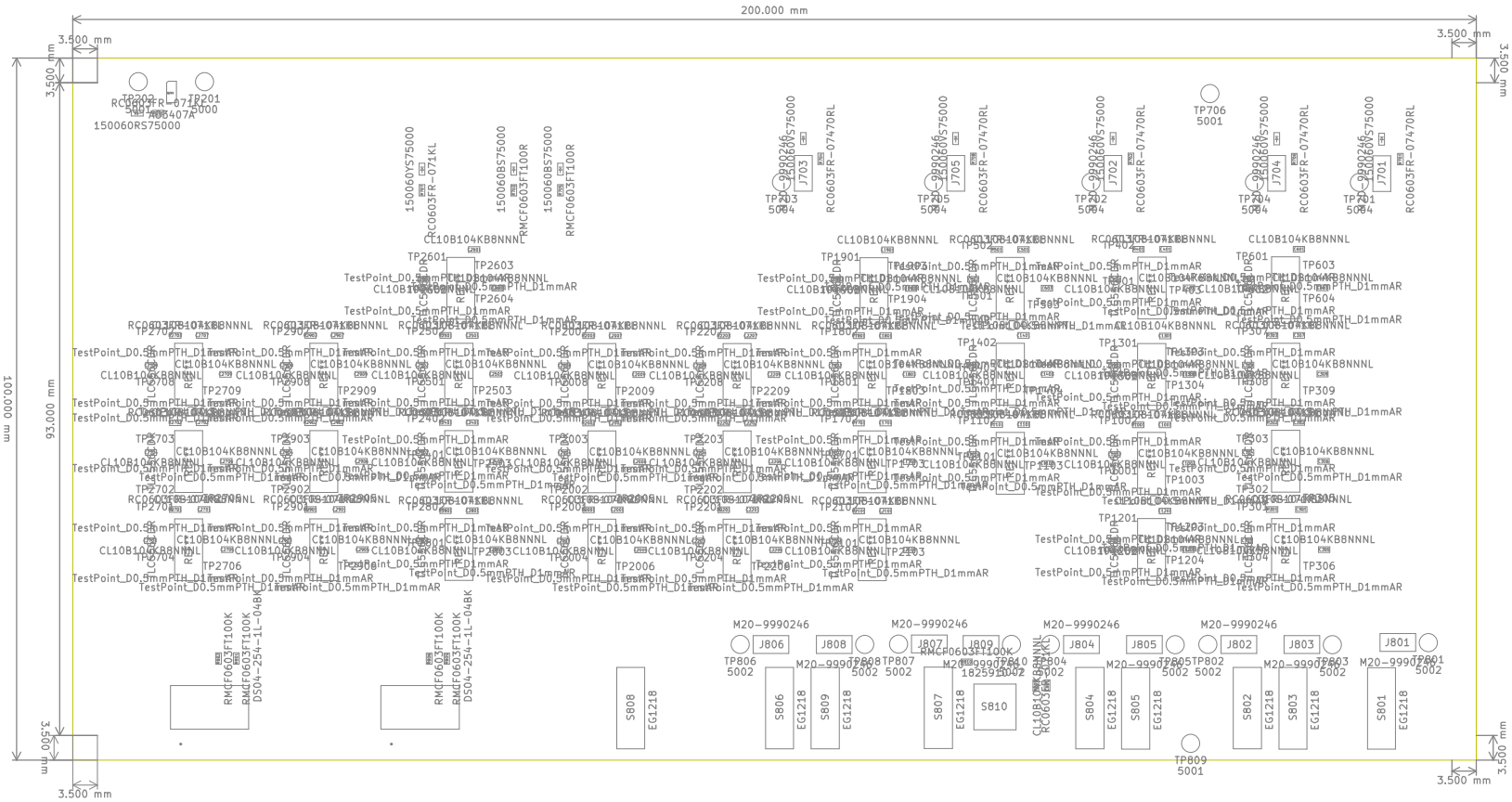

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