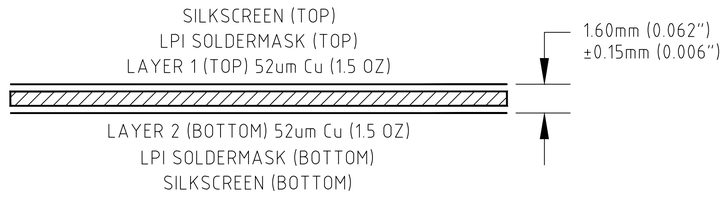
NOTES: UNLESS OTHERWISE SPECIFIED

1. MILLIMETERS (mm) ARE THE CONTROLLING DIMENSIONS FOR THE DRAWINGS AND SUPPLIED DATA. INCH DIMENSIONS ARE FOR REFERENCE ONLY.
2. FABRICATE PCB IN ACCORDANCE WITH IPC-6012A, CLASS 2; PER IPC-6011 USING CUSTOMER SUPPLIED DATA FILES.
3. MATERIALS:
   - A. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/24 OR IPC-4101/26. MATERIAL MUST MEET UL 94V-0 FLAMABILITY RATING.
   - B. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED, ALL COPPER WEIGHT FOR INNER LAYERS TO BE 17um (0.5 OZ) AND FOR OUTER LAYERS 35um (1.0 OZ). COPPER WEIGHT IS TO BE CONSIDERED "FINISHED".
4. ALL HOLES SHALL BE LOCATED WITHIN 0.216 (0.0085") DIAMETER TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.127 (0.005")..
5. FINISH:
   - A. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDERMASK OR OTHER PLATING SHALL BE HOT AIR SOLDER LEVELED (HASL) USING SN63A TIN LEAD SOLDER PER ANSI/J-STD-006.
   - A. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDERMASK OR OTHER PLATING SHALL BE PLATED WITH ORGANIC SURFACE PROTECTANT (OSP).
   - A. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDERMASK OR OTHER PLATING SHALL BE PLATED WITH IMMERSION GOLD OVER ELECTROLYSIS NICKEL (NiAu) OVER COPPER.
   - A. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDERMASK OR OTHER PLATING SHALL BE PLATED WITH IMERSION WHITE TIN (IWT).
   - A. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDERMASK OR OTHER PLATING SHALL BE PLATED WITH IMMERSION SILVER (IAg).
   - B. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES COVERED WITH SOLDERMASK DO NOT NEED TO BE PLUGGED. ONLY SOLDER MASK IMAGES THAT ARE THE SAME SIZE AS THE COMPONENT PADS MAY BE ENLARGED, AND SHALL NOT BE ENLARGED BEYOND 0.08 (.003") PER SIDE OR 0.15 (.006") OVERALL. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED.
   - C. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD.
6. MARKING:
   - A. BOARD PART NUMBER AND REVISION LETTER IS RENDERED IN ETCH ON THE BOTTOM SIDE OF THE BOARD. REVISION LETTER SHOULD BE IDENTICAL TO THIS DRAWING.
   - B. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN ETCH ON THE BOTTOM SIDE OF THE BOARD APPROXIMATELY WHERE SHOWN.
7. TEST REQUIREMENTS:
   - A. 100% NETLIST ELECTRICAL VERIFICATION USING CUSTOMER SUPPLIED IPC-D-356 NETLIST FOR OPENS AND SHORTS. ALL NETS SHALL BE ACCESSED SIMULTANEOUSLY OR AS OTHERWISE MUTUALLY AGREED UPON.
   - B. HIPOT TEST ALL PREPREG/CORE MATERIAL LESS THAN 0.0025 THICK AT 500VDC FOR 30 SECONDS MINIMUM. TEST SHOULD BE DONE AT THE LAYER STAGE AND AGAIN PRIOR TO PACKAGING.
8. TOLERANCES:
   - A. WARP OR TWIST OF BOARD SHALL NOT EXCEED 1%.
   - B. CONDUCTOR WIDTHS AND SPACING SHALL BE WITHIN +/- 0.03 (0.001") OF GERBER DATA.
   - C. REMOVE ALL BURRS AND BREAK SHARP EDGES 0.4 (0.015") MAXIMUM.
   - D. SURFACE MOUNT PAD PLATING MUST BE FLAT TO A MAXIMUM OF 0.08 (0.003") ABOVE BOARD SURFACE.
   - E. 1.5 (0.059") MAXIMUM RADIUS ON ANY INSIDE CORNERS.
   - F. CONTROLLED IMPEDANCE:
     1. 50 OHMS ON OUTER LAYERS. IMPEDANCE STRUCTURE DEFINED AS xxmm STRIPLINE REFERENCED TO LAYERS 2 AND x.
     2. 50 OHMS ON INNER LAYERS. IMPEDANCE STRUCTURE DEFINED AS xxmm MICROSTRIP REFERENCED TO NEAREST PLANE.
9. THIEVING:
   - A. SUPPLIER MAY ADD THIEVING TO COMPENSATE FOR HIGH COPPER DENSITY AREAS ON THIS DESIGN.
   - B. THE FOLLOWING GUIDELINES MUST BE ADHERED TO IN ORDER TO MAINTAIN ELECTRICAL AND MECHANICAL INTEGRITY OF THE DESIGN:
     1. THIEVING TO CARD EDGE SPACING 2.5 (.100") MINIMUM.
     2. THIEVING TO FIDUCIAL SPACING 5.0 (.200") MINIMUM.
     3. THIEVING TO NON-PLATED THROUGH HOLES 5.0 (.200") MINIMUM.
     4. THIEVING TO ALL OTHER FEATURES 0.25 (.100") MINIMUM.
     5. THERE SHALL BE NO EXPOSED THIEVING IN ANY AREA FREE OF SOLDERMASK OR INTERNAL COPPER PLANE.
10. PLATE EDGE CONNECTOR 0.8um (0.000032") MIN. GOLD THICKNESS OVER 2.5um (0.00098") MIN. LOW STRESS NICKEL.
11. LAYER STACKUP DETAIL AS BELOW.

2 LAYER STACKUP (02A)



12. DRILL TOLERANCES AS BELOW.

DRILL TOLERANCE CHART

SIZE RANGE (FINISHED)	PLATED (PLTD)	NONPLATED (NPLTD)
LESS THAN 0.25 (0.010")	±0.06 (±0.002")	N/A
0.25 - 2.5 (0.010" - 0.100")	±0.08 (±0.003")	±0.06 (±0.002")
GREATER THAN 2.5 (0.100")	±0.10 (±0.004")	±0.08 (±0.003")
ALL SLOTS	±0.12 (±0.005")	±0.10 (±0.004")

REV.	DATE	DRAWN BY	CHECKED BY	DESCRIPTION
00	20200327	BERT TIMMERMAN		FIRST ISSUE

AUTOCAD 2015

REVISION: 00 20200327	SCALE: -	DRAWN: BERT TIMMERMAN	OPEN SOURCE HARDWARE
	DIMENSIONS: mm	DEPT.: ELECTRONICS	COPYRIGHT (C)
	DATE: 20200327	CHECKED:	CC BY-SA 4.0

DESCRIPTION:
POWER SUPPLY UNIT
MAIN PCB FABRICATION NOTES

NUMBER: 31.003.00 .02.01 1 OF 1

FORM.: A3