Migrating from Philips: P89C51RB2, P89C51RC2, P89C51RD2, P89C660, P89C662, P89C664 To Atmel: AT89C51RB2, AT89C51RC2, AT89C51IC2, AT89C51RD2, AT89C51ED2, AT89C51ID2

8051 Microcontrollers

Application Note

1. Introduction

This application note is a guide to help current Philips® P89C51RB2/RC2/RD2/C660/C662/C664 users convert existing designs to Atmel® AT89C51RB2/RB2/RC2/IC2/RD2/1ED2/ID2. Check the datasheets of these products for detailed information.

7605A–8051–04/06

2. Features

The table below summarizes the main feature of these C51 microcontrollers:

	Memory					Timer					Serial interface										
	FLASH	RAM	BOOT (R: ROM F: Flash)	EEPROM	VP (Prog. Supply Voltage)	# of 8-bit	# of 16-bit	PWM	PCA (16-bits Timer)	WD	UART	I2C / TWI	SPI	ADC bits / ch	I/O Pins	Interrupt (Ext)	Power Supply	DC Freq. at 6/12 MHz/clk	Freq. Range @ 3V (MHz)	Freq. Range @ 5V (MHz)
Atmel																				
AT89C51RB2	16KB	1.25KB	R 2KB	-	N	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	1	-	32	9(2)4	I : 2.7V-3.6V I : 2.7V-5.5V	30/60	20-40	30-60
AT89C51RC2	32KB	1.25KB	R 2KB	-	N	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	1	-	32	9(2)4	I : 2.7V-3.6V I : 2.7V-5.5V	30/60	20-40	30-60
AT89C51IC2	32KB	1.25KB	R 2KB	-	N	T0/T1	T2	5 * 8-bits	5 ch.	1	1	1	1	-	32	9(2)4	I : 2.7V-3.6V I : 2.7V-5.5V	30/60	20-40	30-60
AT89C51RD2	64KB	2KB	R 2KB	-	N	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	1	-	34/50	9(2)4	I : 2.7V-5.5V	30/60	20-40	30-60
AT89C51ED2	64KB	2KB	R 2KB	2KB	N	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	1	-	34/50	9(2)4	I : 2.7V-5.5V	30/60	20-40	30-60
AT89C51ID2	64KB	2KB	R 2KB	2KB	N	T0/T1	T2	5 * 8-bits	5 ch.	1	1	1	1	-	34	9(2)4	I : 2.7V-5.5V	30/60	20-40	30-60
AT89C51AC3	64KB	2.2KB	F 2KB	2KB	N	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	1	10/8	34	9(2)4	I : 3V-5.5V I : 4.5V-5.5V	30/60	20-40	30-60
Philips																				
P89C51RB2	16KB	512B	R 1KB	-	Y	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	-	-	32	7(2)4	C : 4.5-5.5V	20/33	-	0-20/33
P89C51RC2	32KB	512B	R 1KB	-	Y	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	-	-	32	7(2)4	C : 4.5-5.5V I : 4.75-5.25V	20/33	-	0-20/33
P89C51RD2	64KB	1KB	R 1KB	-	Y	T0/T1	T2	5 * 8-bits	5 ch.	1	1	-	-	-	32	7(2)4	C : 4.5-5.5V	20/33	-	0-20/33
P89C660	16KB	512B	R 1KB	-	Y	T0/T1	T2	5 * 8-bits	5 ch.	1	1	1	-	-	32	8(2)/4	C : 4.5-5.5V I : 4.75-5.25V	20/33	-	0-20/33
P89C662	32KB	1KB	R 1KB	-	Y	T0/T1	T2	5 * 8-bits	5 ch.	1	1	1	-	-	32	8(2)/4	C : 4.5-5.5V I : 4.75-5.25V	20/33	-	0-20/33
P89C664	64KB	2KB	R 1KB	-	Y	T0/T1	T2	5 * 8-bits	5 ch.	1	1	1	-	-	32	8(2)/4	C : 4.5-5.5V I : 4.75-5.25V	20/33	-	0-20/33
P89C668	64KB	8KB	R 1KB	-	Y	T0/T1	T2	5 * 8-bits	5 ch.	1	1	1	-	-	32	8(2)/4	C : 4.5-5.5V I : 4.75-5.25V	20/33	-	0-20/33

C : 0 to +70°C
I : -40 to +85°C
PCA : Programmable Counter Array

3. Packaging

Product	PDIL40	PLCC44	QFP44	VQFP64	PLCC68
AT89C51RB2	X	X	X		
AT89C51RC2	X	X	X		
AT89C51IC2		X	X		
AT89C51RD2	X	X	X	X	X
AT89C51ED2	X	X	X	X	X
AT89C51ID2		X	X		
P89C51RB2	X	X	X		
P89C51RC2	X	X	X		
P89C51RD2	X	X	X		
P89C660		X	X		
P89C662		X	X		
P89C664		X	X		

4. Temperature Range

Product	Commercial (0°C / +70°C)	Industrial (-40°C / +85°C)
AT89C51RB2	X	X
AT89C51RC2	X	X
AT89C51IC2	X	X
AT89C51RD2	-	X
AT89C51ED2	-	X
AT89C51ID2	-	X
P89C51RB2	X	-
P89C51RC2	X	X
P89C51RD2	X	-
P89C660	X	X
P89C662	X	X
P89C664	X	X

5. Frequency Range

Frequency	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2
X1 mode	Up to 33MHz	Up to 33MHz	Up to 60MHz	Up to 60MHz	Up to 60MHz	Up to 60MHz
X2 mode	Up to 20MHz	Up to 20MHz	Up to 30MHz	Up to 30MHz	Up to 30MHz	Up to 30MHz

6. Pinning Configuration (on identical packages)

	PDIL40		PLCC44		VQFP44	
	PHILIPS	ATMEL	PHILIPS	ATMEL	PHILIPS	ATMEL
Vss	20	20	22	22	16	16
Vcc	40	40	44	44	38	38
P0.0 – P0.7	32 - 39	32 - 39	43 - 36	43 - 36	37 - 30	37 - 30
P1.0 – P1.7	1 - 8	1 - 8	2 - 9	2 - 9	40 – 44 1 - 3	40 – 44 1 - 3
PI2.0 – PI2.1	NC	NC	NC	IC2 & ID2 34-12	NC	IC2 & ID2 28-6
XTALA1	19	19	21	21	15	15
XTALA2	18	18	20	20	14	14
P2.0 – P2.7	21 – 28	21 – 28	24 - 31	24 - 31	18 - 25	18 - 25
P3.0 – P3 .7	10 - 17	10 - 17	11, 13 - 19	11, 13 - 19	5, 7 - 13	5, 7 - 13
RST	9	9	10	10	4	4
ALE	30	30	33	33	27	27
PSEN	29	29	32	32	26	26
EA	31	31	35	35	29	29

6.1 Pin Out Identical between Philips & Atmel Except:

	Pin 3.1	Pin 3.0
PHILIPS	$\overline{EA}$ / VPP	ALE
ATMEL	EA	ALE / $\overline{Prog}$

7. Alternate Function

Find below the alternate function table and the different place of them:

		P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2
	P1.0	T2	T2	T2	T2 / XTALB1	T2	T2 / XTALB1
	P1.1	T2EX	T2EX	T2EX / SS/	T2EX / SS/	T2EX / SS/	T2EX / SS/
	P1.2	ECI	ECI	ECI	ECI	ECI	ECI
	P1.3	CEX0	CEX0	CEX0	CEX0	CEX0	CEX0
	P1.4	CEX1	CEX1	CEX1	CEX1	CEX1	CEX1
	P1.5	CEX2	CEX2	CEX2 / MISO	CEX2 / MISO	CEX2 / MISO	CEX2 / MISO
	P1.6	CEX3	SCL	CEX3 / SCK	CEX3 / SCK	CEX3 / SCK	CEX3 / SCK
P1.0 – P1.7	P1.7	CEX4	SDA	CEX4 / MOSI	CEX4 / MOSI	CEX4 / MOSI	CEX4 / MOSI
	P3.0	RxD	RxD	RxD	RxD	RxD	RxD
	P3.1	TxD	TxD	TxD	TxD	TxD	TxD
	P3.2	INT0	INT0	INT0	INT0	INT0	INT0
	P3.3	INT1	INT1	INT1	INT1	INT1	INT1
	P3.4	T0	CEX3/T0	T0	T0	T0	T0
	P3.5	T1	CEX4/T1	T1	T1	T1	T1
	P3.6	WR/	WR/	WR/	WR/	WR/	WR/
P3.0 – P3.7	P3.7	RD/	RD/	RD/	RD/	RD/	RD/
	PI2.0	-	-	-	SCL	-	SCL
PI2.0 – PI2.1	PI2.1	-	-	-	SDA	-	SDA

T2 = Timer/Counter 2 external count input/Clock out

T2EX = Timer/Counter 2 Reload/Capture/Direction Control

ECI = External Clock Input to the PCA

SS/ = SPI Slave Select

CEX* = Capture compare External I/O for PCA module*

SCL = I2C bus clock line (open drain)

SDA = I2C bus data line (open drain)

MISO = SPI Master Input Slave Output line

SCK = SPI Serial Clock

MOSI = SPI Master Output Slave Input line

XTALB1 = Sub Clock input to the inverting oscillator amplifier

8. SFR Mapping

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
80	P0 1111 1111	P0 1111 1111	P0 1111 1111	P0 1111 1111	P0 1111 1111	P0 1111 1111
81	SP 0000 0111	SP 0000 0111	SP 0000 0111	SP 0000 0111	SP 0000 0111	SP 0000 0111
82	DPL 0000 0000	DPL 0000 0000	DPL 0000 0000	DPL 0000 0000	DPL 0000 0000	DPL 0000 0000
83	DPH 0000 0000	DPH 0000 0000	DPH 0000 0000	DPH 0000 0000	DPH 0000 0000	DPH 0000 0000
84						
85		Reserved		Reserved		
86		Reserved		Reserved		
87	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000
88	TCON 0000 0000	TCON 0000 0000	TCON 0000 0000	TCON 0000 0000	TCON 0000 0000	TCON 0000 0000
89	TMOD 0000 0000	TMOD 0000 0000	TMOD 0000 0000	TMOD 0000 0000	TMOD 0000 0000	TMOD 0000 0000
8A	TL0 0000 0000	TL0 0000 0000	TL0 0000 0000	TL0 0000 0000	TL0 0000 0000	TL0 0000 0000
8B	TL1 0000 0000	TL1 0000 0000	TL1 0000 0000	TL1 0000 0000	TL1 0000 0000	TL1 0000 0000
8C	TH0 0000 0000	TH0 0000 0000	TH0 0000 0000	TH0 0000 0000	TH0 0000 0000	TH0 0000 0000
8D	TH1 0000 0000	TH1 0000 0000	TH1 0000 0000	TH1 0000 0000	TH1 0000 0000	TH1 0000 0000
8E	AUXR Xx0x 0000	AUXR Xx0x 0000	AUXR Xx0x 0000	AUXR Xx0x 0000	AUXR Xx0x 0000	AUXR Xx0x 0000
8F	CKCON0 0000 0000	CKCON0 0000 0000	CKCON0 0000 0000	CKCON0 0000 0000		
90	P1 1111 1111	P1 1111 1111	P1 1111 1111	P1 1111 1111	P1 1111 1111	P1 1111 1111
91						
92						
93		SSCON 0000 0000		SSCON 0000 0000		

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
94		SSCS 1111 1000		SSCS 1111 1000		
95		SSDAT 1111 1111		SSDAT 1111 1111		
96		SSADR 1111 1110		SSADR 1111 1110		
97	CKRL 1111 1111	CKRL 1111 1111	CKRL 1111 1111	CKRL 1111 1111		
98	SCON 0000 0000	SCON 0000 0000	SCON 0000 0000	SCON 0000 0000	SCON 0000 0000	S0CON 0000 0000
99	SBUF Xxxx xxxx	SBUF Xxxx xxxx	SBUF Xxxx xxxx	SBUF Xxxx xxxx	SBUF Xxxx xxxx	S0BUF Xxxx xxxx
9A	BRL Xxxx xxxx	BRL Xxxx xxxx	BRL Xxxx xxxx	BRL Xxxx xxxx		
9B	BDRCON Xxx0 0000	BDRCON Xxx0 0000	BDRCON Xxx0 0000	BDRCON Xxx0 0000		
9C	Reserved	Reserved	Reserved	Reserved		
9D	Reserved	Reserved	Reserved	Reserved		
9E	Reserved	Reserved	Reserved	Reserved		
9F						
A0	P2 1111 1111	P2 1111 1111	P2 1111 1111	P2 1111 1111	P2 1111 1111	P2 1111 1111
A1						
A2	AUXR1 xxxx x0x0	AUXR1 xxxx x0x0	AUXR1 xxxx x0x0	AUXR1 xxxx x0x0	AUXR1 xxxx x0x0	AUXR1 xxxx x0x0
A3						
A4						
A5						
A6	WDTRST xxxx xxxx	WDTRST xxxx xxxx	WDTRST xxxx xxxx	WDTRST xxxx xxxx	WDTRST xxxx xxxx	WDTRST xxxx xxxx
A7	WDTPRG xxxx x000	WDTPRG xxxx x000	WDTPRG xxxx x000	WDTPRG xxxx x000		
A8	IEN0 0000 0000	IEN0 0000 0000	IEN0 0000 0000	IEN0 0000 0000	IE 0000 0000	IEN0 0000 0000

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
A9	SADDR 0000 0000	SADDR 0000 0000	SADDR 0000 0000	SADDR 0000 0000	SADDR 0000 0000	SADDR 0000 0000
AA						
AB						
AC						
AD						
AE						
AF	CKCON1 xxxx xxx0	CKCON1 xxxx xxx0	CKCON1 xxxx xxx0	CKCON1 xxxx xxx0		
B0	P3 1111 1111	P3 1111 1111	P3 1111 1111	P3 1111 1111	P3 1111 1111	P3 1111 1111
B1	IEN1 xxxx x000	IEN1 xxxx x000	IEN1 xxxx x000	IEN1 xxxx x000		
B2	IPL1 xxxx x000	IPL1 xxxx x000	IPL1 xxxx x000	IPL1 xxxx x000		
B3	IPH1 xxxx x000	IPH1 xxxx x000	IPH1 xxxx x000	IPH1 xxxx x000		
B4						
B5						
B6						
B7	IPH0 x000 0000	IPH0 x000 0000	IPH0 x000 0000	IPH0 x000 0000	IPH x000 0000	IPH x000 0000
B8	IPL0 X000 0000	IPL0 X000 0000	IPL0 X000 0000	IPL0 X000 0000	IP X000 0000	IP X000 0000
B9	SADEN 0000 0000	SADEN 0000 0000	SADEN 0000 0000	SADEN 0000 0000	SADEN 0000 0000	SADEN 0000 0000
BA						
BB						
BC						
BD						

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
BE						
BF						
C0		PI2 bit addressable xxxx xx11	Reserved	Reserved		CCON 0000 0000
C1						CMOD 0000 0000
C2						CCAPM0 0000 0000
C3	Reserved	Reserved	Reserved	Reserved		CCAPM1 0000 0000
C4	Reserved	Reserved	Reserved	Reserved		CCAPM2 0000 0000
C5	Reserved	Reserved	Reserved	Reserved		CCAPM3 0000 0000
C6						CCAPM4 0000 0000
C7			Reserved	Reserved		
C8	T2CON 0000 0000	T2CON 0000 0000	T2CON 0000 0000	T2CON 0000 0000	T2CON 0000 0000	T2CON 0000 0000
C9	T2MOD xxxx xx00	T2MOD xxxx xx00	T2MOD xxxx xx00	T2MOD xxxx xx00	T2MOD xxxx xx00	T2MOD xxxx xx00
CA	RCAP2L 0000 0000	RCAP2L 0000 0000	RCAP2L 0000 0000	RCAP2L 0000 0000	RCAP2L 0000 0000	RCAP2L 0000 0000
CB	RCAP2H 0000 0000	RCAP2H 0000 0000	RCAP2H 0000 0000	RCAP2H 0000 0000	RCAP2H 0000 0000	RCAP2H 0000 0000
CC	TL2 0000 0000	TL2 0000 0000	TL2 0000 0000	TL2 0000 0000	TL2 0000 0000	TL2 0000 0000
CD	TH2 0000 0000	TH2 0000 0000	TH2 0000 0000	TH2 0000 0000	TH2 0000 0000	TH2 0000 0000
CE						
CF						
D0	PSW 0000 0000	PSW 0000 0000	PSW 0000 0000	PSW 0000 0000	PSW 0000 0000	PSW 0000 0000
D1	FCON(1) xxxx 0000	FCON(1) xxxx 0000	FCON(1) xxxx 0000	FCON(1) xxxx 0000		

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
D2			EECON Xxxx xx00	EECON Xxxx xx00		
D3						
D4						
D5						
D6						
D7						
D8	CCON 00x0 0000	CCON 00x0 0000	CCON 00x0 0000	CCON 00x0 0000	CCON 00x0 0000	S1SCON 0000 0000
D9	CMOD 00xx x000	CMOD 00xx x000	CMOD 00xx x000	CMOD 00xx x000	CMOD 00xx x000	S1STA 1111 1000
DA	CCAPM0 x000 0000	CCAPM0 x000 0000	CCAPM0 x000 0000	CCAPM0 x000 0000	CCAPM0 x000 0000	S1DAT 0000 0000
DB	CCAPM1 x000 0000	CCAPM1 x000 0000	CCAPM1 x000 0000	CCAPM1 x000 0000	CCAPM1 x000 0000	S1ADR 0000 0000
DC	CCAPM2 x000 0000	CCAPM2 x000 0000	CCAPM2 x000 0000	CCAPM2 x000 0000	CCAPM2 x000 0000	
DD	CCAPM3 x000 0000	CCAPM3 x000 0000	CCAPM3 x000 0000	CCAPM3 x000 0000	CCAPM3 x000 0000	
DE	CCAPM4 x000 0000	CCAPM4 x000 0000	CCAPM4 x000 0000	CCAPM4 x000 0000	CCAPM4 x000 0000	
DF						
E0	ACC 0000 0000	ACC 0000 0000	ACC 0000 0000	ACC 0000 0000	ACC 0000 0000	ACC 0000 0000
E1						
E2						
E3						
E4						
E5						
E6						

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
E7						
E8			Reserved	Reserved		IEN1 0000 0000
E9	CL 0000 0000	CL 0000 0000	CL 0000 0000	CL 0000 0000	CL 0000 0000	CL 0000 0000
EA	CCAP0L xxxx	CCAP0L xxxx	CCAP0L xxxx	CCAP0L xxxx	CCAP0L xxxx	CCAP0L xxxx
EB	CCAP1L xxxx	CCAP1L xxxx	CCAP1L xxxx	CCAP1L xxxx	CCAP1L xxxx	CCAP1L xxxx
EC	CCAPL2L xxxx	CCAPL2L xxxx	CCAPL2L xxxx	CCAPL2L xxxx	CCAPL2L xxxx	CCAPL2L xxxx
ED	CCAPL3L xxxx	CCAPL3L xxxx	CCAPL3L xxxx	CCAPL3L xxxx	CCAPL3L xxxx	CCAPL3L xxxx
EE	CCAPL4L xxxx	CCAPL4L xxxx	CCAPL4L xxxx	CCAPL4L xxxx	CCAPL4L xxxx	CCAPL4L xxxx
EF						
F0	B 0000 0000	B 0000 0000	B 0000 0000	B 0000 0000	B 0000 0000	B 0000 0000
F1						
F2						
F3						
F4						
F5						
F6						
F7						
F8			PI2 Xxxx xx11	PI2 Xxxx xx11		
F9	CH 0000 0000	CH 0000 0000	CH 0000 0000	CH 0000 0000	CH 0000 0000	CH 0000 0000
FA	CCAP0H xxxx	CCAP0H xxxx	CCAP0H xxxx	CCAP0H xxxx	CCAP0H xxxx	CCAP0H xxxx
FB	CCAP1H xxxx	CCAP1H xxxx	CCAP1H xxxx	CCAP1H xxxx	CCAP1H xxxx	CCAP1H xxxx

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
FC	CCAPL2H xxxx	CCAPL2H xxxx	CCAP2H xxxx	CCAP2H xxxx	CCAP2H xxxx	CCAP2H xxxx
FD	CCAPL3H xxxx	CCAPL3H xxxx	CCAP3H xxxx	CCAP3H xxxx	CCAP3H xxxx	CCAP3H xxxx
FE	CCAPL4H xxxx	CCAPL4H xxxx	CCAP4H xxxx	CCAP4H xxxx	CCAP4H xxxx	CCAP4H xxxx
FF						

9. Oscillators

In order to optimise the power consumption and the execution time needed for a specific task, an internal prescaler feature has been implemented between the selected oscillator and the CPU. This prescaler is only available on the Atmel microcontroller and is manage with the CKRL register.

Table 9-1. Oscillator SFR mapping

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
87	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000	PCON 00x1 0000
97	CKRL 1111 1111	CKRL 1111 1111	CKRL 1111 1111	CKRL 1111 1111		

PCON @87h is on all the microcontroller

CKRL is available on Atmel microcontroller only and offer the possibility to adjust prescaler divider and then adjust the Peripheral and CPU clock.

Table 9-2. CKRL Register

CKRL – Clock Reload Register (97h)

7	6	5	4	3	2	1	0
CKRL7	**CKRL6**	**CKRL5**	**CKRL4**	**CKRL3**	**CKRL2**	**CKRL1**	**CKRL0**

Bit Number	Mnemonic	Description
7:0	CKRL	Clock Reload Register Prescaler Value

Reset Value = 1111 1111b

Figure 9-1. AT89C51RB2, AT89C51RC2, AT89C51RD2, AT89C51ED2 Functional Oscillator Block Diagram

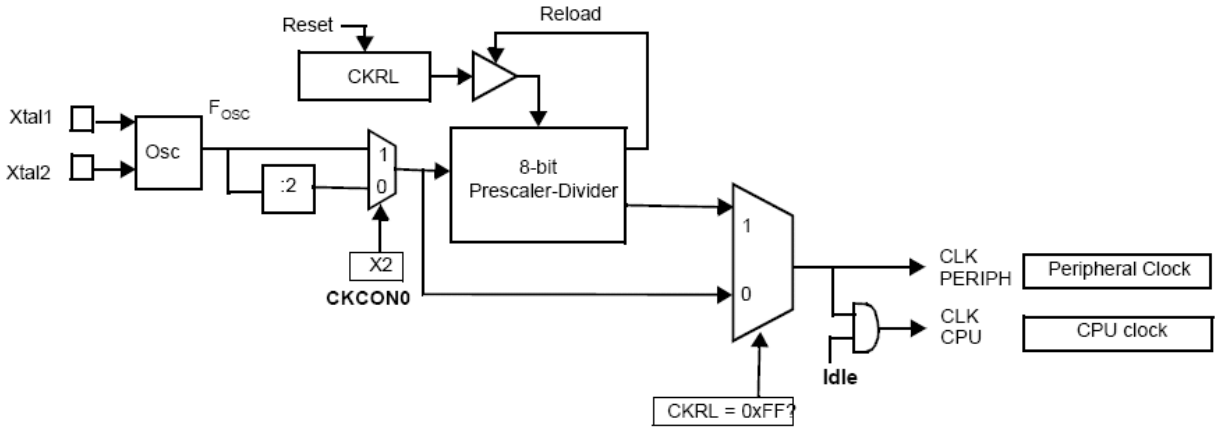
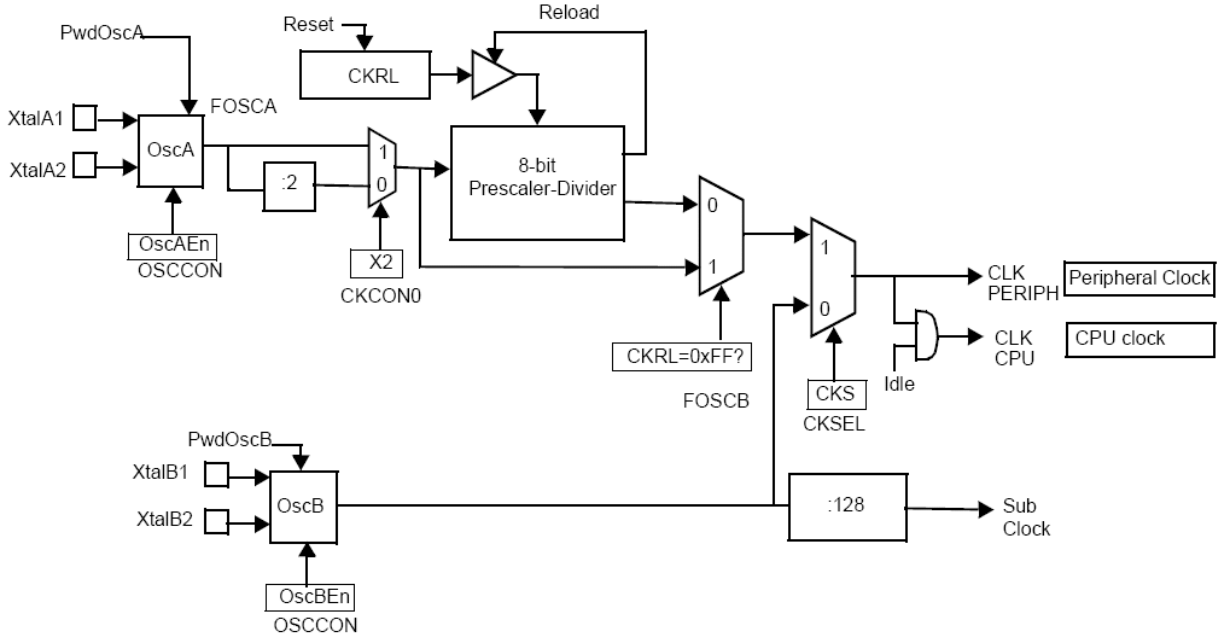


Figure 9-2. AT89C51IC2, AT89C51ID2 Functional Oscillator Block Diagram



10. Enhanced Features - X2 Features

The ***AT89C51RB2/RC2/IC2RD2/ED2/ID2*** core needs only 6 clock periods per machine cycle.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software. **It easily possible to change from X1 to X2 and X2 to X1 with bit X2 of CKCON0 register .**

P89C51RB2/RC2/RD2 and the ***P89C51C660/662/664*** device are configured at the factory to operate using 6 clock periods per machine cycle, referred to in this datasheet as “6 clock mode”. It may be optionally configured on commercially-available EPROM programming equipment to operate at 12 clock periods per machine cycle, referred to in this datasheet as “12 clock mode”. **Once 12 clock mode has been configured, it cannot be changed back to 6 clock mode**.

Address (h)	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
8F	CKCON0 0000 0000	CKCON0 0000 0000	CKCON0 0000 0000	CKCON0 0000 0000		
AF	CKCON1 xxxx xxx0	CKCON1 xxxx xxx0	CKCON1 xxxx xxx0	CKCON1 xxxx xxx0		

Table 10-1. CKCON0 Register

CKCON0 – Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Bit Number	Mnemonic	Description
7	-	
6	WDX2	Watchdog Clock (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bithas no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PCAX2	Programmable Counter Array Clock (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bithas no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clockperiods per peripheral clock cycle.
4	SIX2	Enhanced UART Clock (Mode 0 and 2) (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.

Bit Number	Mnemonic	Description
3	T2X2	Timer 2 Clock (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	T1X2	Timer 1 Clock (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
1	T0X2	Timer0 Clock (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
0	X2	CPU Clock Cleared to select 12 clock periods per machine cycle (STD, X1 mode) for CPU and all the peripherals. Set to select 6 clock periods per machine cycle (X2 mode) and to enable the individual peripherals'X2' bits. Programmed by hardware after Power-up regarding Hardware Security Byte (HSB), Default setting, X2 is cleared.

Reset Value = 0000 000'HSB. X2'b

Not bit addressable

Table 10-2. CKCON1 Register

CKCON1 – Clock Control Register (AFh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**SPIX2**

Bit Number	Mnemonic	Description
7	-	
6	-	
5	-	
4	-	
3	-	
2	-	
1	-	
0	SPIX2	**SPI** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.

11. Dual Data Pointer Register (DPTR)

The additional data pointer can be used to speed up code execution and reduce code size.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1.0 that allows the program code to switch between them (see Figure XXDDP).

Figure 11-1. DDP. Use of Dual Data Pointer

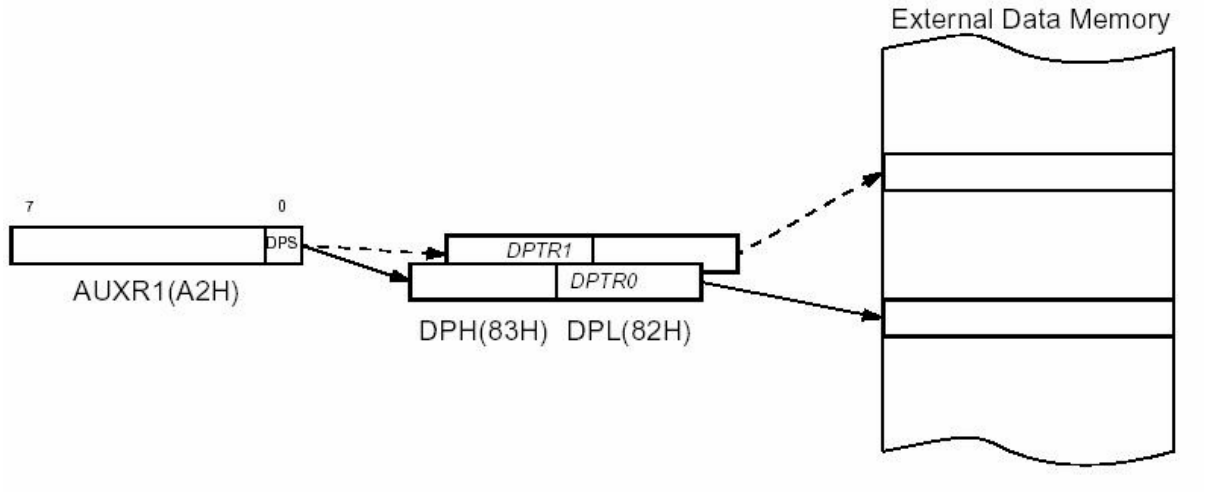


Table 11-1. AUXR1 Register

AUXR1 – Auxiliary Register (A2h)

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF2 (1) GF3 (2)	0	-	DPS (3)

Bit Number	Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	ENBOOT	Enable Boot Flash Cleared to disable boot ROM. Set to map the boot ROM between F800h - 0FFFFh.
4	-	
3	GF2 (1) GF3 (2)	The GF2 bit is a general purpose user-defined flag This bit is a general-purpose user flag
2	0	Always Cleared
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	DPS (3)	Data Pointer Selection Cleared to select DPTR0. Set to select DPTR1.

Reset Value = XXXX XX0X0b

Not bit addressable

(1) on P89C51RB2/RC2/RD2 and P89C51C660/662/664

(2) on AT89C51RB2/RC2/IC2/RD2/ED2/ID2

(3) The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

12. Expended RAM (XRAM)

The Philips and Atmel microcontroller provides additional bytes of random access memory (RAM)

space for increased data parameter handling and high-level language usage.

Figure 12-1. Internal and External Data Memory Address Space with EXTRAM = 0 on Atmel devices

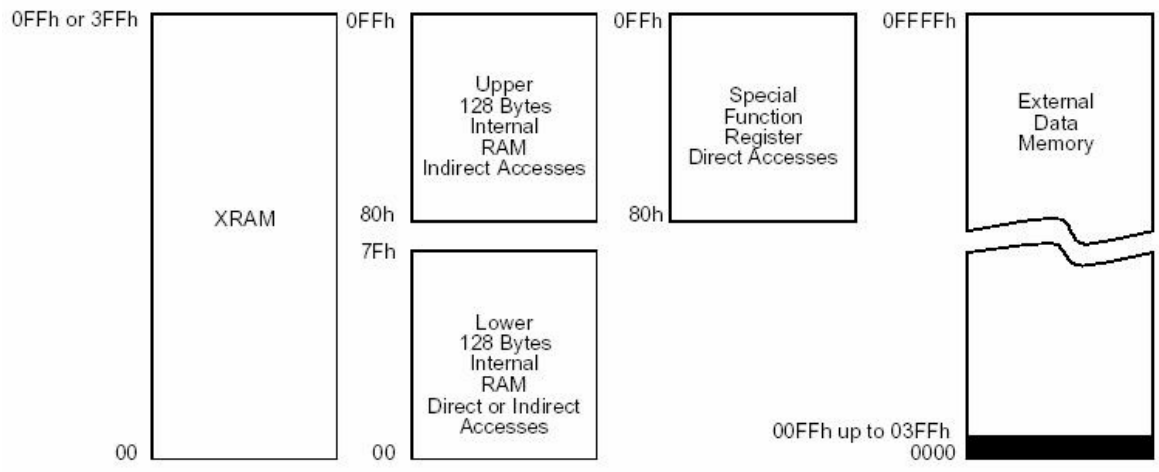


Figure 12-2. Internal and External Data Memory Address Space with EXTRAM = 0 on Philips devices

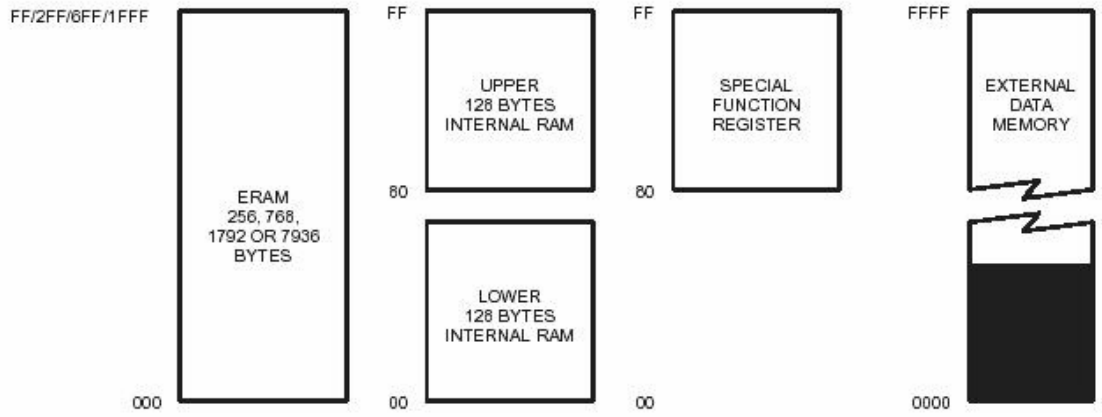


Table 12-1. AUXR Register

AUXR – Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
DPU (1)	**-**	**M0 (1)**	**-**	**XRS1 (1)**	**XRS0 (1)**	**EXTRAM**	**AO**

Bit Number	Mnemonic	Description
7	DPU (1)	Disable Weak Pull-up Cleared to activate the permanent weak pull up when latch data is logical 1 Set to disactive the weak pull-up (reduce power consumption)
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	M0 (1)	Pulse Length Cleared to stretch MOVX control: the RD and the WR pulse length is 6 clock periods (default). Set to stretch MOVX control: the RD and the WR pulse length is 30 clock periods.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	XRS1 (1)	XRAM Size XRS1 XRS0 XRAM size 0 0 256 Bytes (default) 0 1 512 Bytes 1 0 768 Bytes 1 1 1024 Bytes
2	XRS0 (1)	
1	EXTRAM	EXTRAM Bit Cleared to access internal XRAM using movx @ Ri/ @ DPTR. Set to access external memory
0	AO	ALE Output Bit Cleared, ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used). (default) Set, ALE is active only during a MOVX or MOVC instruction is used.

(1) Only on AT89C51RB2/RC2/IC2/RD2/ED2/ID2, note available on P89C51RB2/RC2/RD2 and P89C51C660/662/664

13. Programmable Counter Array (PCA)

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy.

The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Its clock input can be programmed to count any one of the following signals:

Find below the PCA mapping address, only Philips P89C660/P89C662/P89C664 have some register without the same address.

SFR with same address and same function

CL @ E9h PCA Counter Low

CH @ F9h PCA Counter High

CCAP0L@ EAh Module 0 Capture Low
CCAP1L@ EBh Module 1 Capture Low
CCAP2L@ ECh Module 2 Capture Low
CCAP3L@ EDh Module 3 Capture Low
CCAP4L@ EEh Module 4 Capture Low

CCAP0H@ FAh Module 0 Capture High

CCAP1H@ FBh Module 1Capture High
CCAP2H@ FCh Module 2 Capture High
CCAP3H@ FDh Module 3 Capture High
CCAP4H@ FEh Module 4 Capture High

Warning on the SFR address register below

Mnemonic	AT89C51RB2 AT89C51RC2	AT89C51IC2	AT89C51RD2 AT89C51ED2	AT89C51ID2	P89C51RB2 P89C51RC2 P89C51RD2	P89C660 P89C662 P89C664
CCON 00x0 0000	D8h	D8h	D8h	D8h	D8h	C0h
CMOD 00xx x000	D9h	D9h	D9h	D9h	D9h	C1h
CCAPM0 x000 0000	DAh	DAh	DAh	DAh	DAh	C2h
CCAPM1 x000 0000	DBh	DBh	DBh	DBh	DBh	C3h
CCAPM2 x000 0000	DCh	DCh	DCh	DCh	DCh	C4h
CCAPM3 x000 0000	DDh	DDh	DDh	DDh	DDh	C5h
CCAPM4 x000 0000	DEh	DEh	DEh	DEh	DEh	C6h

13.1 PCA High Speed Output Mode

	Part Number	Reference	Document Reference
Philips	P89C51 RB2/RC2/RD2	refer to figure 23	Datasheet 2002 May, 20
	P89C51 C660/662/664	refer to figure 49	Datasheet 2002 Oct, 28
Atmel	AT89C51RB2/RC2	refer to page 41 figure 15	doc 4180D - 06/05
	AT89C51IC2	refer to page 45 figure 15	doc 4301B - 01/06
	AT89C51RD2/ED2	refer to page 20 figure 20	doc 4235G - 08/05
	AT89C51ID2	refer to page 50 figure 18	doc 4289C - 11/05

14. I2C / TWI

The 2-wire bus is a bi-directional 2-wire serial communication standard. It is designed primarily for simple but efficient integrated circuit (IC) control. The system is comprised of two lines, SCL (Serial Clock) and SDA (Serial Data) that carry information between the ICs connected to them. The serial data transfer is limited to 400 Kbit/s in standard mode. Various communication configuration can be designed using this bus. All the devices connected to the bus can be master and slave.

The Philips I2C bus as the Atmel TWI (Two Wire Interface) uses two wires SDA and SCL to transfer information between devices connected to the bus. The I2C and TWI are fully compatible.

The main features of the bus are:

- Bi-directional data transfer between masters and slaves
- Multimaster bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I2C/TWI bus may be used for test and diagnostic purposes

This bus is available on the Philips P89C660/662/664 and on the Atmel AT89C51IC2/ID2.

The pinning configuration is quite different. Refer to the table below in order to use the right pin out :

Table 14-1. Pin configuration

	P89C660/662/664		AT89C51IC2/ID2	
	PLCC44	QFP44	PLCC44	QFP44
SCL	P1.6 / Pin 8	P1.6 / Pin 2	PI2.0 / Pin 34	PI2.0 / 28
SDA	P1.7 / Pin 9	P1.7 / Pin 3	PI2.1 / Pin 12	PI2.1 / 6

The SFR mapping address are quite different and must be updated when you need to migrate from P89C660 to AT89C51IC2, AT89C51ID2 as show below:

Table 14-2. SFR Mapping

Mnemonic	AT89C51IC2 AT89C51ID2	P89C660 P89C662 P89C664	Name
SSCON S1CON	93h	D8h	Synchronous Serial control
SSCS S1STA	94h	D9h	Synchronous Serial Status
SSDAT S1DAT	95h	DAh	Synchronous Serial Data
SSADR S1ADR	96h	DBh	Synchronous Serial Address

Table 14-3. Synchronous Serial control Register description

		7	6	5	4	3	2	1	0
Atmel	**SSCON**		**SSIE**						
Philips	**S1CON**	**CR2**	**ENS1**	**STA**	**STO**	**SI**	**AA**	**CR1**	**CR0**

Bit Number	Mnemonic	Description
7	CR2	Control Rate bit 2
6	SSIE ENS1	Synchronous Serial Interface Enable bit Clear to disable the TWI module. Set to enable the TWI module.
5	STA	Start flag Set to send a START condition on the bus.
4	STO	Stop flag Set to send a STOP condition on the bus.
3	SI	Synchronous Serial Interrupt flag Set by hardware when a serial interrupt is requested. Must be cleared by software to acknowledge interrupt.
2	AA	Assert Acknowledge flag Clear in master and slave receiver modes, to force a not acknowledge (high level on SDA). Clear to disable SLA or GCA recognition. Set to recognise SLA or GCA (if GC set) for entering slave receiver or transmitter modes. Set in master and slave receiver modes, to force an acknowledge (low level on SDA). This bit has no effect when in master transmitter mode.
1	CR1	Control Rate bit 1
0	CR0	Control Rate bit 0

15. Watchdog Timer

15.1 Introduction

Philips P89C51RB2/P89C51RC2/P89C51RD2 as well as P89C660/P89C662/P89C664 feature a watchdog timer with Reset Output. Atmel AT89C51RB2/AT89C51RC2/AT89C51RD2 have a watchdog timer with Reset Out fully compatible with Philips controllers. Atmel added a programmable prescaller between the CPU clock and the watchdog timer to further extend the timeout period of the watchdog. Atmel controllers default into a Philips compatible mode.

15.2 Watchdog Timer Initialization

To enable the watchdog timer the user shall write 1Eh then E1h to the register WDTRST at address 0A6h. Once enable the watchdog cannot be disable. Only a reset will disable the watchdog.

15.3 Watchdog Timer Timeout

The watchdog timer is a 14 bit counter which overflow when it reaches 16383 (3FFFh). The watchdog timer increment with each machine cycle (6 clock cycles in X2 mode and 12 clock cycles in non X2 mode)

When it timed out, the watchdog generate a Reset pulse of 96 clock cycles in X2 mode (192 clock cycle in non X2 mode) for the Atmel AT89C51RB2/AT89C51RC2/AT89C51RD2 and 98 clock cycles for the Philips P89C51RB2/P89C51RC2/P89C51RD2 as well as P89C660/P89C662/P89C664

In normal operation, the user shall reset the watchdog counter by writing 1Eh then E1h to the WDTRST register.

The watchdog reset output is also driving the Reset I/O (PLCC44 pin 10, PDIL40 pin 9, VQFP44 pin 4).

15.4 Watchdog Timer Timeout Extension (Atmel only)

A programmable 7 bit programmable counter can extend the watchdog counter timeout period. 16ms to 2s timeout is possible with a 12MHz Xtal clock.

The WDTPRG register at address A7h includes 3 bit S2,S1,S0 to program the counter extension.

S2,S1,S0=0,0,0 is the reset value for Philips compatible mode $(2^{14} - 1)$

S2,S1,S0=1,1,1 is the configuration for the maximum timeout value $(2^{21} - 1)$

16. Reduce EMI Mode, and Dual Data Pointer and ERAM Control

16.1 EMI Reduction

With Philips P89C51RB2/P89C51RC2/P89C51RD2 as well as P89C660/P89C662/P89C664 and Atmel AT89C51RB2/AT89C51RC2/AT89C51RD2 it is possible to reduce the EMI emission generated by the ALE pulse.

Both Philips and Atmel controllers have an AUXR register at address 8Eh to control ALE output disable and External RAM enable.

AUXR[0] = AO bit : when clear the ALE is emitted at a constant rate of 1/3 of the oscillator frequency in X2 mode and 1/6 of the oscillator frequency in non X2 mode. When set the ALE is active only during a MOVX instruction with external RAM or MOVC instruction with external code

AUXR[1] = EXTRAM : when clear internal ERAM access during MOVX @Ri or MOVX @ DPTR. When set External memory data access.

16.2 Dual Data Pointer

Philips P89C51RB2/P89C51RC2/P89C51RD2 as well as P89C660/P89C662/P89C664 and Atmel AT89C51RB2/AT89C51RC2/AT89C51RD2 feature a Dual Data Pointer for MOVX @DPTR instruction.

With the bit DPS it is possible to toggle between DPTR0 and DPTR1. Reading and writing into DPTR0/1 is done at address 82h and 83h.

The DPS bit is located in AUXR1[0] at address A2h.

16.3 Further control of the ERAM (Atmel only)

In Atmel controllers controllers the register AUXR includes in position AUXR[4,2] 3 bits XRS[2,0] to control the ERAM. These 2 bit positions are not used in the Philips AUXR implementation.

With XRS[2,0] it is possible to program the size of the internal ERAM used. The default mode is compatible with the Philips P89C51RB2/P89C51RC2/P89C51RD2 ERAM size.

For instance, in AT89C51RD2

Default value is XRS[2,0]= 010 : 768 bytes ERAM fully compatible with P89C51RD2.

Minimum configuration is XRS[2,0]= 000 : 256 bytes

Maximum configuration is XRS[2,0]=101 : 1792 bytes compatible with P89C664.

Note for P89C662/P89C664 users, it will be necessary to program the XRS[2,0] field in AUXR register in order to program the AT89C51RC2 in P89C662 compatible mode and AT89C51RD2 in P89C664 compatible mode.

17. Flash Memory

17.1 Introduction

Philips P89C51RB2/P89C51RC2/P89C51RD2 as well as P89C660/P89C662/P89C664 and Atmel AT89C51RB2/AT89C51RC2/AT89C51RD2 have respectively 16KB/32KB/64KB Flash memories. The flash memories are byte programmable, They are organized in

2 blocks of 8KB for P89C51RB2/P89C660 and AT89C51RB2

Same as above + one block of 16KB for P89C51RC2/P89C662 and AT89C51RC2

Same as above + 2 blocks of 16KB for P89C51RD2/P89C664 and AT89C51RD2

Philips controllers and Atmel controllers have a 1Kbyte ROM bootloader. The bootloader contain low level in system programming routine and a default loader. User program can call these routines to perform In-Application Programming (IAP). Philips and Atmel controllers also offer the same mechanism for the user to implement a custom bootloader within the Flash memory by way of activating a boot vector. Finally hardware activation of the bootloader is available for Philips and Atmel with the same conditions (PSEN=LOW, P2.6= HIGH, ALE=HIGH, EA#=HIGH)

Philips and Atmel controllers offer In System Programming using UART communication and a free PC program : WinISP for Philips and FLIP for Atmel. Parallel programming is also possible for all controllers.

Philips and Atmel use the same 4 levels Hardware Program lock mechanism, and 3 levels Software Program lock mechanism.

Philips controllers need 5 volts on EA#/VPP(12 volts tolerant) pin while Atmel doesn't need this and support ISP and IAP down to Vcc=2.7 volts.

Atmel flash controllers are qualified up to 100K cycles (10K for Philips). Atmel Flash write use a self timed mechanism while Philips use the Xtal clock. In ISP routines one should pass the Xtal frequency as a parameter for Philips. Atmel doesn't need it. Would the user passes the frequency parameter such as Philips while using an Atmel controller, this parameter would be discarded. This way a seamless transition Philips to Atmel is possible.

17.2 Boot Program and Power On Reset Execution

Upon Reset falling edge, Philips controllers test the STATUS BYTE.

If STATUS BYTE = 0, The power-up execution start at 0000h (user program)

If STATUS BYTE not= 0, the content of the BOOT VECTOR BYTE is used as the high byte of the execution address (low byte = 00h). The factory default value is FC00h (address of the ROM bootloader)

Hardware conditions : PSEN=LOW, P2.6= HIGH, ALE=HIGH, EA#=HIGH force execution of the bootloader whatever the STATUS BYTE VALUE.

Upon Reset falling edge, Atmel controllers test the Bootloader Jump bit (BLJB).

If BLJB not= 0, The power-up execution start at 0000h (user program)

If BLJB= 0, the content of the SOFTWARE BOOT VECTOR is used as the high byte of the execution address (low byte = 00h). The factory default value is FC00h (address of the ROM bootloader)

Hardware conditions : PSEN=LOW, P2.6= HIGH, ALE=HIGH, EA#=HIGH force execution of the bootloader whatever the STATUS BYTE VALUE.

Remark1 : the Philips and Atmel mechanisms are similar. Care must be taken only of the difference between STATUS BYTE (Philips) and BLJB (Atmel). Both are controlled by their respective ISP (Philips WINISP and Atmel FLIP)

Remark2 : Factory programming of Philips and Atmel controllers always branch to the factory ROM bootloader.

18. In System Programming

In System Programming is similar for Philips and Atmel. It uses TXD, RXD, VSS, VCC. Intel HEX format are used.

First the baud Rate is established with the Host sending a continuous character “U”. The chip respond by echoing the character for all Philips and Atmel controllers.

Philips ISP set of commands and Atmel ISP set of commands are extremely similar. Below are recommendations for customers using their own serial programming tool. All of this is transparent when Philips WINISP and Atmel FLIP tools are used.

Recommendations for ISP set of commands usage.

- Philips record type 2 specifies oscillator frequency is not used when using Atmel controllers (Atmel has a self timed Flash write controller).
- Philips record type 6 direct load of Baud Rate is not supported by Atmel (Autobaud is mandatory)
- Atmel has a record type 3 with data[0]=03h for Hardware Reset (not supported by Philips)
- Atmel has a record type 3 with data[0]=0Ah and data[1]= 04h for program the BLJB
- Atmel has a record type 3 with data[0]=0Ah and data[1]= 08h for program the X2 mode (not supported by Philips. See also the clock control chapter)
- Atmel has extra records type 5 with data[0]=07h and data[1]=06h to read an extra byte, and data[0]= 0Bh , 0Eh, 0Fh to read Hardware byte, device ID1nad ID2 and bootloader version (not supported by Philips)

19. In Application Programming

Philips and Atmel bootloaders contain low level in system programming routines and a default loader. User program can call these routines to perform In-Application Programming. Philips and Atmel set of routines are extremely similar. Below are highlighted the differences to help customer using Philips controllers to migrate to Atmel controllers. Handling watchdog and IAP is detailed in a specific paragraph below

- Philips includes an Erase Boot Vector (this command also erase the Status Byte : input parameter R1=04. This command is not supported by Atmel. Please notice the command Program boot vector exists in both Philips and Atmel with the same parameters : R1=06h, DPL=01h. The command Program Status Byte also exists in both Philips and Atmel with the same parameters : R1=06h, DPL=00h. (Philips Status Byte is called BSB by Atmel)
- Program Security Bit. The same command exists for Philips and Atmel with code R1=05h. The difference is the parameters passed to get Level 0, 1, 2
- Security bit #1 inhibit write flash : Philips DPL=00h, Atmel DPL=01h
- Security bit #2 inhibit flash verify : Philips DPL=01h, Atmel DPL=02h
- Security bit #3 disable external memory : Philips DPL=02h. Mode not supported by Atmel
- Read Device Data code R1=03h supported by Philips only. Atmel doesn't support this mode as it is easier to do a MOVC (Move Code instruction)
- Atmel has a third device ID (device ID3) and has an API call to read it : R1=00h, DPL=03h
- Atmel has a Program Data Page routine (see note below) R1=09h. This mode is not supported by Philips.
- Atmel has a Program X2 fuse, Program BLJB R1=0Ah, DPL=08h and 04h. These modes are not supported by Philips
- Atmel has a read Hardware byte (can read the hardware lock bits) R1=0Bh. This mode is not supported by Philips
- Atmel has a read boot ID1 ID2 : R1=0Eh, DPL=00h and 01h. This mode is not supported by Philips
- Atmel has a read boot version : R1=0Fh. This mode is not supported by Philips

Note: Atmel offers a page programming mode : each pages is 128 bytes. One can write from 1 byte to a full 128 bytes page in one write sequence greatly improving the write throughput performance.

19.1 In Application Programming and Watchdog

Philips and Atmel provide the same watchdog feature inside the controllers. Once the watchdog has been enabled, it cannot be disabled. Only a Reset will disable the watchdog.

When using IAP care must be taken to refresh the watchdog prior to enter an IAP routine, and make sure the routine execution time is smaller than the watchdog timeout.

Philips includes a feature to refresh the watchdog as an option for each IAP routine. It is realized by adding 80h to the R1 parameter. For instance

- Erase block normal : R1=01h
- Erase block with Watchdog refresh. : R1=81h

This feature is not supported by Atmel. User shall make sure a refresh watchdog instruction is inserted prior to calling an IAP routine to perform the same thing.

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