Chapter 1 .VSR Specification

I. Interface

1. Communication

The below figure presents structure overview among ARM, VSR (VietNam Speech Recognition), FLASH and SRAM components.

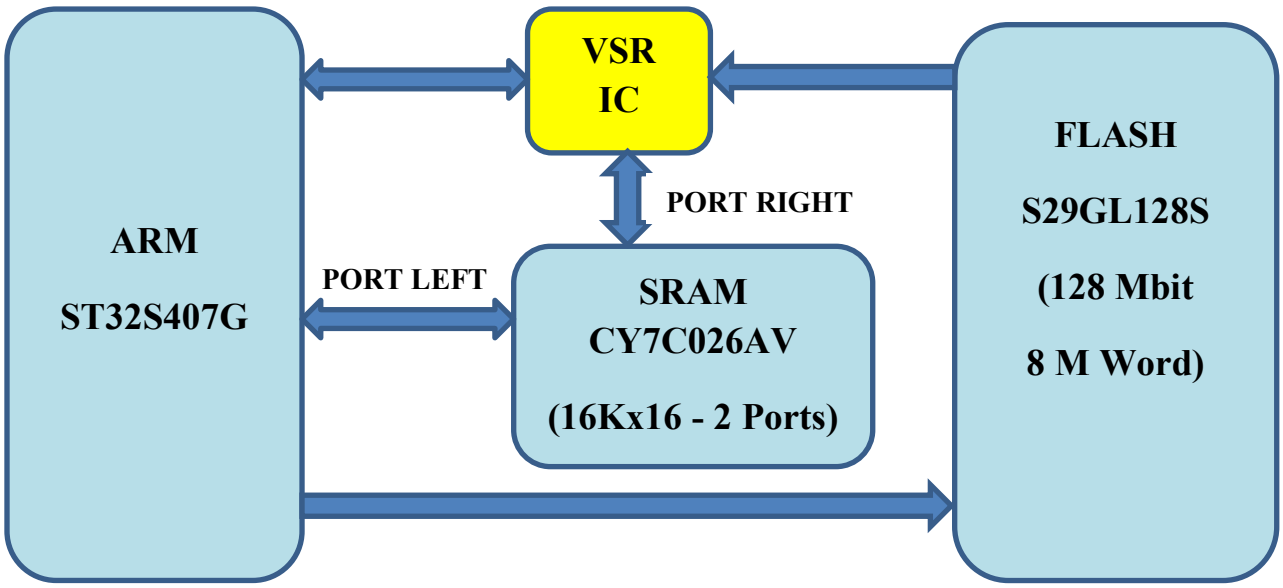

Figure 1-1 Structure Overview

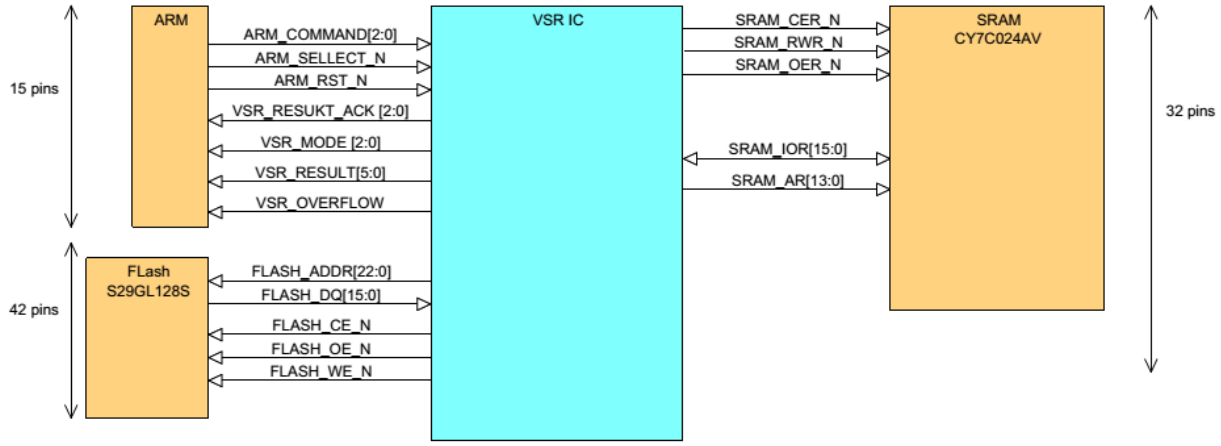

Figure 1-2 VSR IC Interface

Table 1-1 VSR Interface

No.	Port Name	Property				
		Port Num	In/ Output	Active	Initial	Description
1	GND		Input			Ground
2	VCC		Input			Power source
3	CLK	1	Input			Clock form Generated Clock IC
4	ARM_RST_N	1	input	Low	1'b1	Reset VSR IC from ARM
5	ARM_SELECT_N	1	Input	Low	1'b1	ARM selects VSR IC as communication
6	ARM_COMMAND	3	Input		3'b000	Command from ARM to VSR IC
7	VSR_MODE	3	Output		3'b000	VSR mode from VSR to ARM
8	VSR_RECOG_RESULT	6	Output		6'b000000	Recognition result from VSR to ARM
9	VSR_RESULT_ACK	1	Output			Result ack from VSR to ARM
10	VSR_OVERFLOW	1	Output			Overflow flag from VSR to ARM
11	SRAM_CER_N	1	Output	Low	1'b1	Chip select from VSR to SRAM
12	SRAM_OER_N	1	Output	Low	1'b1	Read enable from VSR to SRAM
13	SRAM_RWR_N	1	Output	Low	1'b1	Write enable from VSR to SRAM
14	SRAM_IOR	16	InOut		16'b0	Data from/to SRAM to/from VSR
15	SRAM_AR	14	Output		14'b0	Address from VSR to SRAM
16	FLASH_DQ	16	InOut		16'b0	Data to/from FLASH from/to VSR
17	FLASH_ADDR	23	Output		23'b0	Address form VSR to FLASH
18	FLASH_CE_N	1	Output	Low	1'b1	Chip select
19	FLASH_WE_N	1	Output	Low	1'b1	Write enable + WE = 0, OE = x: Write enable
20	FLASH_OE_N	1	Output	Low	1'b1	Read enable WE = 1, OE = 0: Read enable

Table 1-2. Power/Ground Connection

No.	Port Name	Property
1	VCC	Up to the total port of VSR IC
2	GND	Up to the total port of VSR IC
3	CLK	20MHz

Table 1-3 ARM Connection

No.	Port Name	Property
1	ARM_RST_N	VSR IC has one asynchronous active low reset received from ARM + Active low : 1'b0 + Inactive high: 1'b1 (initial)
2	ARM_SELECT_N	+ Active low + It is been active low when ARM wants to set up the new connection to VSR IC. This signal should be kept stable (1'b1) after until finishing configuration process + In the **RECOGNITION** or **TEST** state, the inactive high level does not affect the the operation of VSR.
3	ARM_COMMAND	+ Values: 000: Initial value x01: 50 words recognition – speaker dependent x10: 04 words recognition – speaker independent

		1xx: TEST mode + ARM uses ARM_COMMAND signal to configure the functions of VSR IC. The corresponding states is presented in the Figure 2.1
4	VSR_MODE	+ There are total 6 main states of VSR + The mains states will be exported to ARM by VSR_MODE output port + There are two main flows presenting the VSR operation . (1): INITIAL – READY – SETUPxx - RECOGNITION - IDLE . (2): INITIAL – READY – SETUPxx – RECOGNITION – TEST - IDLE + The (1) flow is used when ARM_COMMAND[3] == 1'b0 + The (2) flow is used when ARM_COMMAND[3] == 1'b1 (Having Test mode)
5	VSR_RESULT	+ There are 6 bits presenting the recognition results as the following details 6'b000000: Initial value 6'b 000001: Word 01 6'b 000010: Word 02 …….. 6'b 110010: Word 50
6	VSR_RESULT_ACK	Confirm the result of recognition process
7	VSR_OVERFLOW	Confirm the overflow situation in recognition process

Table 1-4 FLASH Connection

No.	Port Name	Property
1	FLASH_DQ	Data is read from FLASH to VSR IC. Data is system information including configures, mean, covariance, switching state, initial matrixes to use in recognition process in recognition flow.
2	FLASH_ADDR	Address to read data from FLASH
3	FLASH_CE_N	Should be active firstly before reading data from FLASH
4	FLASH_WE_N	Because VSR only read data from FLASH, FLASH_WE is always inactive 1'b1 in recognition process
5	FLASH_OE_N	Because VSR only read data from FLASH, FLASH_OE_N is always active 1'b0 in recognition process

Table 1-5 SRAM Connection

No.	Port Name	Property
1	SRAM_CER_N	Is always active low before the read/write process is executed
2	SRAM_OER_N	+ 0: For reading process + 1: None process
3	SRAM_RWR_N	+ 0: For writing process + 1: For reading process
6	SRAM_IOR	Data is read/write from/to SRAM/VSR to VSR/SRAM
7	SRAM_AR	Address to read/write data from/to SRAM

2. VSR IC functions

Firstly, overview of all processes is presented as the below figure

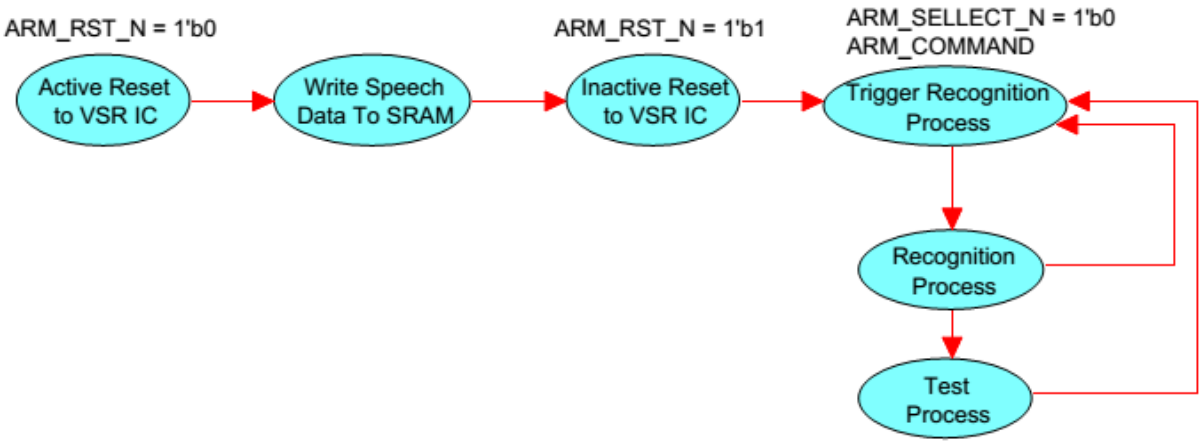

Figure 1-3 Overview of all processes

Following the Figure 1.3, all processes are collected in following detail

- Firstly, the ARM_RST_N is active (1'b0) to reset all VSR IC
- Next, the speech data being fine cutting data is written to SRAM thought out Port Left
- After finishing load data to SRAM, ARM_RST_N is inactive
- Continuously, ARM uses **ARM_SELLECT_N** and **ARM_COMMAND[2:0]** signals to setup and control the operation of VSR IC. In this process, the VSR IC state changes following the values of **ARM_SELLECT_N** and **ARM_COMMAND**[2:0] . However, when state moves to **RECOGNITION** state, the VSR IC will start recognition process in which the VSR operation is not controlled by the signals from ARM accepted the **ARM_RST_N.** The Chapter 2 is referred to clarify the changing states in VSR IC.
- After finish recognition process, if **ARM_COMMAND**[3] is equal to 1'b1, the Test process is started. In test process, the data stored in the internal memory of VSR IC is loaded to SRAM and wait the checking triggered by ARM.
- If **ARM_COMMAND**[3] is equal to 1'b0, the VSR IC moves to IDLE state and wait to new recognition process controlled by **ARM_SELLECT_N** and **ARM_COMMAND[2:0].**

Chapter 2 .VSR State Machine

The following Figure 2-1 VSR State Machine presents the main states of VSR IC in which the details of state transaction and output signals are declared in the Table 2-1

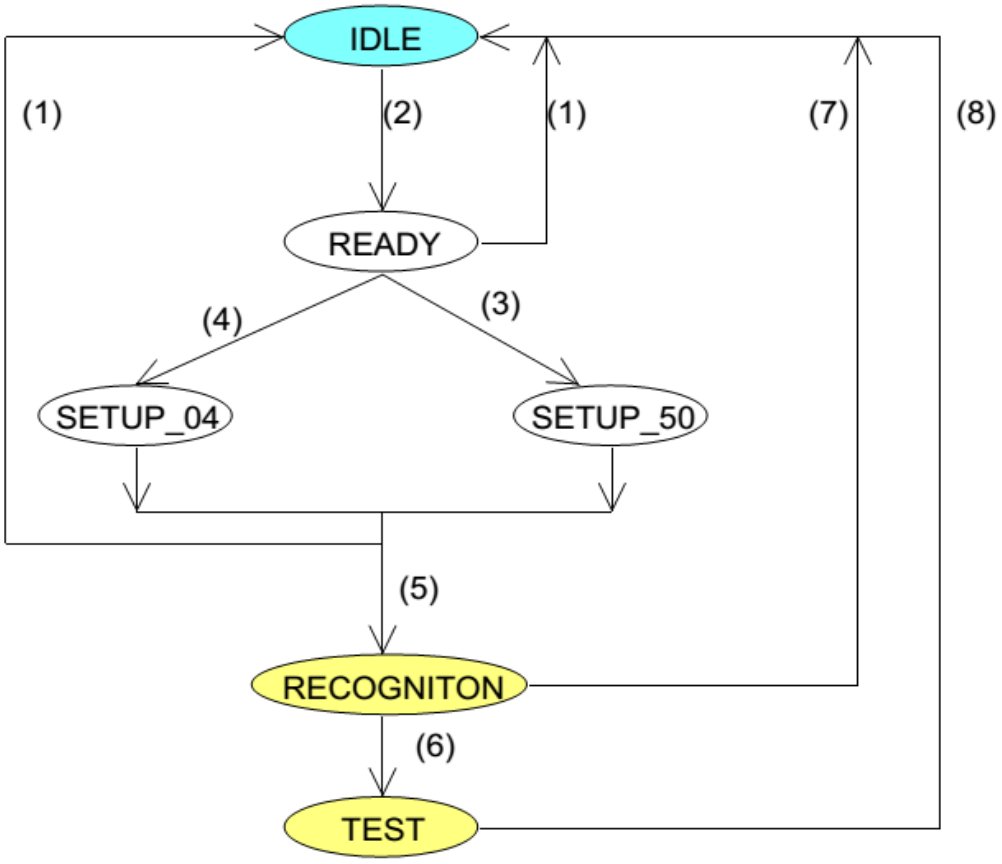

Figure 2-1 VSR State Machine

Table 2-1 State Machine Switching Conditions

No.	Current State	Next State	Condition
1	IDLE	READY	(2) ARM_SELECT is active low
2	READY	IDLE	(1) ARM_SELECT is inactive high
		SETUP_50	(3) ARM_COMMAND is 3'bx01
		SETUP_04	(4) ARM_COMMAND is 3'bx10
3	SETUP_04	RECOGNITION	(5) Automatically
4	SETUP_50	RECOGNITION	(5) Automatically
5	RECOGNITION	IDLE	(7) ARM_COMMAND is 3'b0xx
		TEST	(6) ARM_COMMAND is 3'b1xx
6	TEST	IDLE	(8) Automatically

Note: All states come to IDLE whenever ARM_RST_N is active low

- The list of single words is showed in below Table 2-2.

Table 2-2. Dependent/Independent Process

Dependent Process			
1	Không	26	Khỏe
2	Một	27	Cây
3	Hai	28	Hoa
4	Ba	29	Bật
5	Bốn	30	Tắt
6	Năm	31	Mở
7	Sáu	32	Đóng
8	Bảy	33	Đèn
9	Tám	34	Quạt
10	Chín	35	Cửa
11	Lịch	36	Phòng
12	Sử	37	Khách
13	Văn	38	Ngủ
14	Hóa	39	Bếp
15	Giáo	40	Dừng
16	Dục	41	Bỏ
17	Khoa	42	Qua
18	Học	43	Tiếp
19	Nông	44	Tục
20	Nghiệp	45	Tôi
21	Cá	46	Nghe
22	Heo	47	Muốn
23	Gà	48	Tin
24	Vịt	49	Chào
25	Sức	50	Bạn

Independent Process	
1	Tắt
2	Mở
3	Lên
4	Xuống

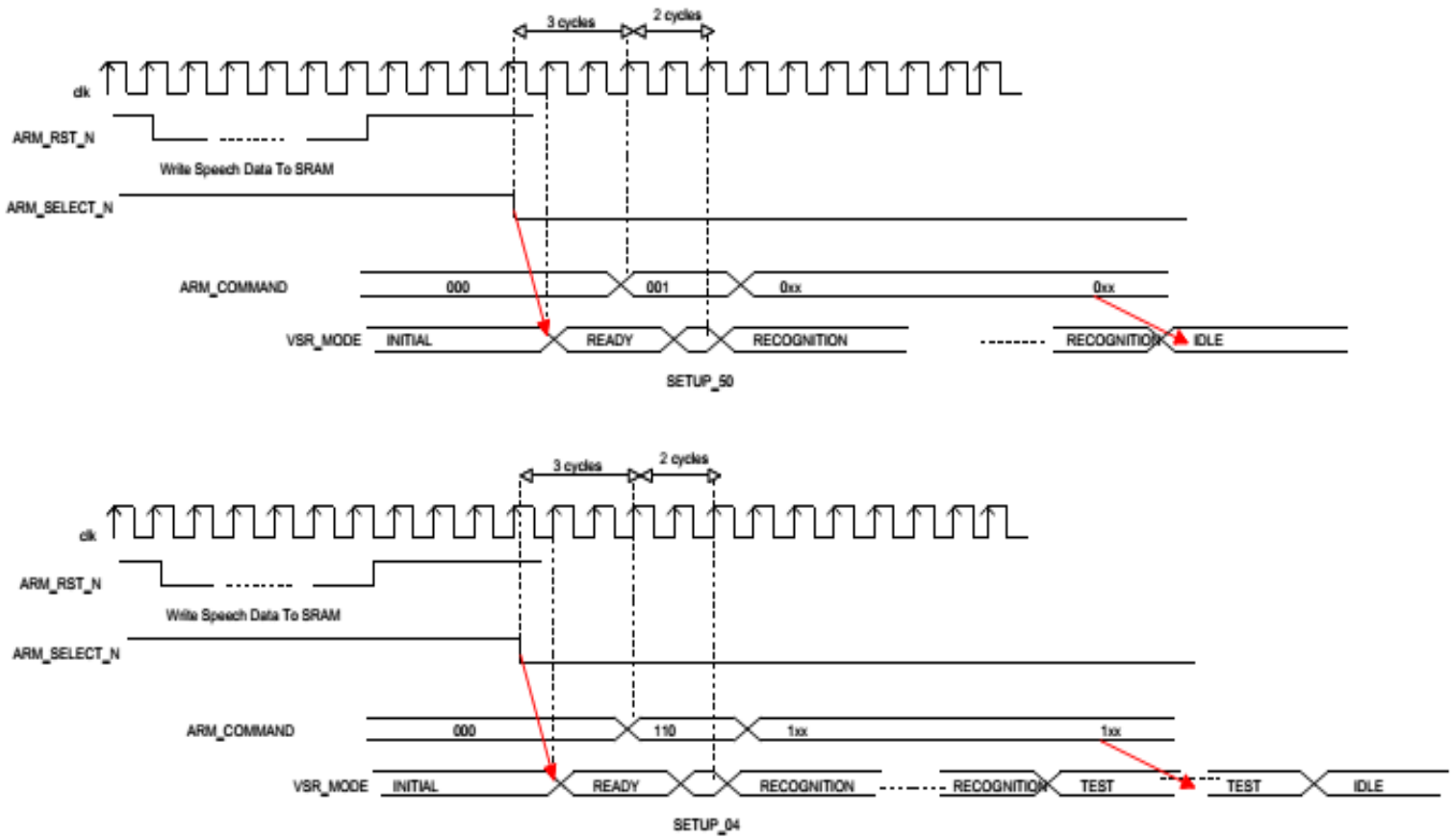

Figure 2-2. State Changing Diagram

Chapter 3 . SRAM Specification

1. SRAM interface

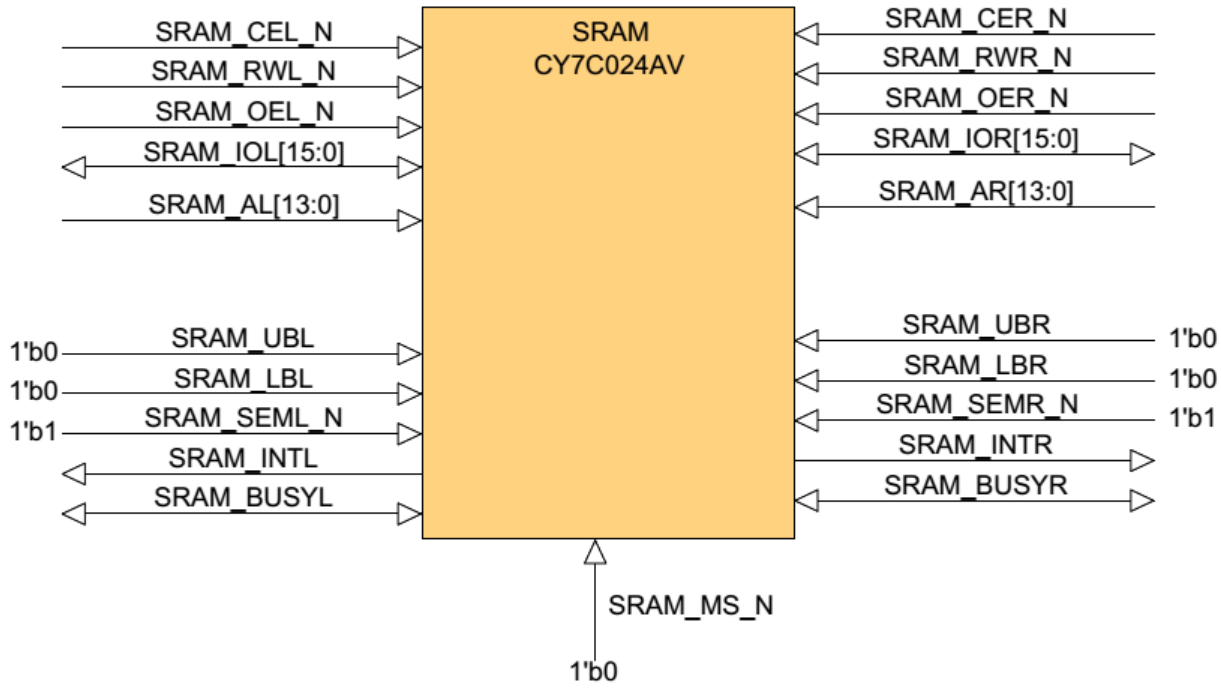

Figure 3-1 SRAM Interface

Two ports SRAM CY7C024AV showed in the Figure 3-1 take following property mainly

- Asynchronous SRAM
- Two Ports
- Can be Master or Slave in system (SRAM_MS_N)
- Support sharing function (SRAM_SEML/R_N)

Table 3-1 SRAM Interface

No.	Port Name	Property				
		Port Num	In/ Output	Active	Initial	Description
1	GND		Input			Ground
2	NC					Not connect
3	VCC		Input			VCC Power
4	SRAM_CER_N	1	Input	Low	1'b1	Chip select from VSR to SRAM
5	SRAM_OER_N	1	Input	Low	1'b1	Read enable from VSR to SRAM
6	SRAM_RWR_N	1	Input	Low	1'b1	Write enable from VSR to SRAM
7	SRAM_IOR	16	InOut		16'b0	Data from/to SRAM to/from VSR
8	SRAM_AR	14	Input		14'b0	Address from VSR to SRAM
9	SRAM_UBR_N	1	Input	Low	1'b1	Should be force 0
10	SRAM_LBR_N	1	Input	Low	1'b1	Should be force 0
11	SRAM_SEMR_N	1	Input	Low	1'b1	Should be force 1
12	SRAM_BUSYR_N	1	Output	Low	1'b1	Busy Flag
13	SRAM_INTR_N	1	Output	Low	1'b1	Interrupt flag
14	SRAM_CEL_N	1	Input	Low	1'b1	Chip select from ARM to SRAM
15	SRAM_OEL_N	1	Input	Low	1'b1	Read enable from ARM to SRAM
16	SRAM_RWL_N	1	Input	Low	1'b1	Write enable from ARM to SRAM
17	SRAM_IOL	16	InOut		16'b0	Data from/to SRAM to/from ARM
18	SRAM_AL	14	Input		14'b0	Address from ARM to SRAM
19	SRAM_UBL_N	1	Input	Low	1'b1	Should be force 0
20	SRAM_LBL_N	1	Input	Low	1'b1	Should be force 0
21	SRAM_SEML_N	1	Input	Low	1'b1	Should be force 1
22	SRAM_BUSYL_N	1	InOut	Low	1'b1	Busy Flag – Should be no connect
23	SRAM_INTL_N	1	Output	Low	1'b1	Interrupt flag
24	SRAM_MS_N	1	Output	High	1'b1	Master or Slave Select – Should be forced 1 as Slave Mode in order to BUSY is as the output port

2. SRAM Behavior

Because some functions of SRAM are not used, the below ports are forced and some are not connected

- SRAM_MS_N = 1'b1: Master Mode
- SEML/R_N = 1'b1: Not use this function
- SRAM_UBL/R_N = 1'b0: Receive upper bits
- SRAM_LBL/R_N = 1'b0: Receive below bits
- SRAM_INTL/R_N : Not connection
- SRAM_BUSYL/R: Not connection

SRAM in this application in only applied in read mode and write mode. The below figure presents the logic levels of all SRAM control ports in these modes.

Inputs						Outputs		Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	IO_8–IO_{15}	IO_0–IO_7	
H	X	X	X	X	H	High Z	High Z	Deselected: Power Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power Down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H	⎍	X	X	X	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
X	⎍	X	H	H	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Figure 3-2 Logic Ports of SRAM in Read mode and Write Mode

3. SRAM Diagram

Because of using SRAM only in Read/Write mode, this section only describes the pulse diagram related to Read/Write processes. Firstly, writing process is introduced.

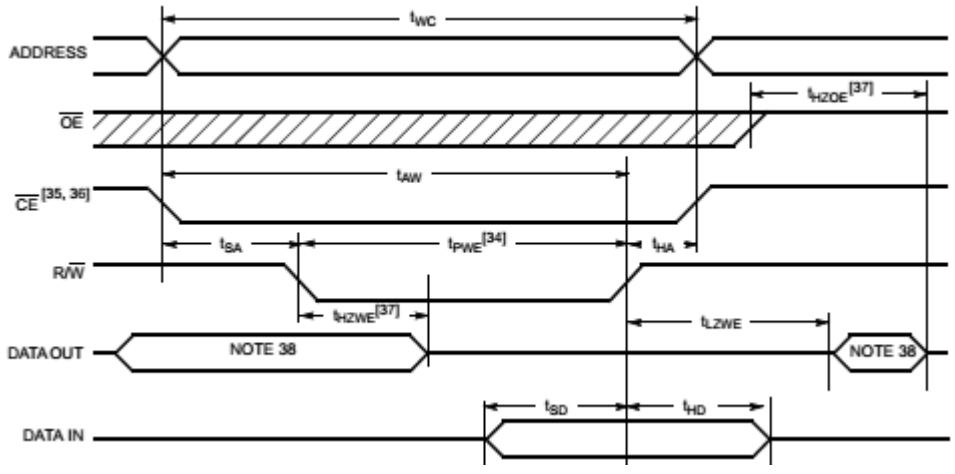

Figure 3-3 Writing process – SRAM_RW_N control

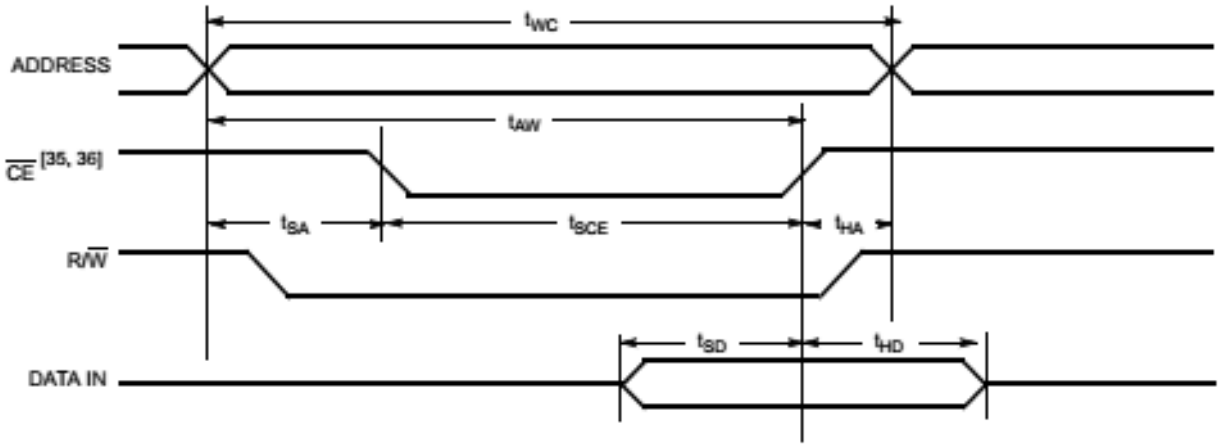

Figure 3-4 Writing process – SRAM_CE_N control

As the result, the writing process can be controlled by two control signals as SRAM_CEL/R_N or SRAM_RWL/R_N. Actually, the writing process is triggered by the falling edge of these signals. One more case of writing process checked with SRAM VHDL model is also presented.

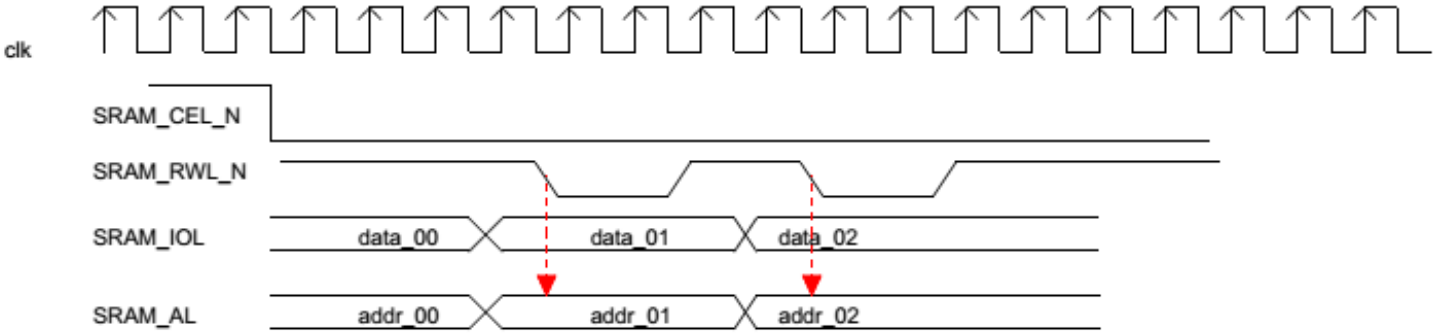

Figure 3-5 Writing process – Following SRAM_RWL_N falling edge

Hence, the reading process examples are also introduced in following diagrams.

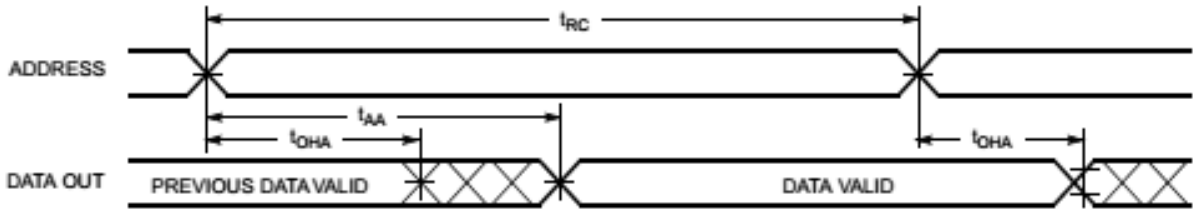

Figure 3-6 Reading process – Following the changing of Address

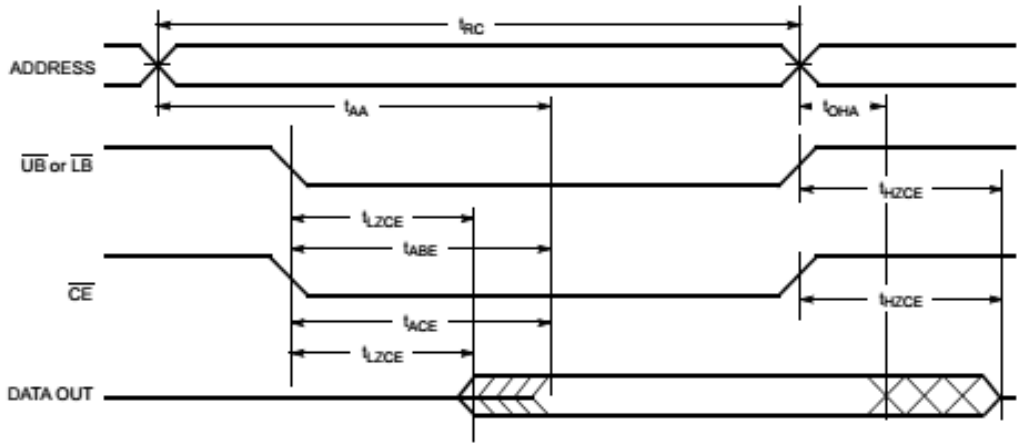

Figure 3-7 Reading process – Following the SRAM_CE edge

Chapter 4 . FLASH Specification

1. FLASH interface

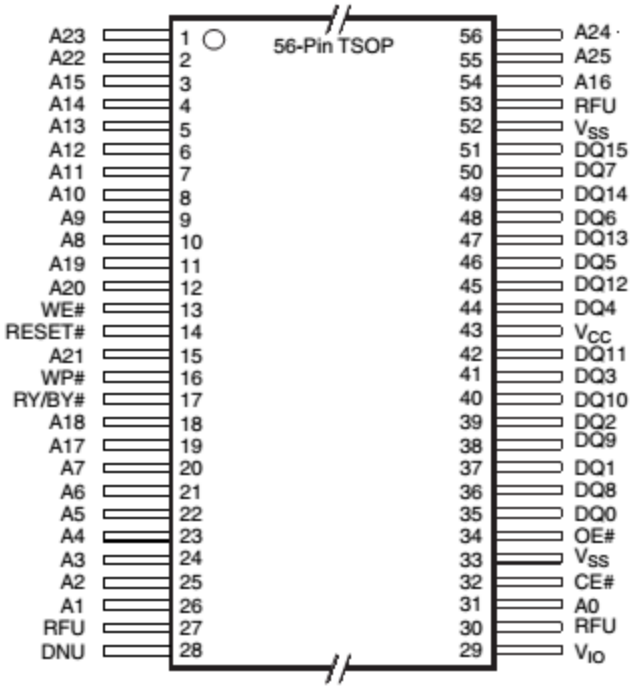

Figure 4-1 FLASH interface

Notes:

1. Pin 28, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to VCCor VSSthrough a series resistor.

2. Pin 27, 30, and 53 Reserved for Future Use (RFU)

Table 4-1 FLASH Interface

No.	Port Name	Property				
		Port Num	In/ Output	Active	Initial	Description
1	VCC	1	Input			Power
2	VSS	2	Input			Ground
3	VIO	1	Input			Power
3	FLASH_DQ	16	InOut		16'b0	Data to/from FLASH from/to VSR
4	FLASH_ADDR	23	Output		23'b0	Address form VSR to FLASH
5	FLASH_CE_N	1	Output	Low	1'b1	Chip select
6	FLASH_WE_N	1	Output	Low	1'b1	Write enable + WE = 0, OE = x: Write enable
7	FLASH_OE_N	1	Output	Low	1'b1	Read enable WE = 1, OE = 0: Read enable
8	FLASH_RESET_N	1	Input	Low	1'b1	Reset the Flash
9	FLASH_WP_N	1	Input	Low	1'b1	Write Protect
10	FLASH_RFU(27, 30, 53)	3				No connection
11	FLASH_DNU(28)	1				Reserve
12	RY/BY	1	Output			Output of FLASH to show the status of FLASH

2. FLASH Behavior

Because some functions of FLASH are not used, the below ports are forced and some are not connected

- FLASH_DNU : Not connection
- FLASH_RFU: Not connection
- FLASH_WP_N : Is connect to ARM so that VSR IC do not care that

The communication between FLASH and VSR IC is only in read mode. Hence, VSR IC just takes care the read process of FLASH presented in following figure

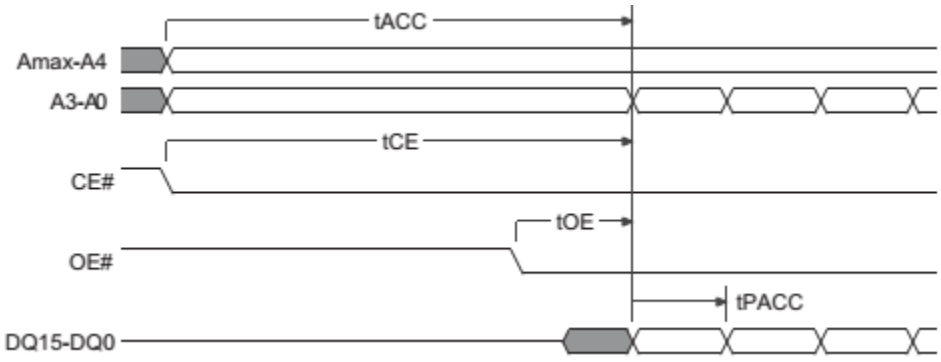

Figure 4-2 Reading process of FLASH

Chapter 5 . Update Table

Table 5-1 Update Table

No.	Version	MM/DD/YY	Update Record
1	**1.4**	**03/01/14**	Chang the forced signal of SRAM: + v1.3: MS = 0 (Slave mode) + MS = 1 (Master Mode)
			Update the connection of WP port of FLASH: + 1.3: WP is not connected + 14: WP port is connected to ARM