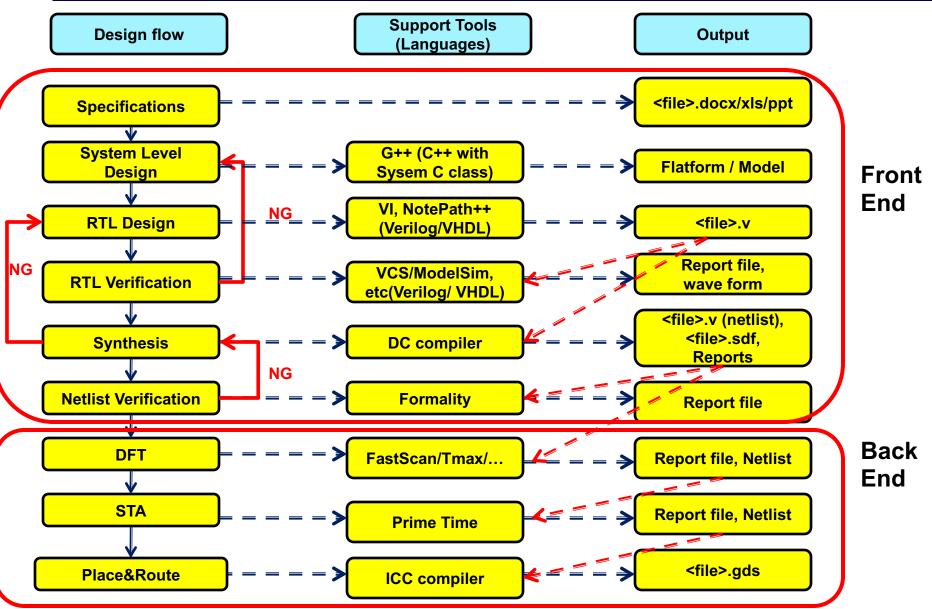


System Level Design in Cell Based Design Flow



Cell Based Design Flow





Cell Based Design Flow

Support Tools Design flow Output (Languages) <file>.docx/xls/ppt **Specifications** Configuration Program Counter FLASH 1K x 14 Program Design the one bit adder: Memory 8-Level Stack bytes + Three inputs (A, B, Cin) Program + Two output (S, Cout) Instruction req STATUS reg MUX Power-up Timer Oscillator OSC1/CLKIN Timing Generation Watchdog Wireq O9C2/CLKOUT Oscillator \times T1CKI \times Timer0 Analog to Digital Converter **EE DATA** Comparator (PIC16F676 only) and reference 128 bytes DATA **EEPROM**

EEADDR

CIN- CIN+ COUT



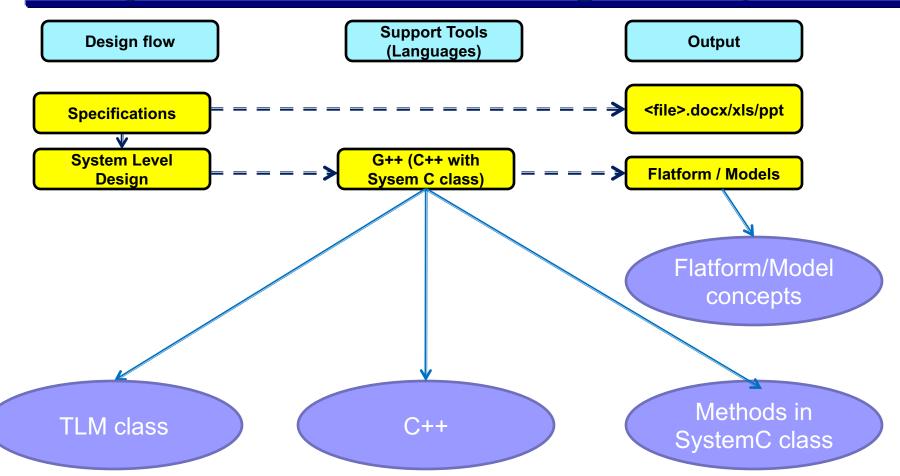
Cell Based Design Flow

Support Tools Design flow Output (Languages) <file>.docx/xls/ppt **Specifications** Configuration Program Counter FLASH 1K x 14 Program Design the one bit adder: Memory 8-Level Stack bytes + Three inputs (A, B, Cin) Program + Two output (S, Cout) Instruction req STATUS reg MUX Power-up Timer Oscillator OSC1/CLKIN Timing Generation Watchdog Wireq O9C2/CLKOUT Oscillator \times T1CKI \times Timer0 Analog to Digital Converter **EE DATA** Comparator (PIC16F676 only) and reference 128 bytes DATA **EEPROM**

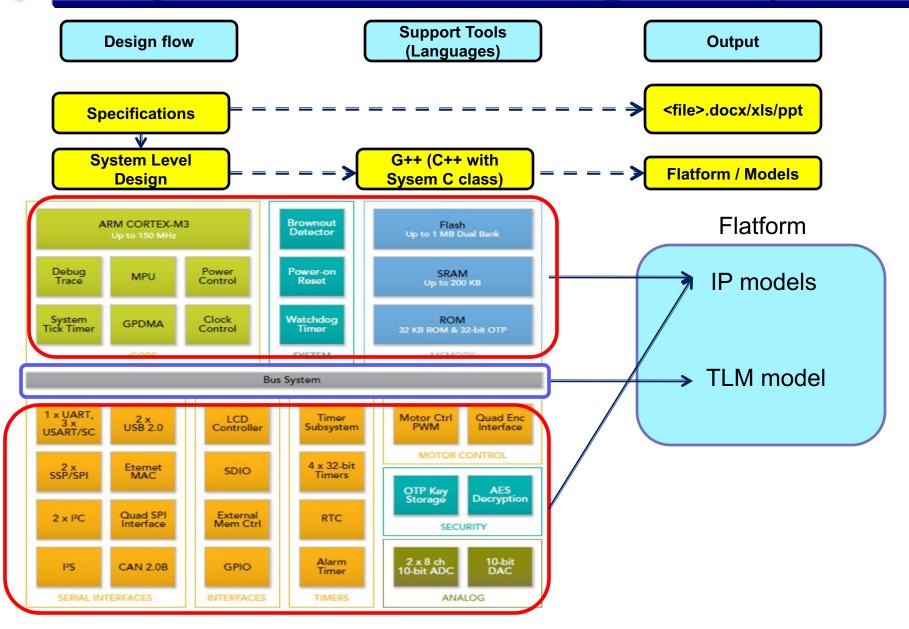
EEADDR

CIN- CIN+ COUT

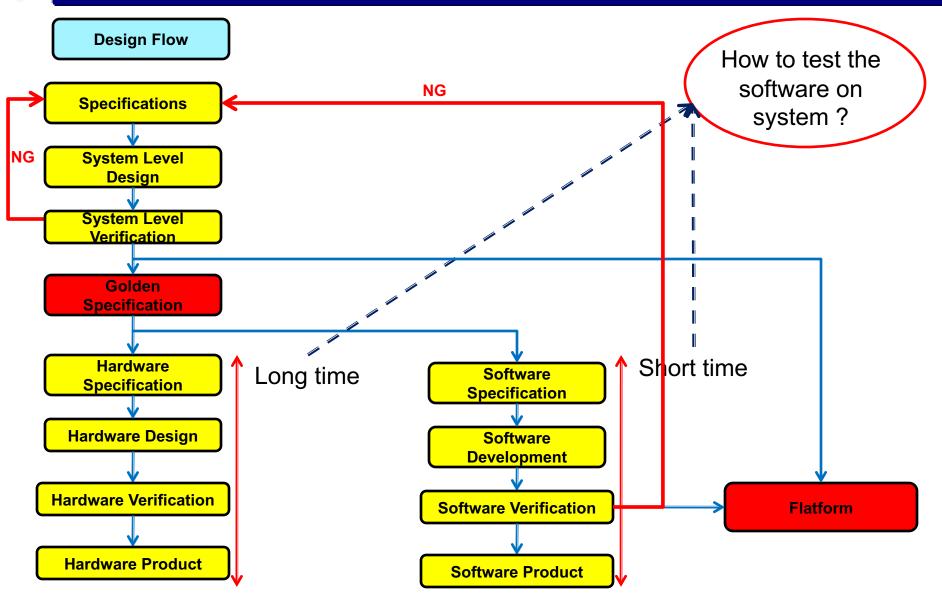






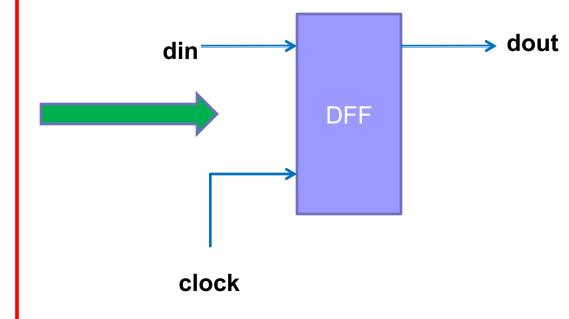








```
#include "systemc.h"
SC_MODULE(d_ff) {
  sc in<bool> din;
  sc in<bool> clock
  sc out<bool> dout;
  void doit() {
    dout = din;
    cout << dout;
  };
  SC_CTOR(d_ff) {
    SC_METHOD(doit);
    sensitive_pos << clock;</pre>
```





Q & A