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# **Short Guide of VCS**



# Synopsys Company

- ❖ Synopsys, Inc. (Nasdaq:SNPS) provides products and services that accelerate innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor intellectual property (IP), Synopsys' comprehensive, integrated portfolio of system-level, IP, implementation, verification, manufacturing, optical and field-programmable gate array (FPGA) solutions help address the key challenges designers face such as power and yield management, system-to-silicon verification and time-to-results.
- ❖ Founded in 1986 by Dr. Aart de Geus and a team of engineers from General Electric's Microelectronics Center in Research Triangle Park, North Carolina, Synopsys was first established as "Optimal Solutions" with a charter to develop and market ground-breaking synthesis technology developed by the team at General Electric
- ❖ <http://www.synopsys.com>
- ❖ **Other companies:** Cadence, Mentor Graphic, Magma, Aldec, etc

# Synopsys Tools

VCS      IC Compiler, Formality, Design Compiler

<b>System-Level Design</b>  Digital signal processing design, high-level synthesis, virtual platforms and analog/mixed-signal simulation.  <a href="#">MORE ▶</a>	<b>Verification</b>  High-performance system, RTL, equivalence checking, mixed-signal verification solutions, and Verification IP  <a href="#">MORE ▶</a>	<b>Implementation &amp; Signoff</b>  Advanced digital and custom IC and FPGA design solutions, including synthesis, test, physical implementation and verification, and signoff.  <a href="#">MORE ▶</a>
<b>Manufacturing</b>  Mask synthesis, mask data prep, lithography simulation and verification, and yield management.  <a href="#">MORE ▶</a>	<b>TCAD</b>  Process and device simulation tools for technology exploration, development and variability analysis.  <a href="#">MORE ▶</a>	<b>Optical Design</b>  Optical design and analysis software and engineering services.  <a href="#">MORE ▶</a>

- ❖ OS: Linux environment (ReadHat 5, Fedora 13 - 14)
- ❖ Mode: Command mode or GUI mode (Command mode)
- ❖ Support tool: DVE (To load the waveform )

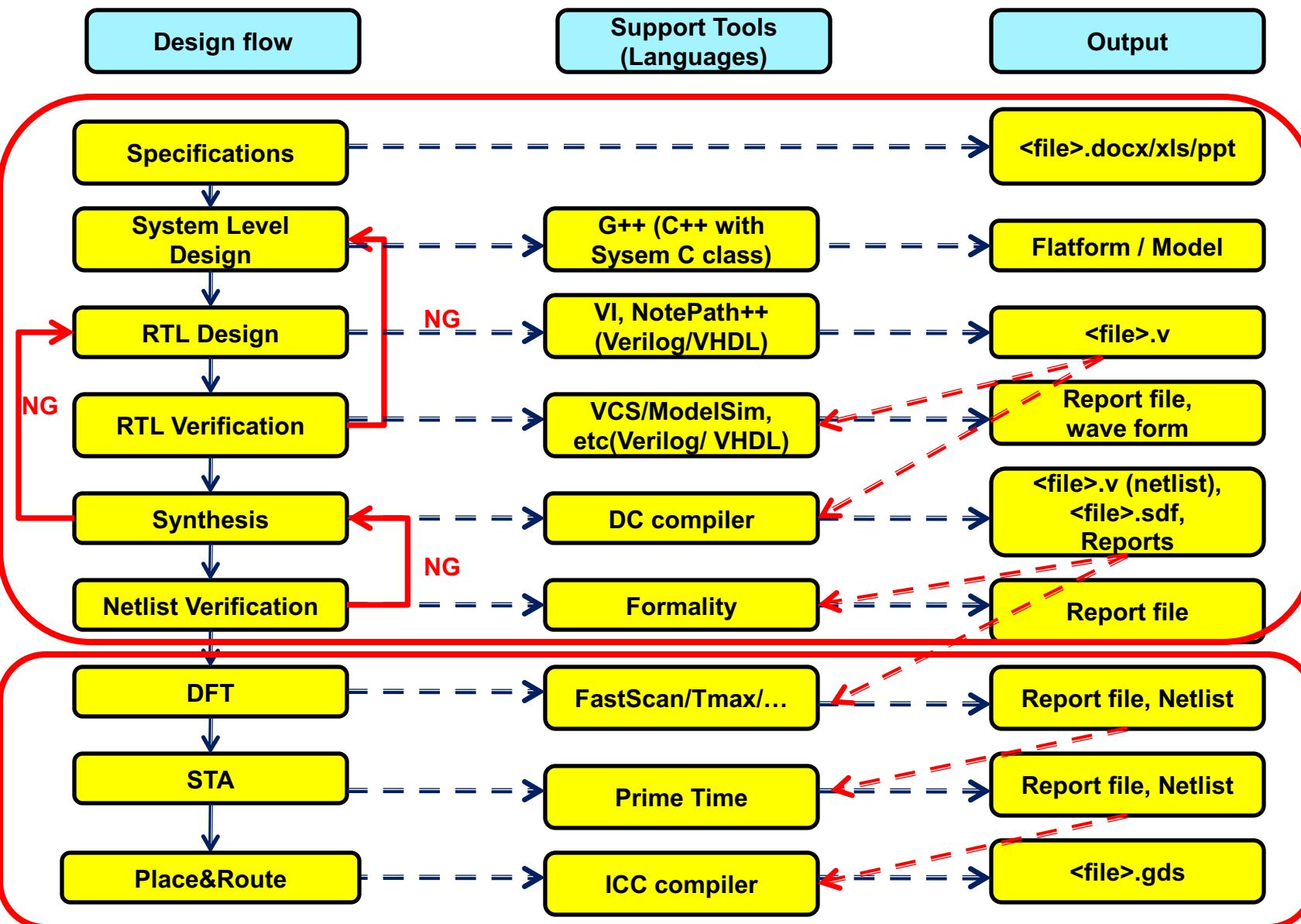
# Synopsys Tools

**VCS****IC Compiler, Formality, Design Compiler**

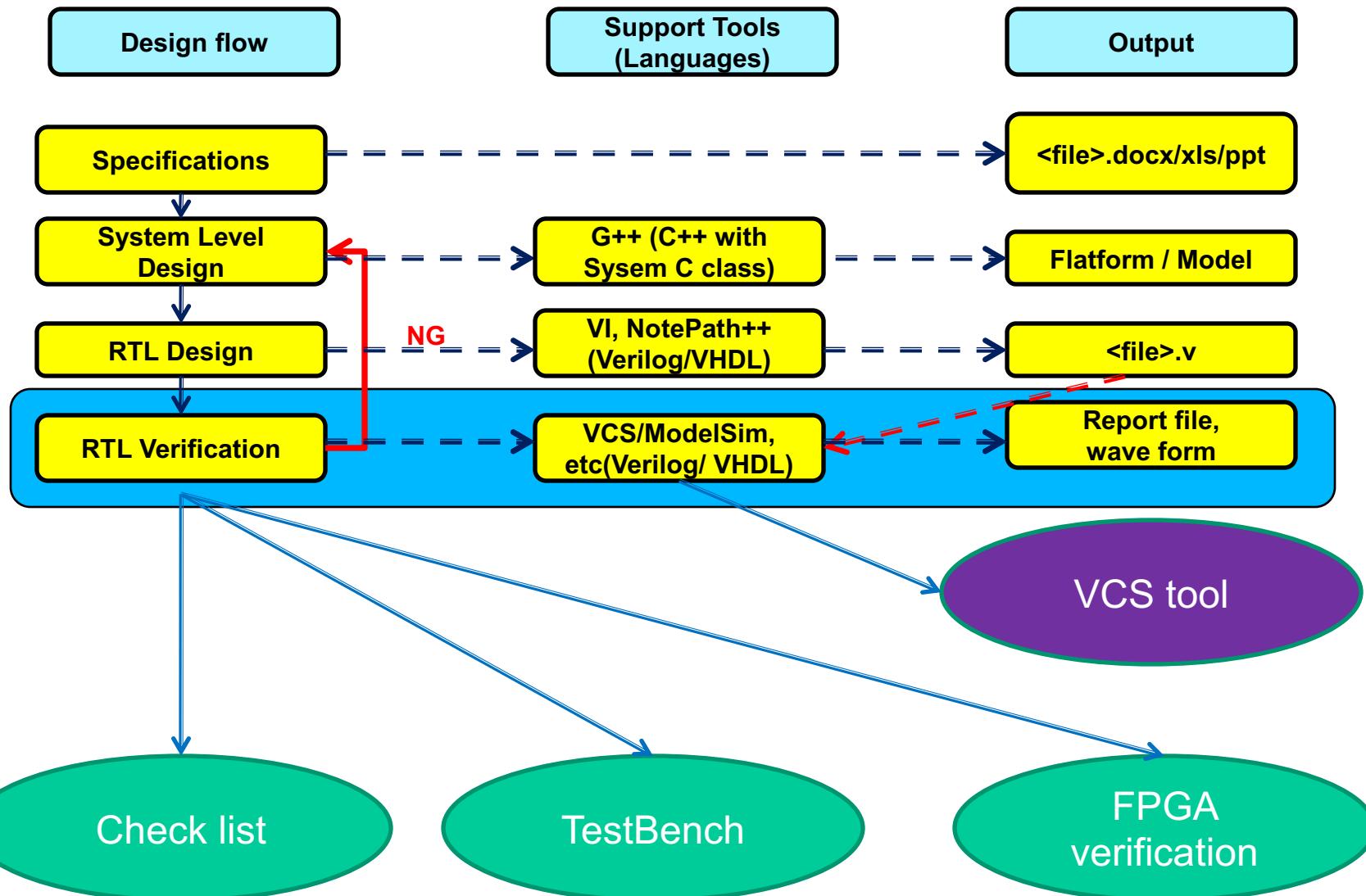
<b>System-Level Design</b>  Digital signal processing design, high-level synthesis, virtual platforms and analog/mixed-signal simulation.  <a href="#">MORE ▶</a>	<b>Verification</b>  High-performance system, RTL, equivalence checking, mixed-signal verification solutions, and Verification IP  <a href="#">MORE ▶</a>	<b>Implementation &amp; Signoff</b>  Advanced digital and custom IC and FPGA design solutions, including synthesis, test, physical implementation and verification, and signoff.  <a href="#">MORE ▶</a>
<b>Manufacturing</b>  Mask synthesis, mask data prep, lithography simulation and verification, and yield management.  <a href="#">MORE ▶</a>	<b>TCAD</b>  Process and device simulation tools for technology exploration, development and variability analysis.  <a href="#">MORE ▶</a>	<b>Optical Design</b>  Optical design and analysis software and engineering services.  <a href="#">MORE ▶</a>

- ❖ OS: Linux environment (ReadHat 5, Fedora 13 - 14)
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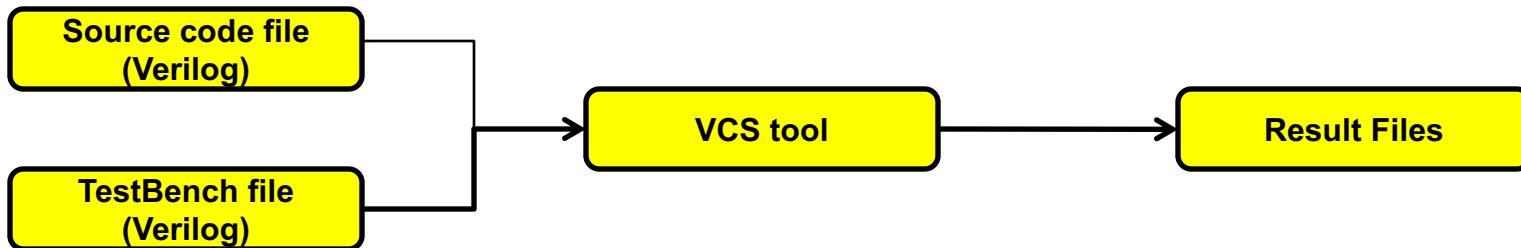
# VCS Tool In Design Flow



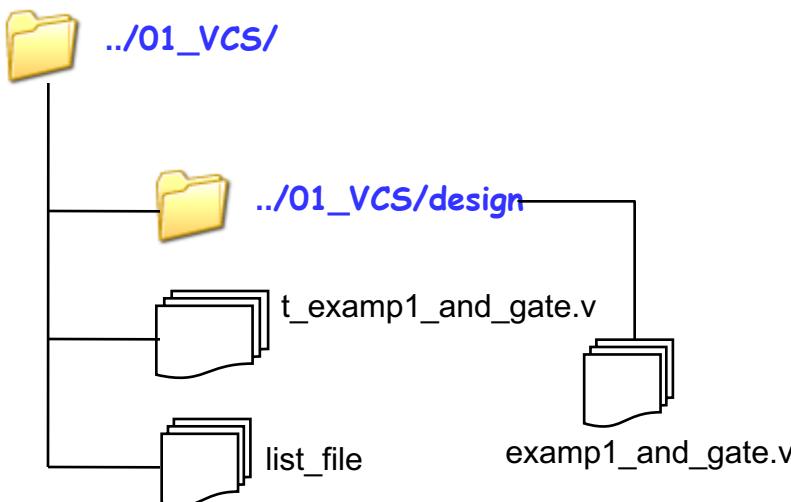
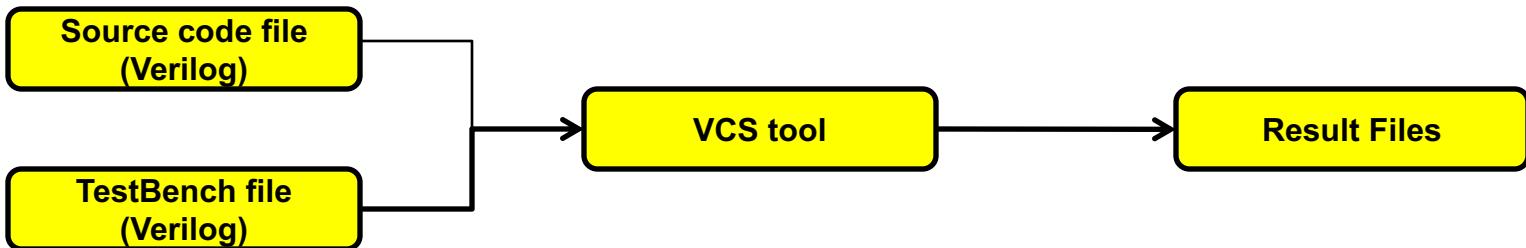
# VCS Tool In Design Flow



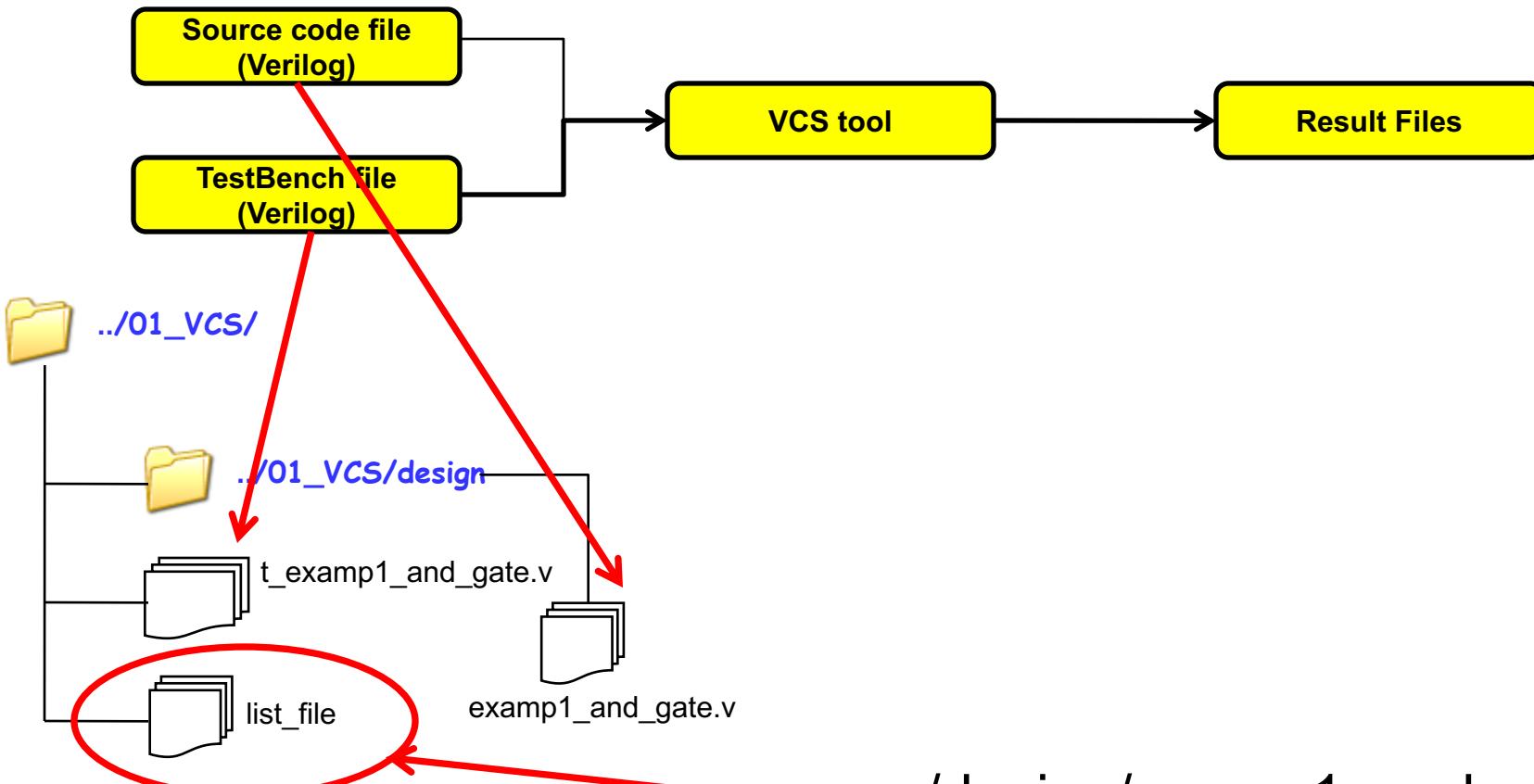
# How to run VCS?



# How to run VCS?

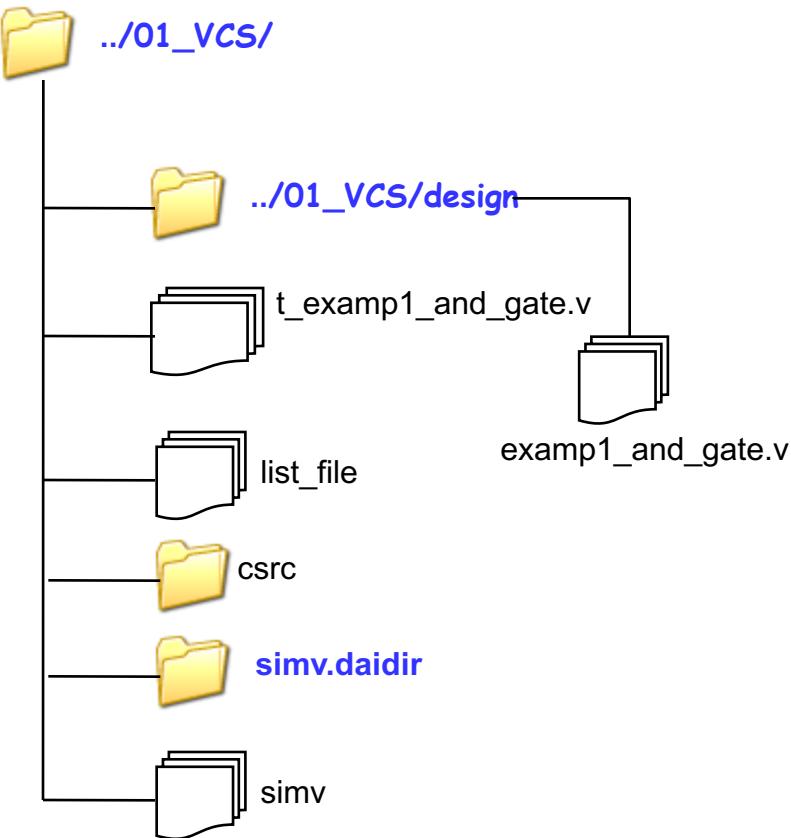
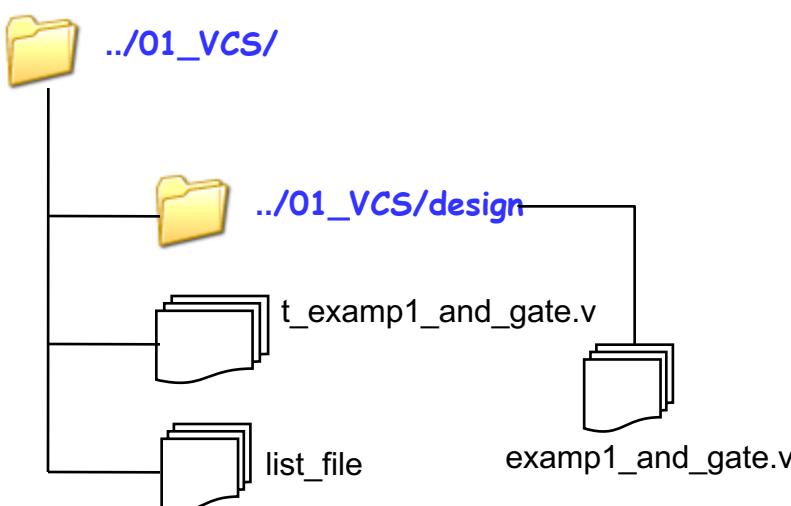
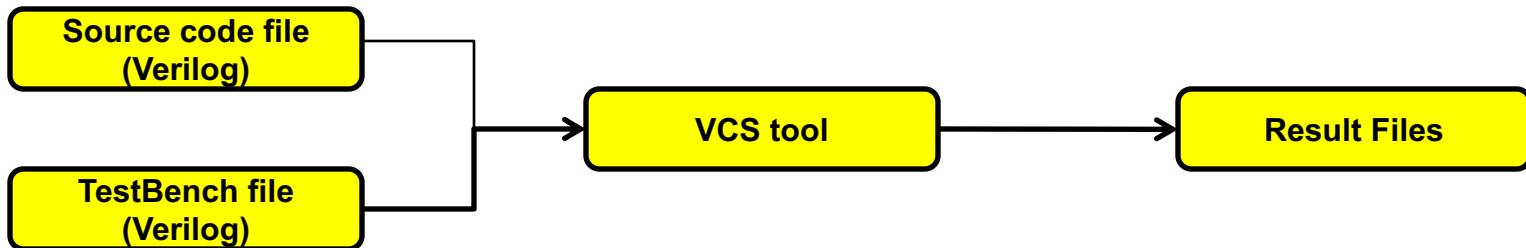


# How to run VCS?

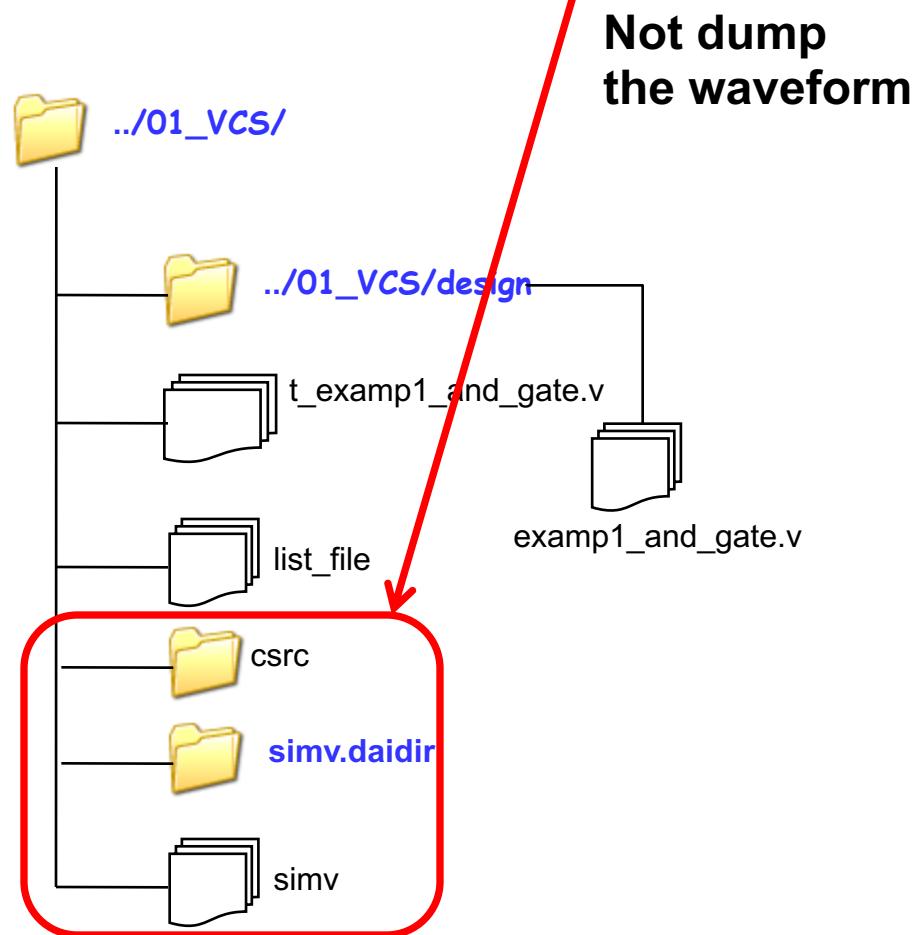
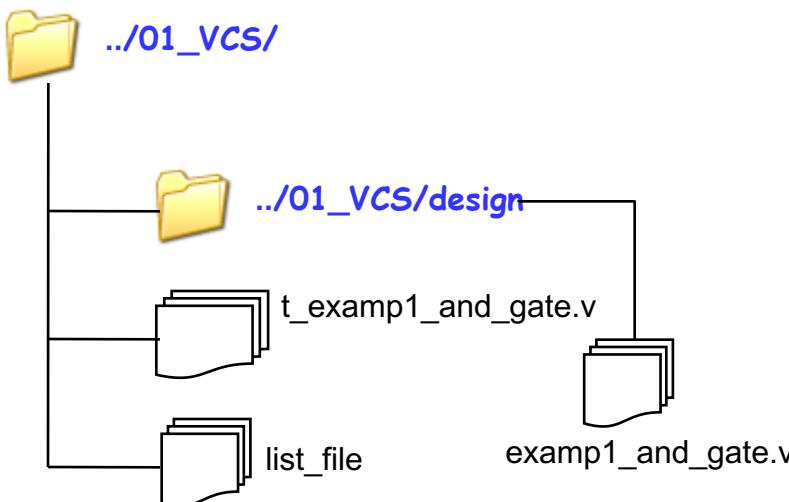
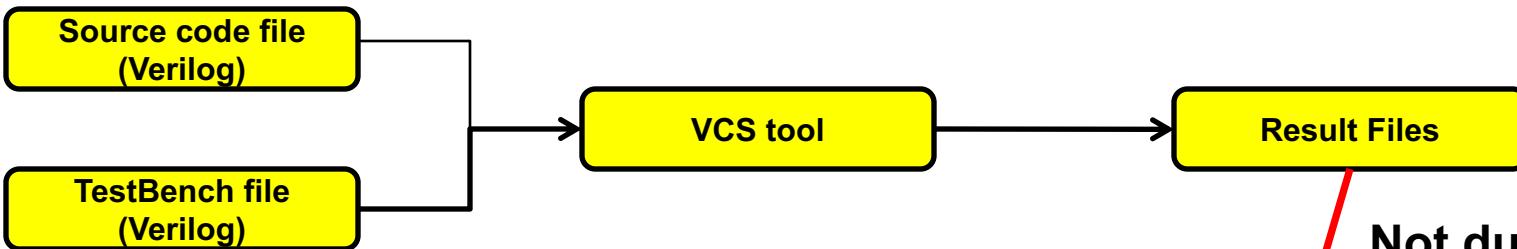


`./design/examp1_and_gate.v  
./t_exampl1_and_gate.v`

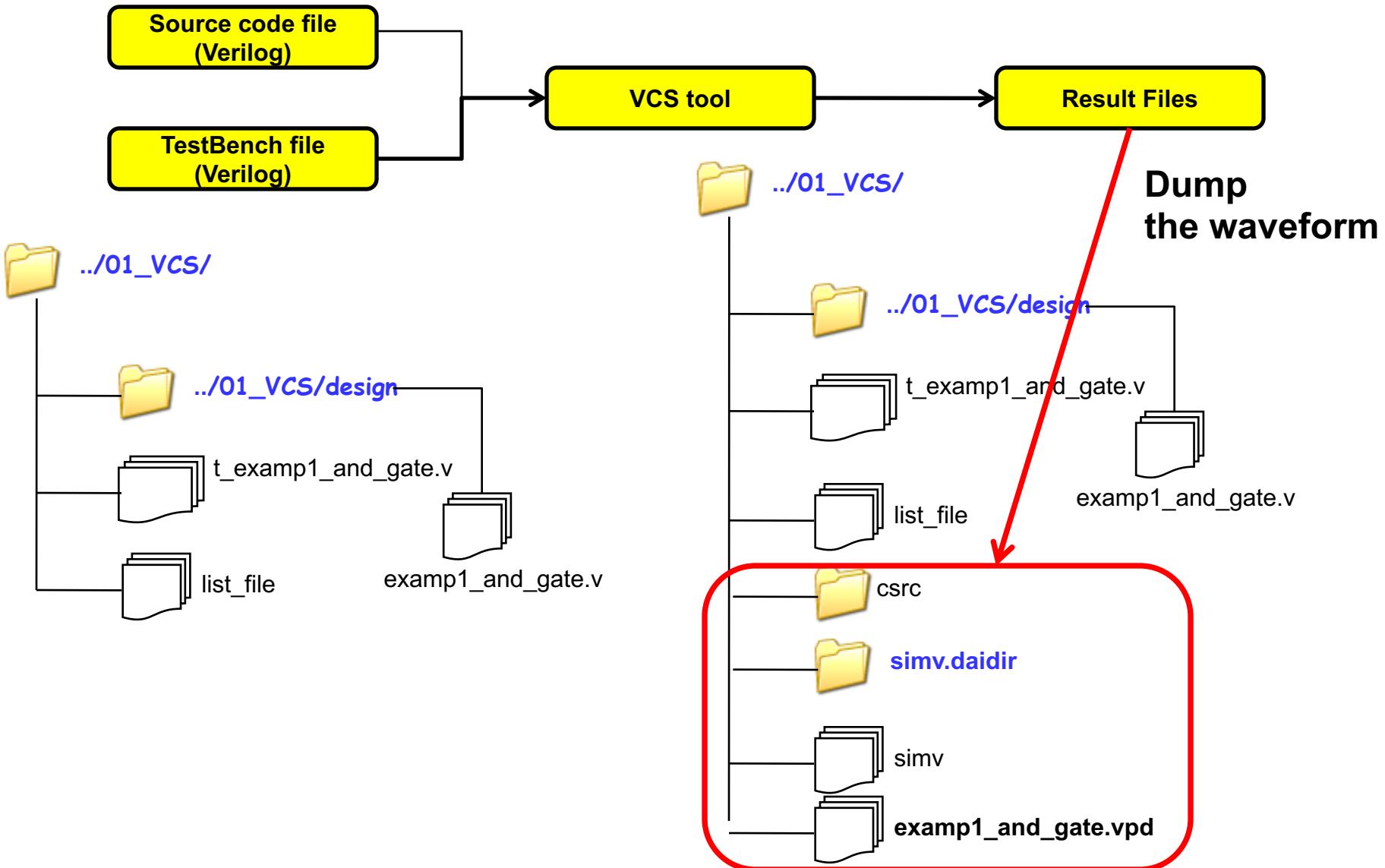
# How to run VCS?



# How to run VCS?



# How to run VCS?





# VCS Command

```
source /home/lampham/synopsys/licenses/linux/bin/s
```

```
vcs <mode option> <debug option> <file option> <version option> ...
```

Option Name	Command	Notes
Mode	-R	Command Mode
	-gui	GUI Mode
Debug	-debug	Export the waveform to debug
	-debug_all	Export the waveform to debug, line debug
File	-f <file>	Compile all files listed in the file
	-o <file>	Export the executed file (sim.v is default)
	-l <file>	Export the log file
Version	+v2K	Add the version 2000
Others	-sverilog	Compile the mis_language (Verilog & System Verilog)



# How to run VCS?

Applications Places System

Fri Mar 22, 10:53 PM phamdanglam

File Edit View Terminal Help

lampham@lampham:~/Work/06\_Lap/01\_VCS

```
/home/lampham/Work/06_Lap/01_VCS
design
[lampham@lampham 01_VCS]$ tree
.
`-- design
    `-- example_and_gate.v

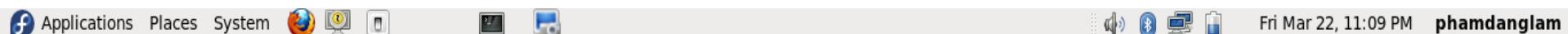
1 directory, 1 file
[lampham@lampham 01_VCS]$
```

**Folder/file hierarchy**

The screenshot shows a Linux desktop environment with a terminal window open. The terminal window title is 'lampham@lampham:~/Work/06\_Lap/01\_VCS'. The terminal content displays a directory tree with one directory ('design') and one file ('example\_and\_gate.v'). The command 'tree' is being run at the prompt. A red circle highlights the word 'tree', and a red arrow points from this circle to the text 'Folder/file hierarchy' in large blue font to the right of the terminal window.



# How to run VCS?



```
File Edit View Terminal Help  
/home/lampham/Work/06_Lap/01_VCS  
design  
[lampham@lampham 01_VCS]$ getlicense
```



A red oval highlights the command 'getlicense' in the terminal window, with a red arrow pointing from it to the text 'Get the synopsys license' located below the terminal.

**Get the synopsys license**



# How to run VCS?



Users of AIM\_ENCRYPT: (Uncounted, node-locked)

Users of aiu\_foundation: (Uncounted, node-locked)

Users of alien2lig\_all: (Uncounted, node-locked)

Users of ALTGEN1: (Uncounted, node-locked)

Users of ALTGEN2: (Uncounted, node-locked)

Users of amat-calib\_all: (Uncounted, node-locked)

Users of amga: (Uncounted, node-locked)

Users of amps: (Uncounted, node-locked)

Users of amps/cso: (Uncounted, node-locked)

Users of amps/pfx: (Uncounted, node-locked)

Users of amps/tr: (Uncounted, node-locked)

Users of AN-Impl3D\_all: (Uncounted, node-locked)

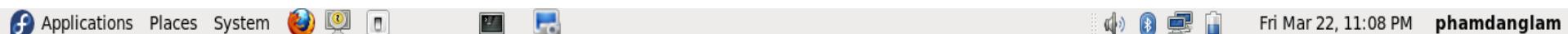
Users of any\_technology: (Uncounted, node-locked)

[lampham@lampham 01\_VCS]\$ █





# How to run VCS?



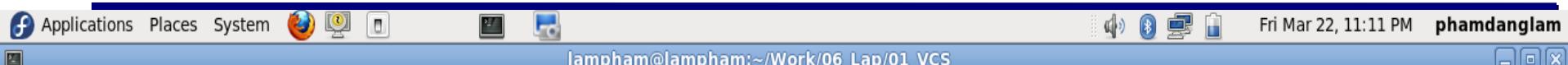
```
File Edit View Terminal Help  
/home/lampham/Work/06_Lap/01_VCS  
design  
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v
```

A red oval highlights the command `vcs -R design/examp1_and_gate.v`. A red arrow points from the text "Compile the design" below to this highlighted command.

**Compile the design**



# How to run VCS?



File Edit View Terminal Help

```
/home/lampham/Work/06_Lap/01_VCS  
design  
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v  
Chronologic VCS (TM)  
Version D-2010.06-SP1 -- Fri Mar 22 23:10:55 2013  
Copyright (c) 1991-2010 by Synopsys Inc.  
ALL RIGHTS RESERVED
```

This program is proprietary and confidential information of Synopsys Inc.  
and may be used and disclosed only as authorized in a license agreement  
controlling such use and disclosure.

```
Parsing design file 'design/examp1_and_gate.v'  
Top Level Modules:  
example1_and_gate  
No TimeScale specified
```

**The error line in design**

```
Error-[ISLHS] Illegal structural left hand side  
design/examp1_and_gate.v, 25
```

Following expression cannot be used on the left hand side of this  
assignment.

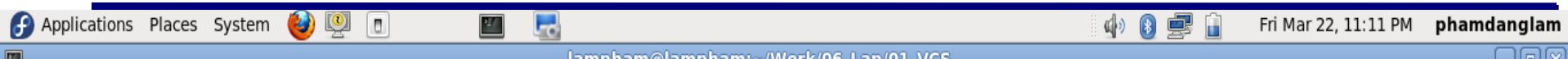
Expression: pre\_data\_out\_and\_gate  
Source info: assign pre\_data\_out\_and\_gate = (fist\_data\_in & second\_data\_in);

```
1 error  
CPU time: .076 seconds to compile  
[lampham@lampham 01_VCS]$
```

**Error in design**



# How to run VCS?



File Edit View Terminal Help

```
/home/lampham/Work/06_Lap/01_VCS  
design  
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v  
Chronologic VCS (TM)  
Version D-2010.06-SP1 -- Fri Mar 22 23:10:55 2013  
Copyright (c) 1991-2010 by Synopsys Inc.  
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```

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controlling such use and disclosure.

Parsing design file 'design/examp1\_and\_gate.v'

Top Level Modules:

example1\_and\_gate

No TimeScale specified

**Open the design**

```
Error-[ISLHS] Illegal structural left hand side  
design/examp1_and_gate.v, 25
```

Following expression cannot be used on the left hand side of this  
assignment.

Expression: pre\_data\_out\_and\_gate

Source info: assign pre\_data\_out\_and\_gate = (first\_data\_in & second\_data\_in);

1 error

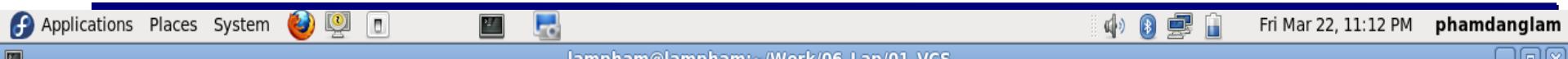
CPU time: .076 seconds to compile

```
[lampham@lampham 01_VCS]$ vi design/examp1_and_gate.v
```





# How to run VCS?



```
===== File name: example1_and_gate.v
===== Version: 1.0
===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
reg [DATA_WIDTH-1:0] pre_data_out_and_gate;

//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
```

Look up the error line



# How to run VCS?



```
//===== File name: example1_and_gate.v
//===== Version: 1.0
//===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
reg [DATA_WIDTH-1:0] pre_data_out_and_gate;

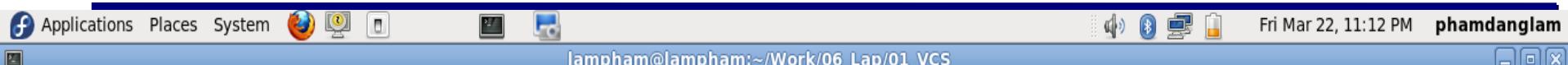
//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
/pre_data_out_and_gate
```

Conflict the type of variable



# How to run VCS?



```
===== File name: example1_and_gate.v
===== Version: 1.0
===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
reg [DATA_WIDTH-1:0] pre_data_out_and_gate;

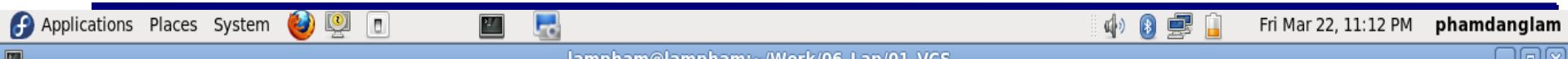
//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
/pre_data_out_and_gate
```

This should be “wire” type



# How to run VCS?



```
File Edit View Terminal Help
//===== File name: example1_and_gate.v
//===== Version: 1.0
//===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg   [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
wire   [DATA_WIDTH-1:0] pre_data_out_and_gate;

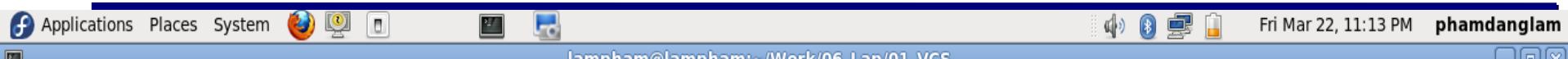
//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
:wq
```

**Store and quit**



# How to run VCS?



File Edit View Terminal Help

```
/home/lampham/Work/06_Lap/01_VCS  
design  
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v  
Chronologic VCS (TM)  
Version D-2010.06-SP1 -- Fri Mar 22 23:10:55 2013  
Copyright (c) 1991-2010 by Synopsys Inc.  
ALL RIGHTS RESERVED
```

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and may be used and disclosed only as authorized in a license agreement  
controlling such use and disclosure.

Parsing design file 'design/examp1\_and\_gate.v'

Top Level Modules:

example1\_and\_gate

No TimeScale specified

Error-[ISLHS] Illegal structural left hand side  
design/examp1\_and\_gate.v, 25

Following expression cannot be used on the left hand side of this  
assignment.

Expression: pre\_data\_out\_and\_gate

Source info: assign pre\_data\_out\_and\_gate = (fist\_data\_in & second\_data\_in);

1 error

CPU time: .076 seconds to compile

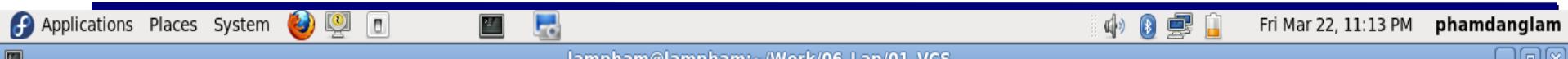
[lampham@lampham 01\_VCS]\$ vi design/examp1\_and\_gate.v

[lampham@lampham 01\_VCS]\$ vcs -R design/examp1\_and\_gate.v

**Compile again**



# How to run VCS?



```
[lampham@lampham 01_VCS]$ vi design/exmpl_and_gate.v
[lampham@lampham 01_VCS]$ vcs -R design/exmpl_and_gate.v
    Chronologic VCS (TM)
Version D-2010.06-SP1 -- Fri Mar 22 23:13:12 2013
Copyright (c) 1991-2010 by Synopsys Inc.
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```

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controlling such use and disclosure.

Parsing design file 'design/exmpl\_and\_gate.v'

Top Level Modules:

example1\_and\_gate

No TimeScale specified

Starting vcs inline pass...

1 module and 0 UDP read.

recompiling module example1\_and\_gate

```
if [ -x ..simv ]; then chmod -x ..simv; fi
g++ -o ..simv -melf_i386 _vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_l.o      rmapats_mop.o rmapats.o      /home/l
ampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libvirsim.so /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libr
terrorinf.so /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libsnpsmalloc.so   /home/lampham/synopsys/VCS_
D-2010.06-SP1/linux/lib/libvcsnew.so      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/vcs_save_restore_
new.o /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
..simv up to date
```

Chronologic VCS simulator copyright 1991-2010

Contains Synopsys proprietary information.

Compiler version D-2010.06-SP1; Runtime version D-2010.06-SP1; Mar 22 23:13 2013

**Finish compile**

V C S   S i m u l a t i o n   R e p o r t

Time: 0

CPU Time: 0.030 seconds; Data structure size: 0.0Mb

Fri Mar 22 23:13:17 2013

CPU time: .082 seconds to compile + .061 seconds to elab + .377 seconds to link + .119 seconds in simulation

[lampham@lampham 01\_VCS]\$ █



# How to run VCS?



```
File Edit View Terminal Help  
/home/lampham/Work/06_Lap/01_VCS  
csimc design simv simv.daidir  
[lampham@lampham 01_VCS]$ ll  
total 516  
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csimc ←  
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 design ←  
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv ←  
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir ←  
[lampham@lampham 01_VCS]$
```

The output files



# How to run VCS?

Applications Places System

Fri Mar 22, 11:15 PM phamdanglam

File Edit View Terminal Help

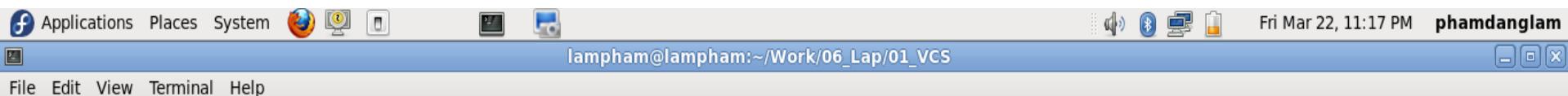
lampham@lampham:~/Work/06\_Lap/01\_VCS

```
/home/lampham/Work/06_Lap/01_VCS
csrc design simv simv.daidir
[lampham@lampham 01_VCS]$ ll
total 516
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 design
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
[lampham@lampham 01_VCS]$ vi t_exampl_and_gate.v
[lampham@lampham 01_VCS]$
```

Compose the testbench



# How to run VCS?



**Copy the same content  
from the other file**

```
:r /home/lampham/Work/01_Speech_Reg/02_Developpt/01_Floating_Point_Mul/t_floating_point_muliple.v
```



# How to run VCS?

Applications Places System

Fri Mar 22, 11:27 PM phamdanglam

File Edit View Terminal Help

```
/home/lampham/Work/06_Lap/01_VCS
csrc design simv simv.daidir t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 520
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:19 design
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
-rw-rw-r--. 1 lampham lampham 1519 Mar 22 23:27 t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ vi list_file
```

A red circle highlights the command "vi list\_file" in the terminal window. A red arrow points from the text "Compose the list file" below to the highlighted command.

Compose the list file



# How to run VCS?

./t\_exampl1\_and\_gate.v  
./design/exampl1\_and\_gate.v

The list file includes :

- + Design file
- + Testbench file

:wq



# How to run VCS?

Applications Places System

Fri Mar 22, 11:29 PM phamdanglam

File Edit View Terminal Help

lampham@lampham:~/Work/06\_Lap/01\_VCS

```
/home/lampham/Work/06_Lap/01_VCS
csrc design list_file simv simv.daidir t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 524
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:27 design
-rw-rw-r--. 1 lampham lampham 49 Mar 22 23:29 list_file
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
-rw-rw-r--. 1 lampham lampham 1319 Mar 22 23:27 t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ █
```

Finish testbench and list file

lampham@lampham:... lampham@lampham:... r0000... .v (New Volum...)



# How to run VCS?

Applications Places System  Fri Mar 22, 11:29 PM phamdanglam

File Edit View Terminal Help

lampham@lampham:~/Work/06\_Lap/01\_VCS

```
/home/lampham/Work/06_Lap/01_VCS
csrc design list_file simv simv.daidir t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 524
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:27 design
-rw-rw-r--. 1 lampham lampham 49 Mar 22 23:29 list_file
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
-rw-rw-r--. 1 lampham lampham 1319 Mar 22 23:27 t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ vcs -R -debug_all -f list_file
```

A red oval highlights the command `vcs -R -debug_all -f list_file`, and a red arrow points from the text "Compose the design and testbench" below to this highlighted command.

Compose the design and testbench

lampham@lampham:... lampham@lampham:... r0000\_and\_r0101\_to\_r... test\_top.v (New Volum...)



# How to run VCS?

Applications Places System

Fri Mar 22, 11:47 PM phamdanglam

File Edit View Terminal Help

```
Parsing design file './design/examp1_and_gate.v'
Top Level Modules:
    t_examp1_and_gate
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module t_examp1_and_gate because:
    This module or some inlined child module(s) has/have been modified.
if [ -x ..simv ]; then chmod -x ..simv; fi
g++ -o ..simv -melf_i386 _vcsobj_1.l.o 5NrI.d.o 5NrIB.d.o SIM_l.o      rmapats_mop.o rmapats.o      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libvirsim.so
/home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/librerrorinf.so /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libsnpsmalloc.so      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libvcsnew.so      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/vcs_save_restore_new.o /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libctype-stubs_32.a -ldl -lm -lc -lpthread -ldl
..simv up to date
Chronologic VCS simulator copyright 1991-2010
Contains Synopsys proprietary information.
Compiler version D-2010.06-SP1; Runtime version D-2010.06-SP1; Mar 22 23:47 2013

VCD+ Writer D-2010.06-SP1 Copyright (c) 1991-2010 by Synopsys Inc.
time=      0, system_clock=0, system_rst_n=x, t_first_data_in:xxxxxxxx, t_second_data_in:xxxxxxxx, data_out_and_gate=xxxxxxxx
time=      1, system_clock=0, system_rst_n=0, t_first_data_in:xxxxxxxx, t_second_data_in:xxxxxxxx, data_out_and_gate=00000000
time=     11, system_clock=0, system_rst_n=1, t_first_data_in:xxxxxxxx, t_second_data_in:xxxxxxxx, data_out_and_gate=00000000
time=    21, system_clock=0, system_rst_n=1, t_first_data_in:11010101, t_second_data_in:10101010, data_out_and_gate=00000000
time=    50, system_clock=1, system_rst_n=1, t_first_data_in:11010101, t_second_data_in:10101010, data_out_and_gate=10000000
time=   100, system_clock=0, system_rst_n=1, t_first_data_in:11010101, t_second_data_in:10101010, data_out_and_gate=10000000

$finish called from file "./t examp1_and_gate.v", line 48.
$finish at simulation time          121
    V C S   S i m u l a t i o n   R e p o r t
Time: 121
CPU Time: 0.030 seconds; Data structure size: 0.0Mb
Fri Mar 22 23:47:28 2013
CPU time: .079 seconds to compile + .041 seconds to elaboration + .164 seconds to link + .089 seconds in simulation
[lampham@lampham 01_VCS]$
```

**Simulation result**

**Finish the compile**

lampham@lampham:... lampham@lampham:... [r0000\_.v (New Volum...]



# How to run VCS?

Applications Places System

Fri Mar 22, 11:48 PM phamdanglam

File Edit View Terminal Help

/home/lampham/Work/06\_Lap/01\_VCS

```
csrc design exempl1_and_gate.vpd list_file simv simv.daidir t_exempl1_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 572
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:47 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:42 design
-rw-rw-r--. 1 lampham lampham 1849 Mar 22 23:47 exempl1_and_gate.vpd
-rw-rw-r--. 1 lampham lampham 49 Mar 22 23:37 list_file
-rwxrwxr-x. 1 lampham lampham 558594 Mar 22 23:47 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:47 simv.daidir
-rw-rw-r--. 1 lampham lampham 1451 Mar 22 23:47 t_exempl1_and_gate.v
[lampham@lampham 01_VCS]$
```

A red arrow points from the text "Use DVE tool to open the wave form" to the file "exempl1\_and\_gate.vpd" in the terminal output.

**Use DVE tool to open the wave form**

File [r0000\_].v (New Volum...)



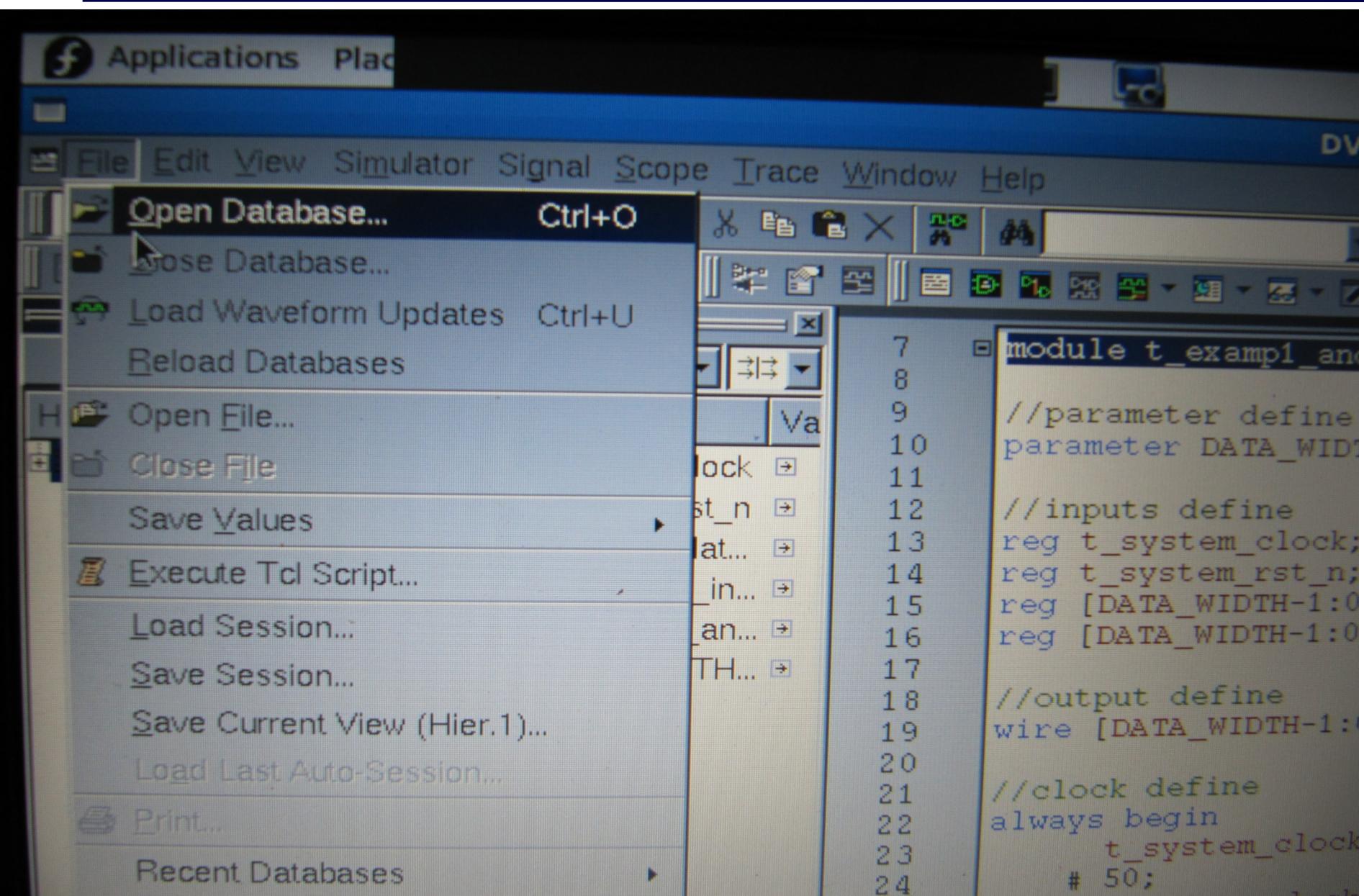
# How to load the wave form?



```
File Edit View Terminal Help  
/home/lampham/Work/06_Lap/01_VCS  
csrc design examp1_and_gate.vpd list_file simv simv.daidir t_examp1_and_gate.v  
[lampham@lampham 01_VCs]$ dve &
```

**Use DVE tool to open the wave form**

# How to load the wave form?





# How to load the wave form?

DVE - TopLevel.1 - [Hier.1]

Trace Window Help

X E D C P S R F G H I J K L M N O P Q R S T U V W X Y Z

module t\_exampl\_and\_gate;

//parameter define

parameter DATA\_WIDTH = 8;

//inputs define

Open Database

Look in: /home/lampham/Work/06\_Lap/01\_VCS/

File name: examp1\_and\_gate.vpd

File type: Database Files (\*.vpd; \*.vcd; \*.dump; \*.evcd)

Designator: V2

Time range from: to: Time Range

t\_exampl\_and\_gate.v



# How to load the wave form?

Screenshot of a Cadence Design System (VCS) DVE (Digital Verification Environment) interface.

The title bar shows: DVE - TopLevel.1 - [Source.1 - t\_exampl\_and\_gate: t\_exampl\_and\_gate.v].

The menu bar includes: File, Edit, View, Simulator, Signal, Scope, Trace, Window, Help.

The toolbar contains various simulation and analysis icons.

The main window displays the Verilog source code for the module `t_exampl_and_gate`:

```
7 module t_exampl_and_gate;
8
9 //parameter define
10 parameter DATA_WIDTH = 8;
11
12 //inputs define
13 reg t_system_clock;
14 reg t_system_rst_n;
15 reg [DATA_WIDTH-1:0] t_second_data_in;
16 reg [DATA_WIDTH-1:0] t_first_data_in;
17
18 //output define
19 wire [DATA_WIDTH-1:0] t_data_out_and_gate;
20
21 //clock define
22 always begin
23     t_system_clock = 1'b0;
24     # 50;
25     t_system_clock = 1'b1;
26     # 50;
27 end
28
```

The code is located at `/home/lampham/Work/06_Lap/01_VCS//t_exampl_and_gate.v`.

The bottom status bar shows: dve> .v (New Volum... DVE - TopLevel.1 - [So...]



# How to load the wave form?

The screenshot shows a logic simulation software interface with a menu bar (File, Edit, View, Simulator, Signal, Scope, Trace, Window, Help) and various toolbars. A signal named 'V1' is selected, and its context menu is open. The menu items include:

- Copy
- Scope Navigator
- Show Source
- Show Schematic
- Show Path Schematic
- Add To Waves
- Add To Lists
- Add To Groups
- Add To Watches
- Show In Class Browser
- Show Full Hierarchy
- Move Up
- Move Down
- Expand by Levels

The "Add To Waves" item is highlighted. Below the menu, a "New Wave View" option is selected from a submenu. The main workspace displays a Verilog code snippet:

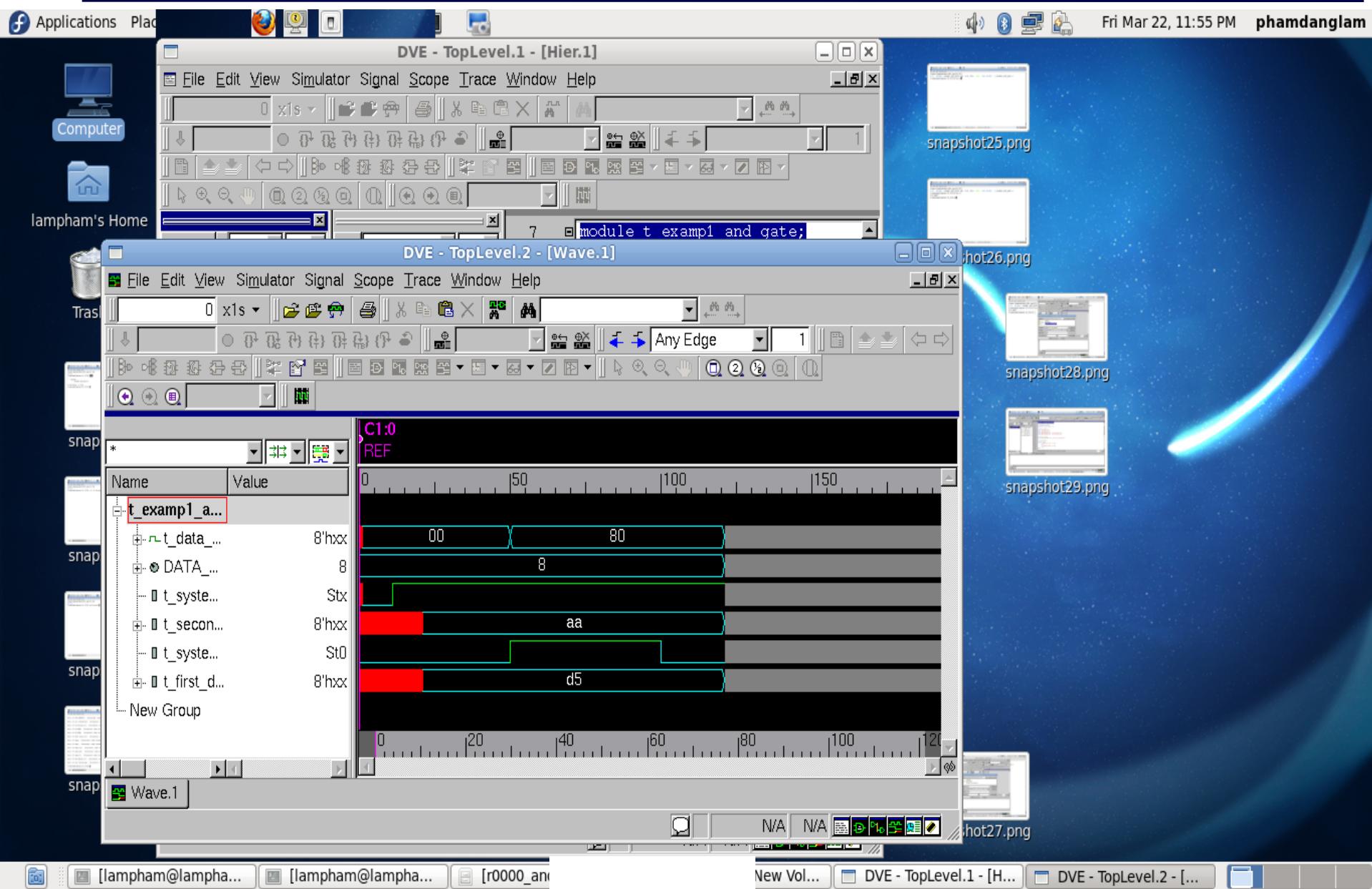
```
module t_exampl_and_gate;
//parameter define
parameter DATA_WIDTH = 8;
//inputs define
reg t_system_clock;
reg t_system_rst_n;
reg [DATA_WIDTH-1:0] t_data_in;
reg [DATA_WIDTH-1:0] t_data_out;
//output define
output [DATA_WIDTH-1:0] t_data_out;
begin
    # 50;
    t_system_clock = 1'b0;
    # 50;
end

```

The code defines a module `t_exampl_and_gate` with parameters, inputs, and outputs. It includes a `begin` block with two `# 50;` statements.

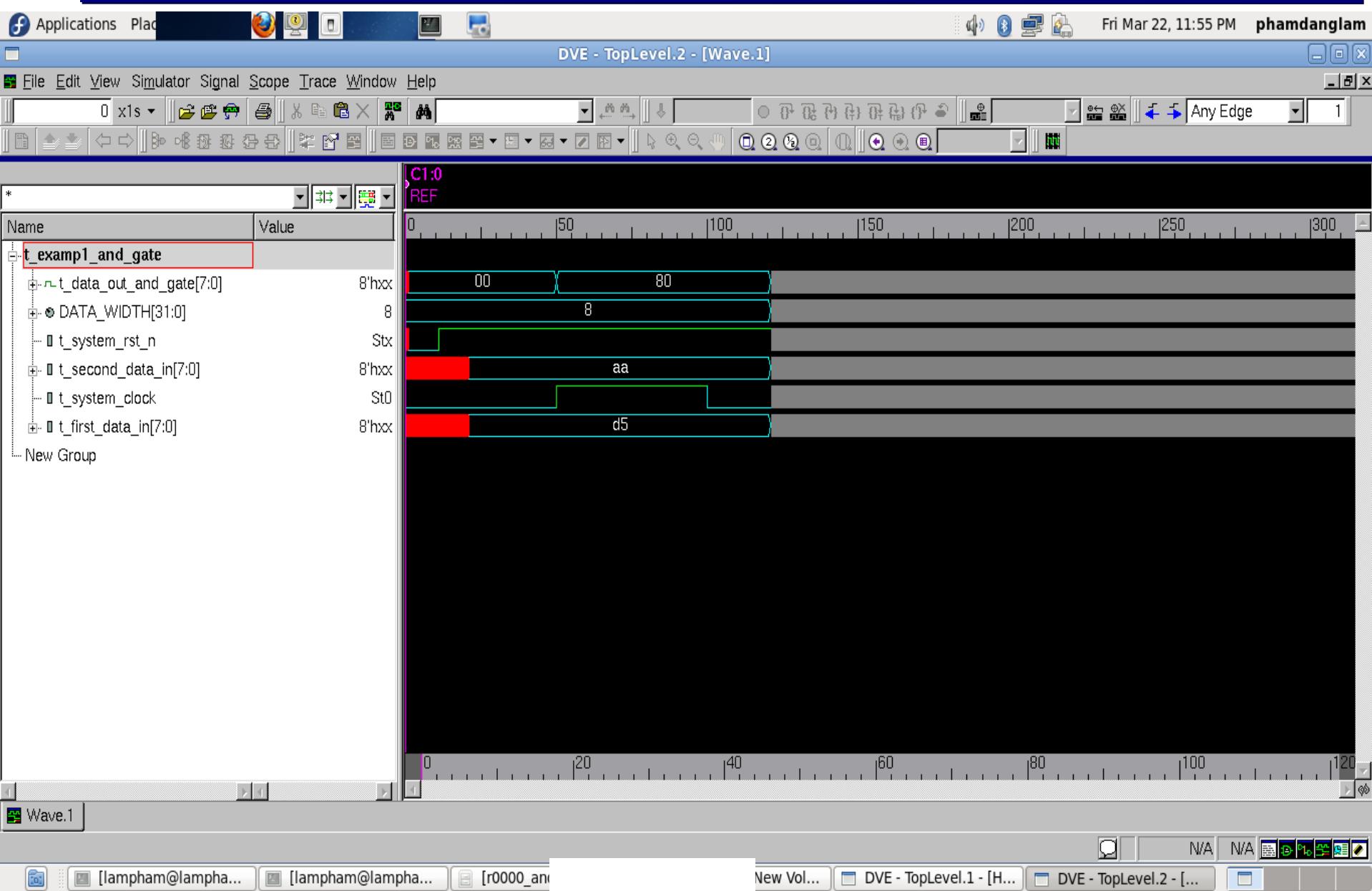


# How to load the wave form?





# How to load the wave form?





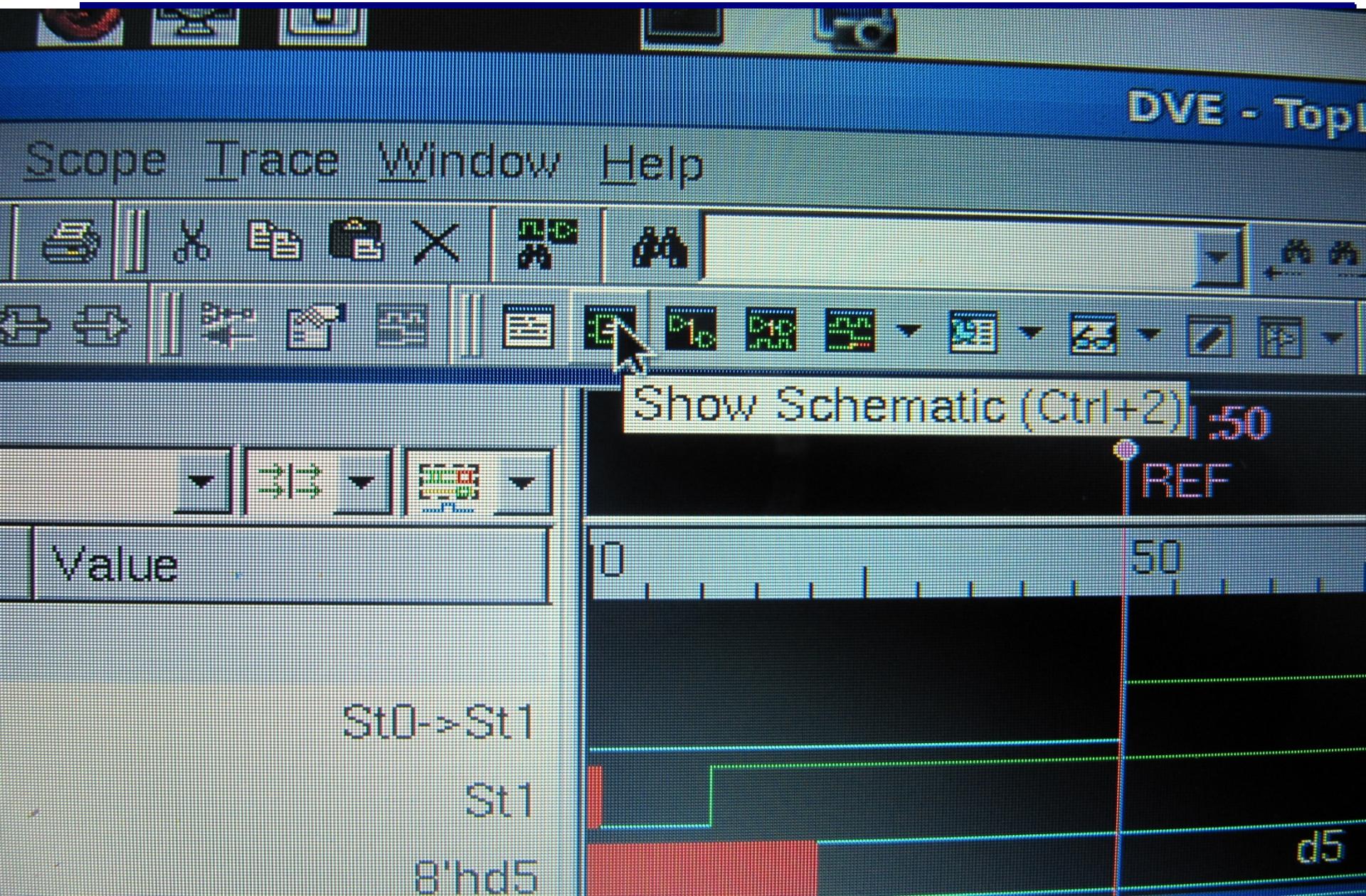
# How to load the wave form?

The screenshot shows a logic simulation interface with the following details:

- Title Bar:** DVE - TopLevel.2 - [Wave.1]
- Toolbar:** Includes icons for file operations, simulation controls, and analysis.
- Menu Bar:** File, Edit, View, Simulator, Signal, Scope, Trace, Window, Help.
- Signal List:** A tree view of signals under the group `t_exampl_and_gate`.
  - `t_system_clock`: Value St0->St1
  - `t_system_rst_n`: Value St1
  - `t_first_data_in[7:0]`: Value 8'hd5
  - `t_second_data_in[7:0]`: Value 8'haa
  - `t_data_out_and_gate[7:0]`: Value 8'h00->8'h80
    - `t_data_out_and_gate[7]`: Value St0->St1
    - `t_data_out_and_gate[6]`: Value St0
    - `t_data_out_and_gate[5]`: Value St0
    - `t_data_out_and_gate[4]`: Value St0
    - `t_data_out_and_gate[3]`: Value St0
    - `t_data_out_and_gate[2]`: Value St0
    - `t_data_out_and_gate[1]`: Value St0
    - `t_data_out_and_gate[0]`: Value St0
- Waveform View:** Displays multiple signal波形. The top two signals are labeled `C1:50` and `REF`, and `C2:100` and `(50)`. The `t_second_data_in[7:0]` signal shows values `d5` and `aa`. The `t_data_out_and_gate[7:0]` group shows a sequence of values starting from `00` and transitioning to `80`.
- Bottom Status Bar:** Shows the current simulation time as `New Vol...`, the current window as `DVE - TopLevel.1 - [H...]`, and the current waveform as `DVE - TopLevel.2 - [...]`.



# How to load the wave form?





# How to load the wave form?

Screenshot of DVE (Digital Verification Environment) showing a logic schematic and waveform viewer.

The schematic window displays a logic circuit for an AND gate. It includes inputs: system\_clock, system\_rst\_n, fist\_data\_in[7:0], second\_data\_in, data\_out\_and\_gate, pre\_data\_out..., and DATA\_WIDTH...; and outputs: system\_clock, system\_rst\_n, ~nd\_data\_in, \*p@25, fist\_data\_in, ~a\_out\_and\_gate, and data\_out\_and\_gate. The circuit uses NOT gates (~) and AND gates (and\_gate).

The waveform viewer shows signals over time. The top row shows system\_clock and system\_rst\_n. The bottom row shows fist\_data\_in, second\_data\_in, ~nd\_data\_in, fist\_data\_in, ~a\_out\_and\_gate, and data\_out\_and\_gate. The data\_out\_and\_gate signal is labeled with a value of 1 at the end of the waveform.

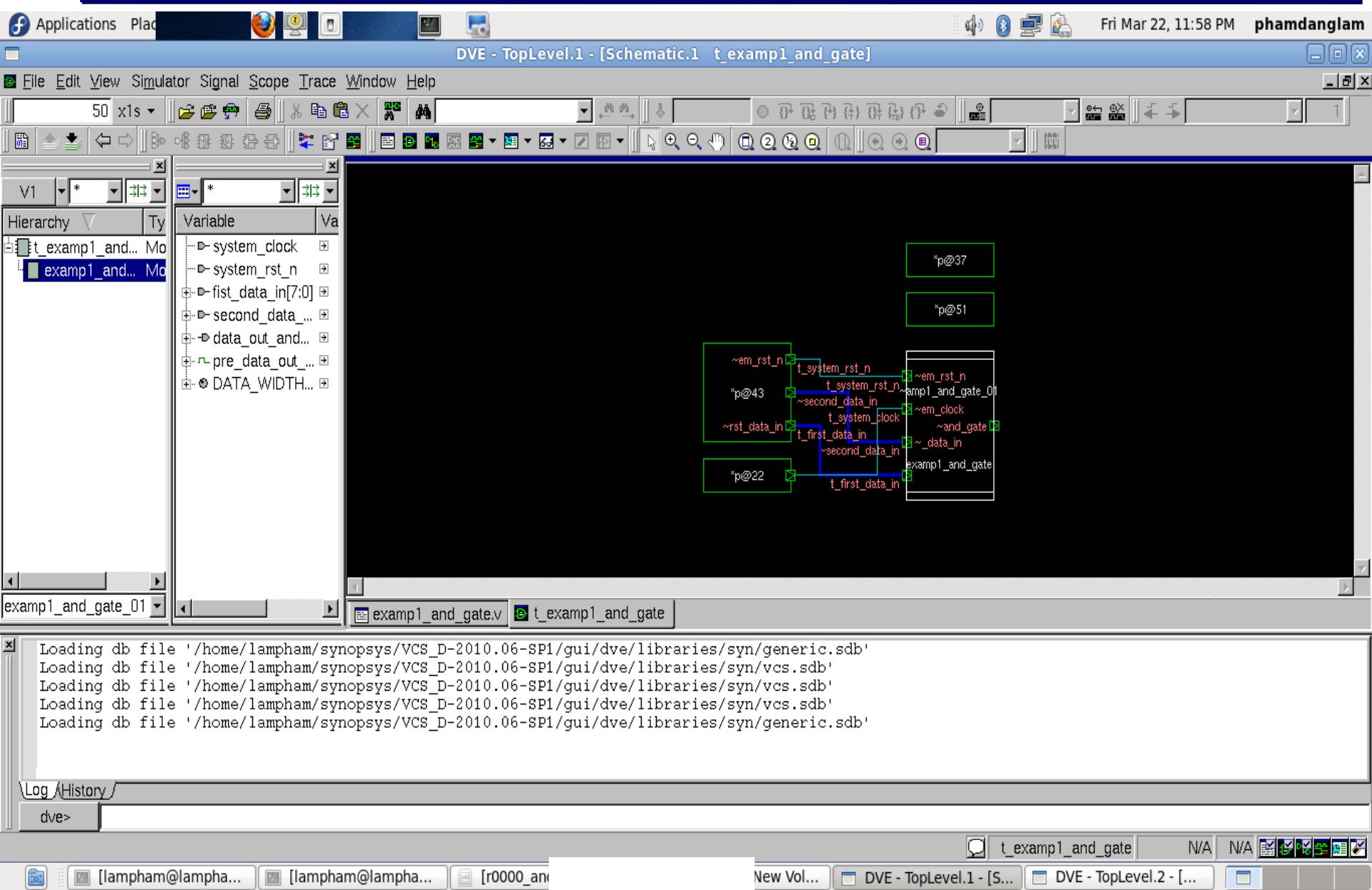
The status bar at the bottom shows log messages about library loading:

```
>Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/generic.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/generic.sdb'
```

The bottom left corner shows the command line interface:

```
dve>
```

# How to load the wave form?





# Q & A