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# ASIC Design Flow

Cell Base Design Flow

Custom Design Flow

# FPGA Design Flow

# Semiconductor Revenue

[https://en.wikipedia.org/wiki/Semiconductor\\_sales\\_leaders\\_by\\_year](https://en.wikipedia.org/wiki/Semiconductor_sales_leaders_by_year)

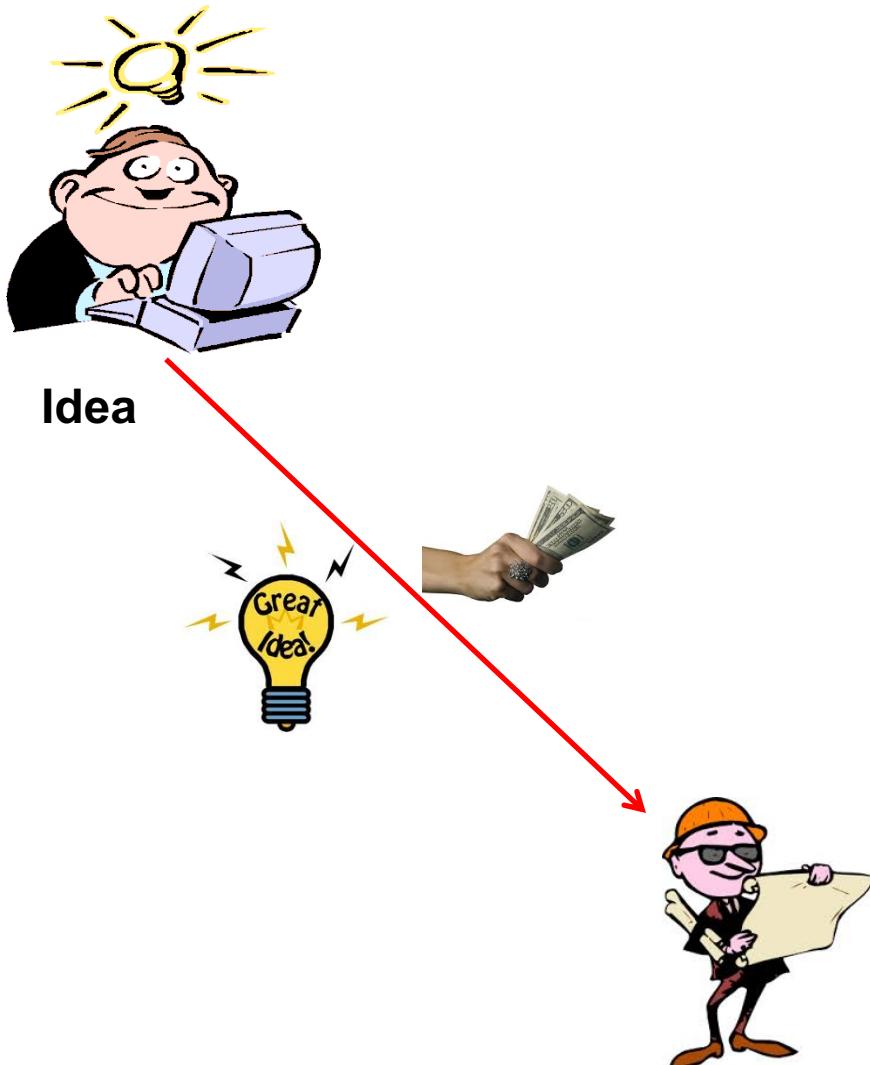
Rank 2014	Rank 2013	Company	Country of origin	Revenue (million \$ USD)	2014/2013 changes	Market share
1	1	Intel Corporation	USA	49 964	+6.3%	14.1%
2	2	Samsung Electronics	South Korea	38 273	+15.6%	10.8%
3	3	Qualcomm	USA	19 266	+11.9%	5.5%
4	4	Micron Technology	USA	16 389	+16.1%	4.6%
5	5	SK Hynix	South Korea	15 737	+22.9%	4.5%
6	6	Texas Instruments	USA	11 420	+6.8%	3.5%
7	7	Toshiba Semiconductor	Japan	8 496	-9.6%	2.4%
8	8	Broadcom	USA	8 387	+2.5%	2.4%
9	9	STMicroelectronics	France Italy	7 395	-8.5%	2.1%
10	15	MediaTek	Taiwan	7 194	+57.5%	2.0%
11	10	Renesas Electronics	Japan	6 910	-13.3%	2.0%
12	11	SanDisk	USA	6 116	+5.6%	1.7%
13	12	Infineon Technologies	Germany	6 071	+17.4%	1.7%
14	14	NXP	Netherlands	5 457	+16.7%	1.5%
15	23	Avago	USA	5 423	+107.9%	1.5%
16	13	AMD	USA	5 388	+4.6%	1.5%
17	17	Freescale Semiconductor	USA	4 560	+15.0%	1.3%
18	16	Sony	Japan	4 528	+1.5%	1.3%
19	18	NVIDIA	USA	4 007	+9.4%	1.1%
20	19	Marvell Technology Group	USA	3 812	+12.0%	1.1%

# ASIC Design Subject



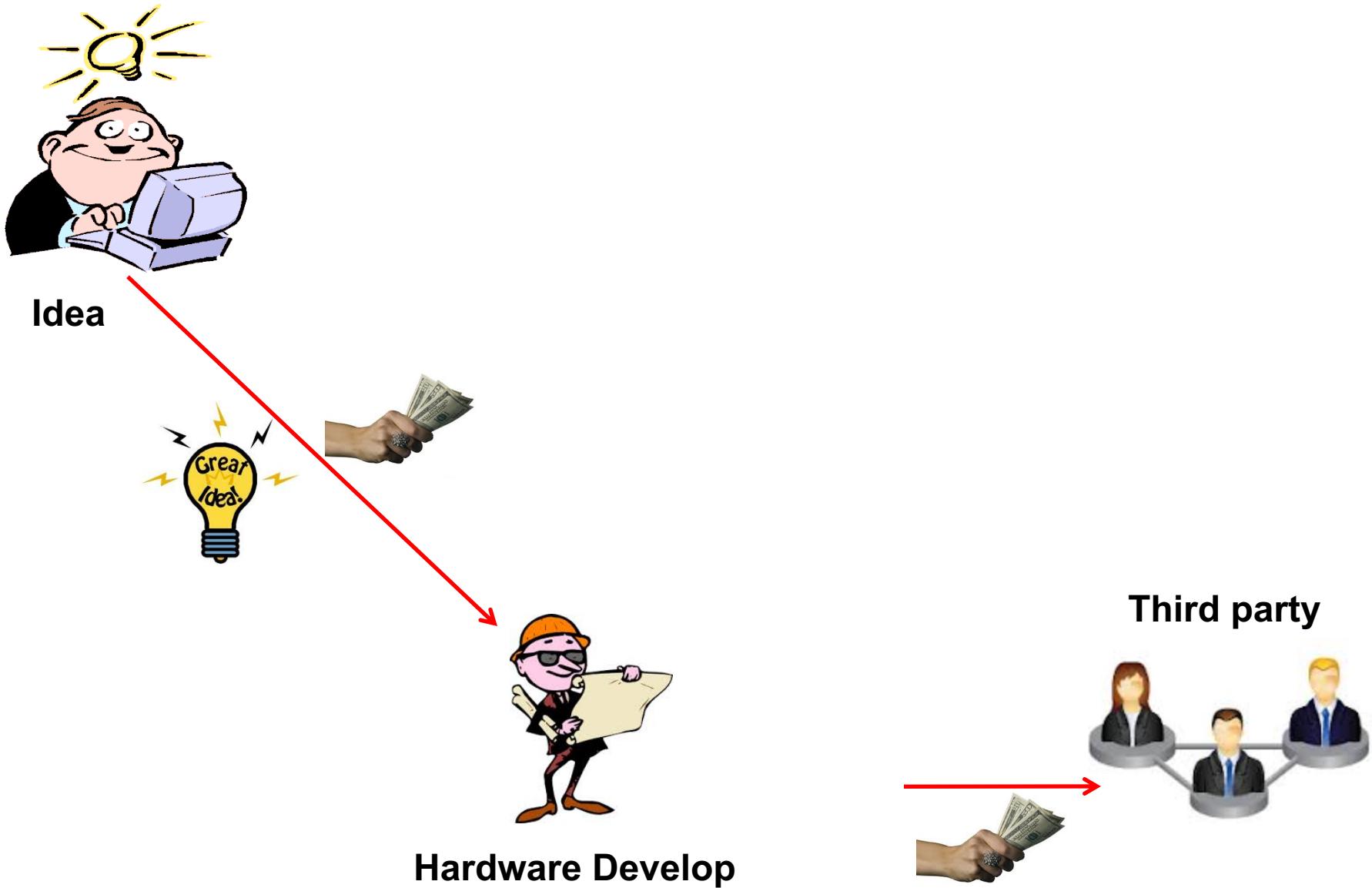
Idea

# ASIC Design Subject

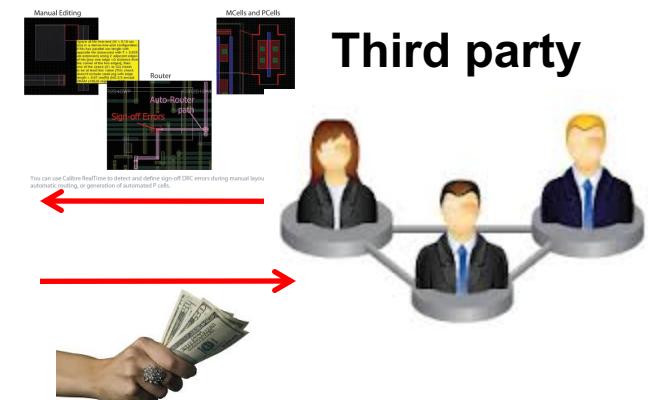
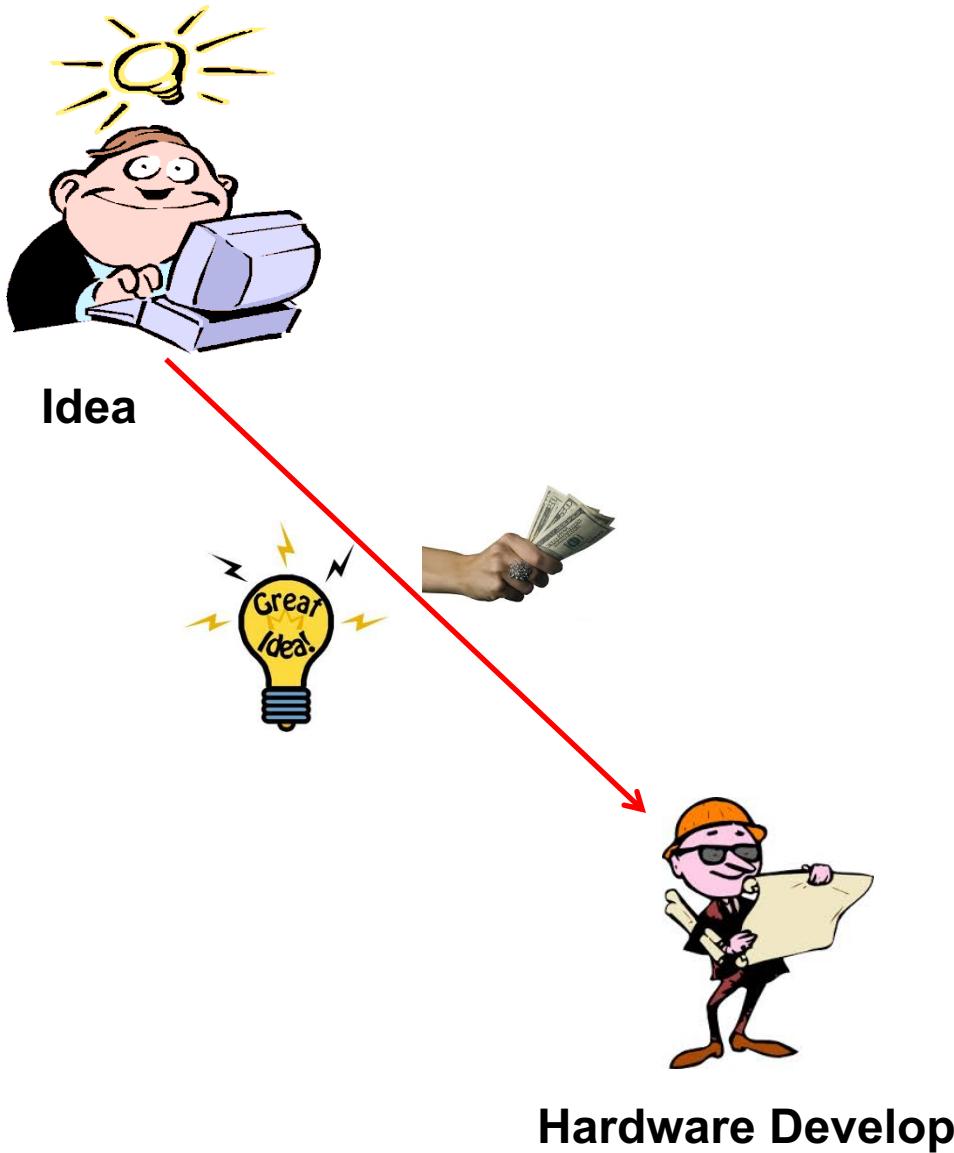


Hardware Develop

# ASIC Design Subject



# ASIC Design Subject



# ASIC Design Subject

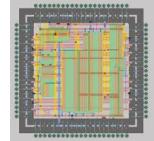


Idea



Hardware Develop

Layout



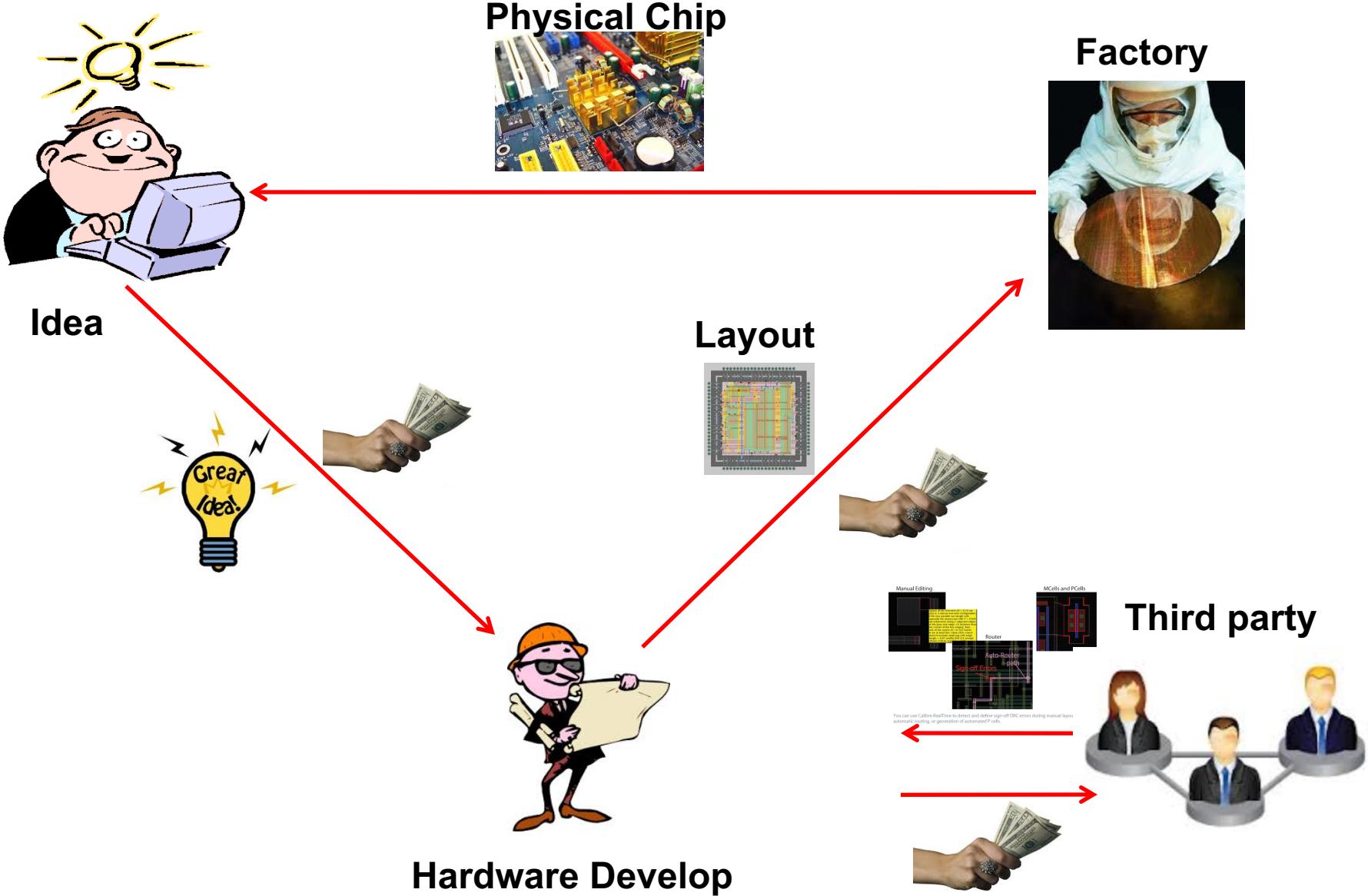
Factory



Third party



# ASIC Design Subject



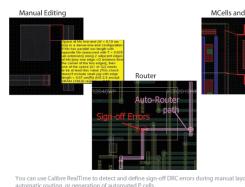
# ASIC Design Subject



Hardware Develop

Can all companies  
cover different roles

Factory



Third party



Synopsys - 1986  
Cadence - 1988  
Mento Graphics - 1981  
Aldec - 1984  
Altera - 1984  
Xilinx - 1984

# ASIC Design Subject

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## Only Fabrication

TSMC (Taiwan)

UMC(Taiwan)

Global Foundries (Germany)

DongbuHiTek (Korean)

.....

## Design & Fabrication

Texas Instruments

Intel

Renesas(Japan)

Micron

Samsung(Korean)

Toshiba(Japan)

.....

.....

[https://en.wikipedia.org/wiki/List\\_of\\_semiconductor\\_fabrication\\_plants](https://en.wikipedia.org/wiki/List_of_semiconductor_fabrication_plants)

# ASIC Design Subject

Half-shrink

Main ITRS node	Stopgap half-node
250 nm	220 nm
180 nm	150 nm
130 nm	110 nm
90 nm	80 nm
65 nm	55 nm
45 nm	40 nm
32 nm	28 nm
22 nm	20 nm
16 nm	14 nm
10 nm	8 nm
7 nm	6 nm
5 nm	4 nm

10 µm – 1971  
6 µm – 1974  
3 µm – 1977  
1.5 µm – 1982  
1 µm – 1985  
800 nm – 1989  
600 nm – 1994  
350 nm – 1995  
250 nm – 1997  
180 nm – 1999  
130 nm – 2001  
90 nm – 2004  
65 nm – 2006  
45 nm – 2008  
32 nm – 2010  
22 nm – 2012  
14 nm – 2014  
10 nm – 2017  
7 nm – 2019?  
5 nm – 2021?

# ASIC Design Subject

Companies

Cover All Technologies?

Half-shrink	
Main ITRS node	Stopgap half-node
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# ASIC Design Subject

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## Design & Fabrication

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Samsung

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## Light Fabrication

Texas Instruments

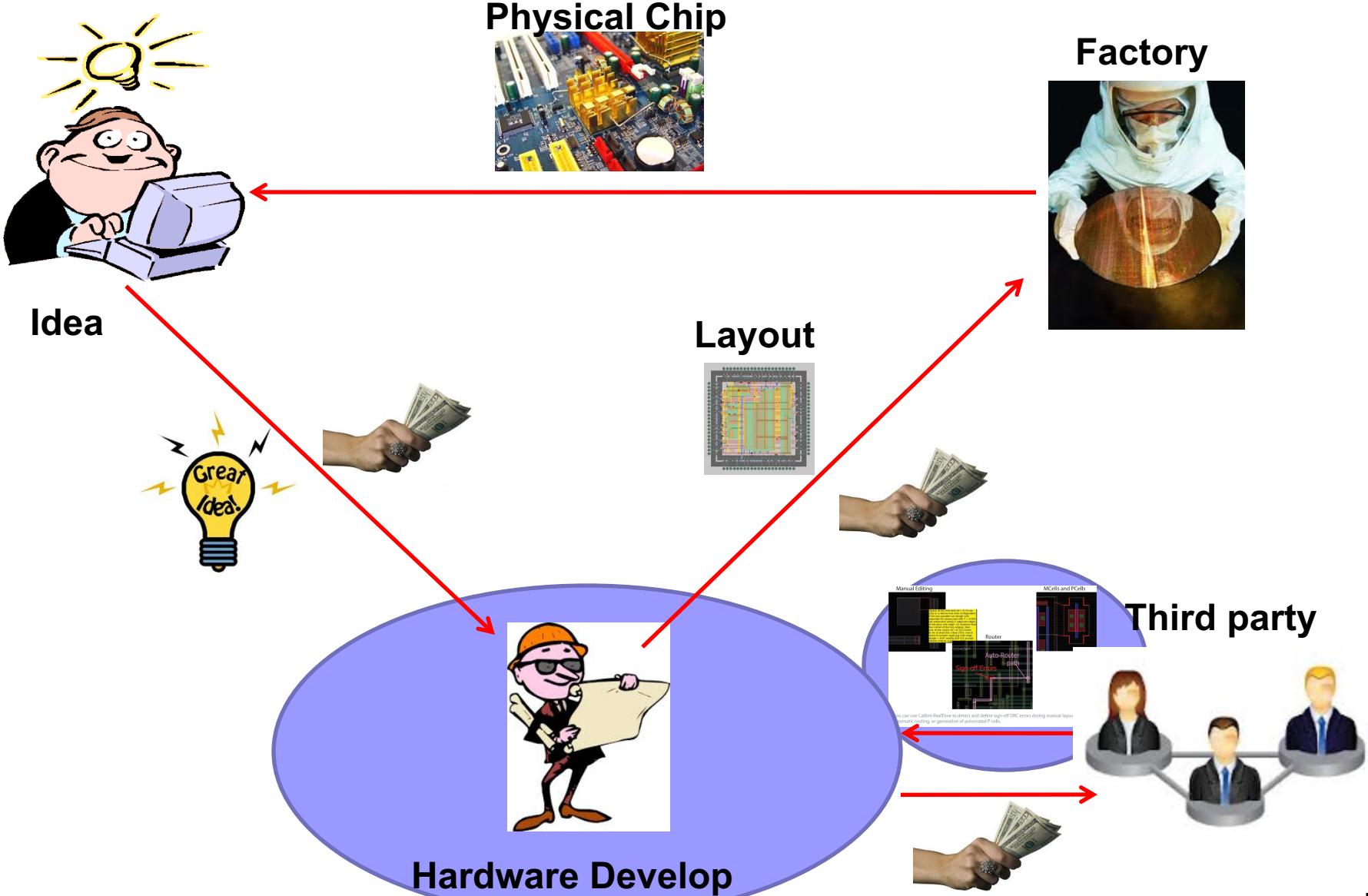
Renesas

Micron

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# ASIC Design Subject



# ASIC Design Subject

**ASIC Design Flow**  
**(Application-Specific  
Integrated circuit)**

Design Methodology

Fully Custom

Semi Custom

Standard Cells

Gate Arrays

Programmable Logic

**FPGA Design Flow**  
**(Field Programmable  
Gate Array)**

F P G A

P L D

# ASIC Design Subject

## Full Custom

- Design a chip from scratch
- Engineer design some or all the logic cells, circuits, and the chip layout specifically for a full-custom IC
- Advantages: Complete flexibility, high degree of optimization performance ad area
- Disadvantages: Large amount of design effort, expensive

## Standard Cell Base

- Use predesigned, pretested and pre-characterized logic cells from the standards-cell library as building blocks.
- The chip layout is customized
- Advantages: Save design time and money, reduce risk compared to full-custom design
- Disadvantages: Still incurs high none-recurring-engineering (NRE) cost and long manufacture time

## Gate Array

- Parts of the chip are pre-fabricated, and other parts are custom fabricated for particular customer's circuit.
- Identical base cells are pre-fabricated in the form of a 2-D array on a gate-array (this partially finished chip is called gate-array template).
- This wires between the transistors inside the cells and between the cells are custom fabricated for each customer
- Custom mask are made for the wiring only

## PLD

- A PLD is a general-purpose chip for implementing logic circuitry.
- Transistors and wires are already prefabricated on a PLD
- Logic cells and interconnect can be programmed by end-user to implement specific circuitry
- No need to create custom masks for each customer

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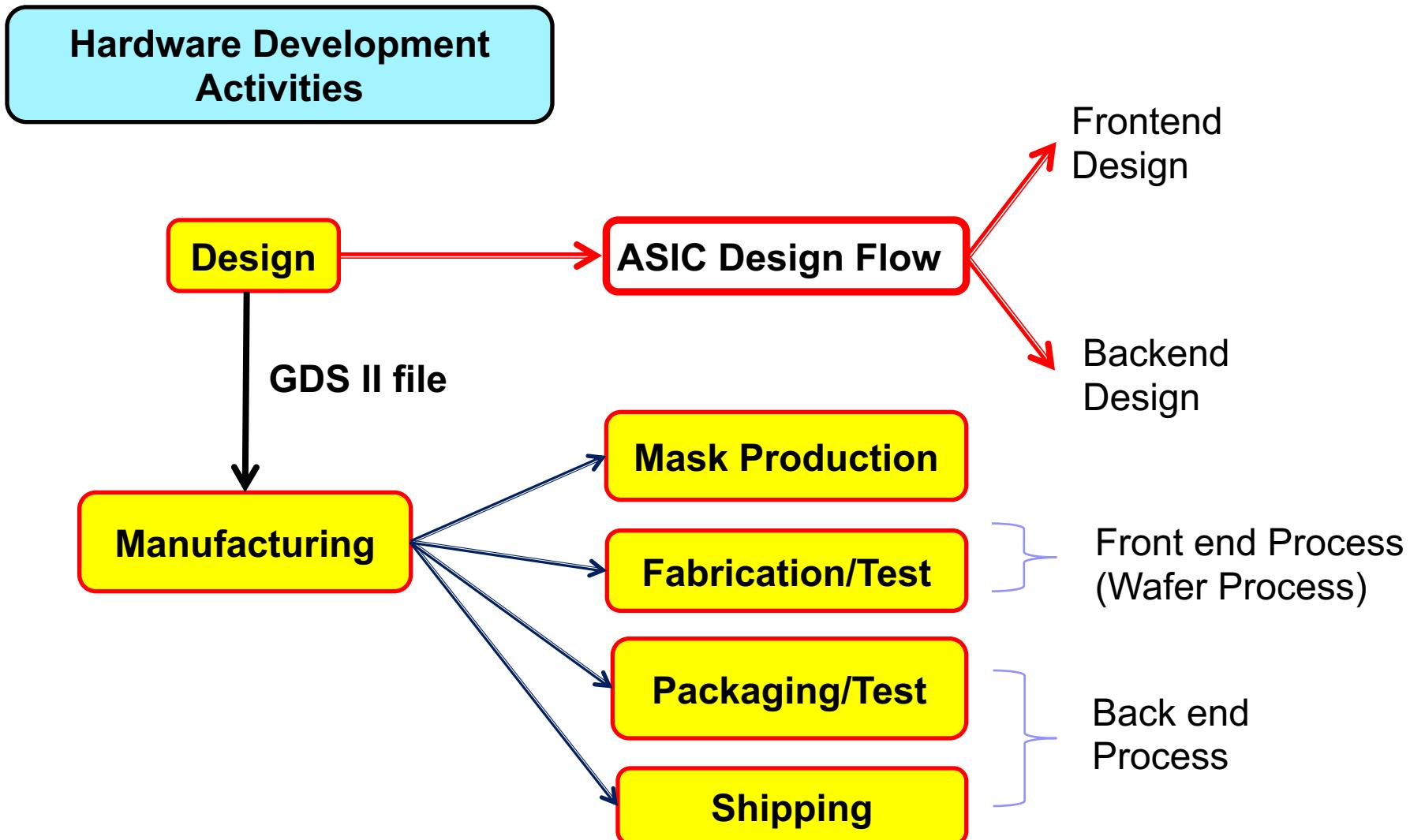
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# ASIC Design Subject



# ASIC Design Subject

Q1. Middleware ?

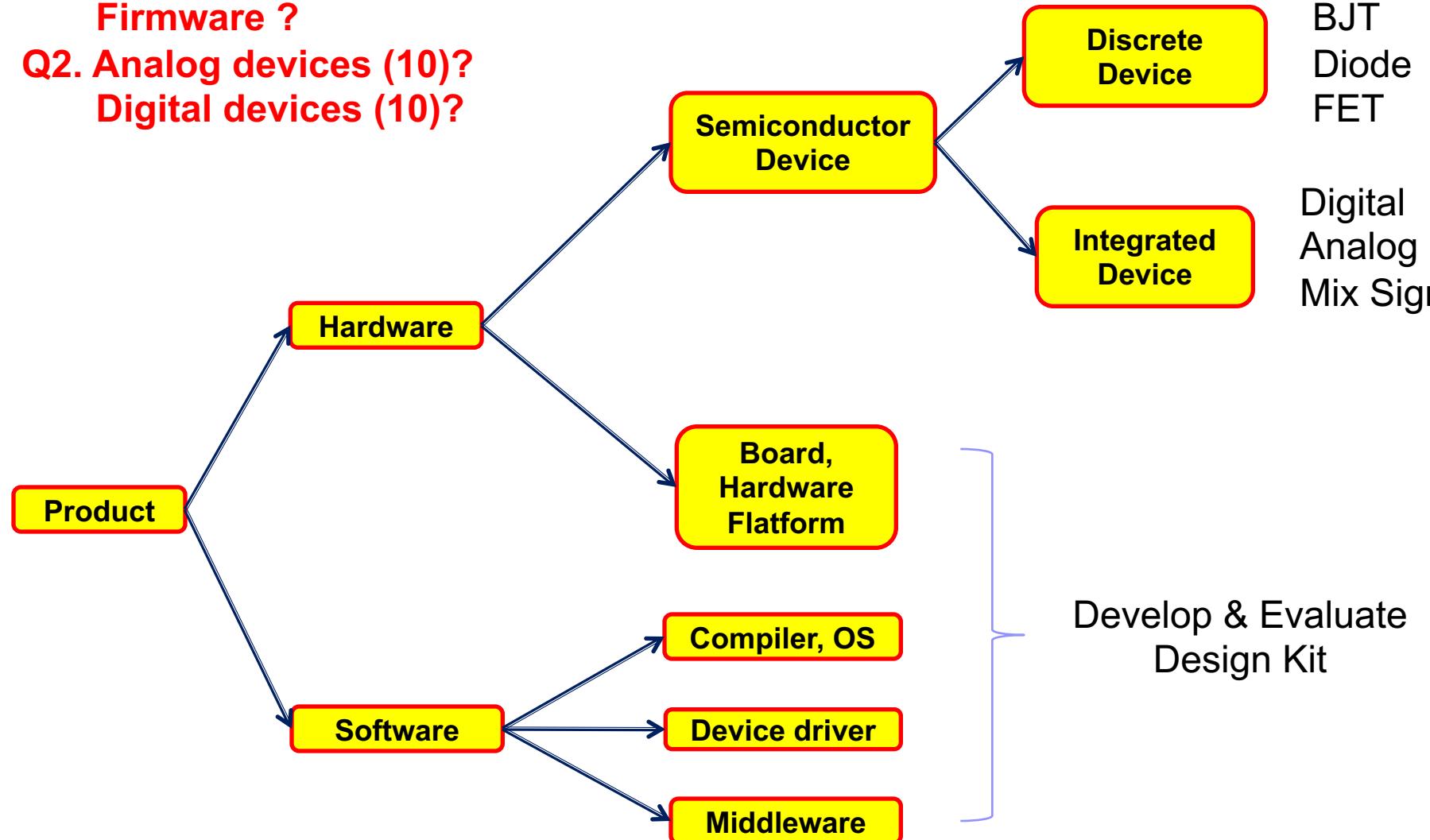
Firmware ?

Q2. Analog devices (10)?

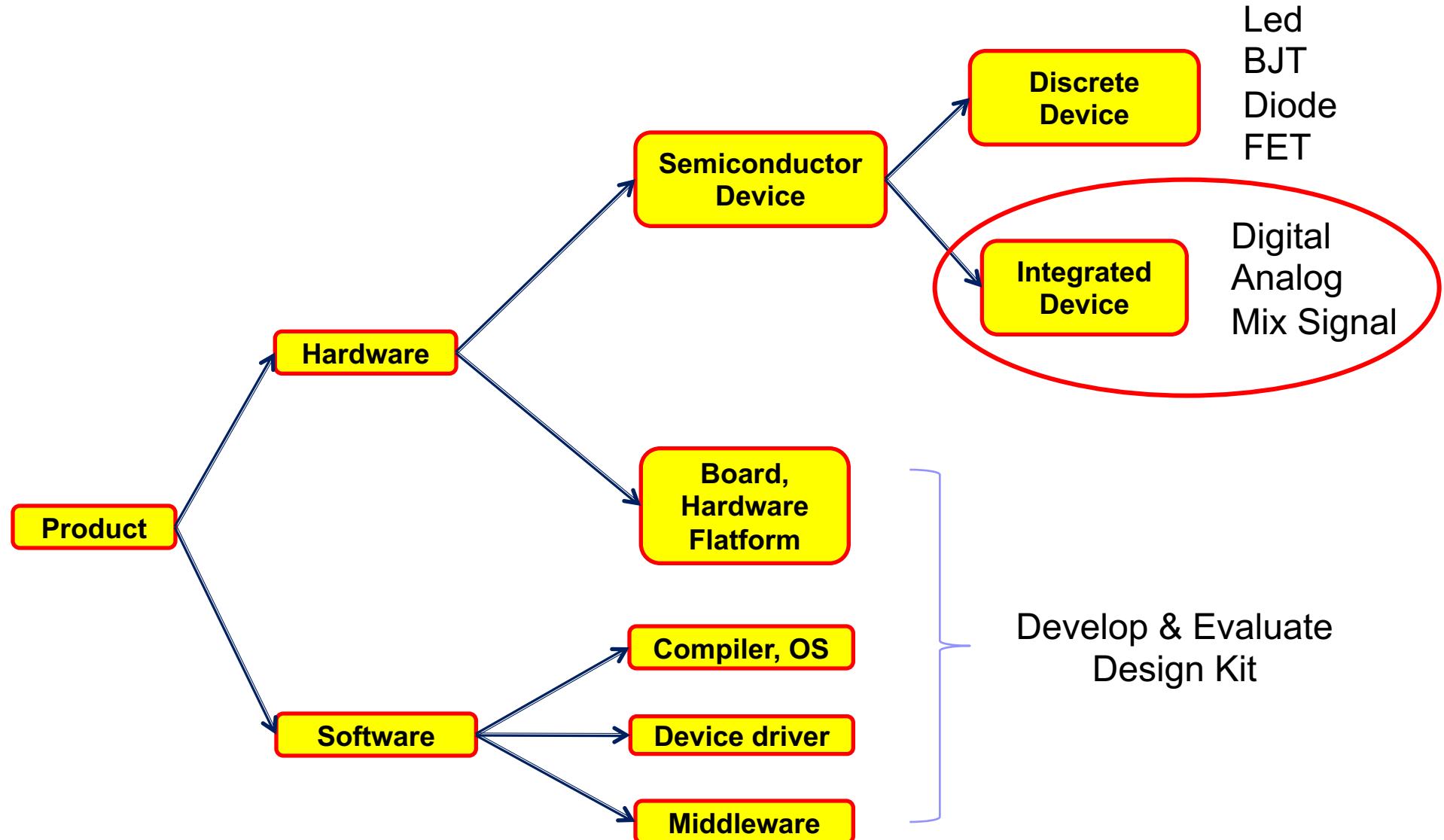
Digital devices (10)?

Led  
BJT  
Diode  
FET

Digital  
Analog  
Mix Signal



# ASIC Design Subject



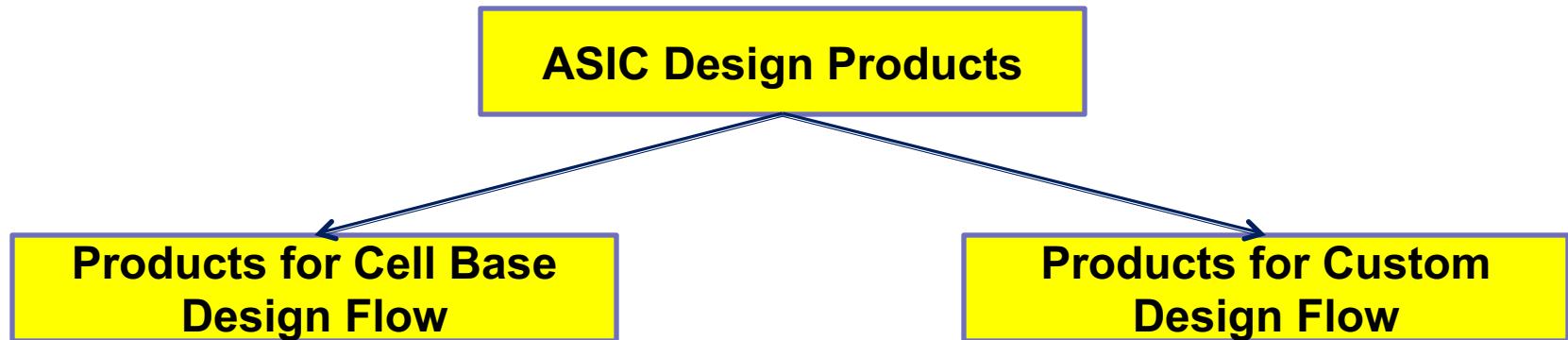
# ASIC Design Flow

- ❖ Cell Base & Custom Design Flow Concepts
- ❖ Custom Design Flow
- ❖ Cell Base Design Flow
- ❖ ASIC vs. FPGA Design Flow

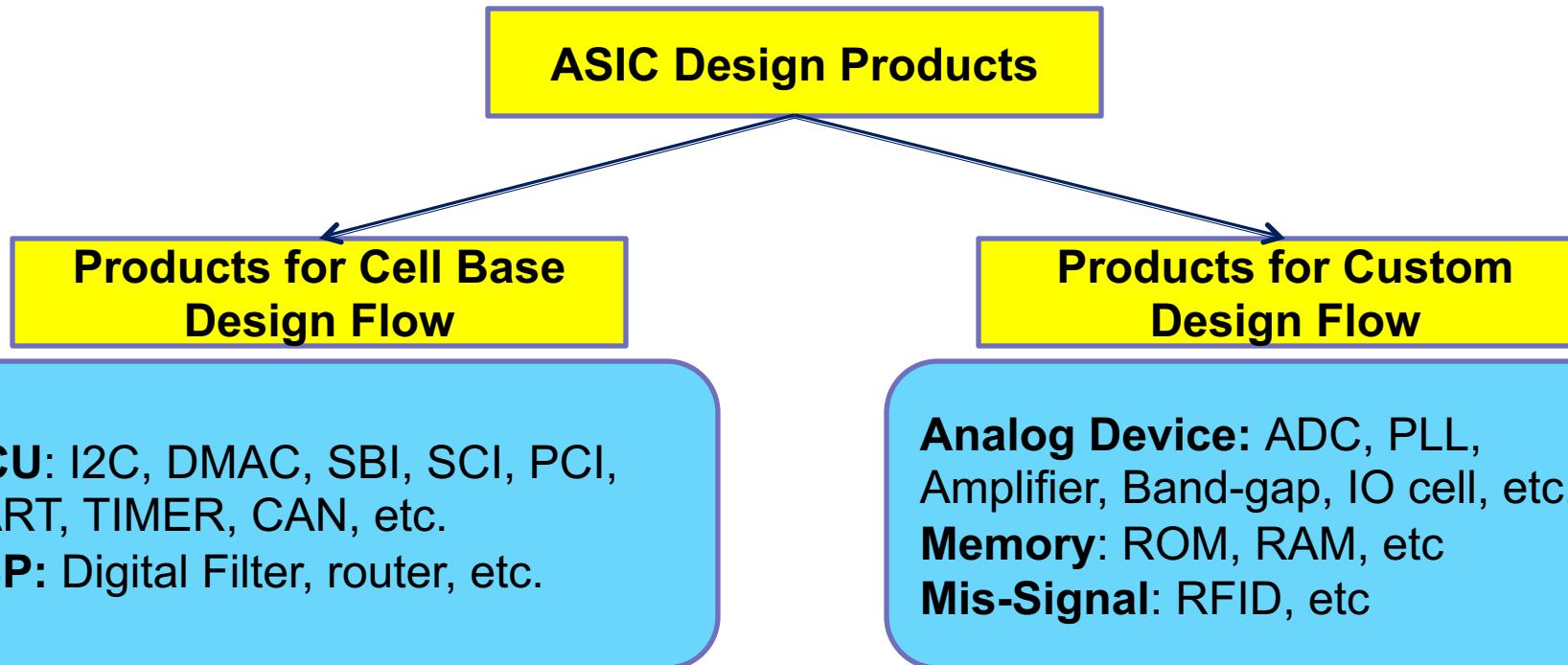
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# Cell Base & Custom Design Flow Concepts

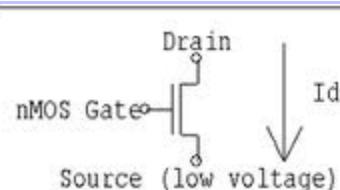
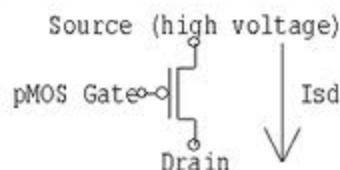


# Cell Base & Custom Design Flow Concepts



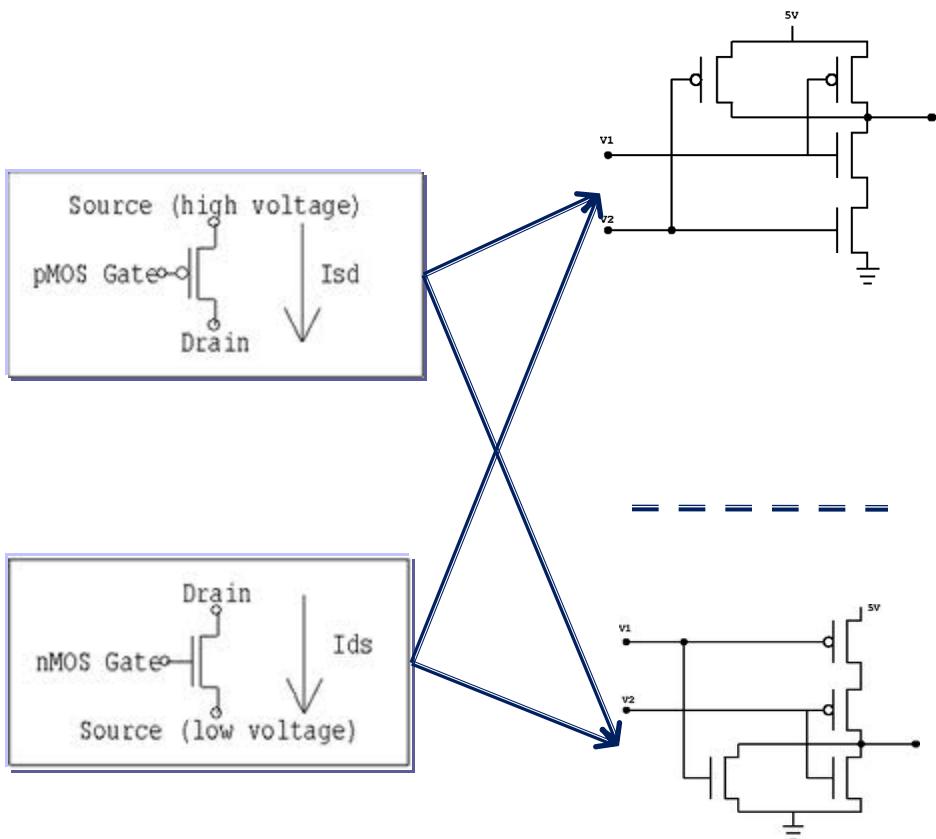
# Cell Base & Custom Design Flow Concepts

## Custom Design Flow



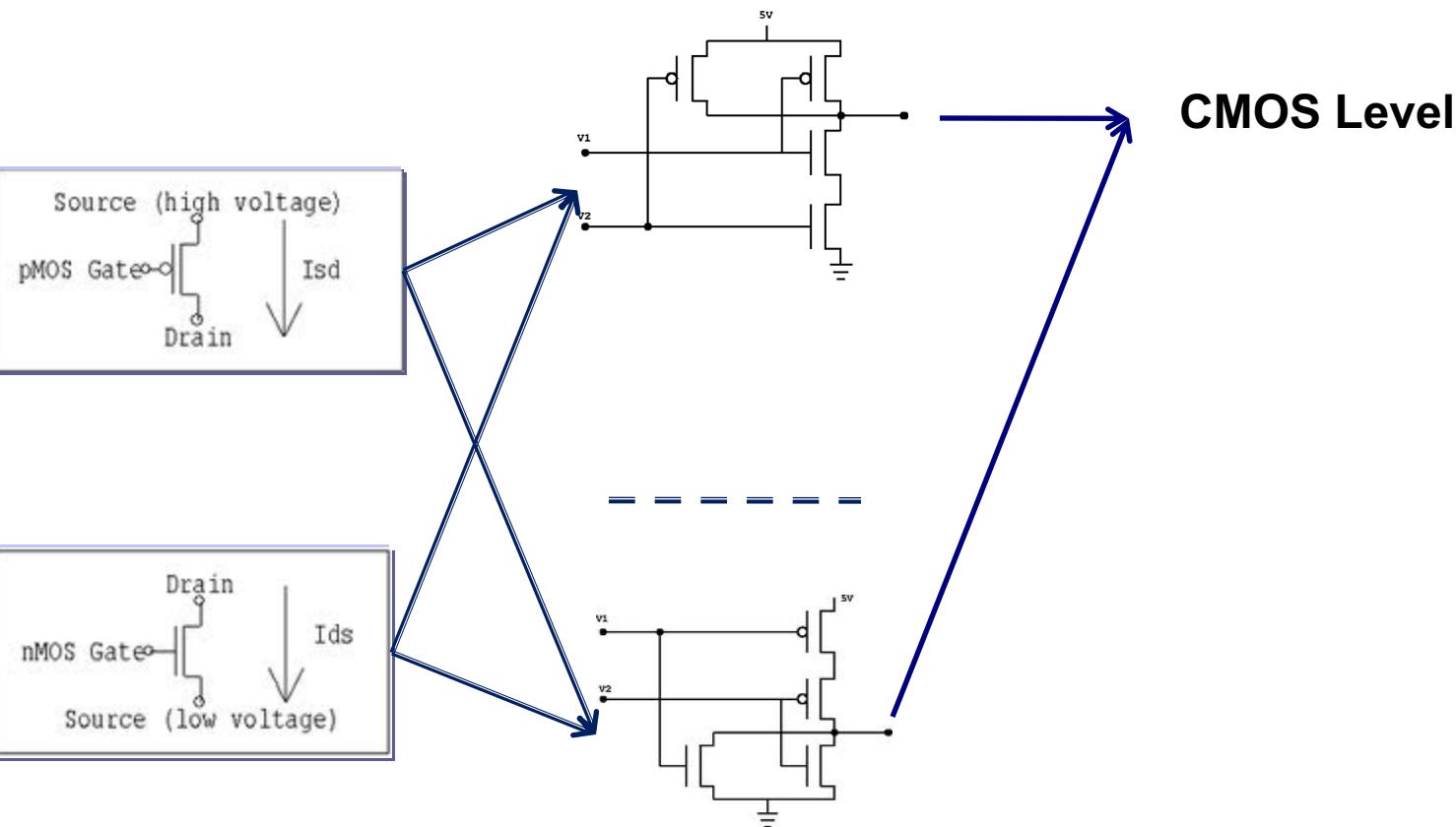
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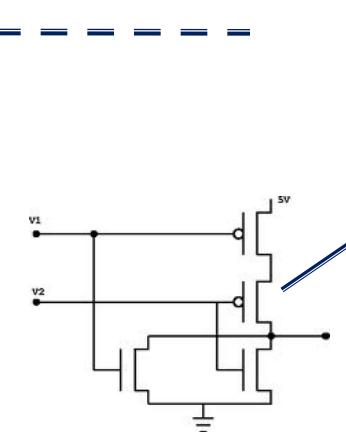
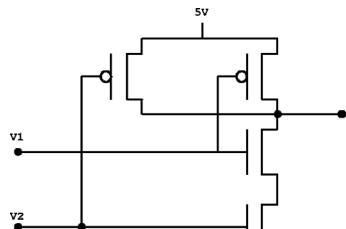
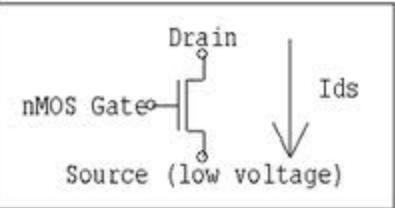
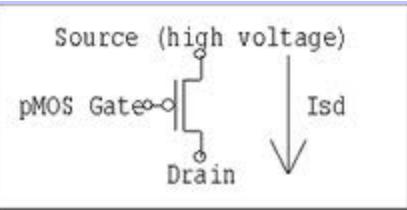
# Cell Base & Custom Design Flow Concepts

## Custom Design Flow

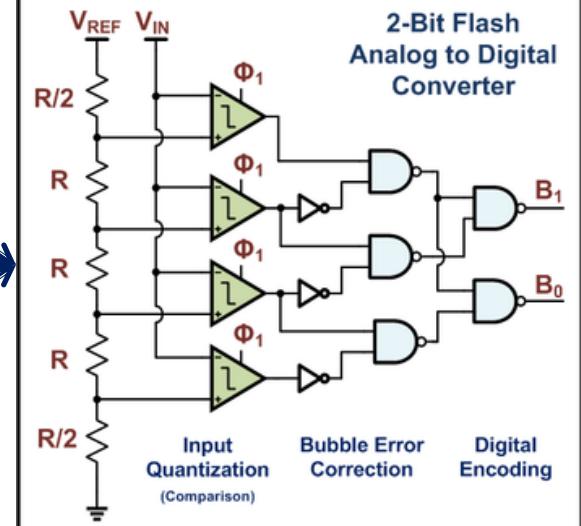


# Cell Base & Custom Design Flow Concepts

## Custom Design Flow



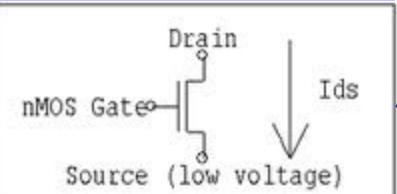
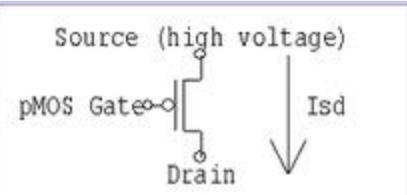
## ADC IP



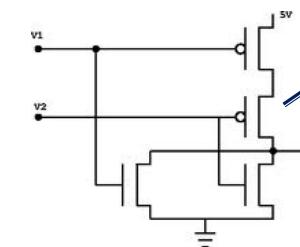
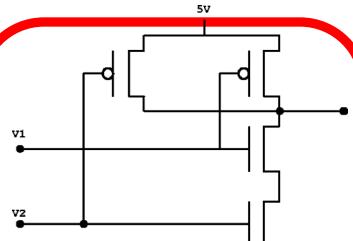
# Cell Base & Custom Design Flow Concepts

## Custom Design Flow

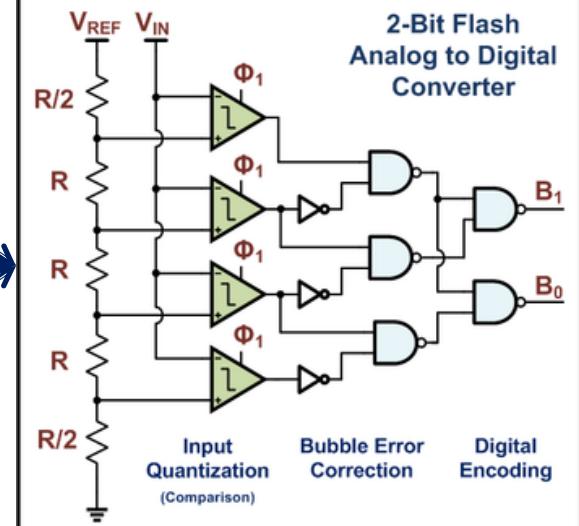
CMOS is library



Build IP  
from the scratch



ADC IP



# Cell Base & Custom Design Flow Concepts

## Cell Base Design Flow

```
assign y = !(x1 & x2);
```

```
assign y = !(x1 | x2);
```

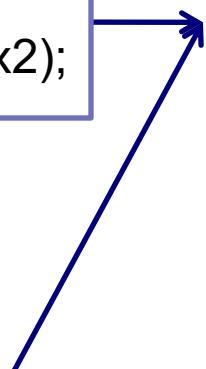
# Cell Base & Custom Design Flow Concepts

## Cell Base Design Flow

RTL Level (**Verilog/VHDL**)

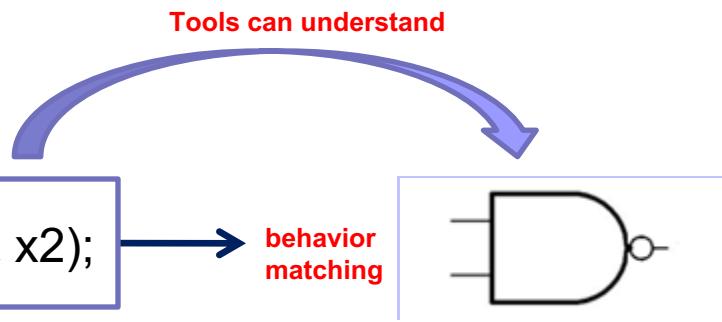
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# Cell Base & Custom Design Flow Concepts

## Cell Base Design Flow



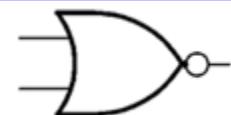
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behavior  
matching



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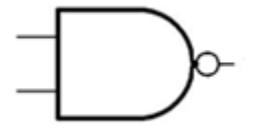
# Cell Base & Custom Design Flow Concepts

## Cell Base Design Flow

Tools can understand

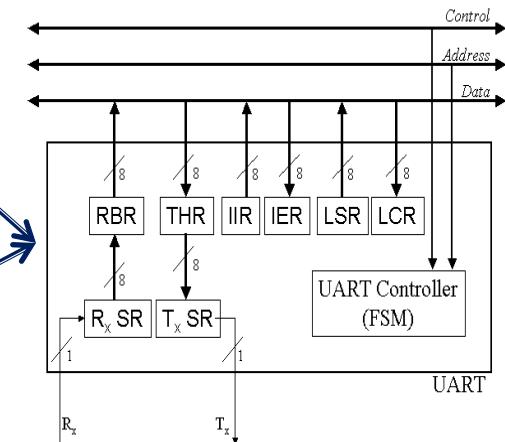
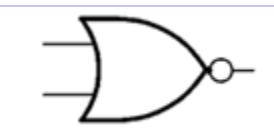
assign y = !(x1 & x2);

behavior matching



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behavior matching



# Cell Base & Custom Design Flow Concepts

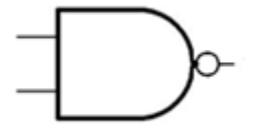
## Cell Base Design Flow

Gate is library

Tools can understand

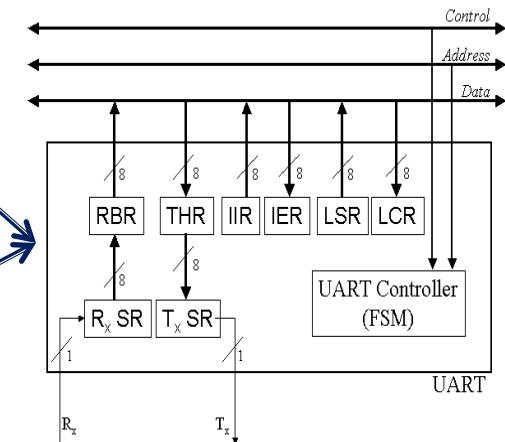
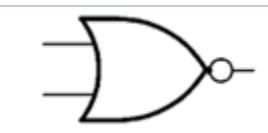
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behavior matching

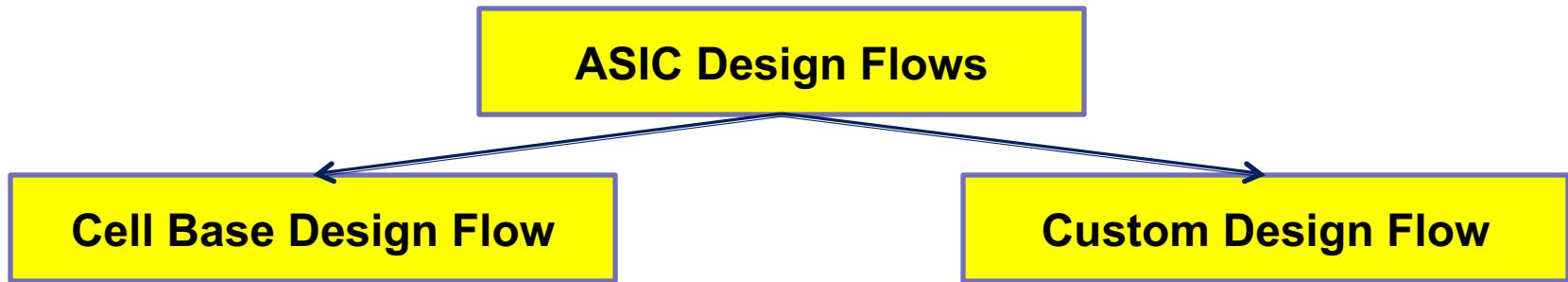


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# Cell Base & Custom Design Flow Concepts



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# Cell Base & Custom Design Flow Concepts

comparision	Cell Base Design	Custom Design
Integration Density		X
Speech		X
Chip Scale	X	
Support Tools	X	
Time to market	X	
Risk reduction		X

[http://www.ami.ac.uk/courses/ami4407\\_dicdes/u03/#3.2](http://www.ami.ac.uk/courses/ami4407_dicdes/u03/#3.2)

[http://www.eng.uwo.ca/people/wwang/ece616a/616\\_extra/notes\\_web/1\\_dintro.pdf](http://www.eng.uwo.ca/people/wwang/ece616a/616_extra/notes_web/1_dintro.pdf)

<http://www.ece.ucdavis.edu/~bbaas/116/notes/Handout.std.cell.design.pdf>



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# Custom Design Flow

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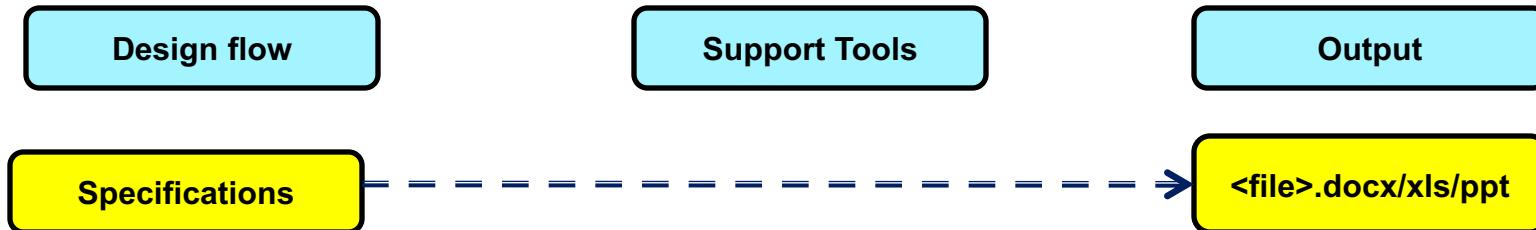
Design flow

Support Tools

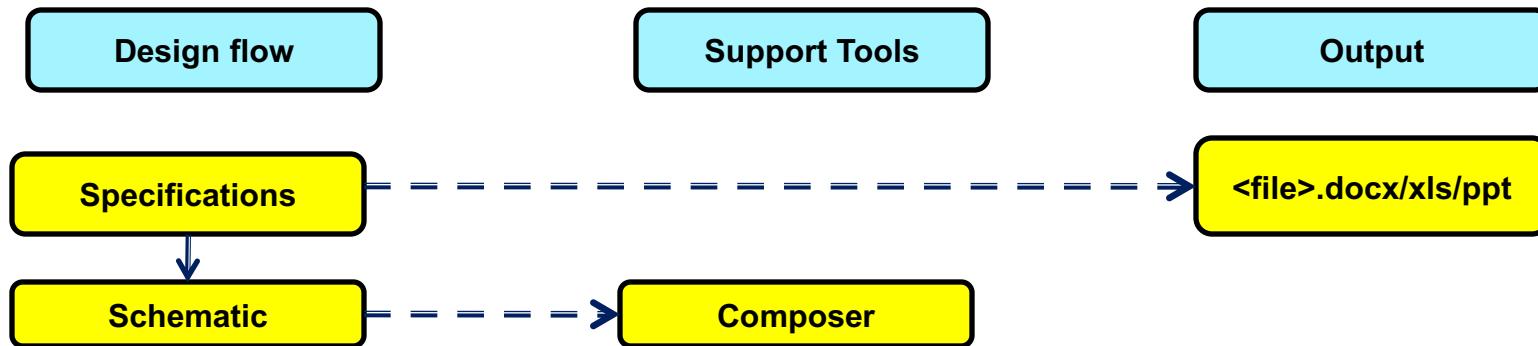
Output

# Custom Design Flow

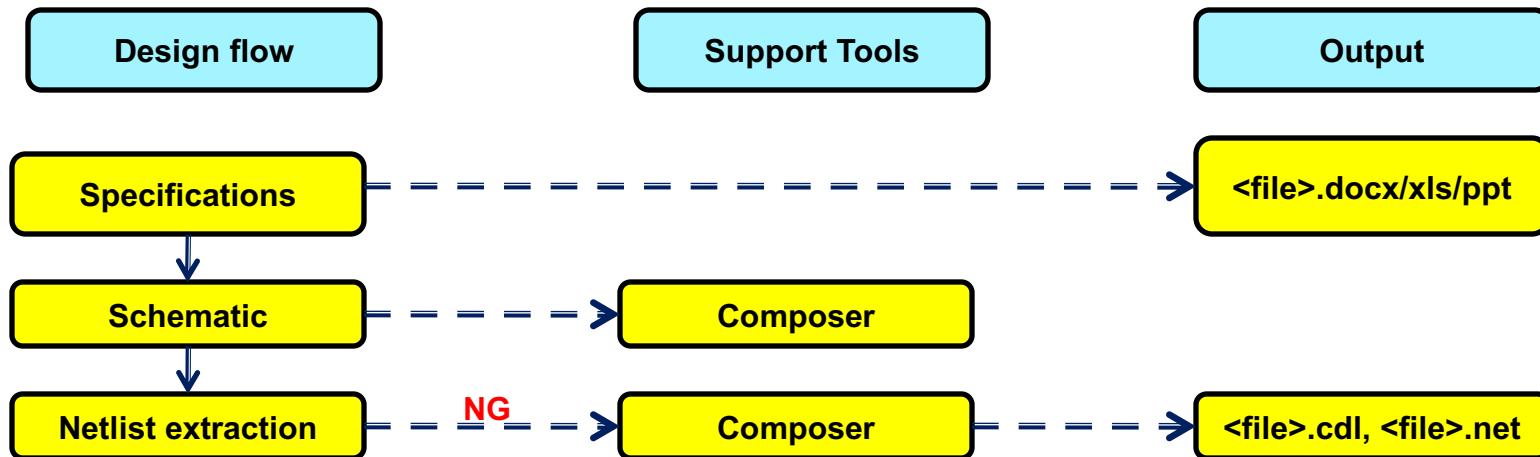
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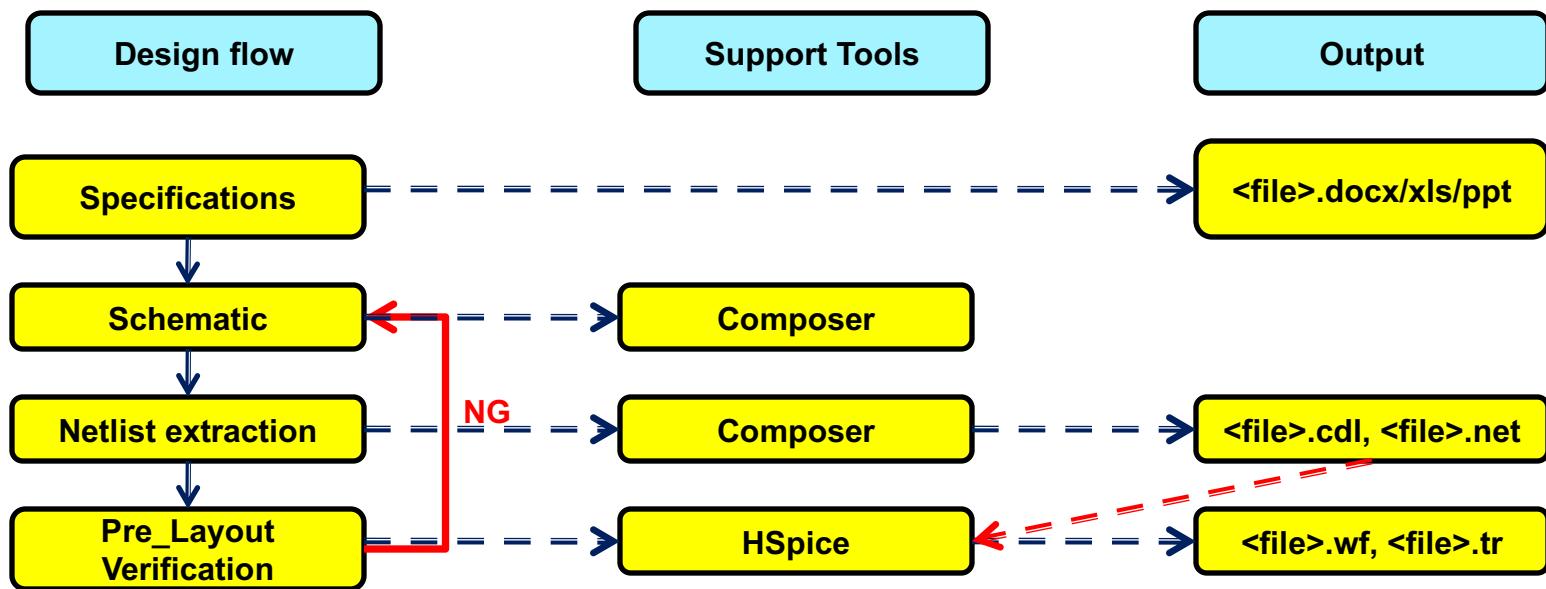
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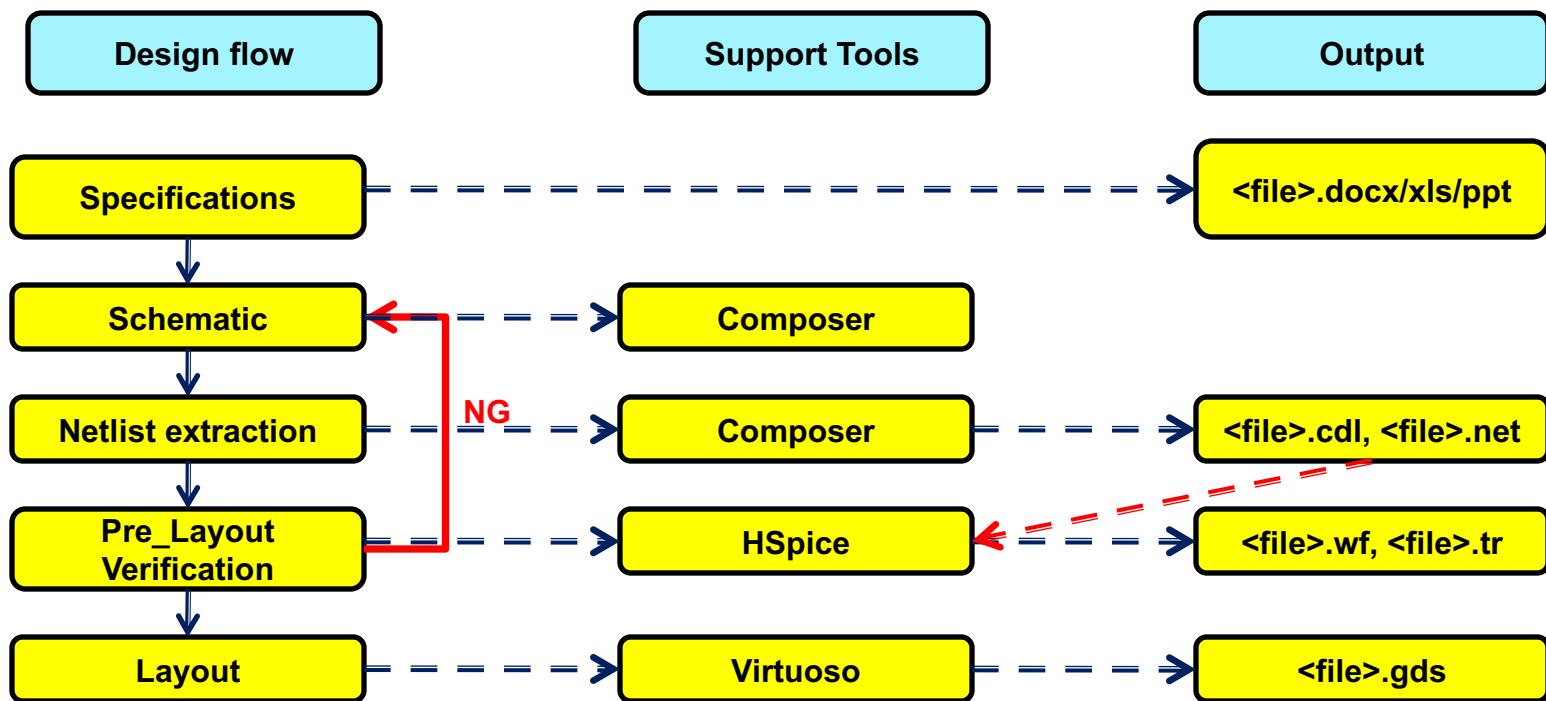
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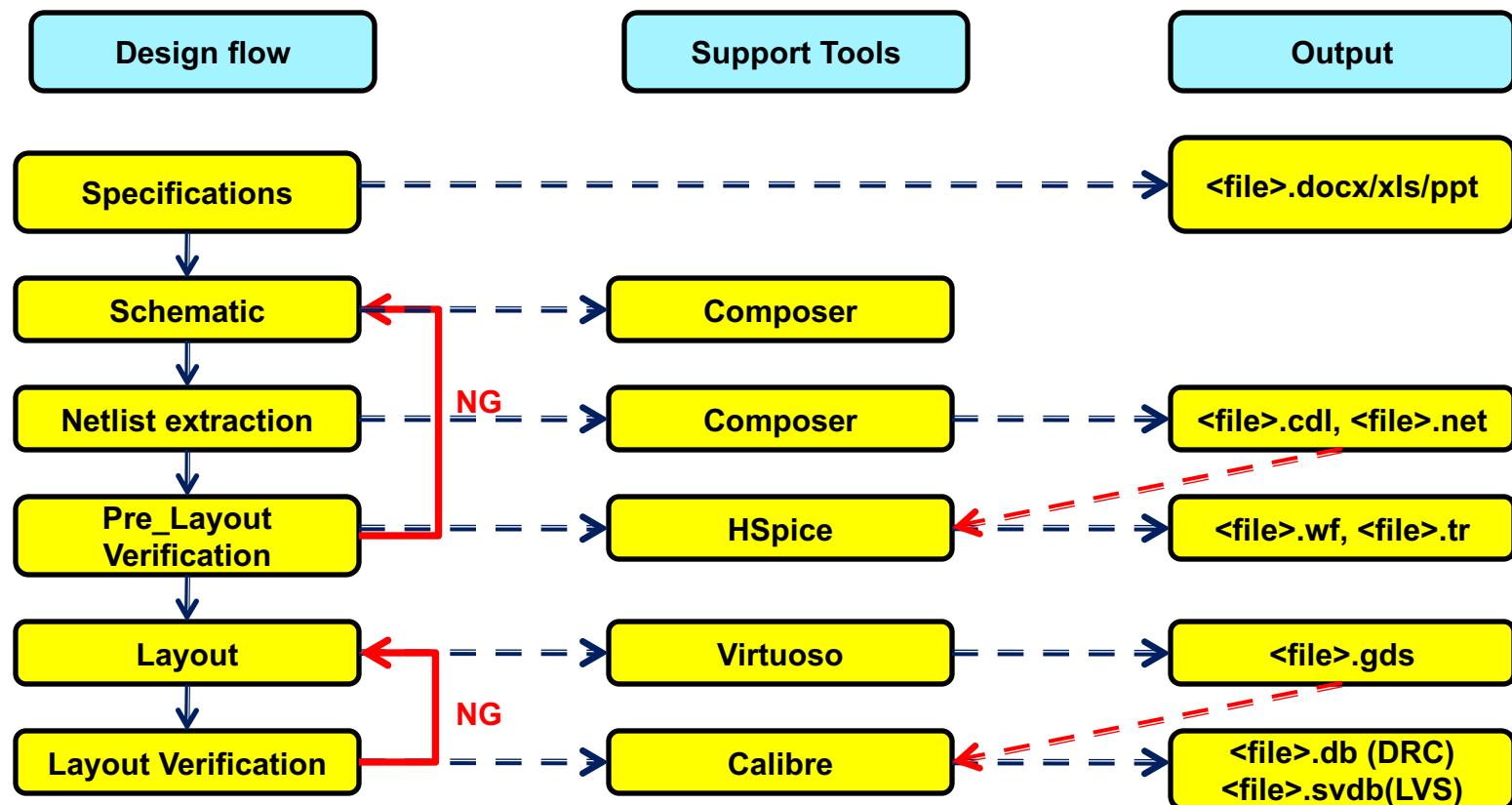
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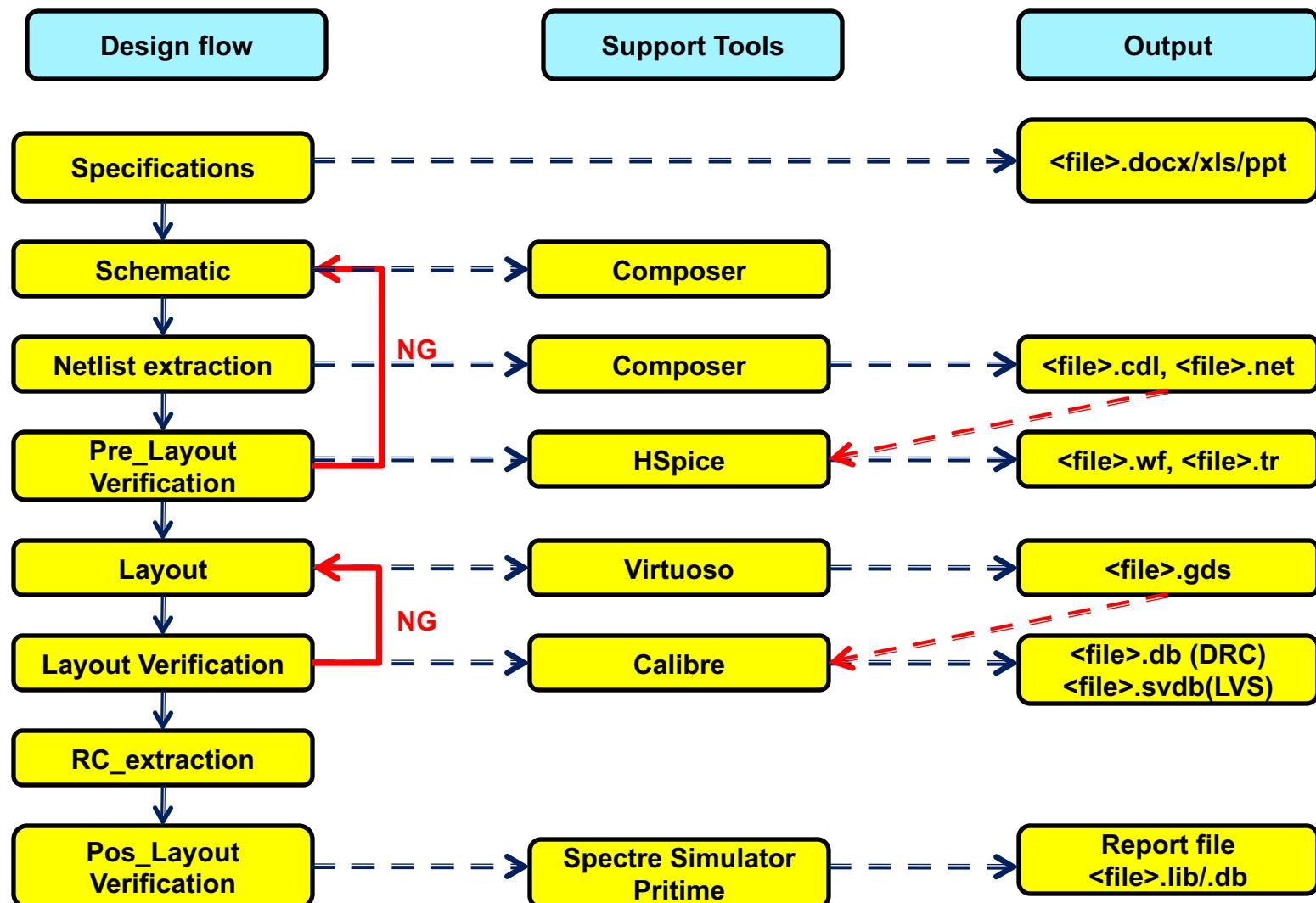
# Custom Design Flow



## DRC: Design Rule Check

## LVS: Layout Versus Schematic

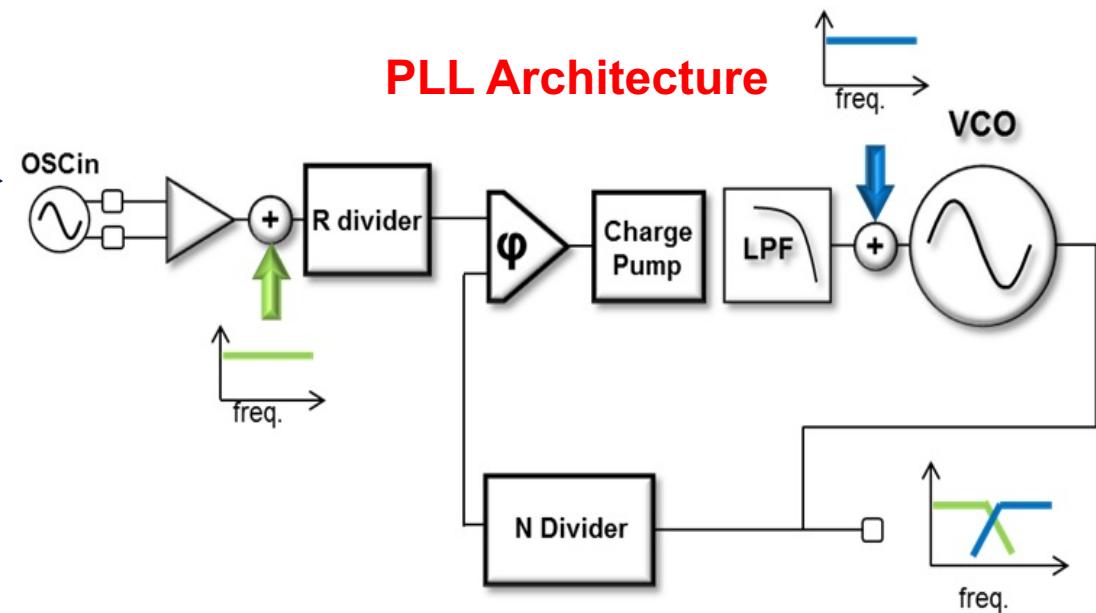
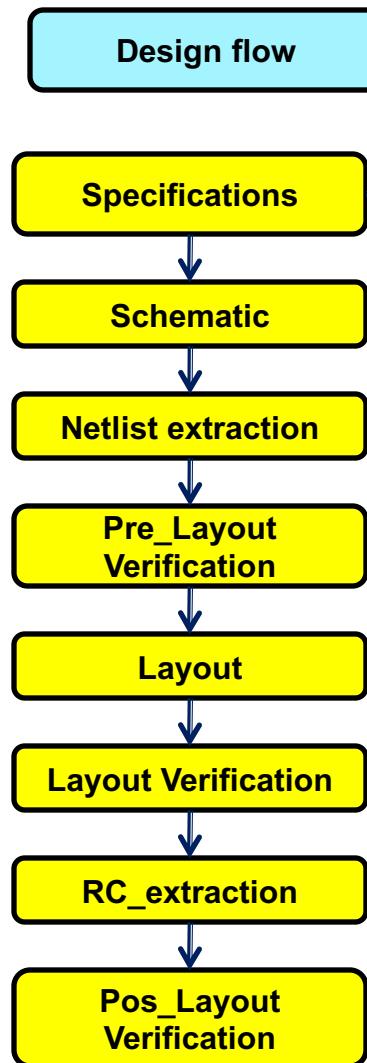
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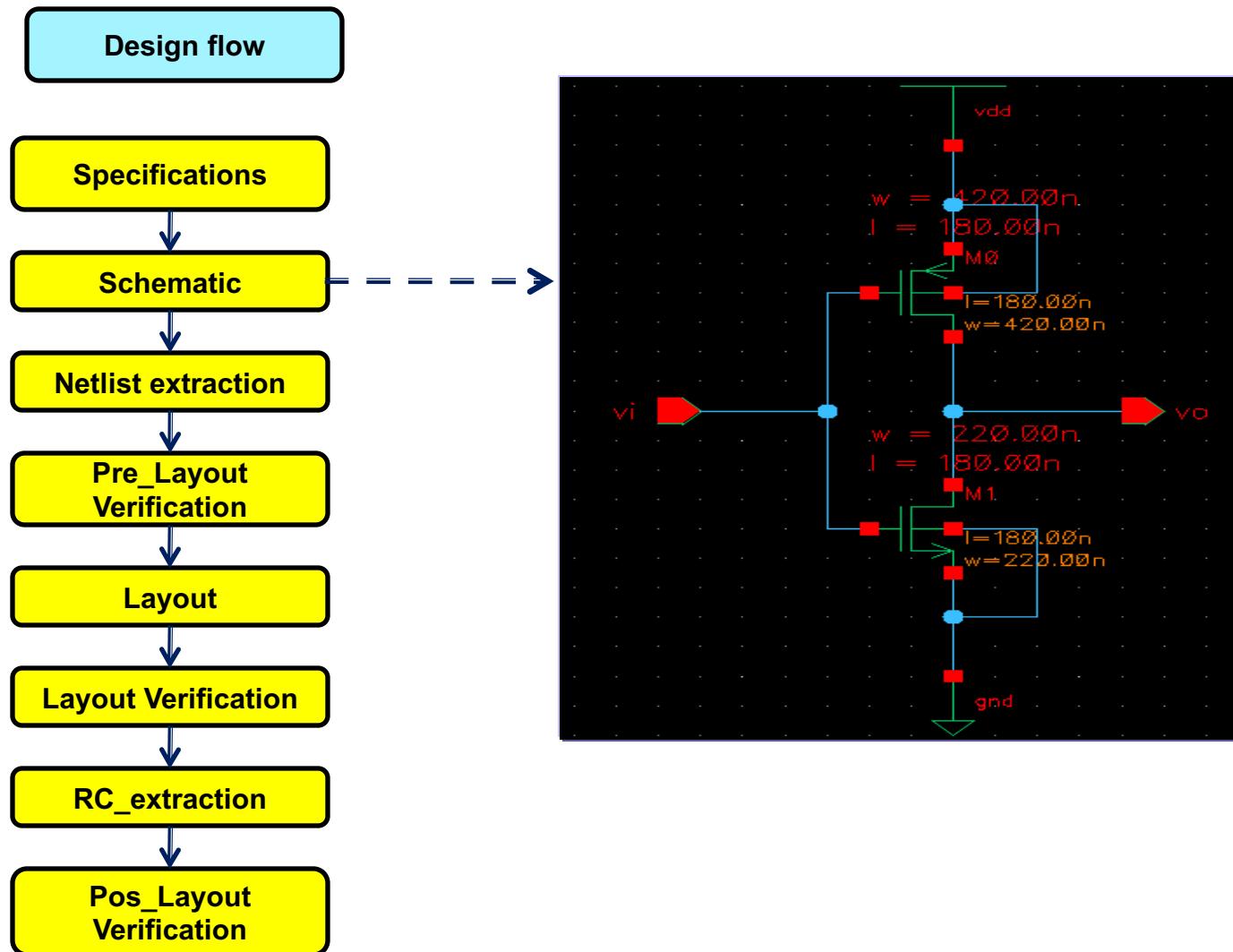
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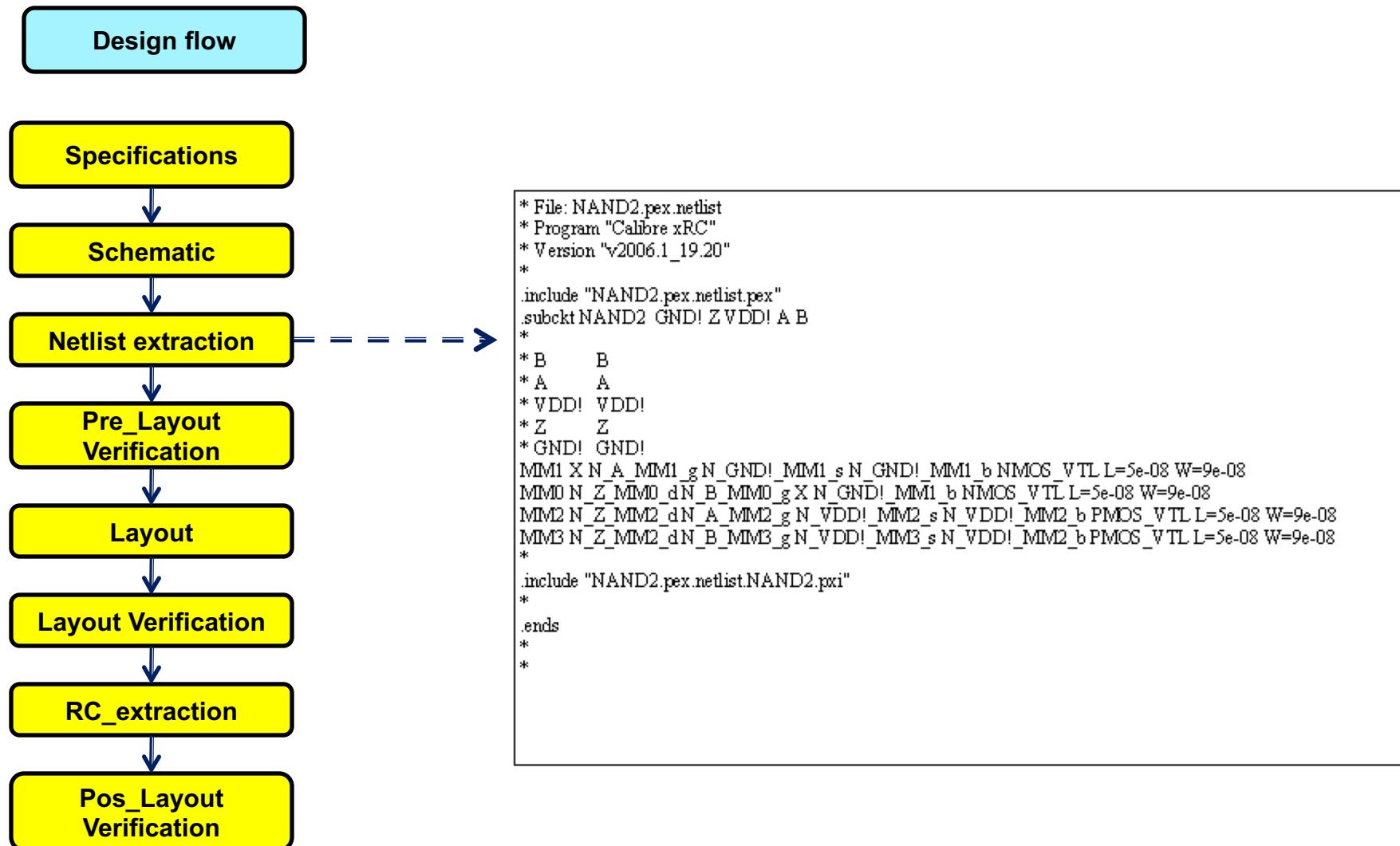
# Custom Design Flow



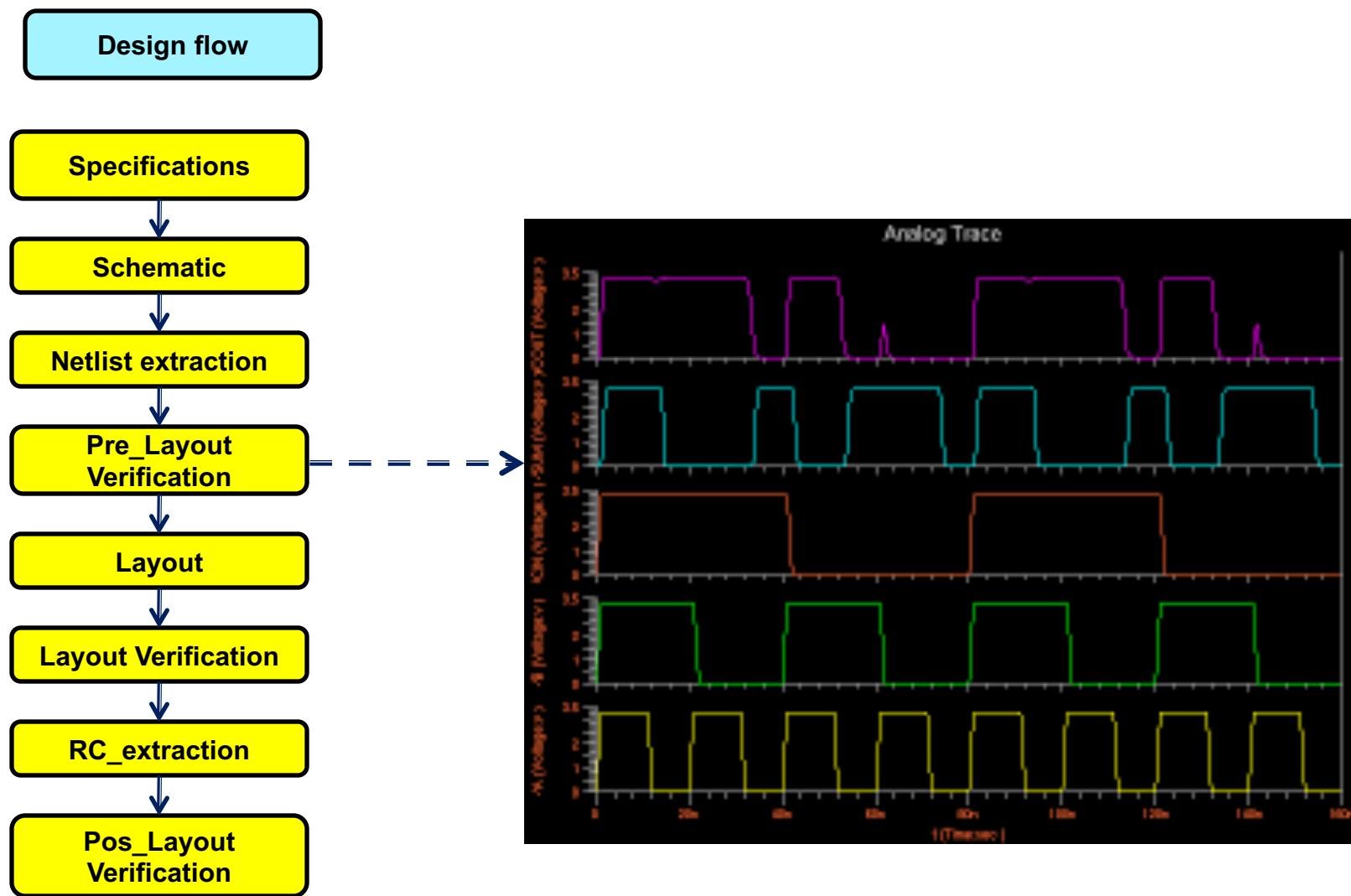
# Custom Design Flow



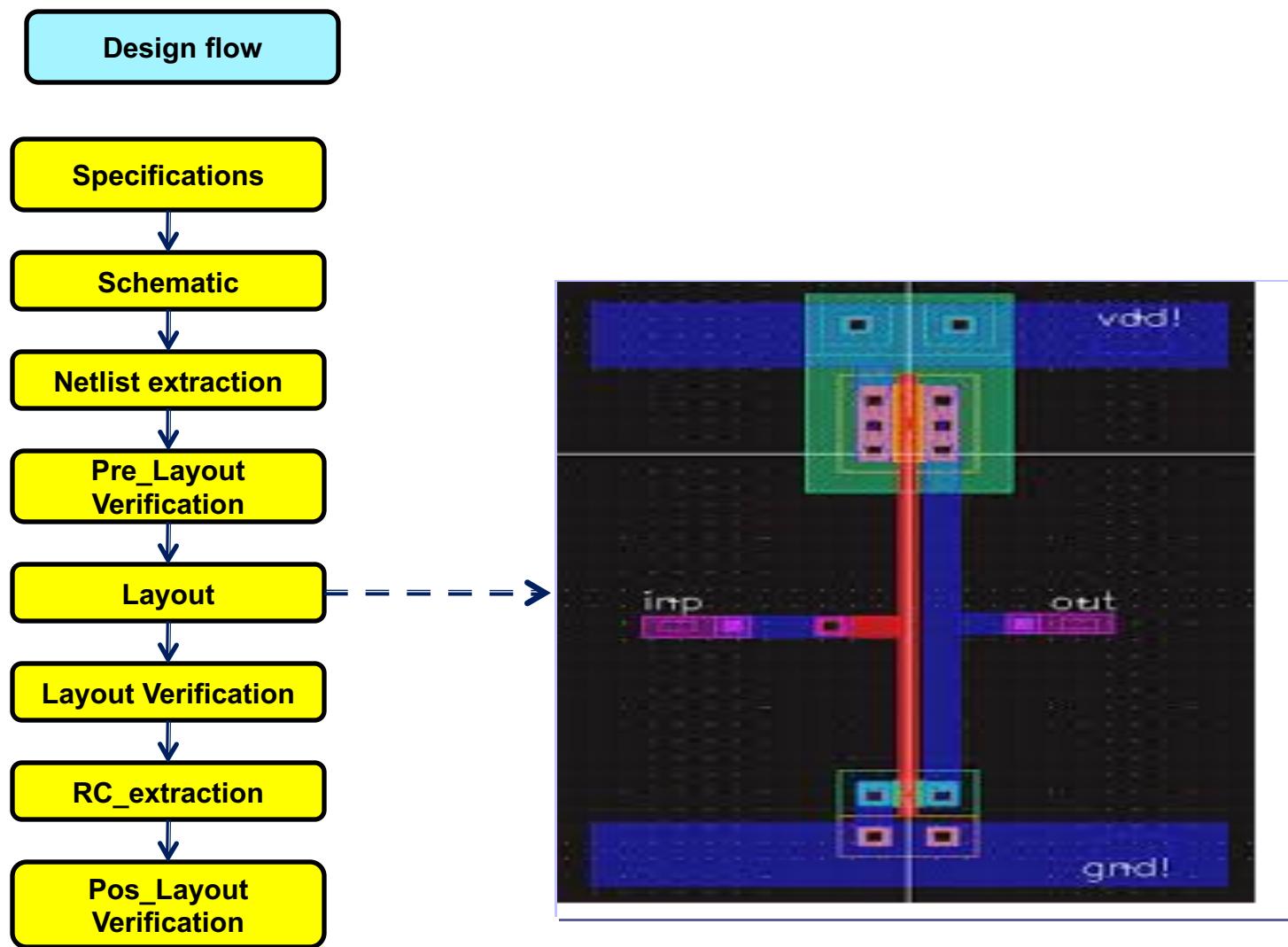
# Custom Design Flow



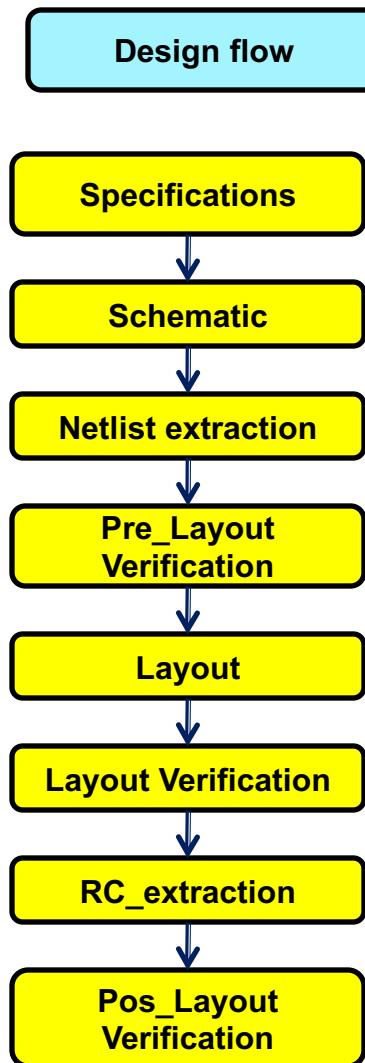
# Custom Design Flow



# Custom Design Flow



# Custom Design Flow

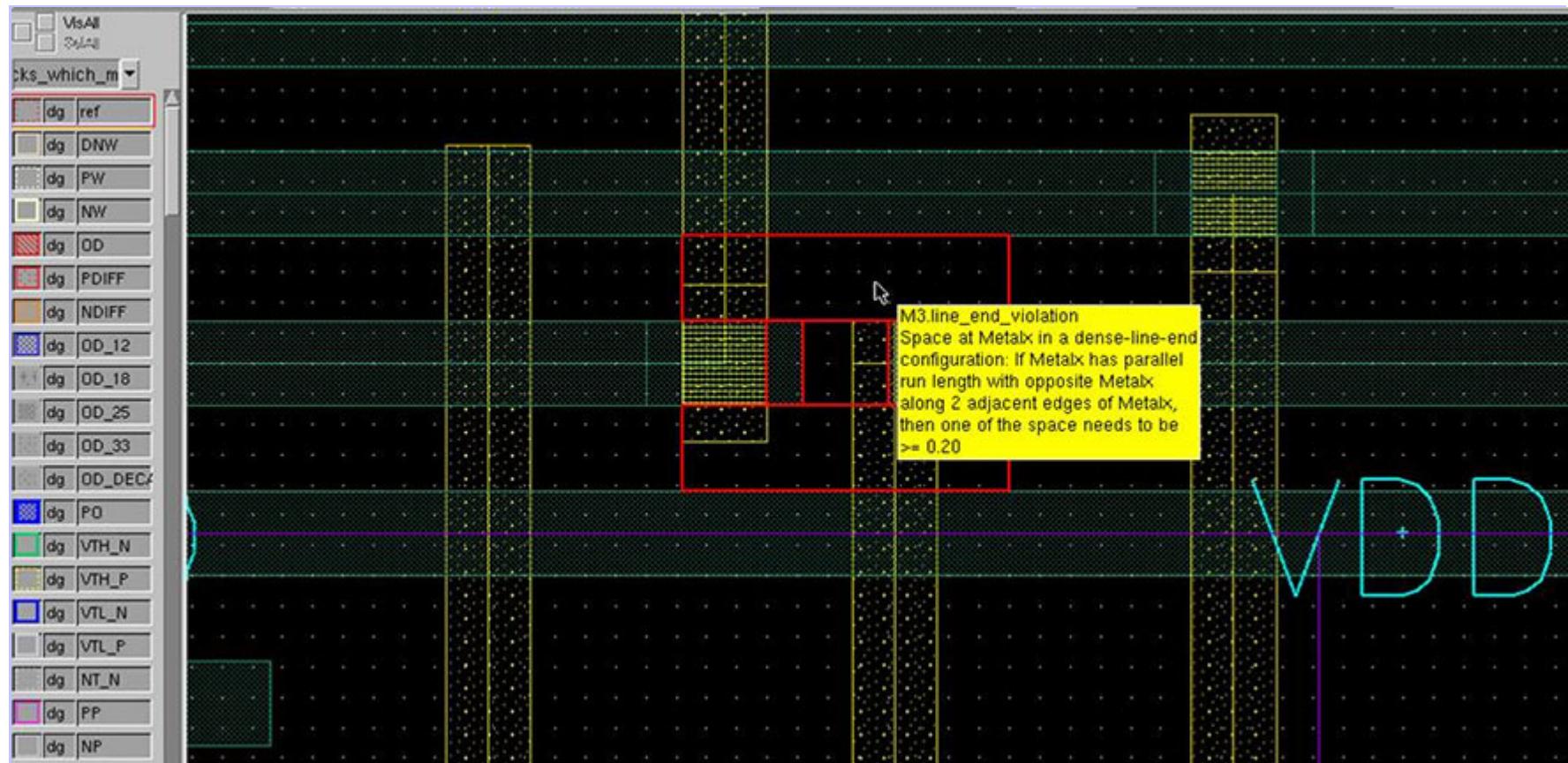


**DRC: Design Rule Check**  
→ Matching to Fabrication Rule

**LVS: Layout vs. Schematic**  
→ Target points are verified to ensure equivalence between Layout and Schematic

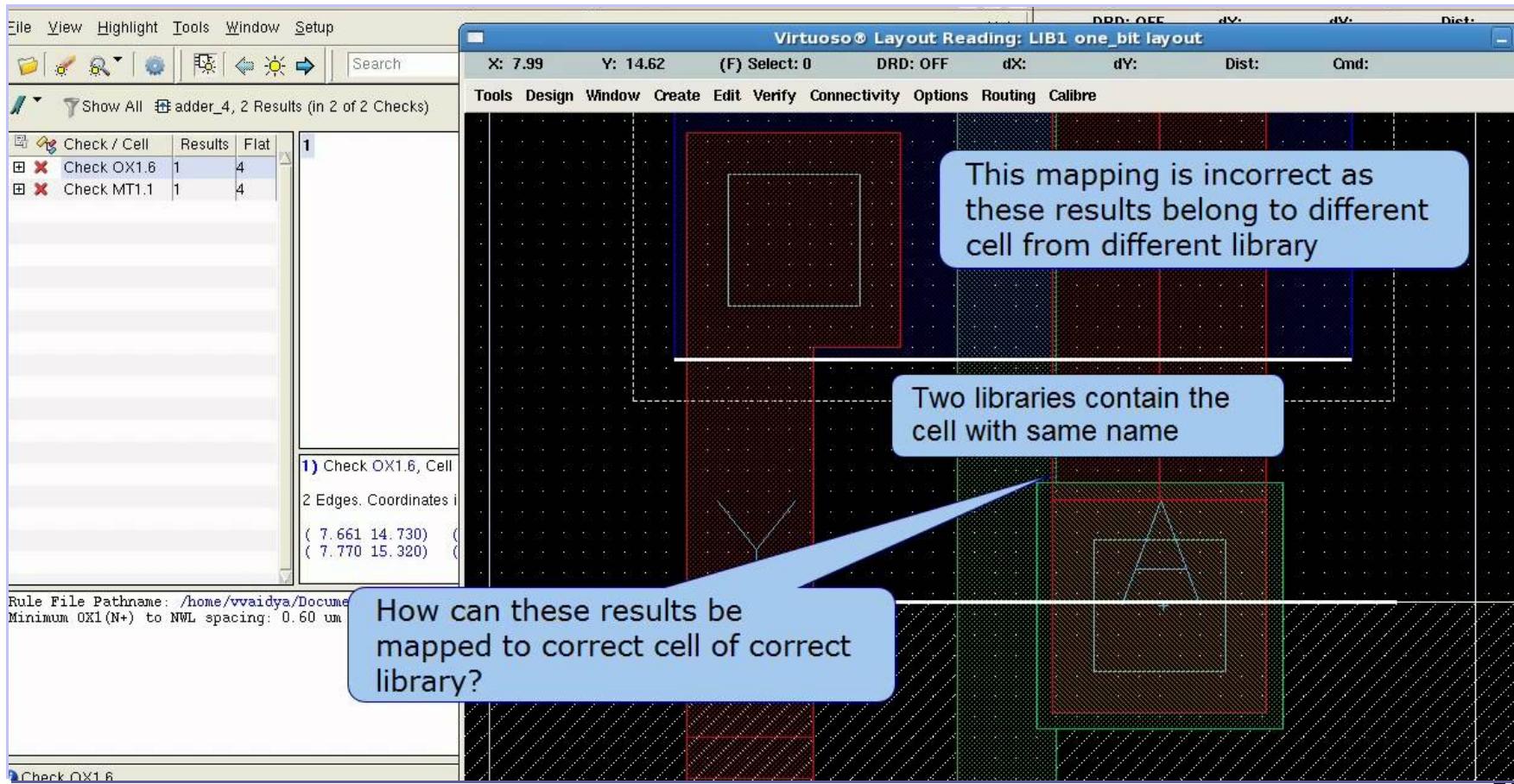
# Custom Design Flow

## DRC: Design Rule Check → Violation of Space Rule

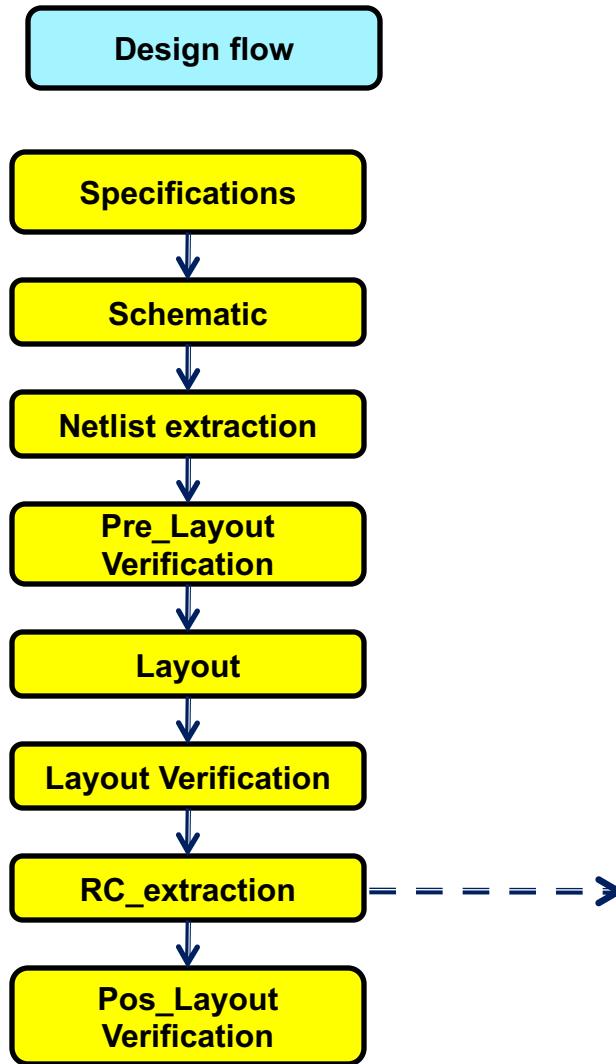


# Custom Design Flow

**LVS: Layout vs. Schematic**  
→ Use other cell having same name from other library

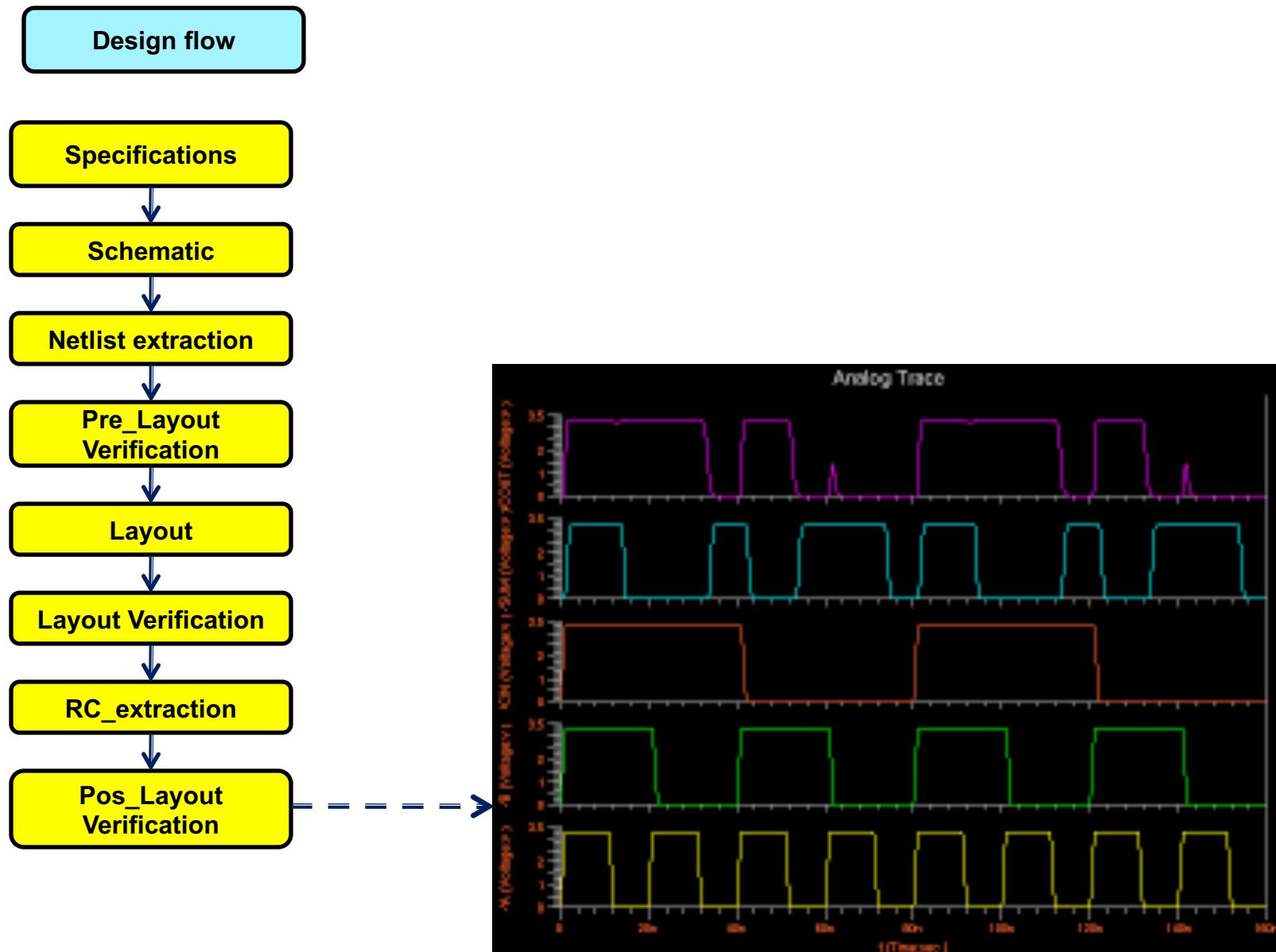


# Custom Design Flow



**Resistance and Capacitance  
Of metals used to connect  
among CMOS devices are  
extracted**

# Custom Design Flow



# ASIC Design Flow

- ❖ Cell Base & Custom Design Flow Concepts
- ❖ Custom Design Flow
- ❖ **Cell Base Design Flow**
- ❖ ASIC vs. FPGA Design Flow

# Cell Base Design Flow

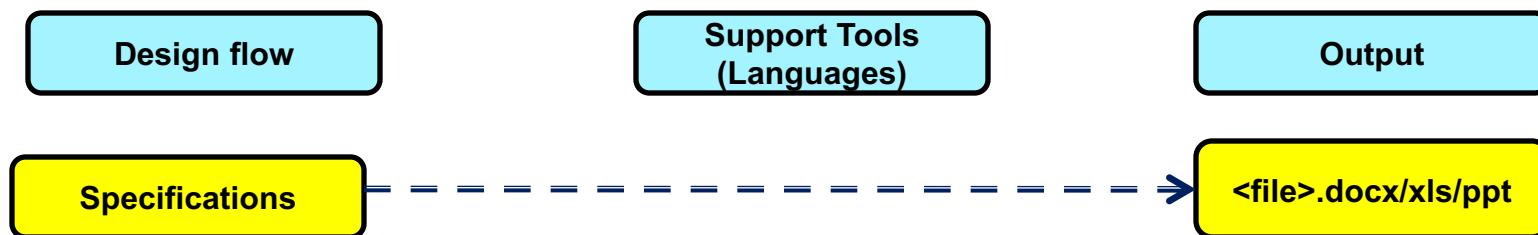
---

Design flow

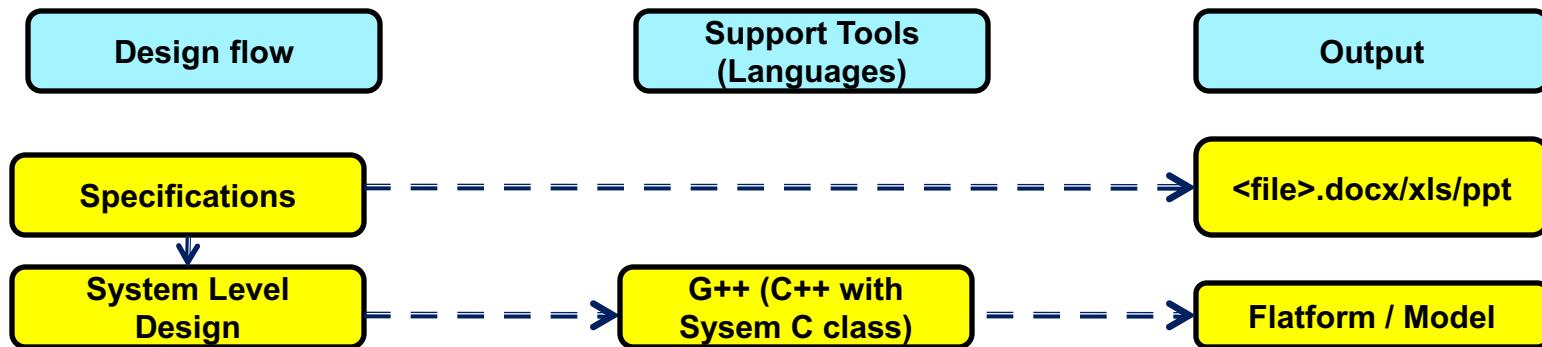
Support Tools  
(Languages)

Output

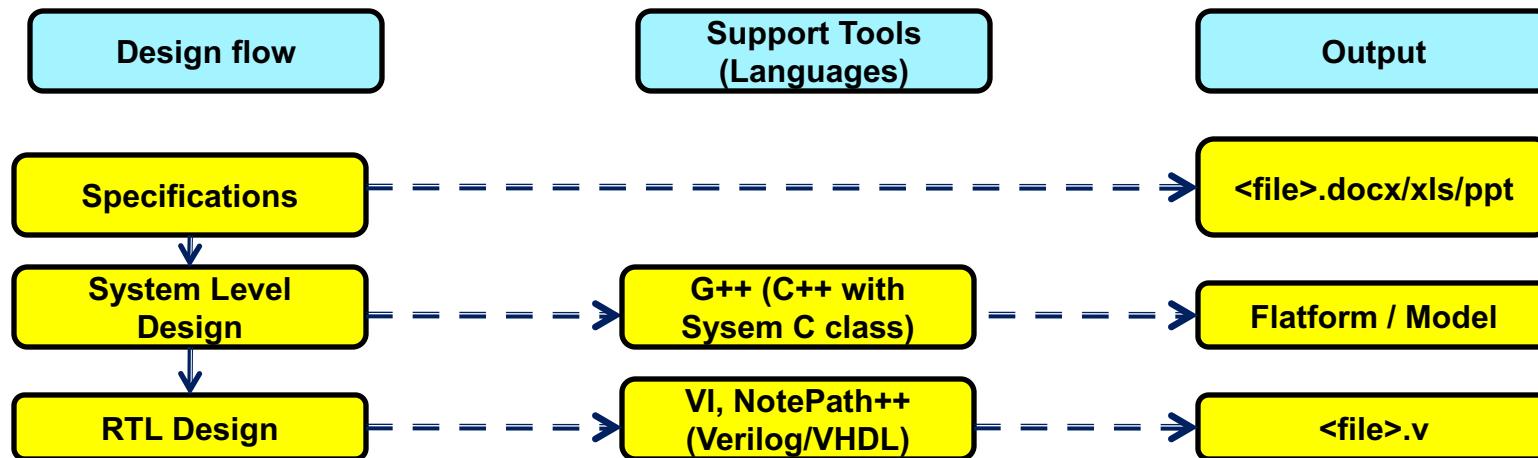
# Cell Base Design Flow



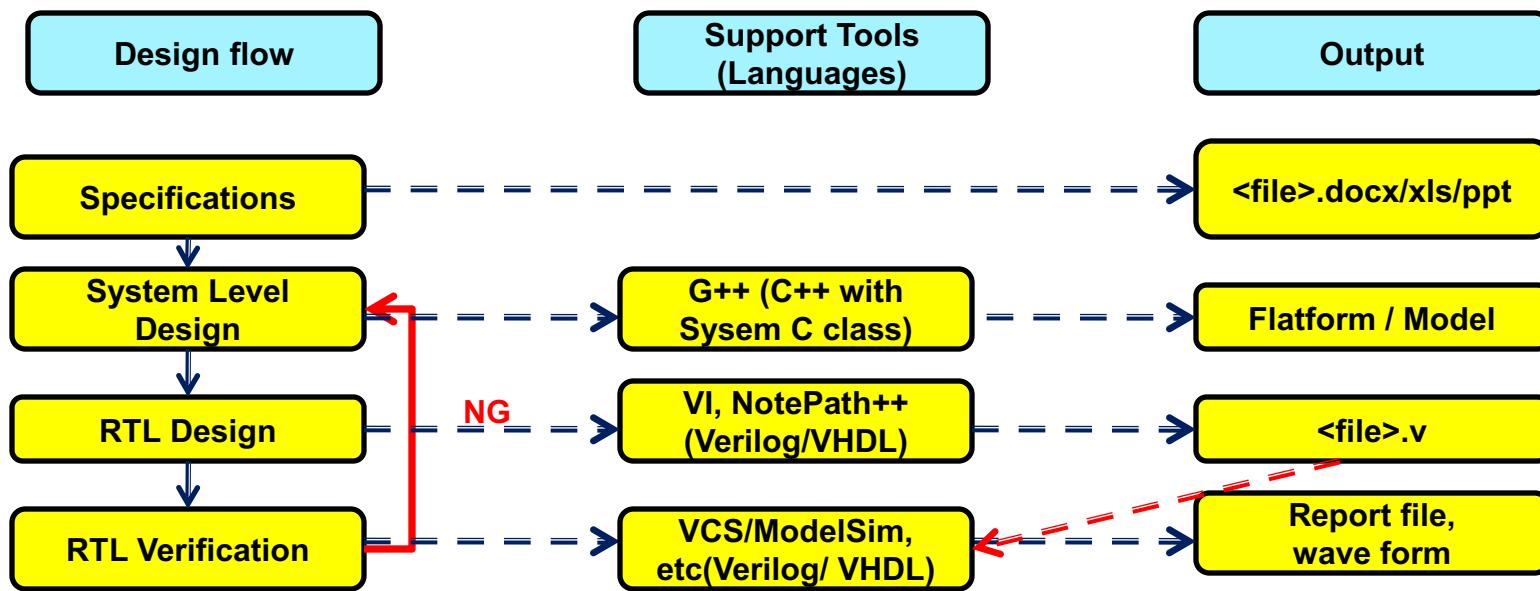
# Cell Base Design Flow



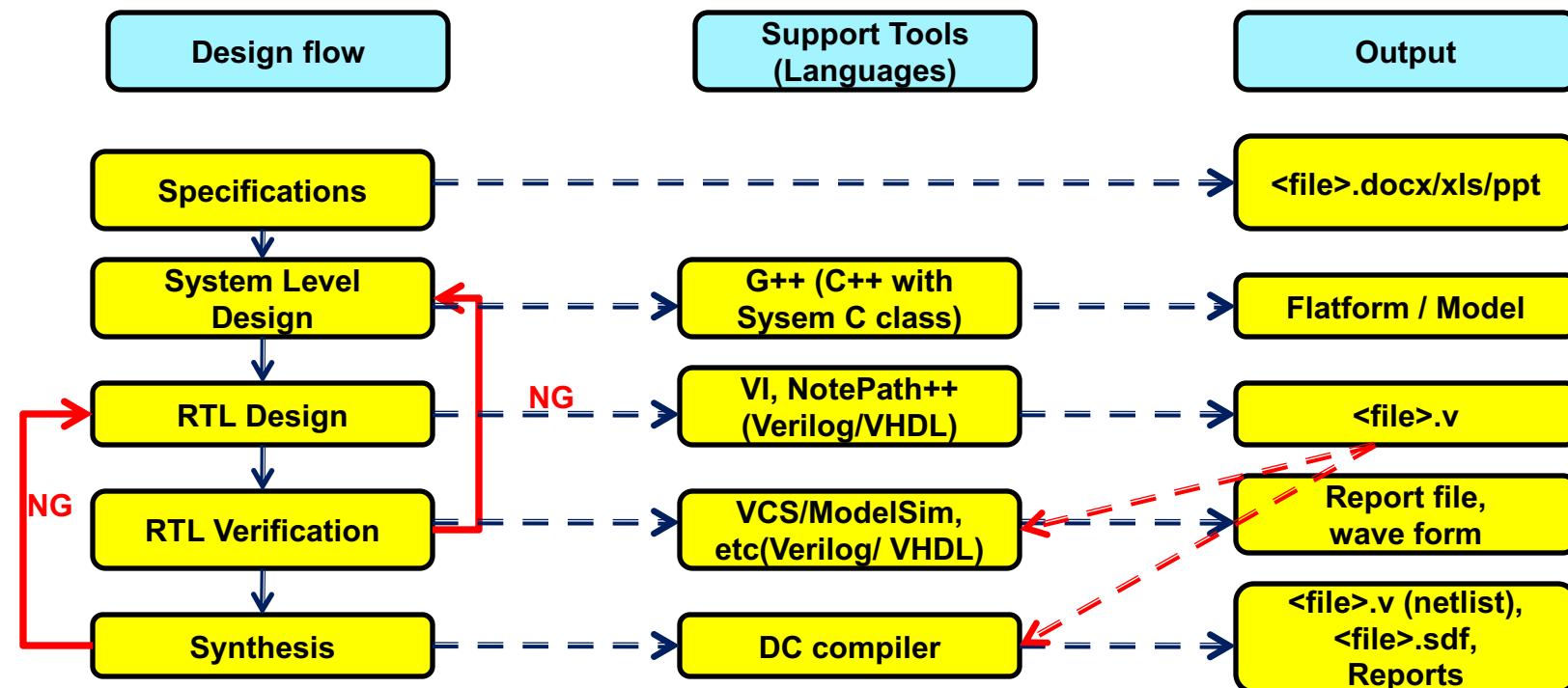
# Cell Base Design Flow



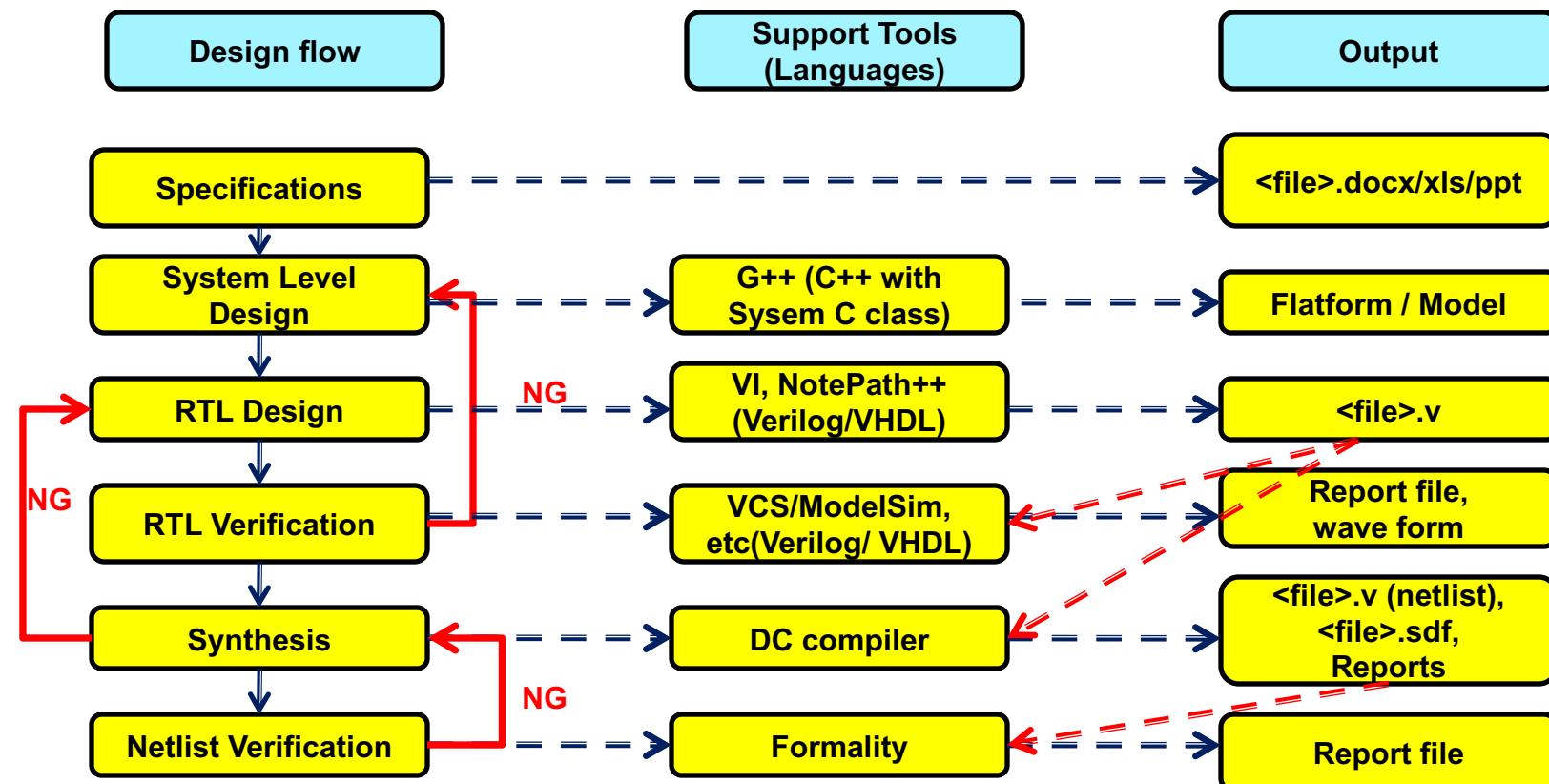
# Cell Base Design Flow



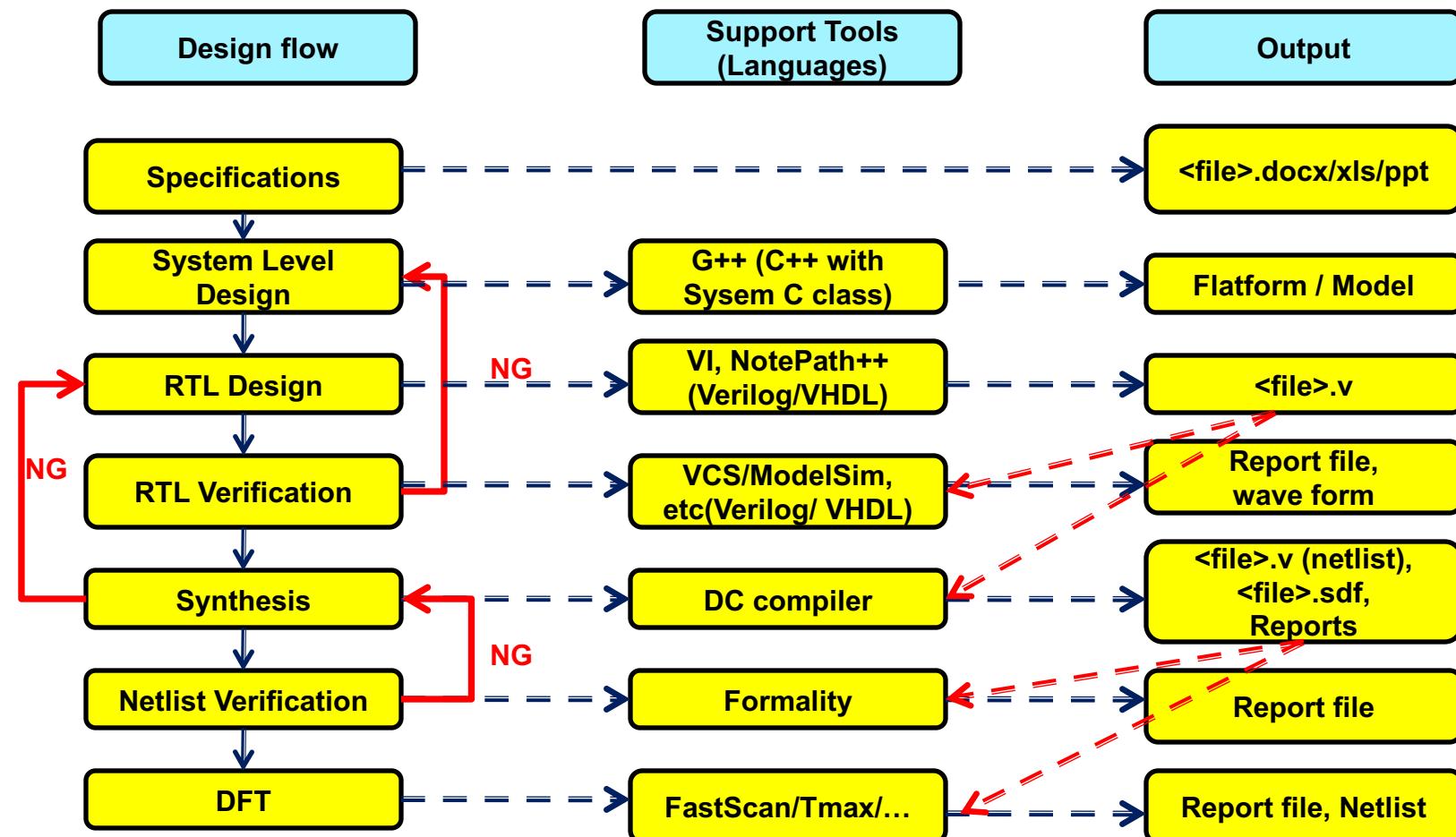
# Cell Base Design Flow



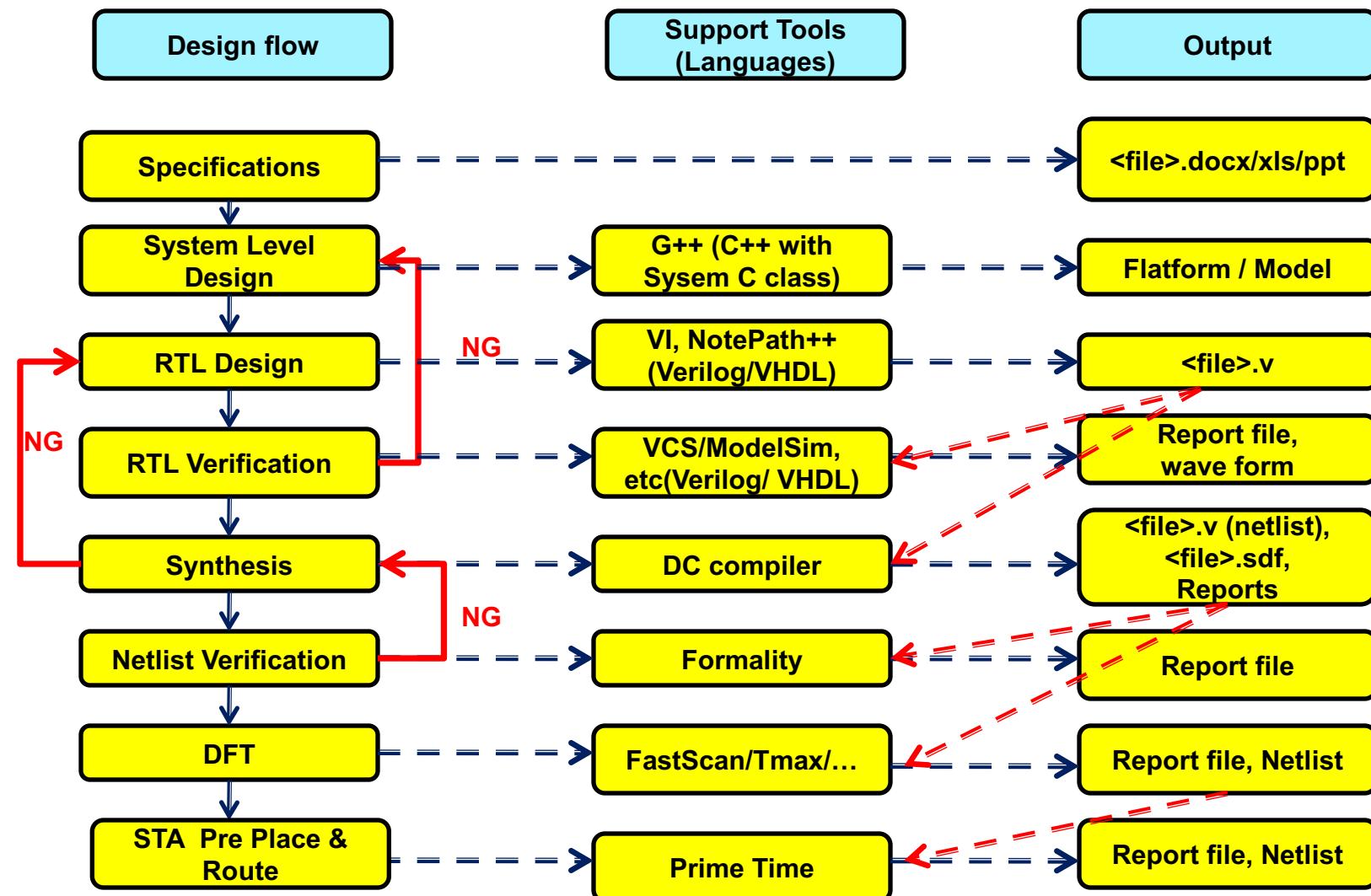
# Cell Base Design Flow



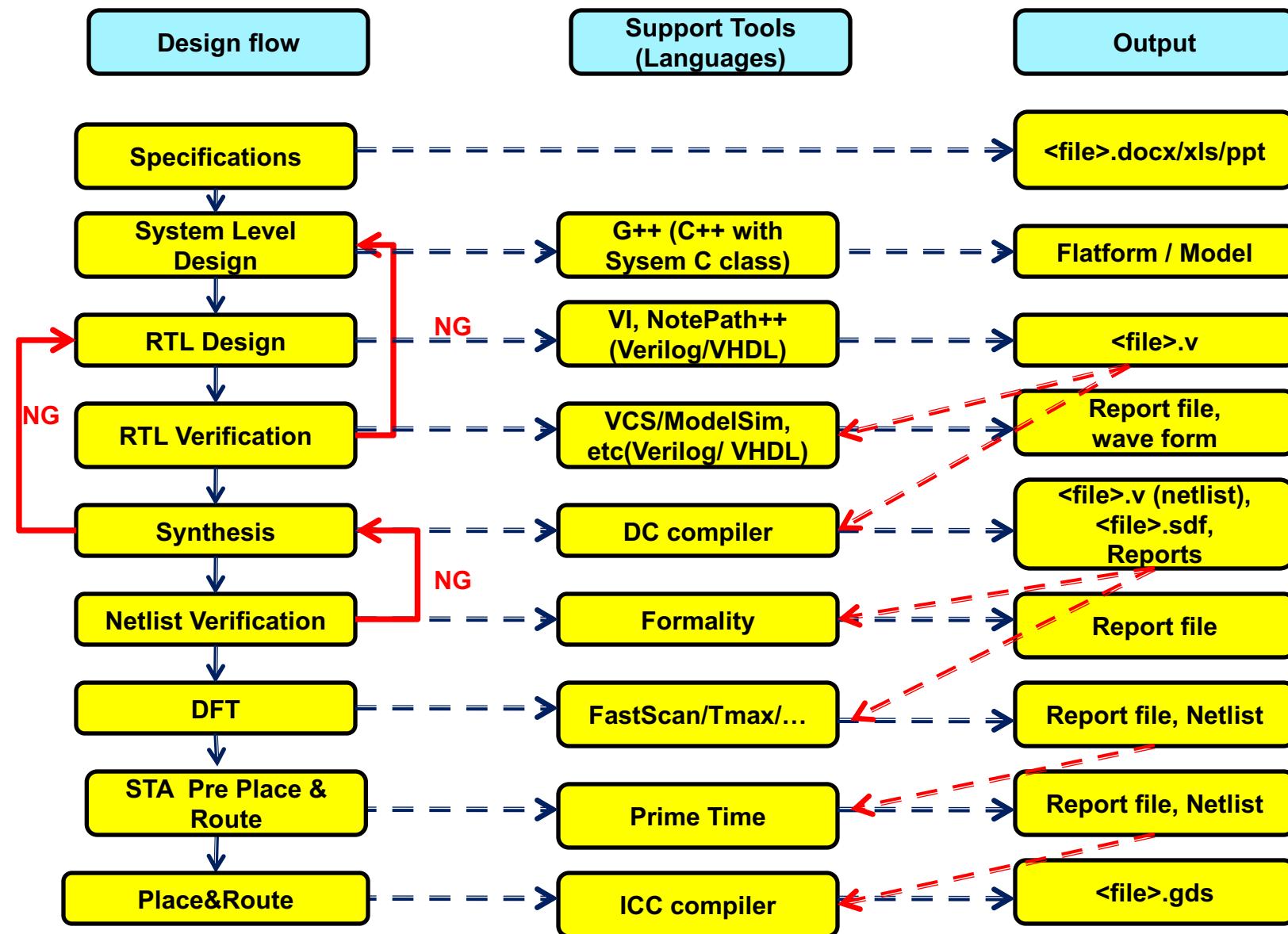
# Cell Base Design Flow



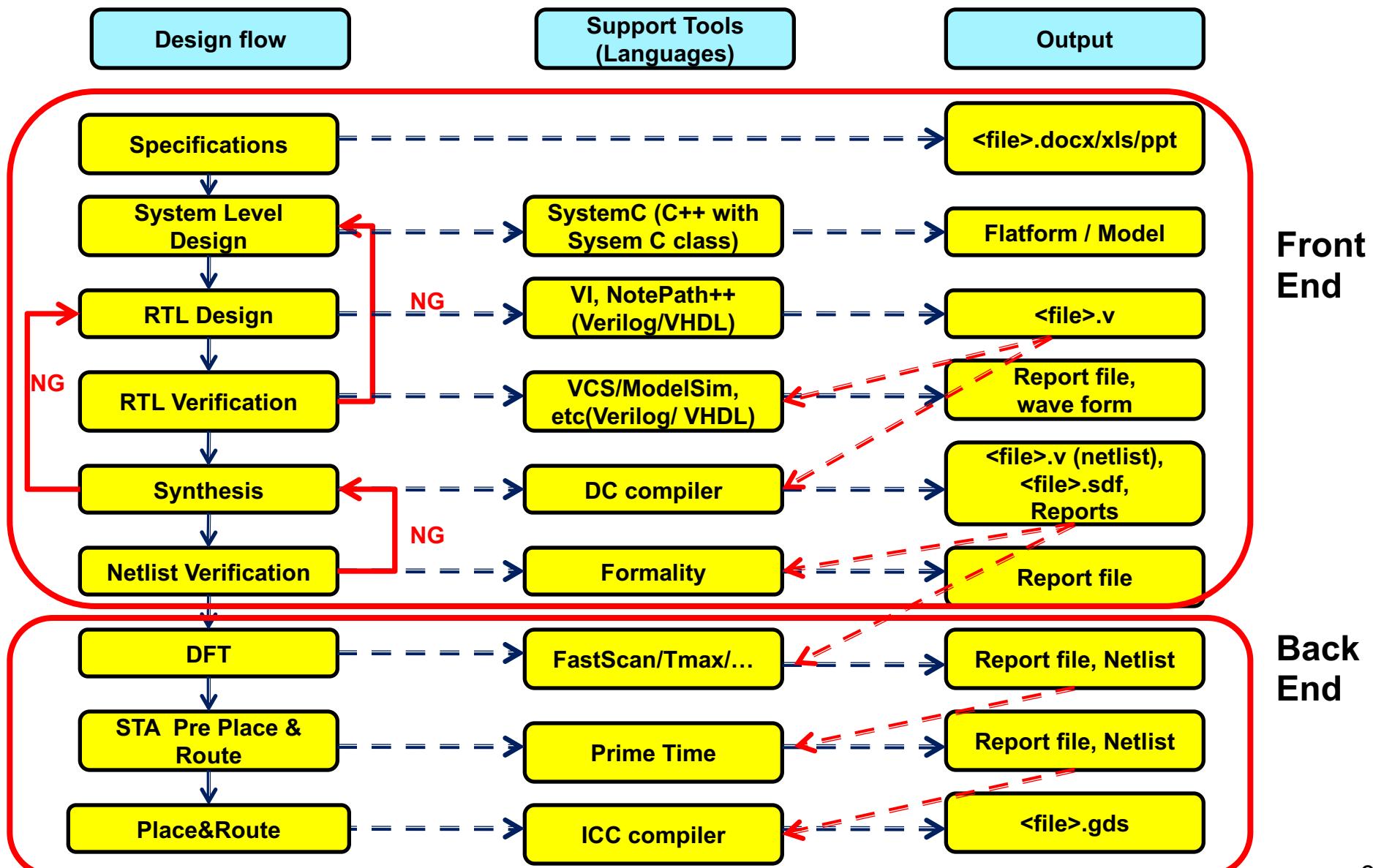
# Cell Base Design Flow



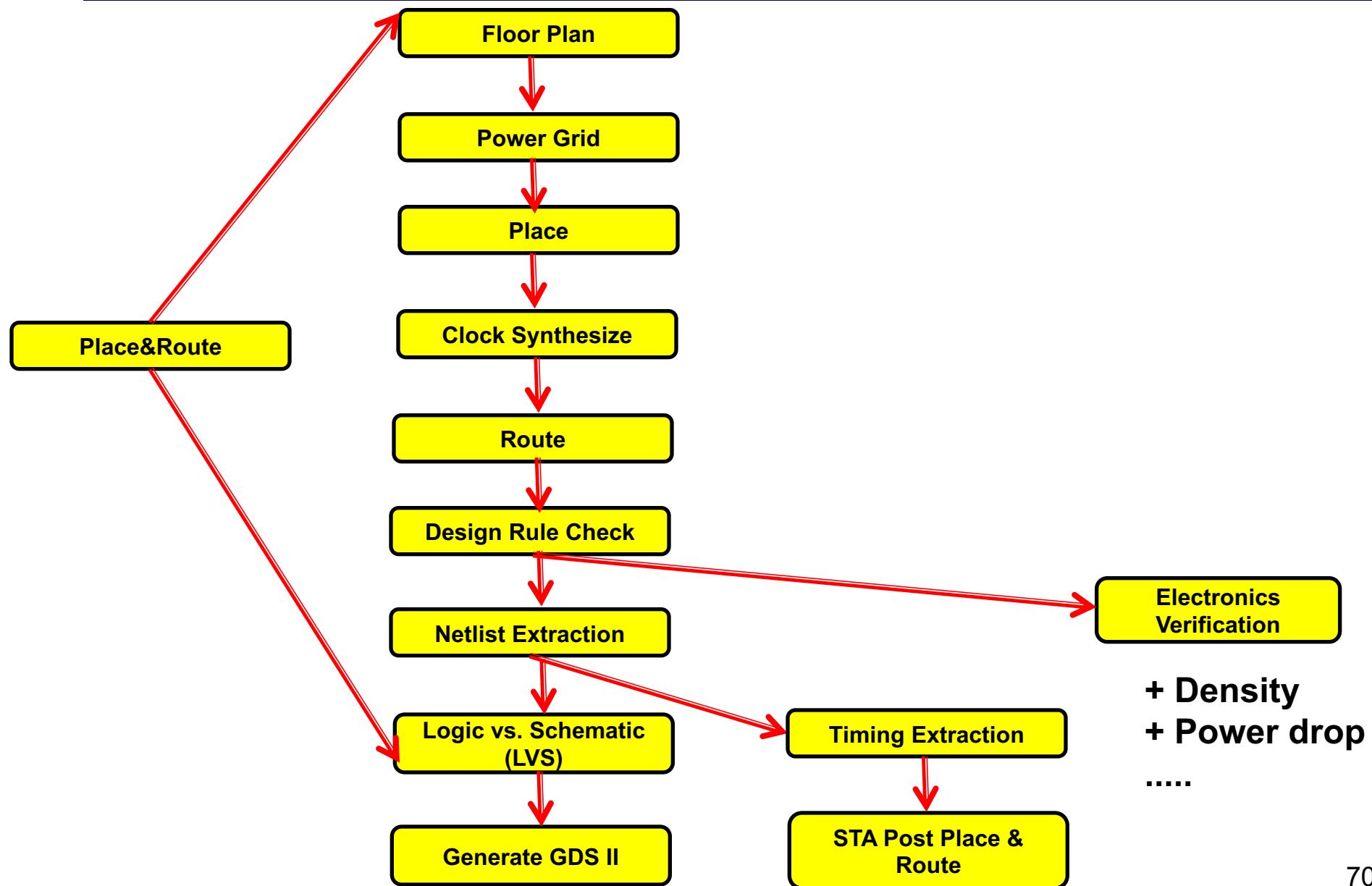
# Cell Base Design Flow



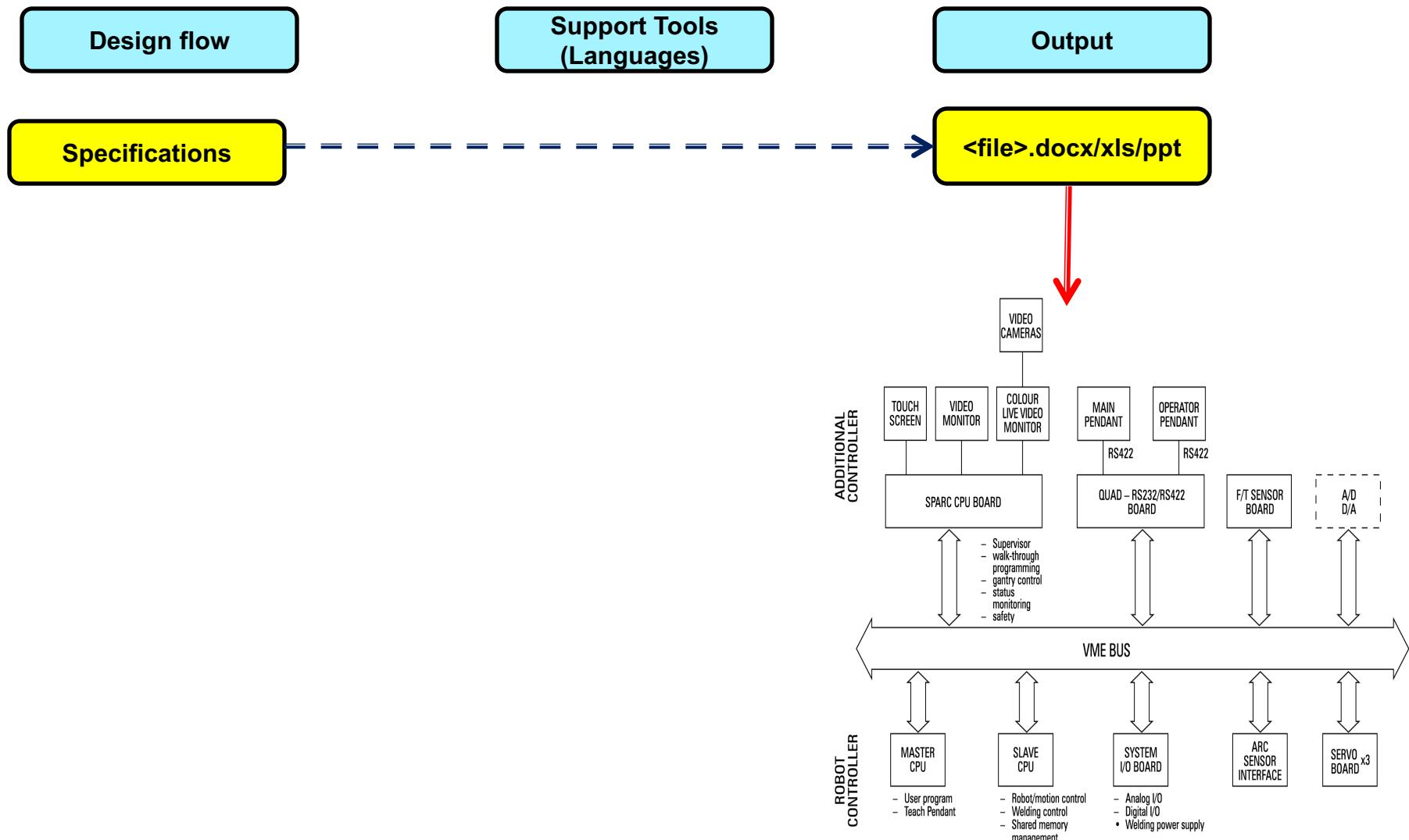
# Cell Base Design Flow



# Cell Base Design Flow



# Cell Base Design Flow



# Cell Base Design Flow

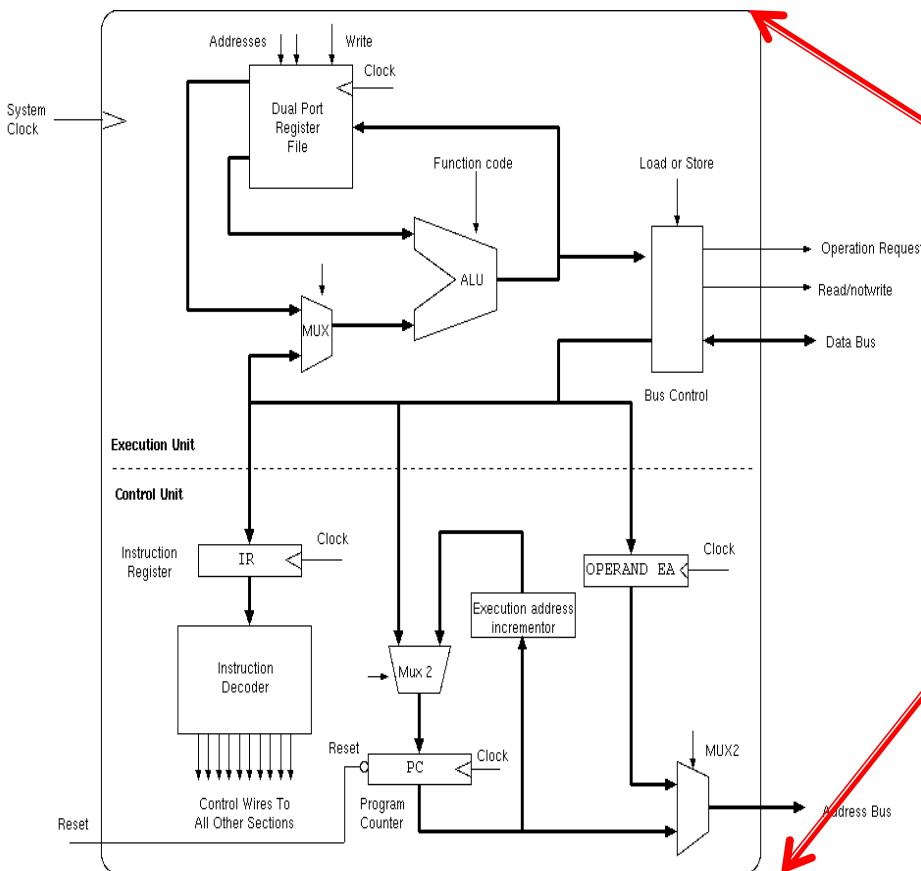
Design flow

Support Tools  
(Languages)

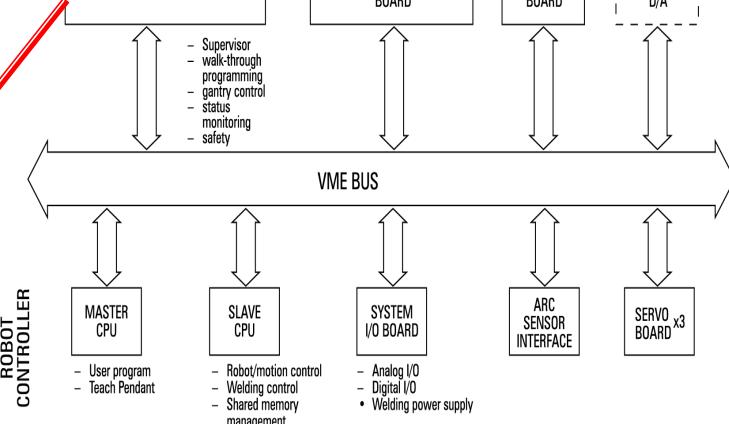
Output

Specifications

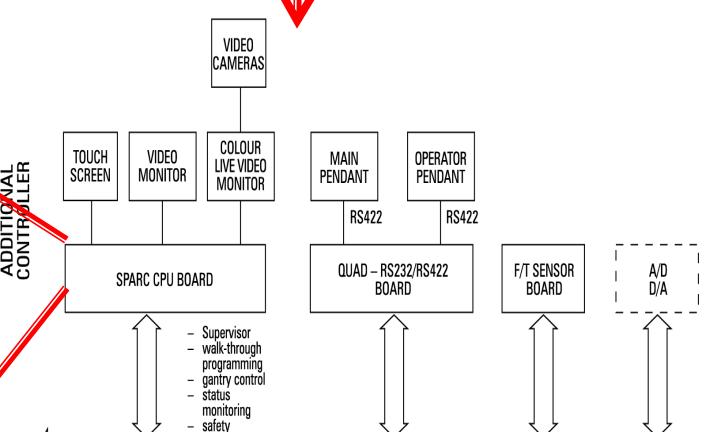
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**ROBOT CONTROLLER**



**ADDITIONAL CONTROLLER**



# Cell Base Design Flow

Design flow

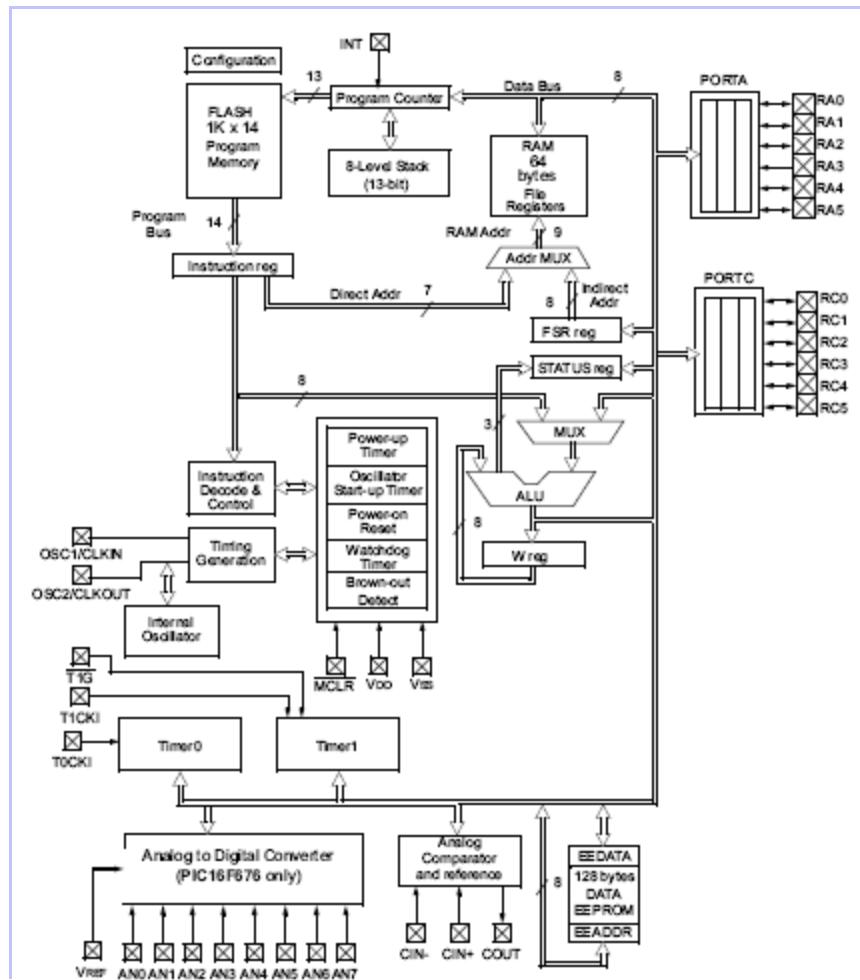
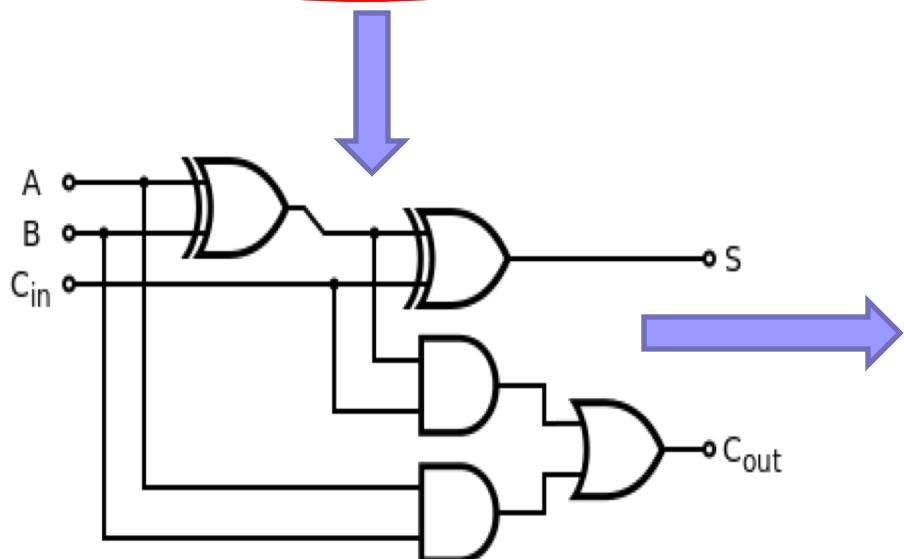
Support Tools  
(Languages)

Output

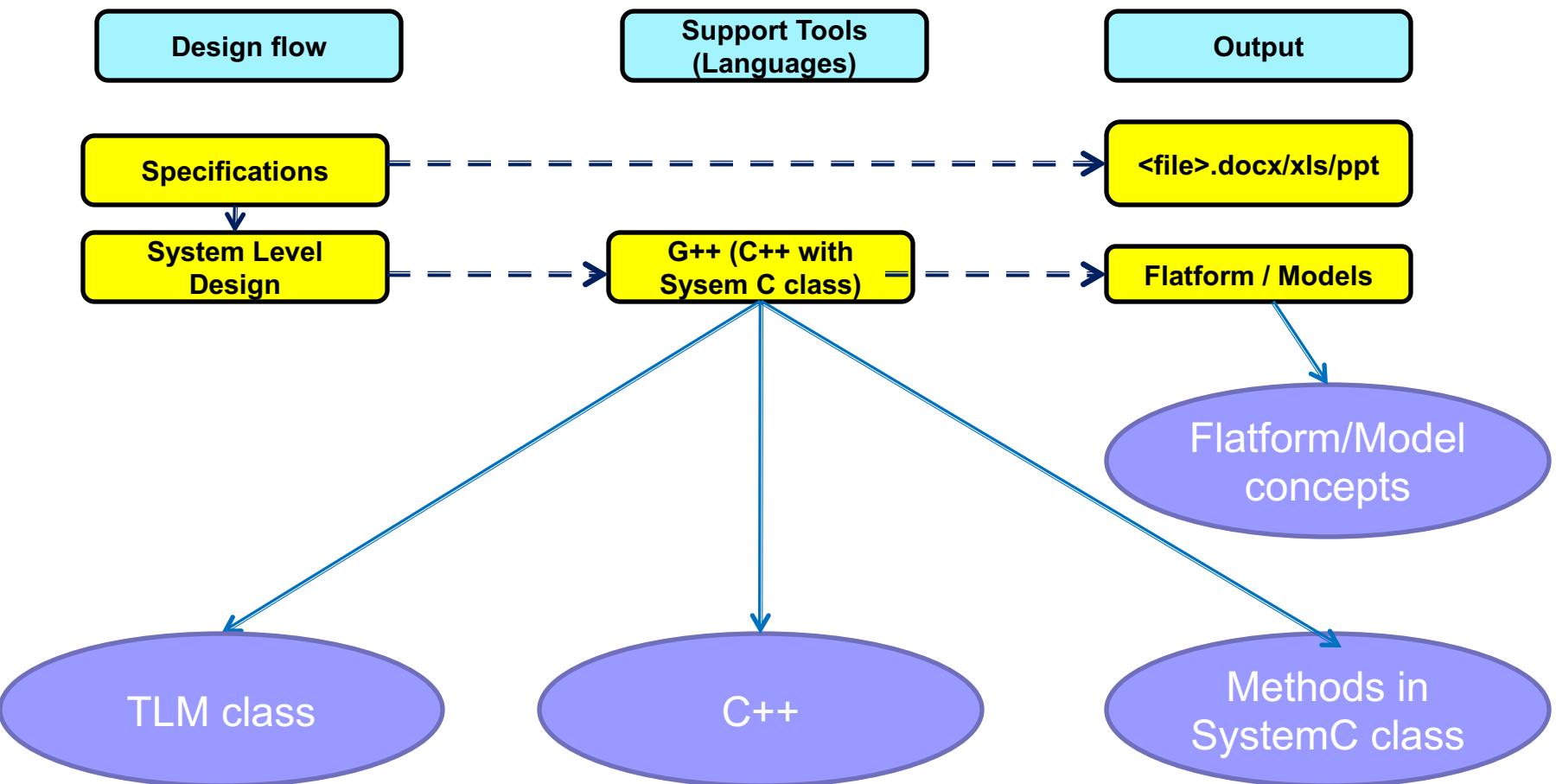
Specifications

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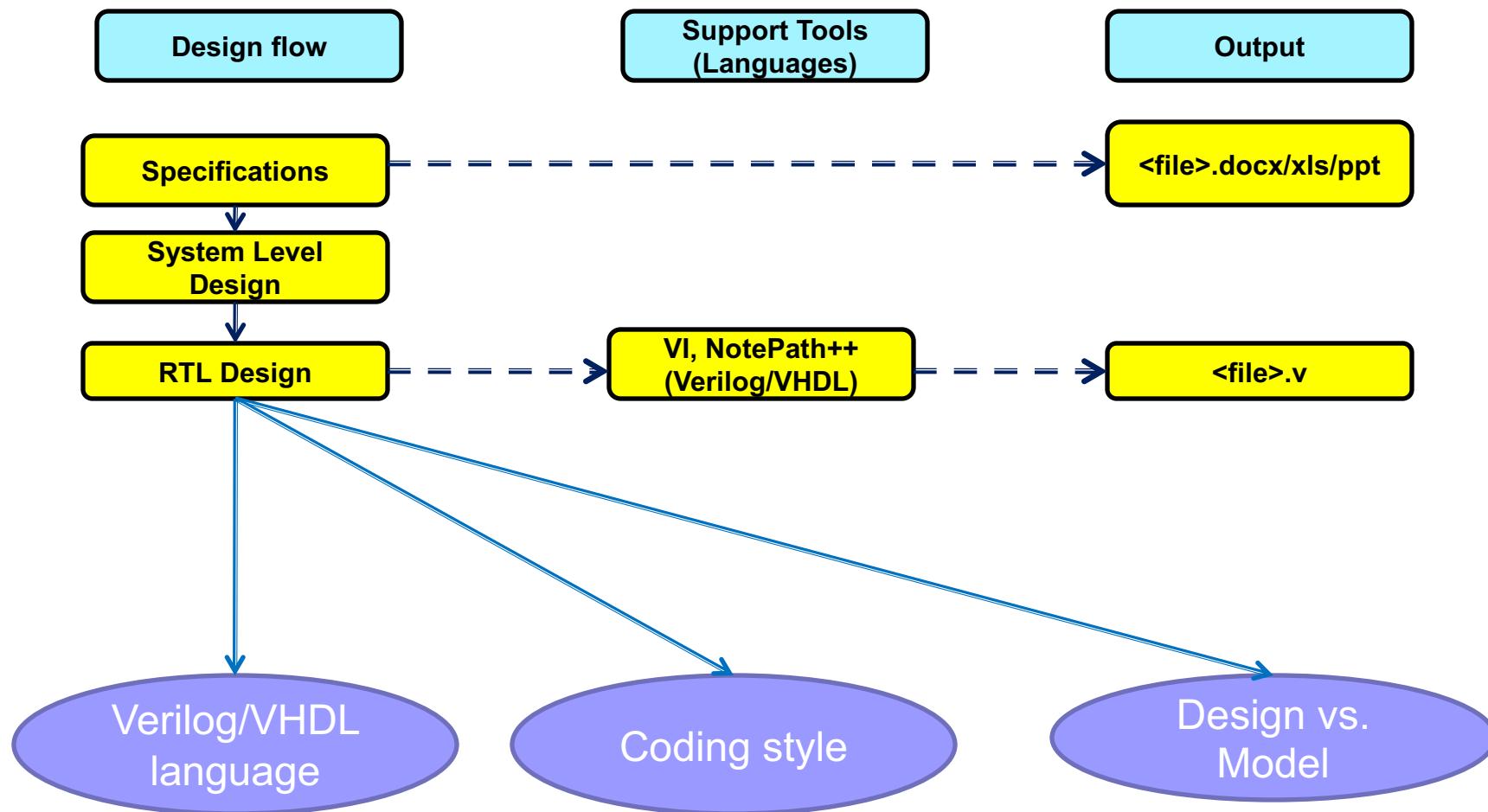
**Design the one bit adder:**  
+ Three inputs (A, B, Cin)  
+ Two output (S, Cout)



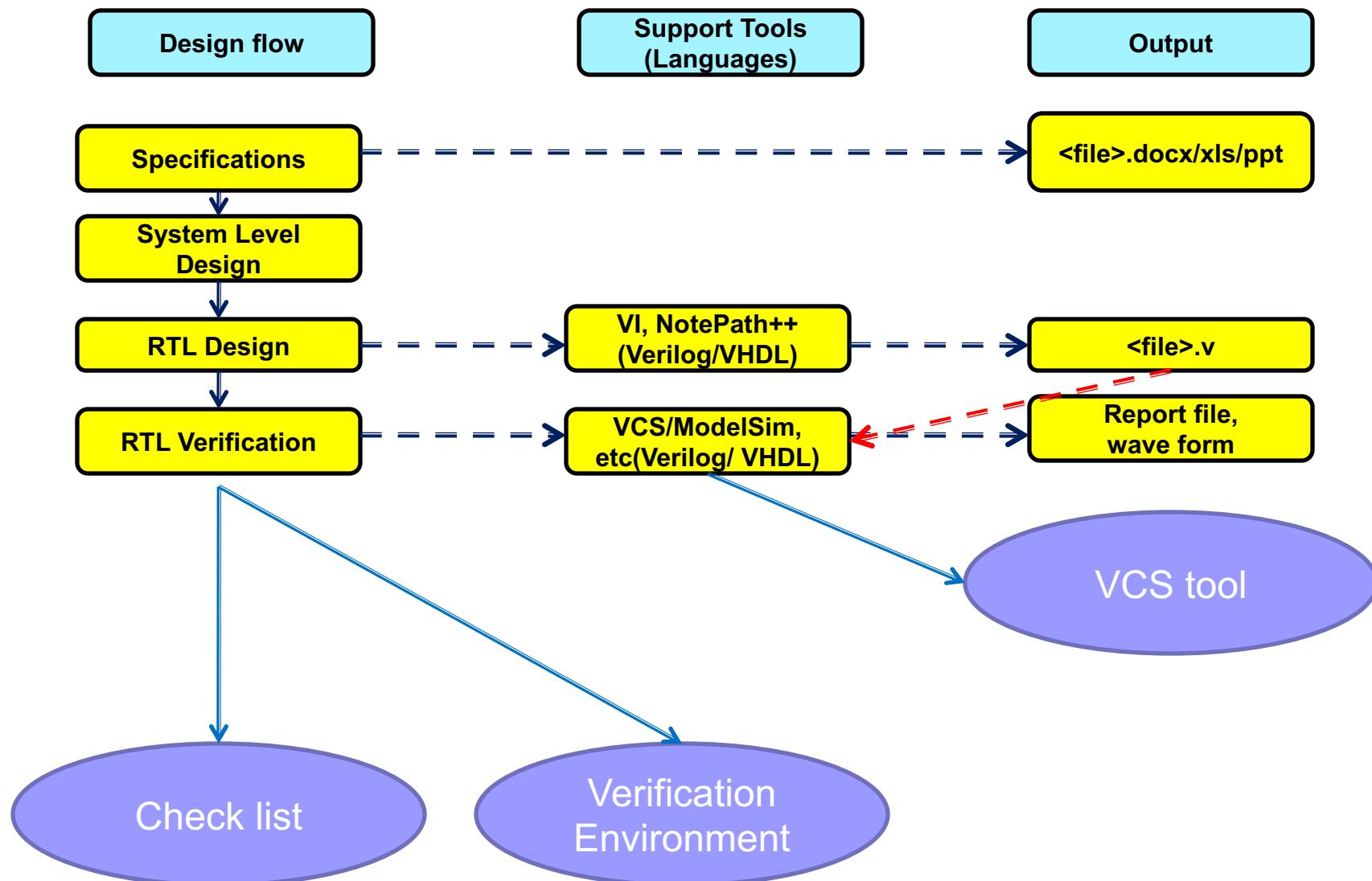
# Cell Base Design Flow



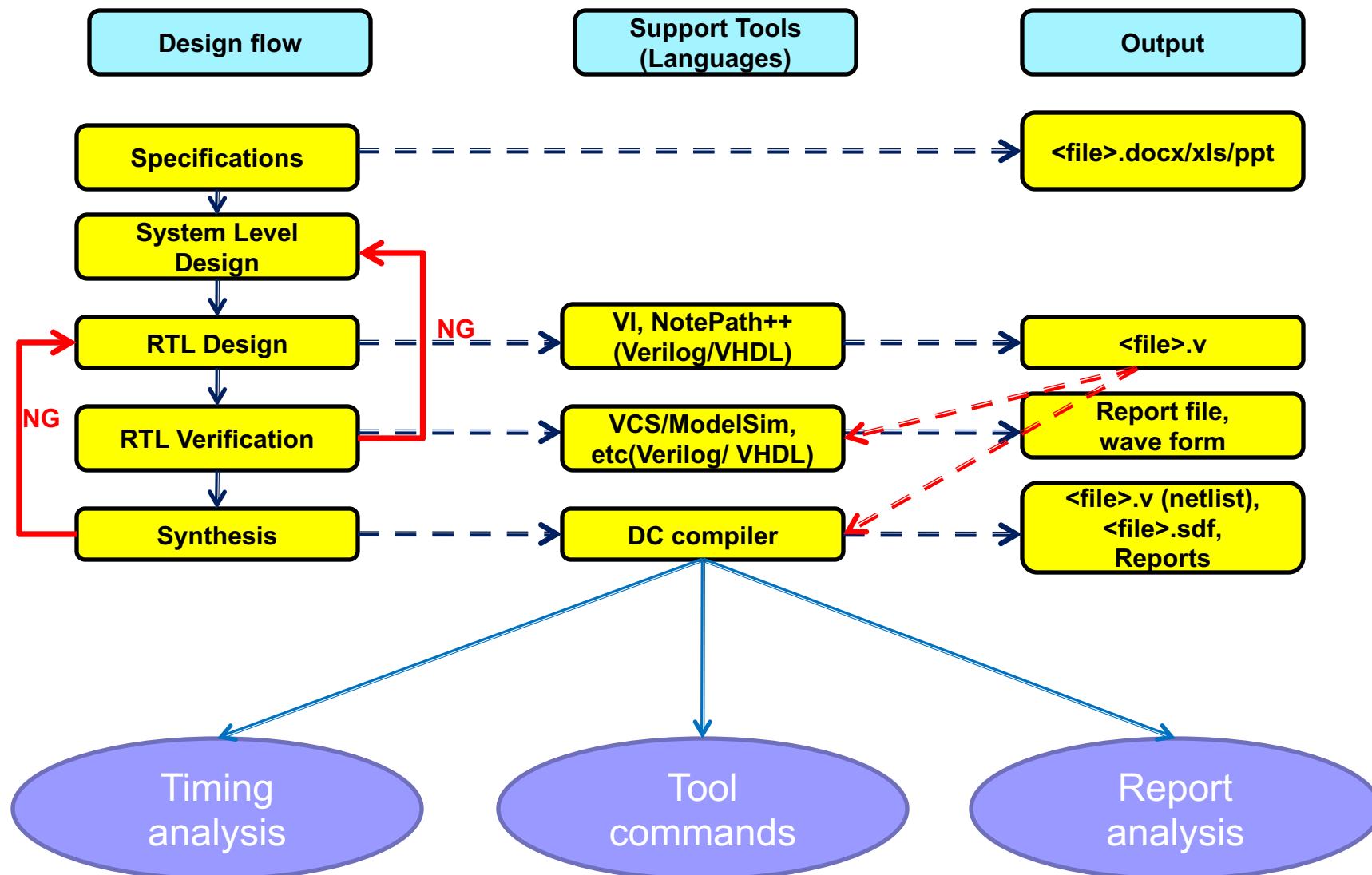
# Cell Base Design Flow



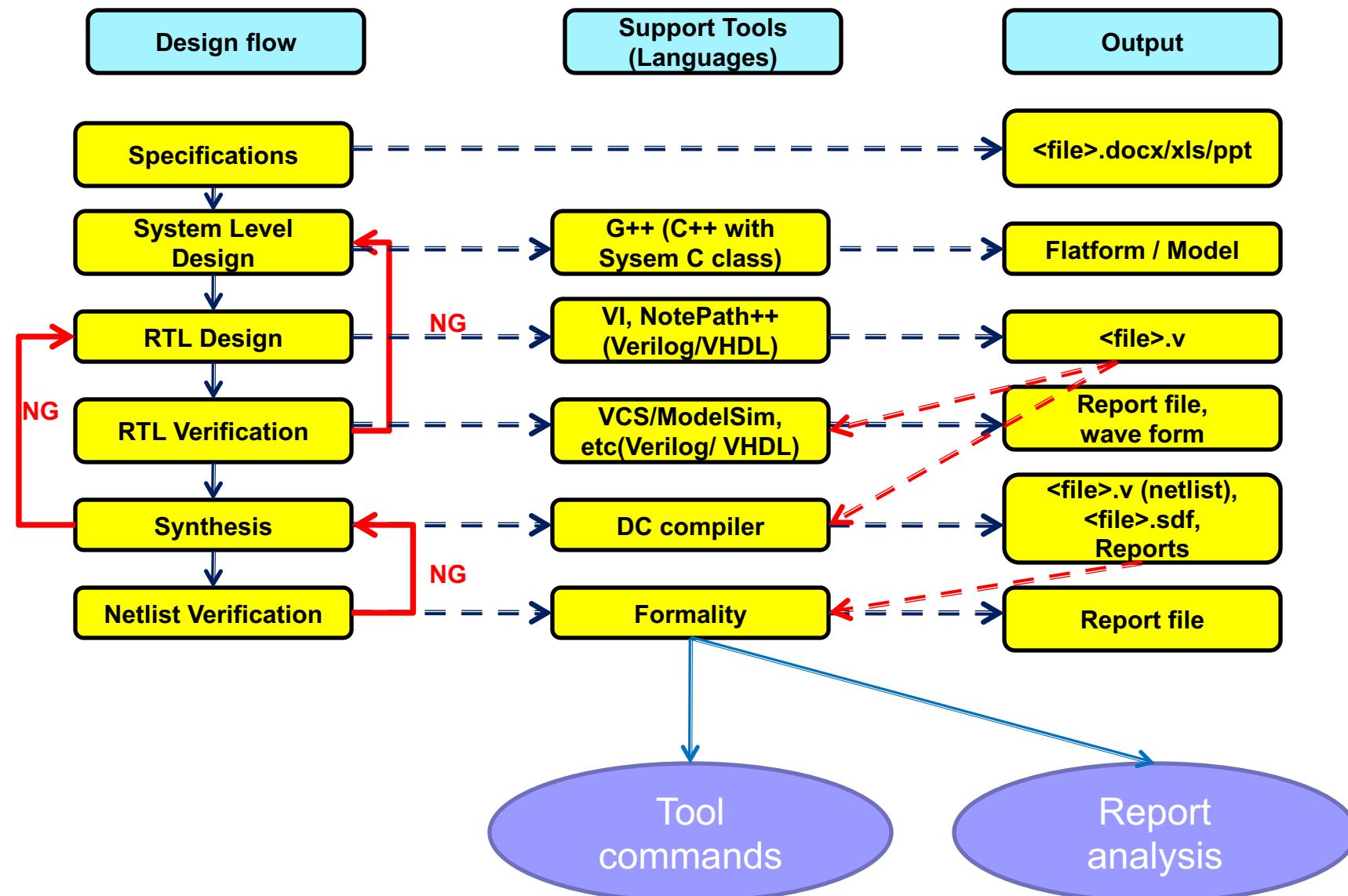
# Cell Base Design Flow



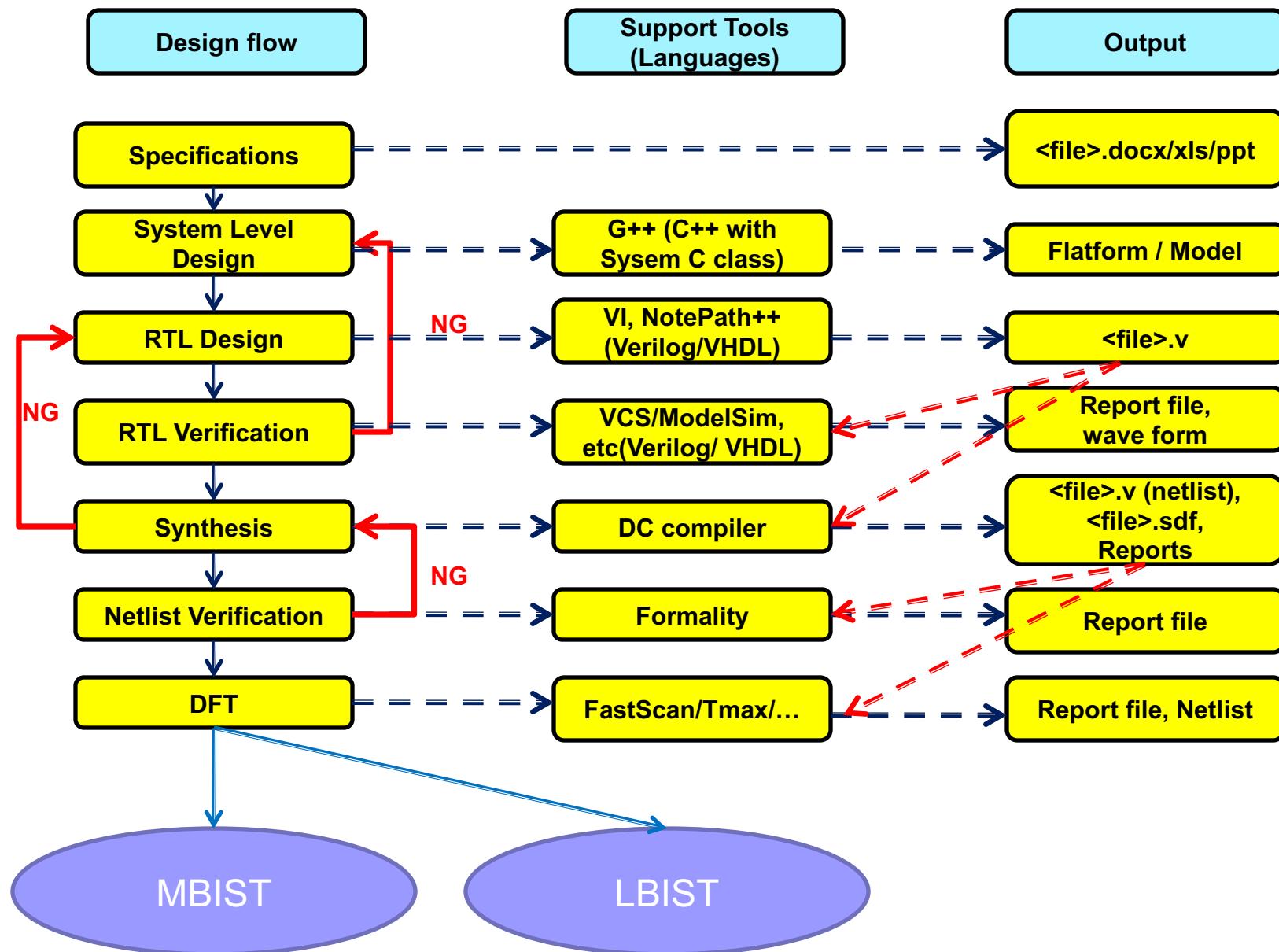
# Cell Base Design Flow



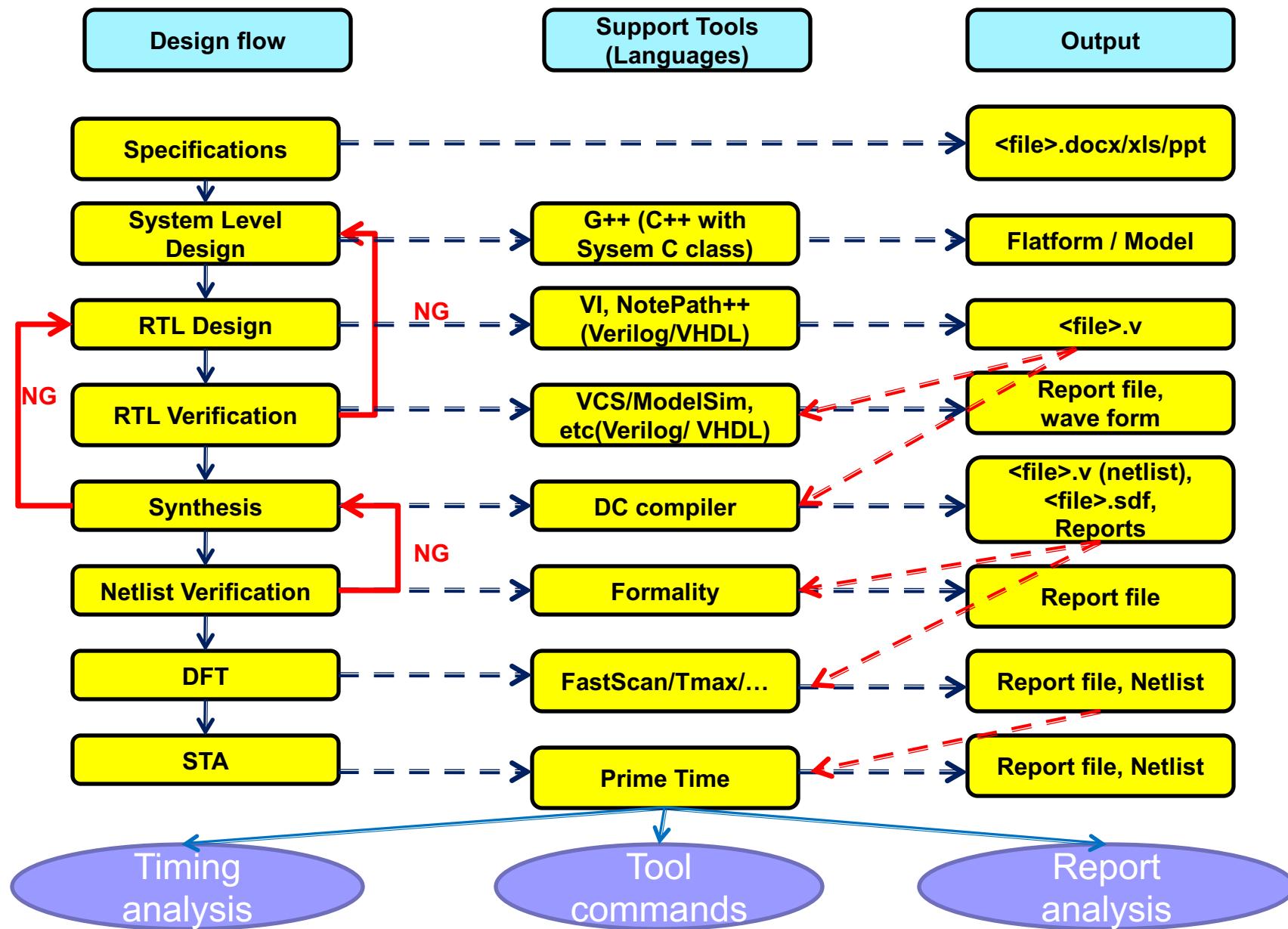
# Cell Base Design Flow



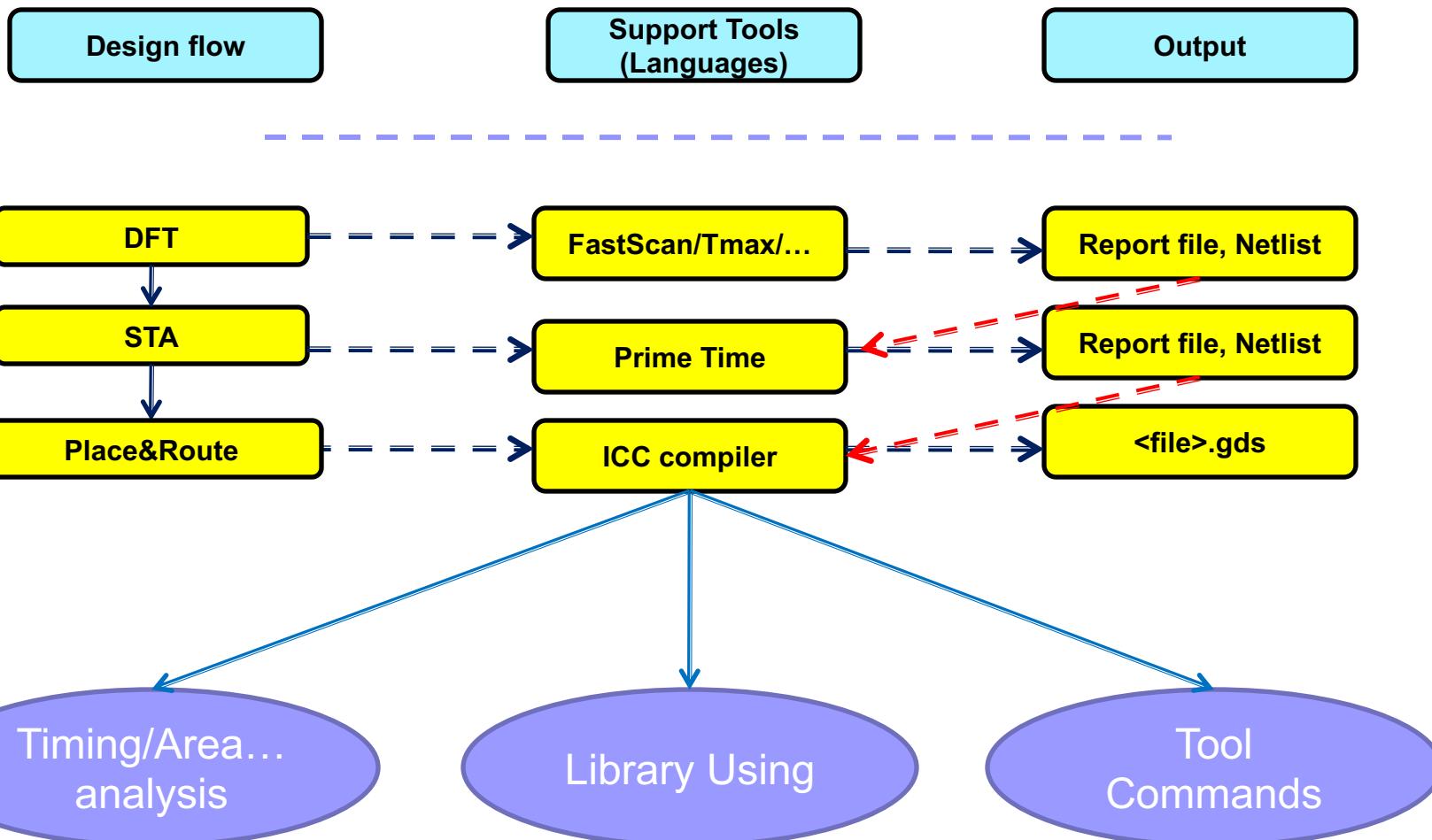
# Cell Base Design Flow



# Cell Base Design Flow



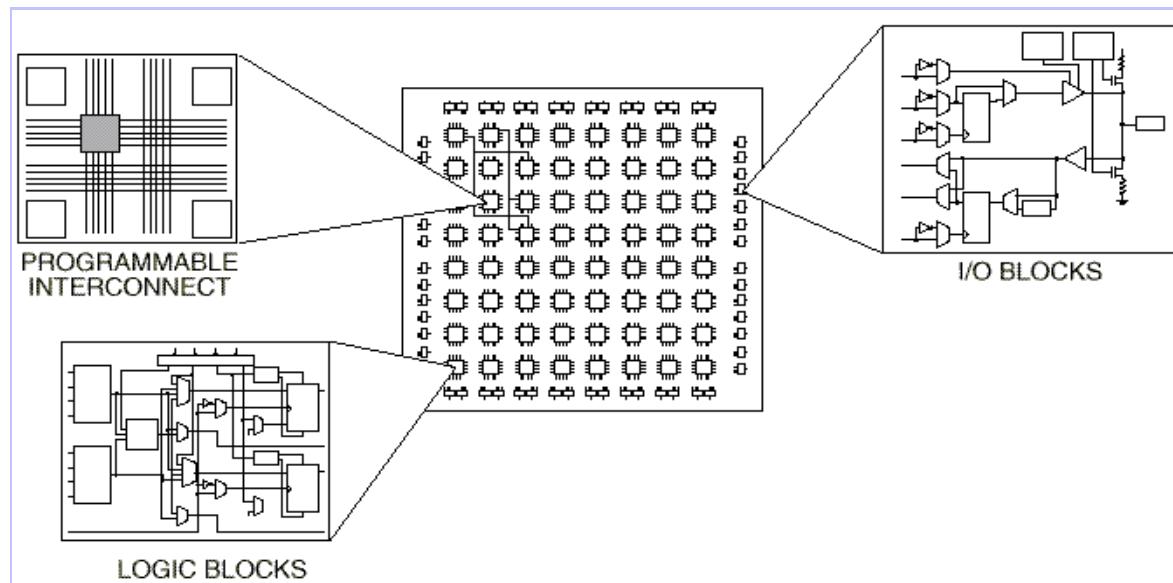
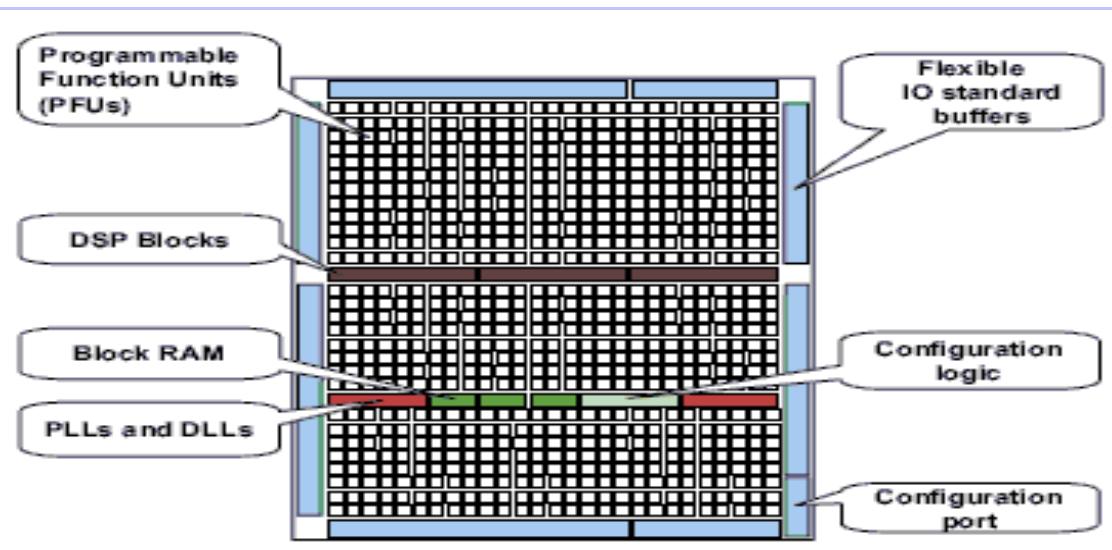
# Cell Base Design Flow



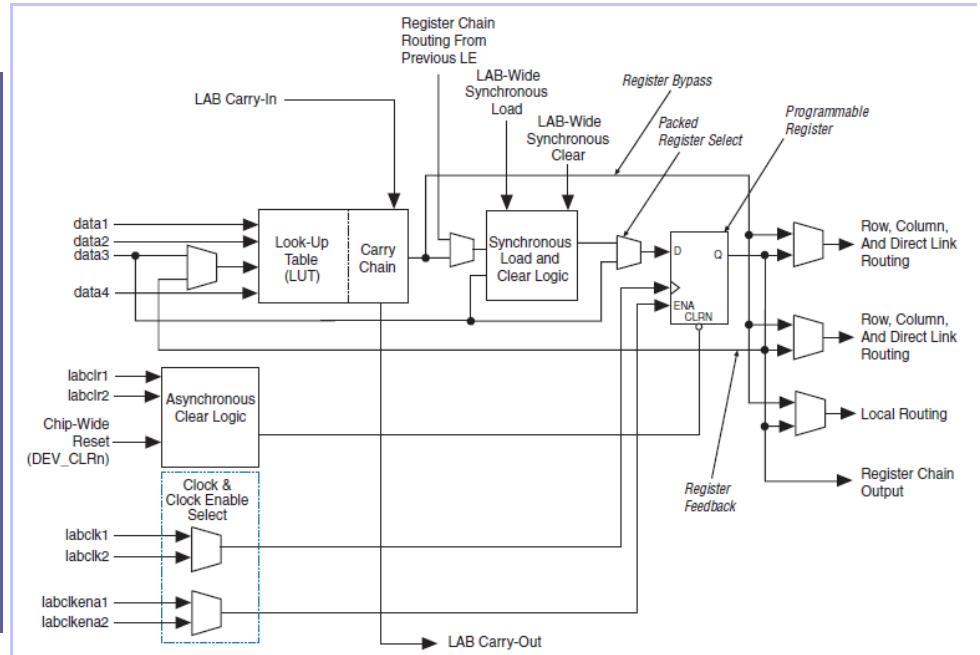
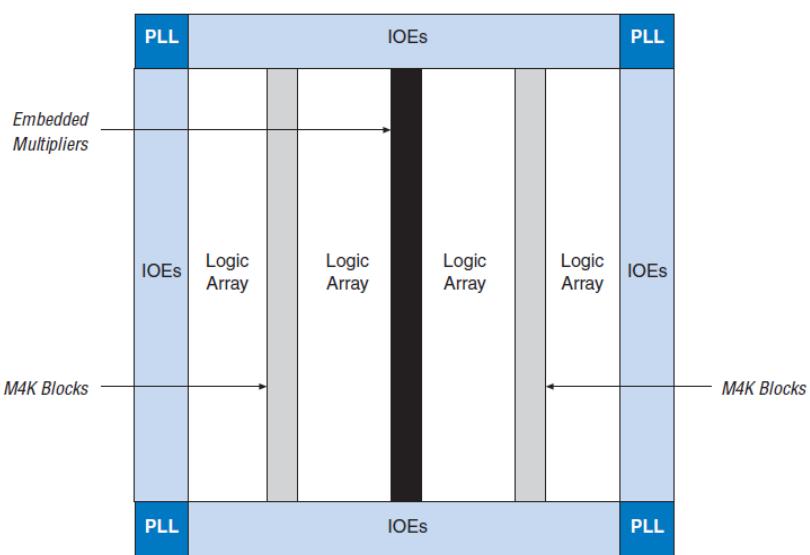
# ASIC Design Flow

- ❖ Cell Base & Custom Design Flow Concepts
- ❖ Custom Design Flow
- ❖ Cell Base Design Flow
- ❖ **ASIC vs. FPGA Design Flow**

# FPGA Field Programmable Gate Array



## Cyclone II EP2C20 Device Block Diagram

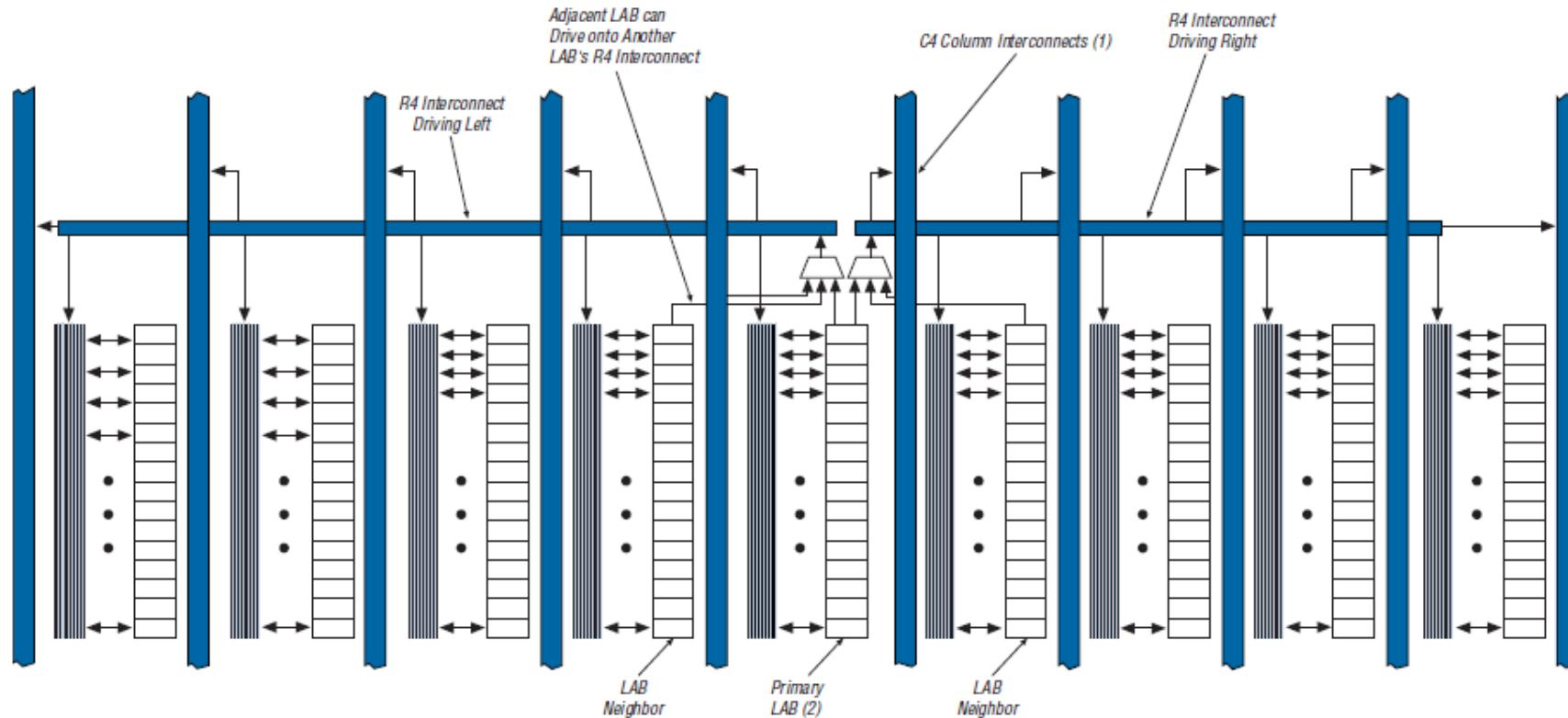


The smallest unit of logic in the Cyclone II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE features:

- A four-input look-up table (LUT), which is a function generator that can implement any function of four variables
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and direct link interconnects
- Support for register packing
- Support for register feedback

# FPGA

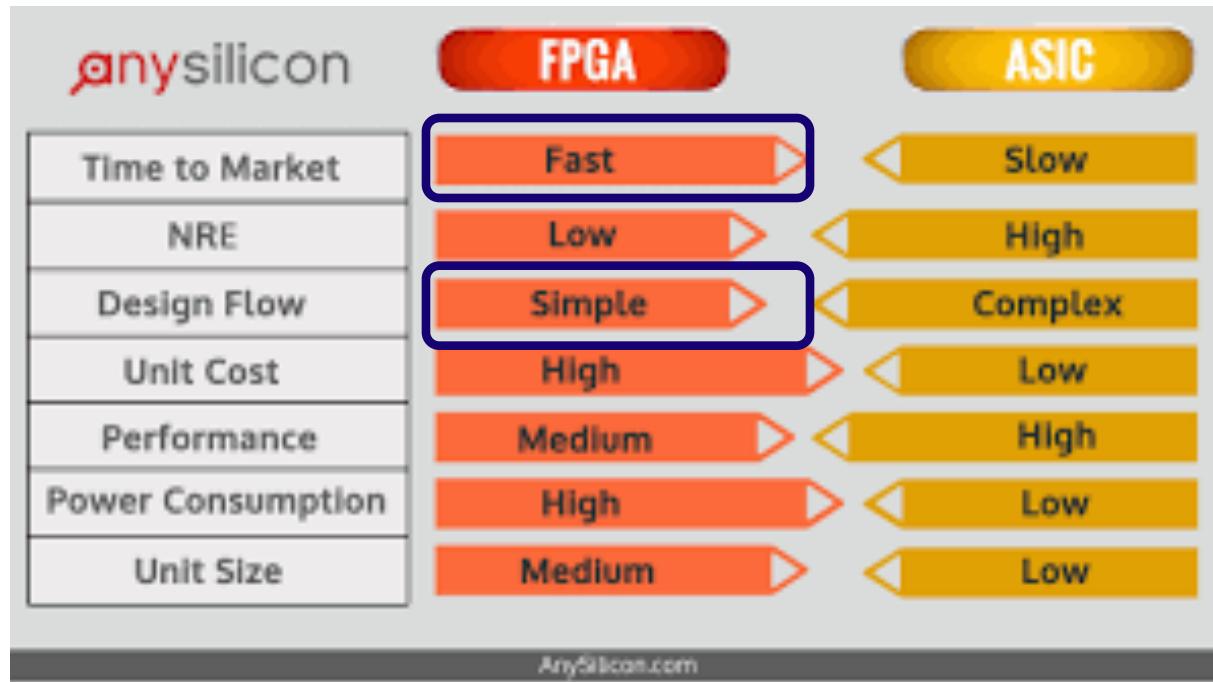
Cyclone<sup>®</sup> Architecture  
[www.altera.com](http://www.altera.com)



## Cyclone II FPGA Family Overview

Device	EP2C5	EP2C8	EP2C15	EP2C20	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	14,448	18,752	33,216	50,528	68,416
M4K RAM Blocks (4 kbits + 512 Parity Bits)	26	36	52	52	105	129	250
Embedded Memory (Kbits)	117	162	234	234	473	581	1,125
18-Bit x 18-Bit Embedded Multipliers	13	18	26	26	35	86	150
PLLs	2	2	4	4	4	4	4
Maximum User I/O Pins	158	182	315	315	475	450	622
Differential Channels	58	77	132	132	205	193	262

# FPGA vs. ASIC



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# Q & A

# Appendix

Language	Design Level	Simulation	Synthesizable	Explicit Hardware Resource	Elapsed Time	Sequence
C++	Transaction	Yes	No	No	No	Yes
SystemC	Transaction	Yes	Yes*	No	Yes	Yes
VHDL	RTL	Yes	Yes*	Yes*	Yes	Yes
Verilog	RTL	Yes	Yes*	Yes*	Yes	Yes
Verilog/VHDL Netlist	Gate	Yes	Yes	Yes	Yes	Yes

**Yes\*:** Base on the **constraints** to be able or not