Static Timing Analysis

Static Timing Analysis

- Dynamic vs. Static Timing Analysis
- Performance of Design
- Synthesis step

Dynamic vs. Static Timing Analysis

❖Timing analysis is integral part of ASIC/VLSI design flow. Anything else can be compromised but not timing! Timing analysis can be **static** or **dynamic**.

❖**Dynamic timing analysis verifies functionality** of the design by applying input vectors and checking for correct output vectors whereas **Static Timing Analysis** checks **static delay requirements** of the circuit without any input or output vectors.

❖**Dynamic timing analysis(DTA)** has to be accomplished and functionality of the design must be cleared **before** the design is subjected to **Static Timing Analysis (STA).**

❖**Dynamic Timing Analysis (DTA)** and **Static Timing Analysis (STA)** are **not alternatives** to each other.

❖**Quality of the Dynamic Timing Analysis (DTA) increases** with the **increase of input test vectors**. Increased test vectors increase simulation time. Dynamic timing analysis can be **used for synchronous as well as asynchronous designs.** Dynamic Timing Analysis (DTA) is also **best suitable for designs having clocks crossing multiple domains**

❖**Static Timing Analysis (STA) can't run on asynchronous deigns** and hence Dynamic Timing Analysis (DTA) is the best way to analyze asynchronous designs. .

Dynamic vs. Static Timing Analysis

❖In **Static Timing Analysis (STA)** static delays such as **gate delay and net delays** are considered in each path and these delays are compared against their required maximum and minimum values.

❖ Circuit to be analyzed is broken into different timing paths constituting of gates, flip flops and their interconnections. Each timing path has to process the data within a clock period which is determined by the maximum frequency of operation.

❖**Cell delays are available in the corresponding technology libraries.** Cell delay values are tabulated based on input transition and fanout load which are characterized by simulation tools.

❖ **Net delays are calculated based on the Wire Load Models(WLM)** or extracted resistance R and capacitance C. Wire Load Models(WLM) are available in the Technology File. These values are Table Look Up(TLU) values calculated based on the net fanout length.

Dynamic vs. Static Timing Analysis

Advantages of STA:

❖All timing paths are considered for the timing analysis. This is not the case in simulation.

❖Analysis times are relatively short when compared with event and circuit simulation.

❖Timing can be analyzed for worst case, best case simultaneously. This type of analysis is not possible in dynamic timing analysis.

❖Static Timing Analysis (STA) works with timing models. STA has more pessimism and thus gives maximum delay of the design. DTA performs full timing simulation. The problem associated with DTA is the computational complexity involved in finding the input patterns (vectors) that produce maximum delay at the output and hence it is slow.

Dynamic vs. Static Timing Analysis

Disadvantages of STA:

❖All paths in the design may not run always in worst case delay. Hence the analysis is pessimistic.

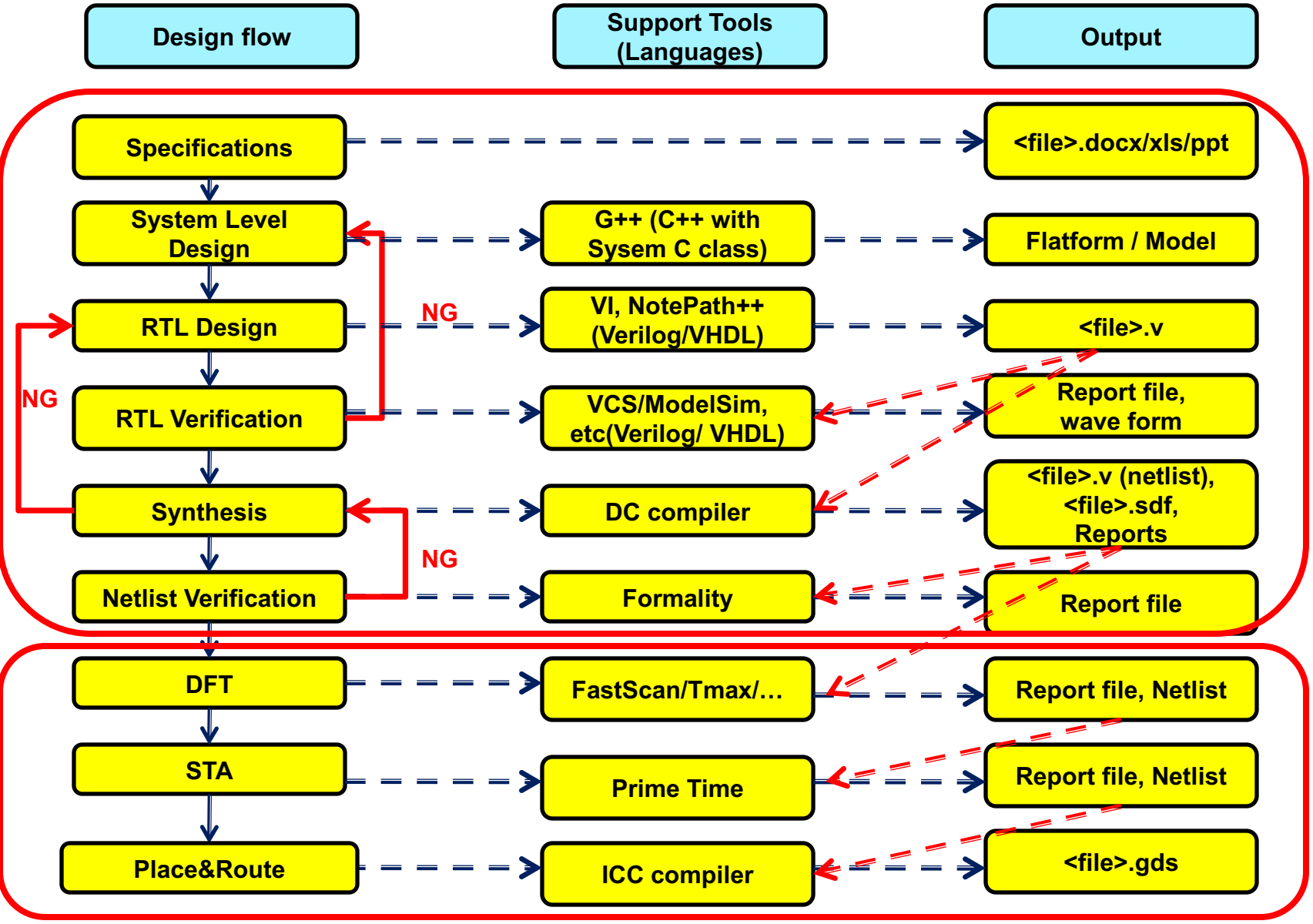
❖Clock related all information has to be fed to the design in the form of constraints.

❖Inconsistency or incorrectness or under constraining of these constraints may lead to disastrous timing analysis.

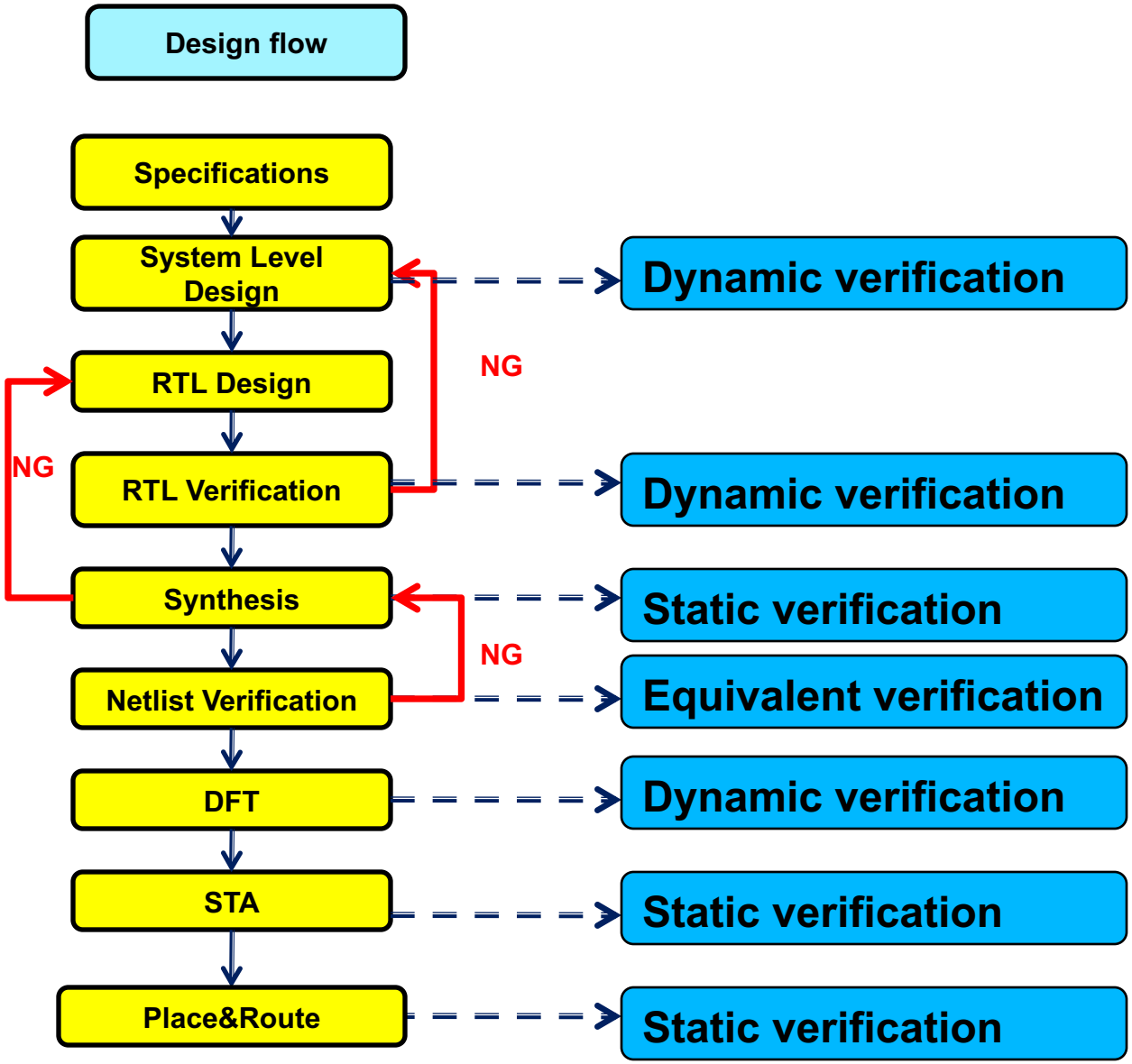
❖STA does not check for logical correctness of the design.

❖STA is not suitable for asynchronous circuits.

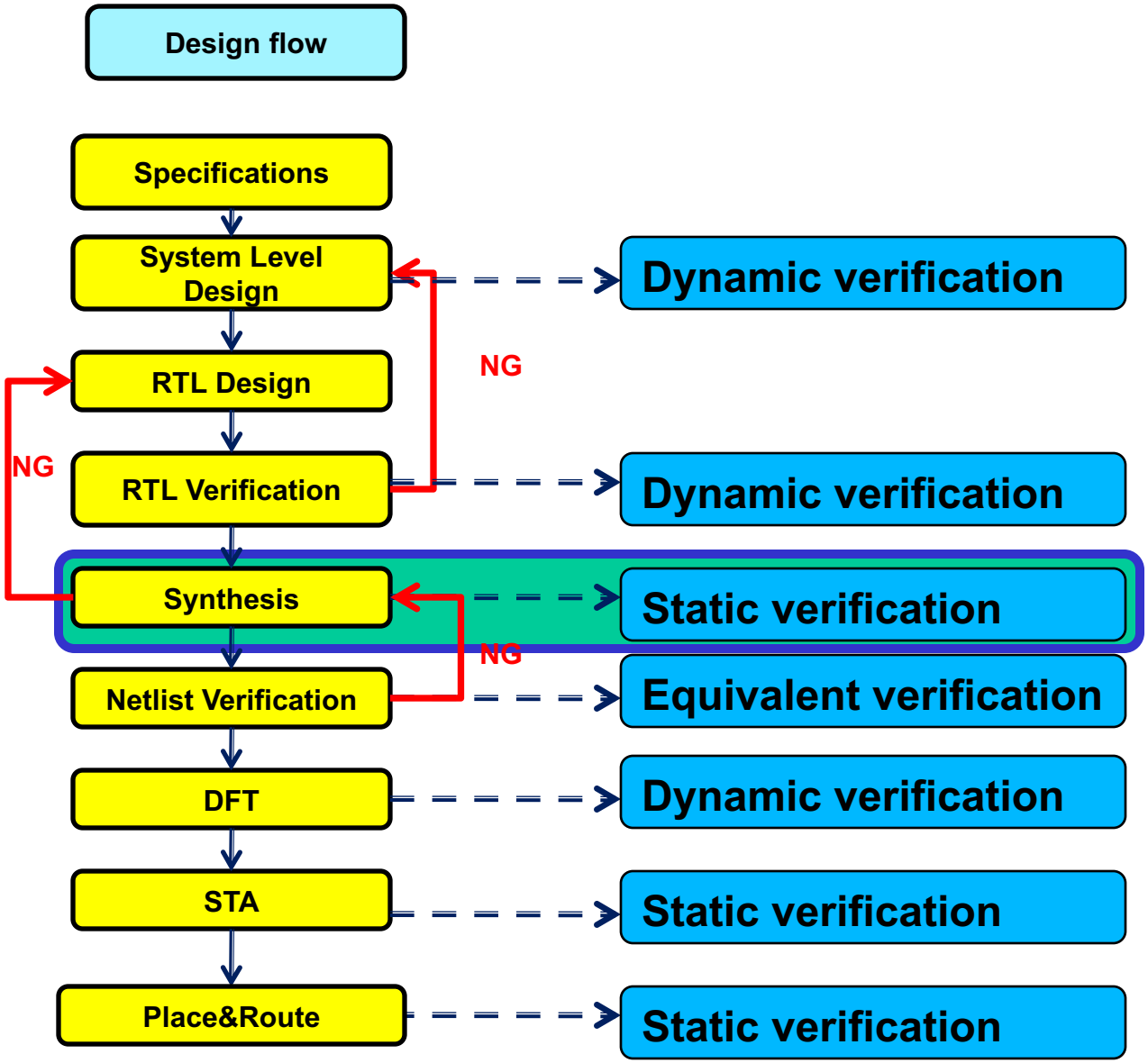
Dynamic vs. Static Timing Analysis



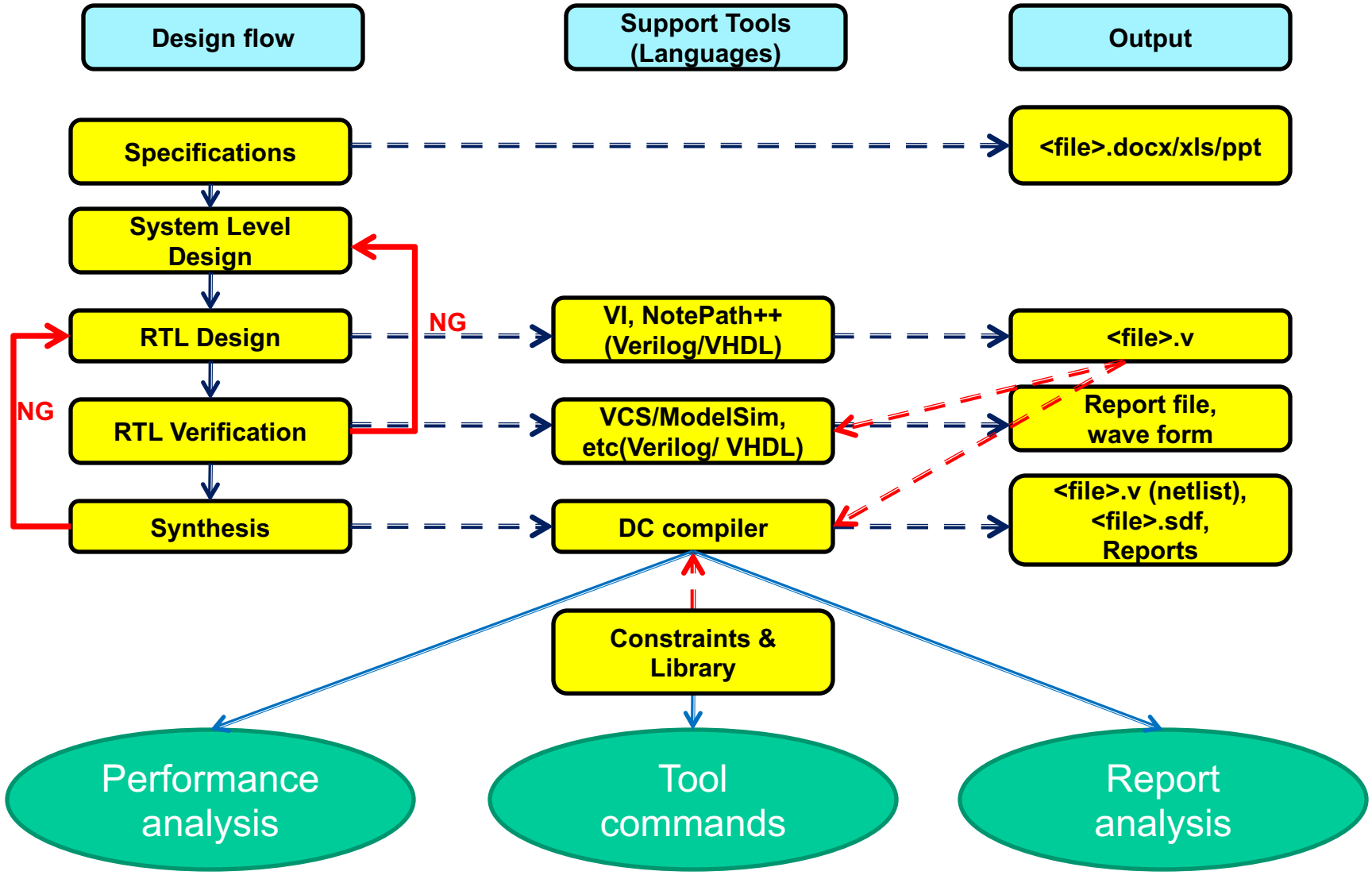
Dynamic vs. Static Timing Analysis



Dynamic vs. Static Timing Analysis



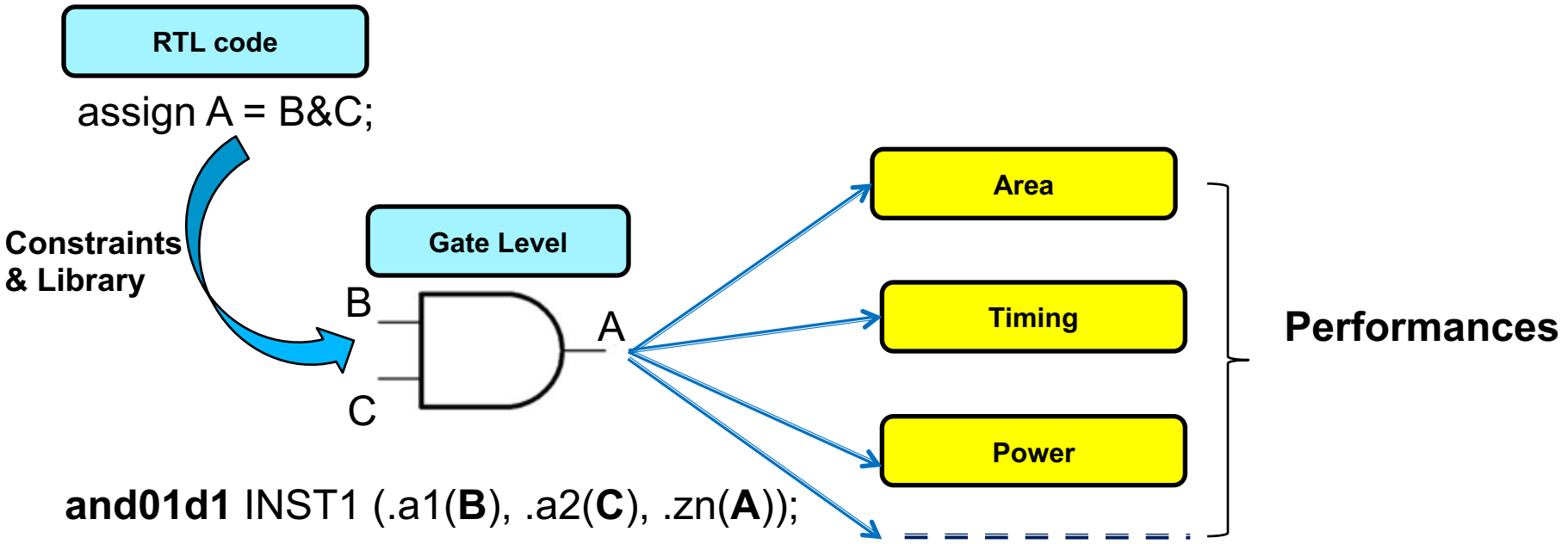
Dynamic vs. Static Timing Analysis



Static Timing Analysis

- Dynamic vs. Static Timing Analysis
- **Performance of Design**
- Synthesis step

Performance of Design

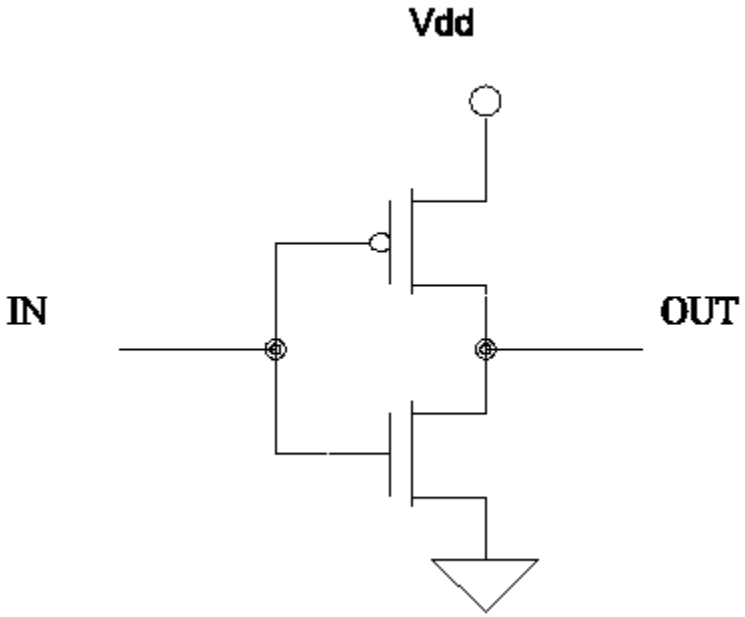


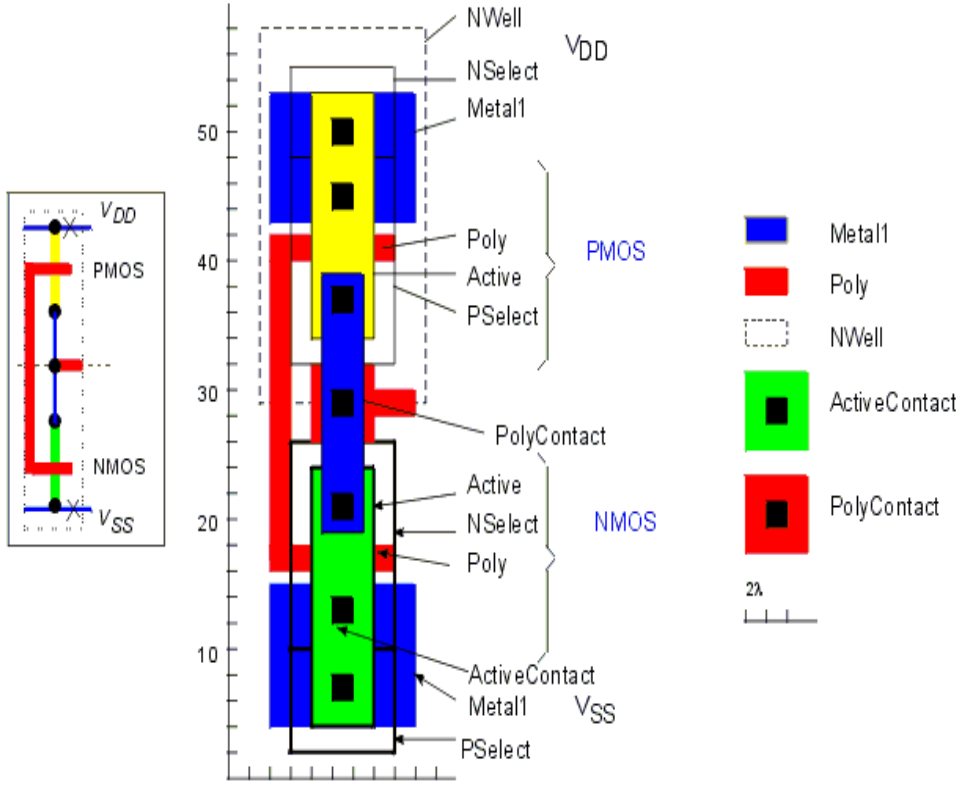
Q1. Why the gates have different performances?

Q2. How to get the best performance ?

Performance of Design

Q1. Why same gates have different performances?

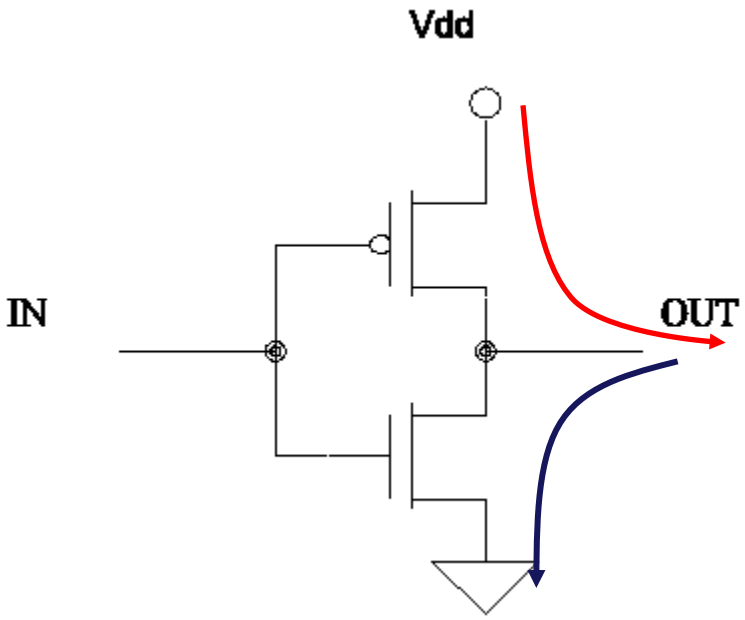


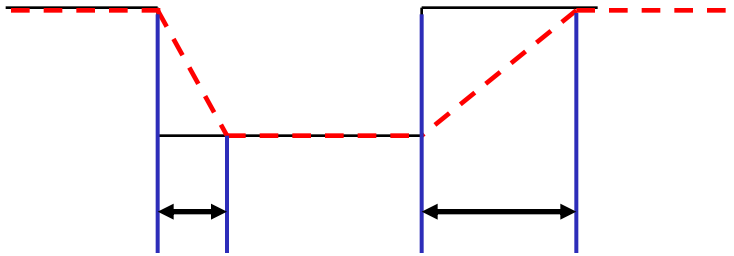


→ The different layouts make the different performances

Performance of Design

Q1. Why the gates have different performances?

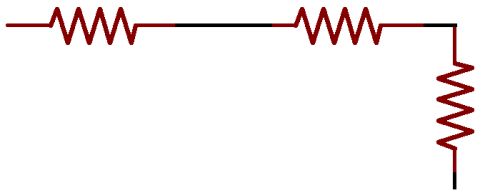




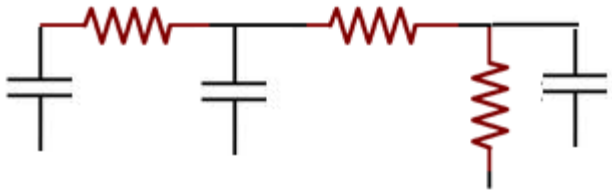
→ The different layouts make the different performances

Dynamic vs. Static Timing Analysis

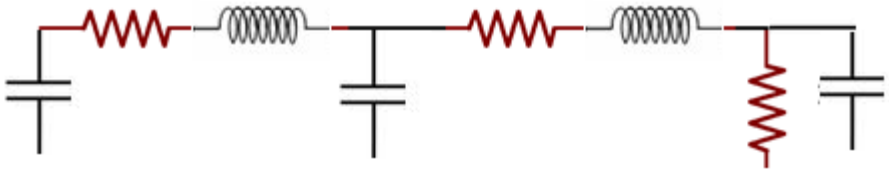
Q1. Why the gates have different performances?



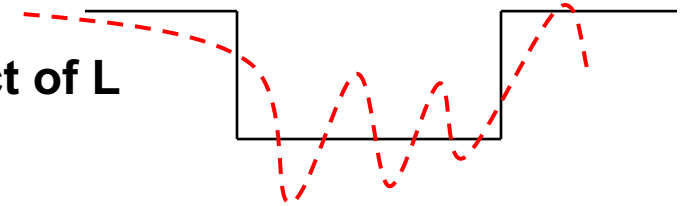
The effect of R



The effect of C



The effect of L

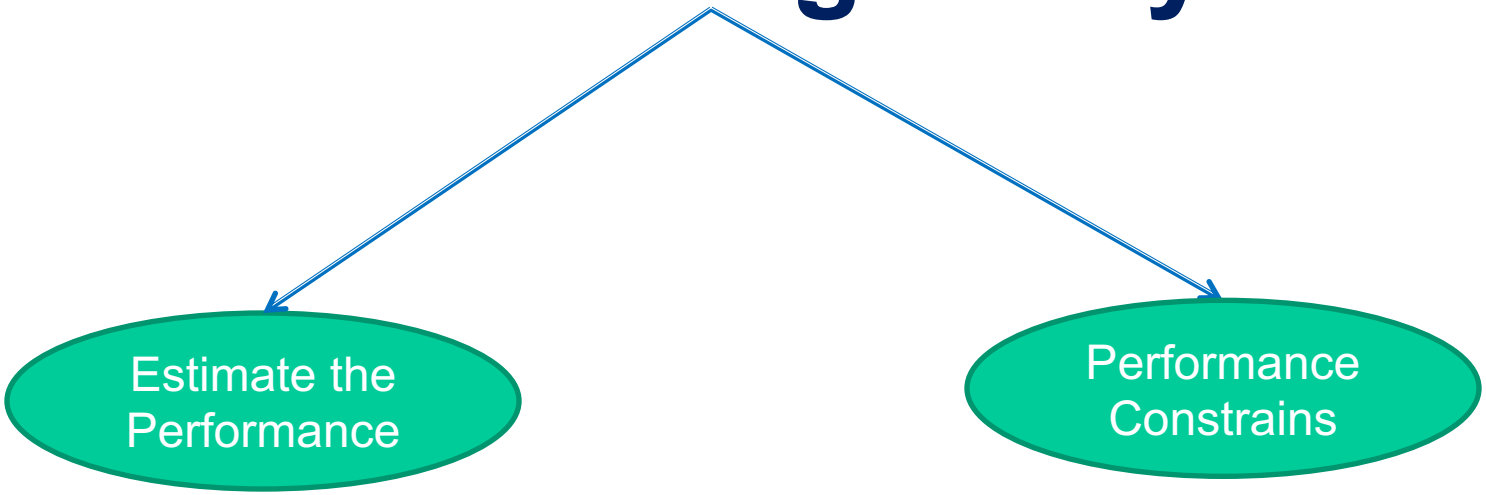


→ The different parasitic C, L, R

Performance of Design

Q2. How to get the best performance ?

Static Timing Analysis



Area, Fanout, Trainsition, Path, Constrain, Clock skew, Setup Time …

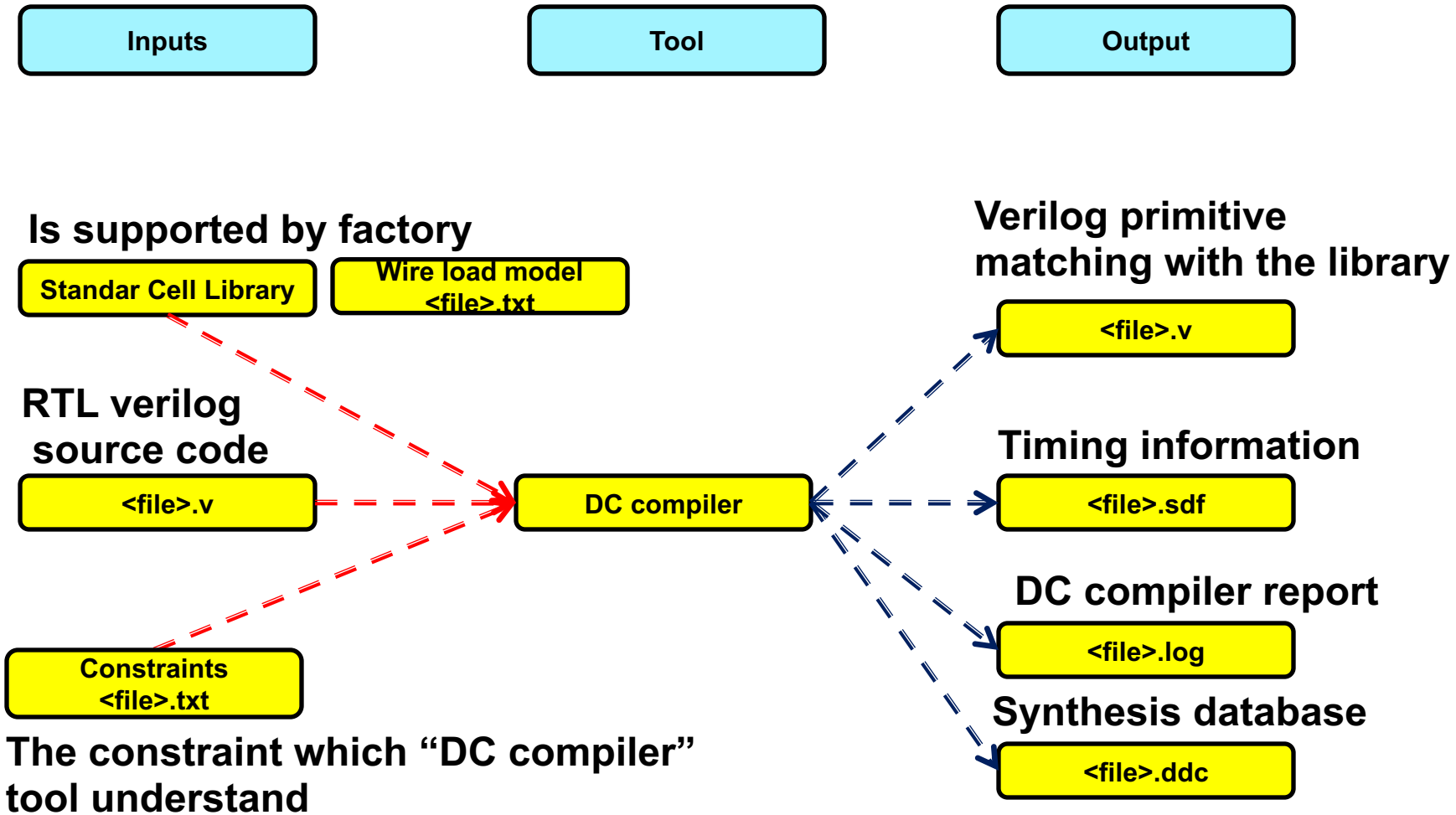
Static Timing Analysis

- Dynamic vs. Static Timing Analysis
- Performance of Design
- **Synthesis step**

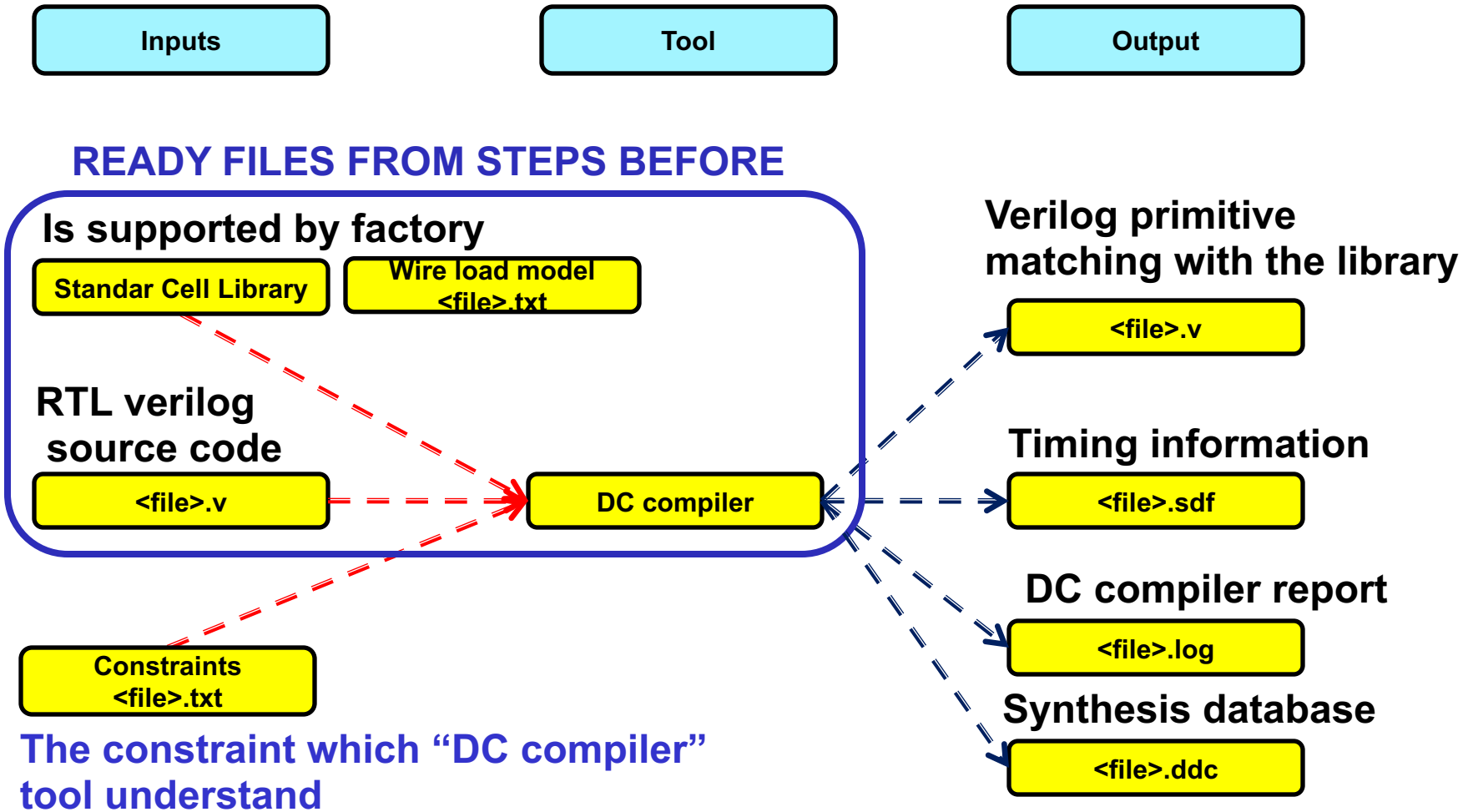
Static Timing Analysis

- Dynamic vs. Static Timing Analysis
- **Synthesis Step**
  - Synthesize RTL to gate level netlist
  - Estimate performance of design approximately
- Analysis
- Constraint
- Violation
- Using DC Tool in Command/GUI mode

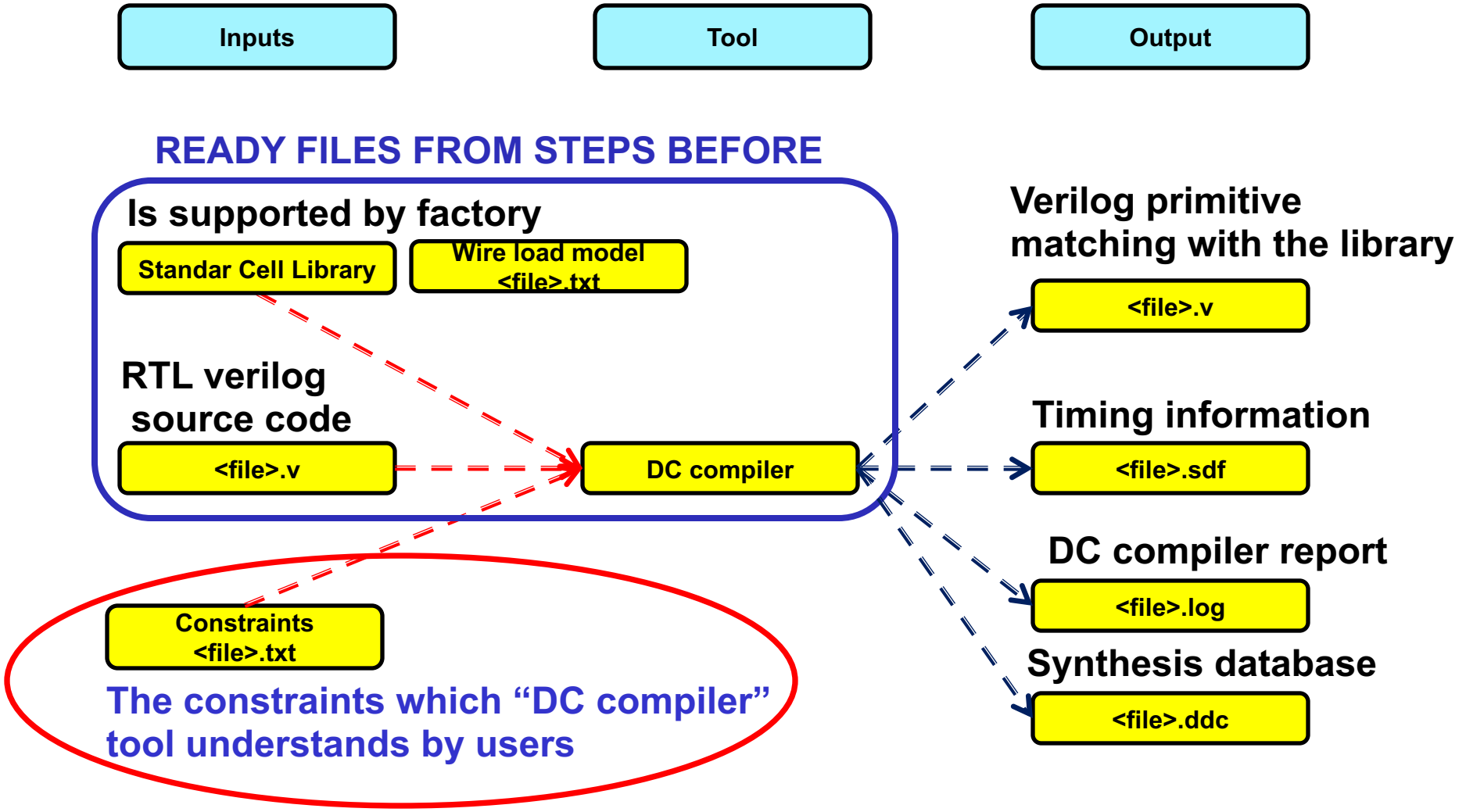
Synthesis step



Synthesis step



Synthesis step



Q1. WHICH FEATURES ARE CONSTRAINED IN CIRCUIT ?
Q2. HOW TO COMPOSE THE CONSTRAINS ?

Q & A