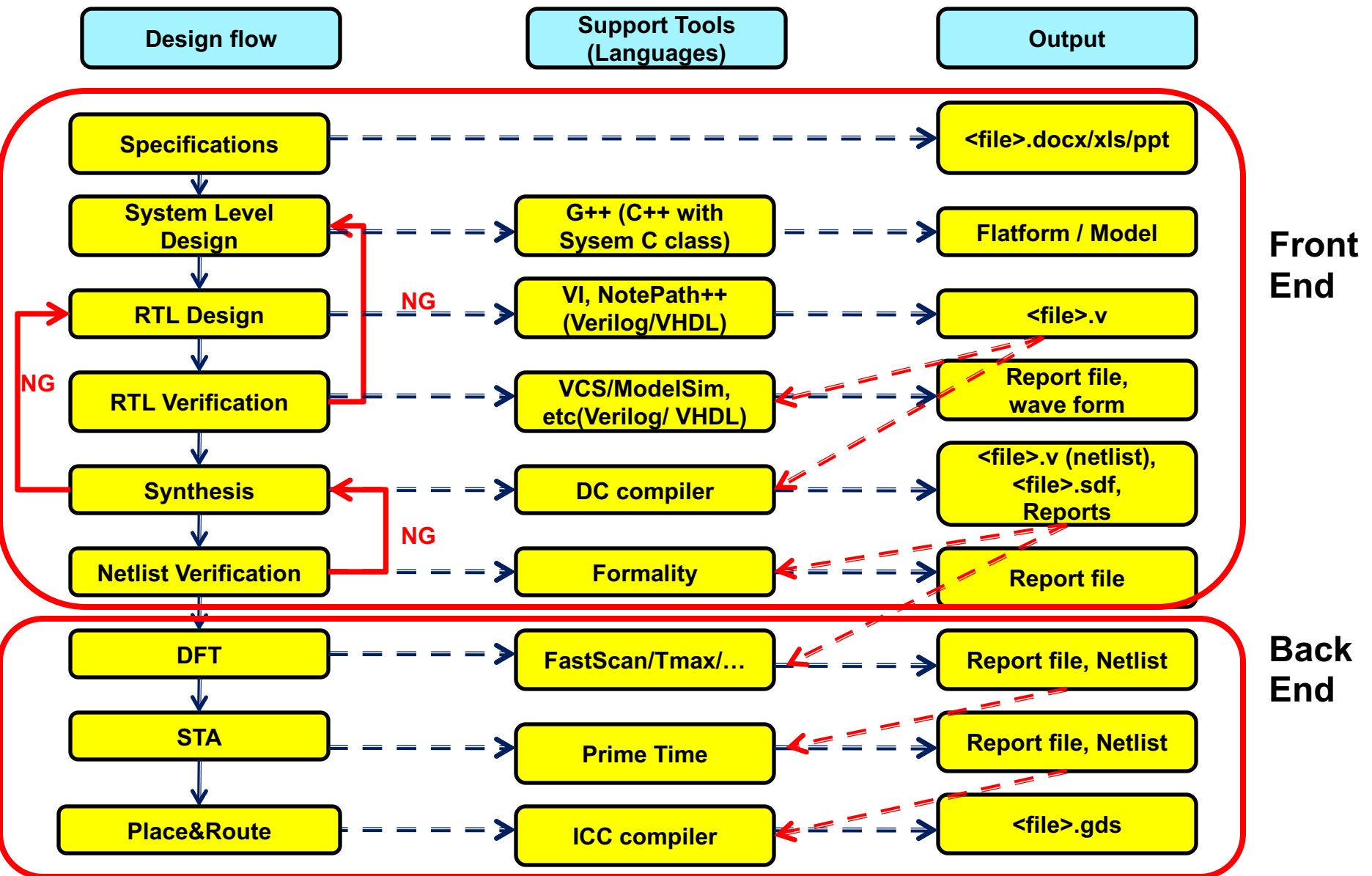


System Level Design in Cell Based Design Flow

Cell Based Design Flow



Cell Based Design Flow

Design flow

Support Tools
(Languages)

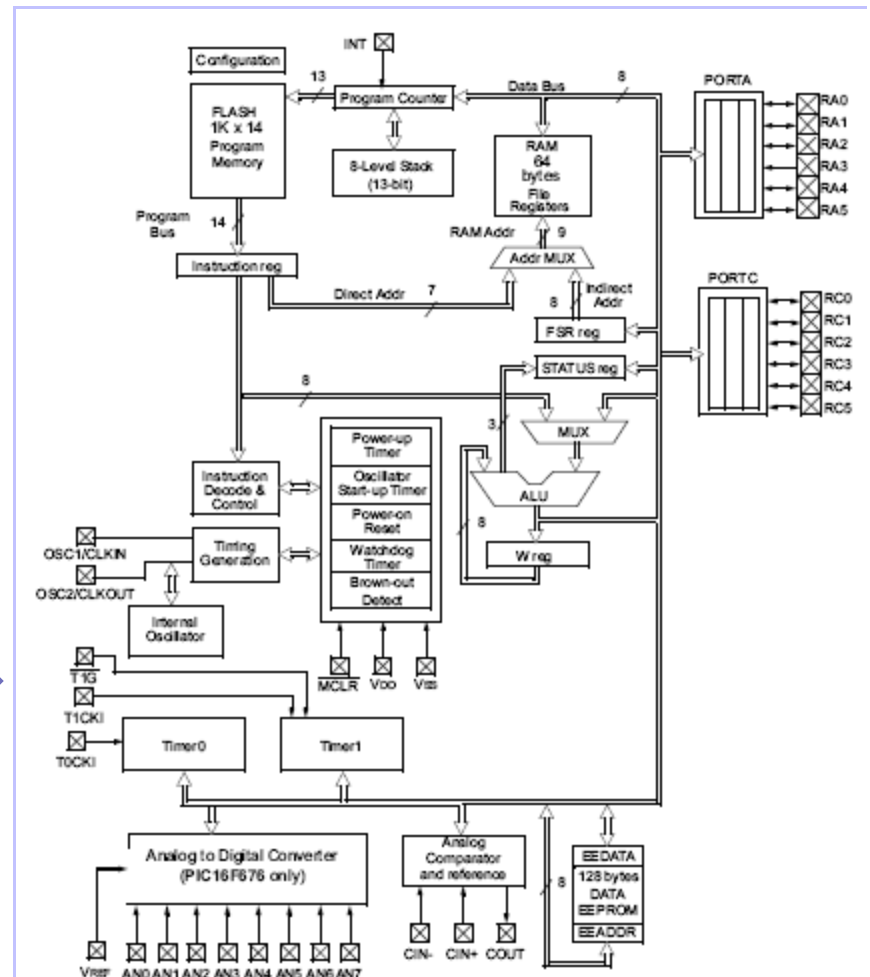
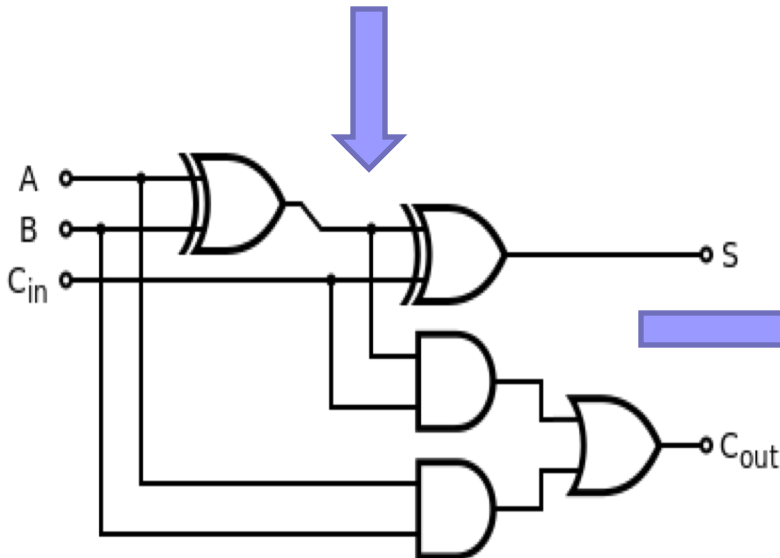
Output

Specifications

<file>.docx/xls/ppt

Design the one bit adder:

- + Three inputs (A, B, Cin)
- + Two output (S, Cout)



Cell Based Design Flow

Design flow

Support Tools
(Languages)

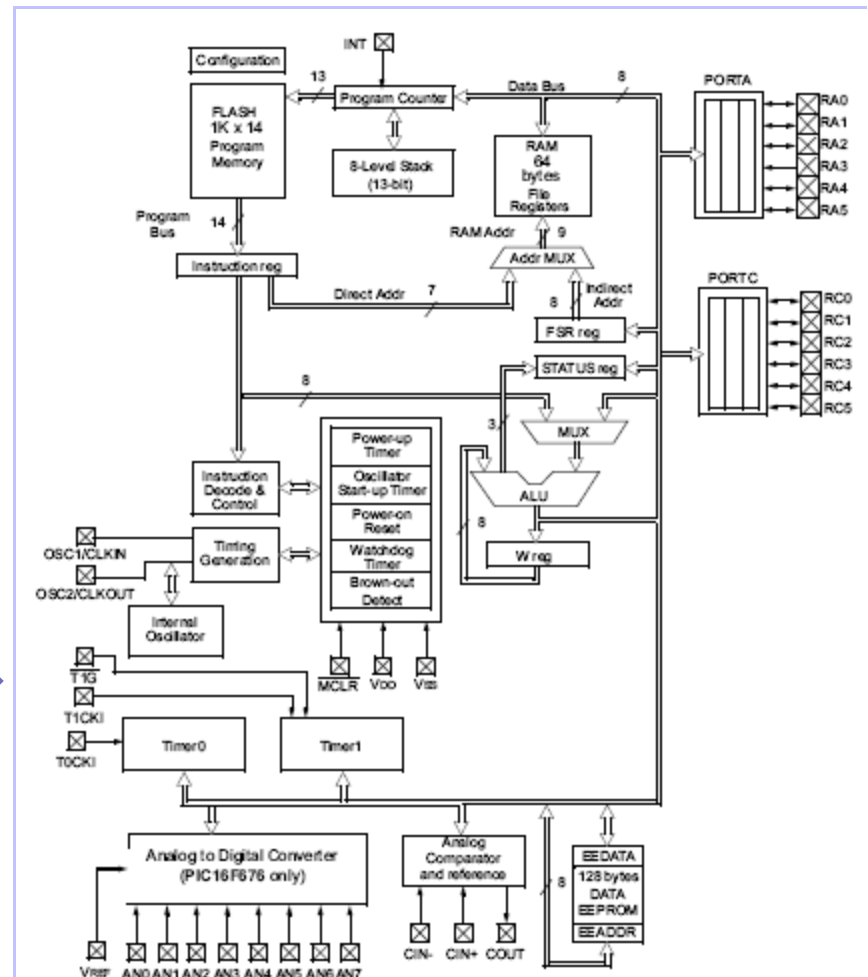
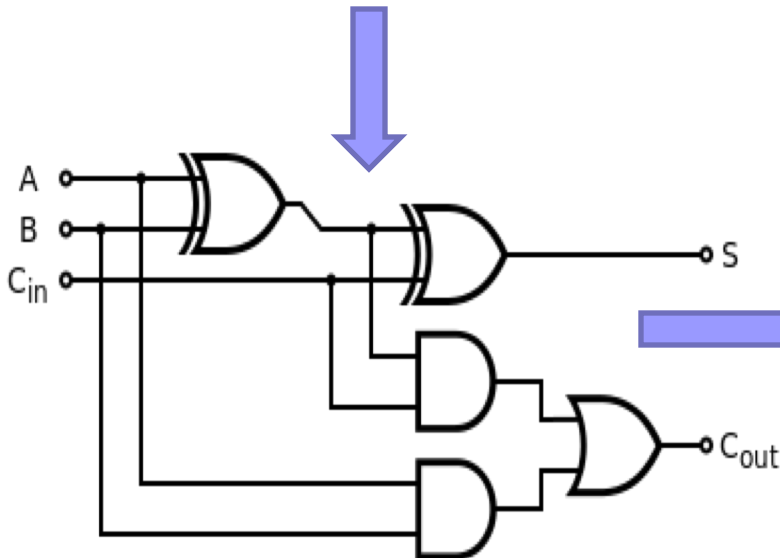
Output

Specifications

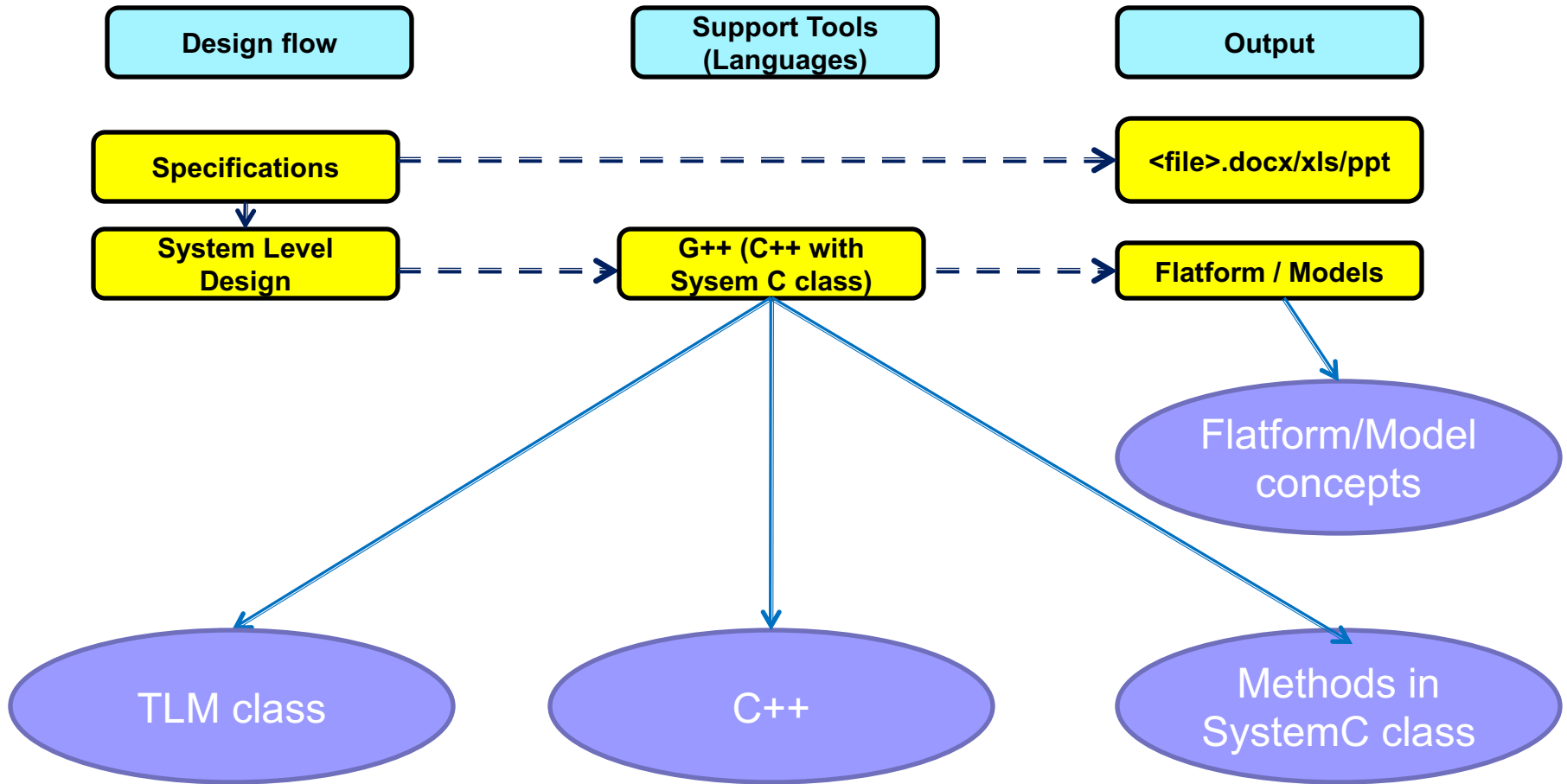
<file>.docx/xls/ppt

Design the one bit adder:

- + Three inputs (A, B, Cin)
- + Two output (S, Cout)



System Level Design Step





System Level Design Step

Design flow

Support Tools
(Languages)

Output

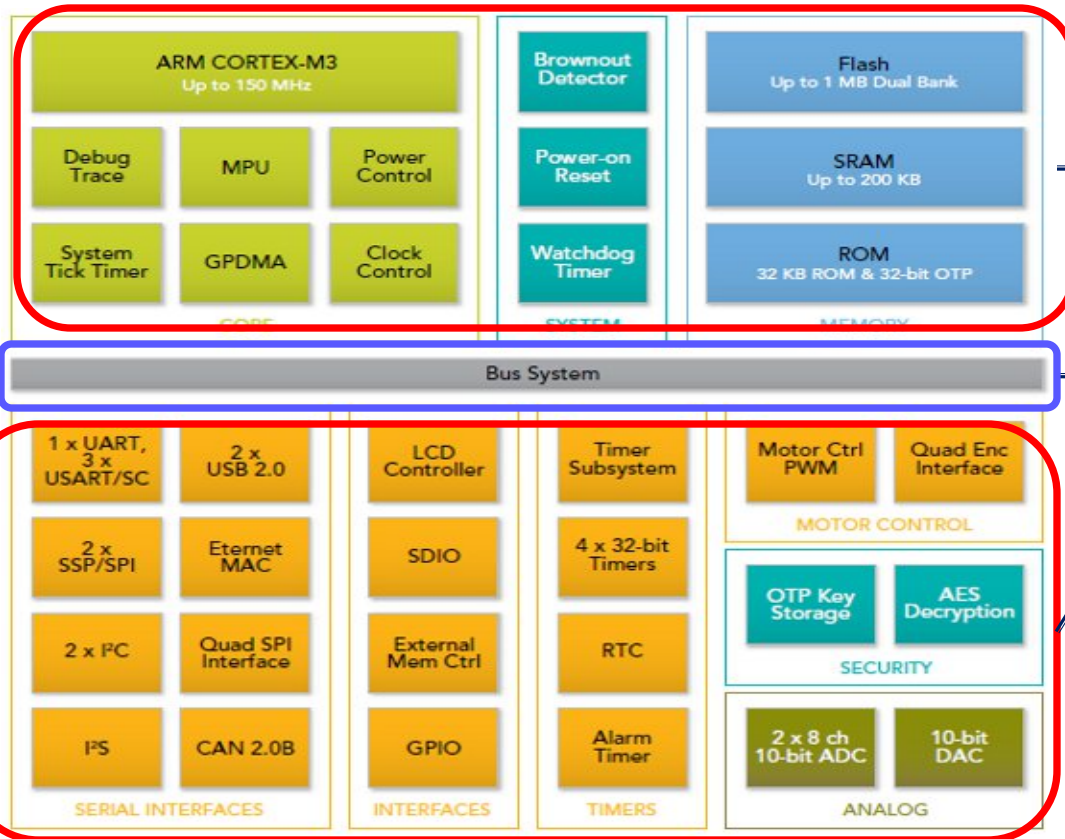
Specifications

<file>.docx/xls/ppt

System Level
Design

G++ (C++ with
Sysmem C class)

Platform / Models

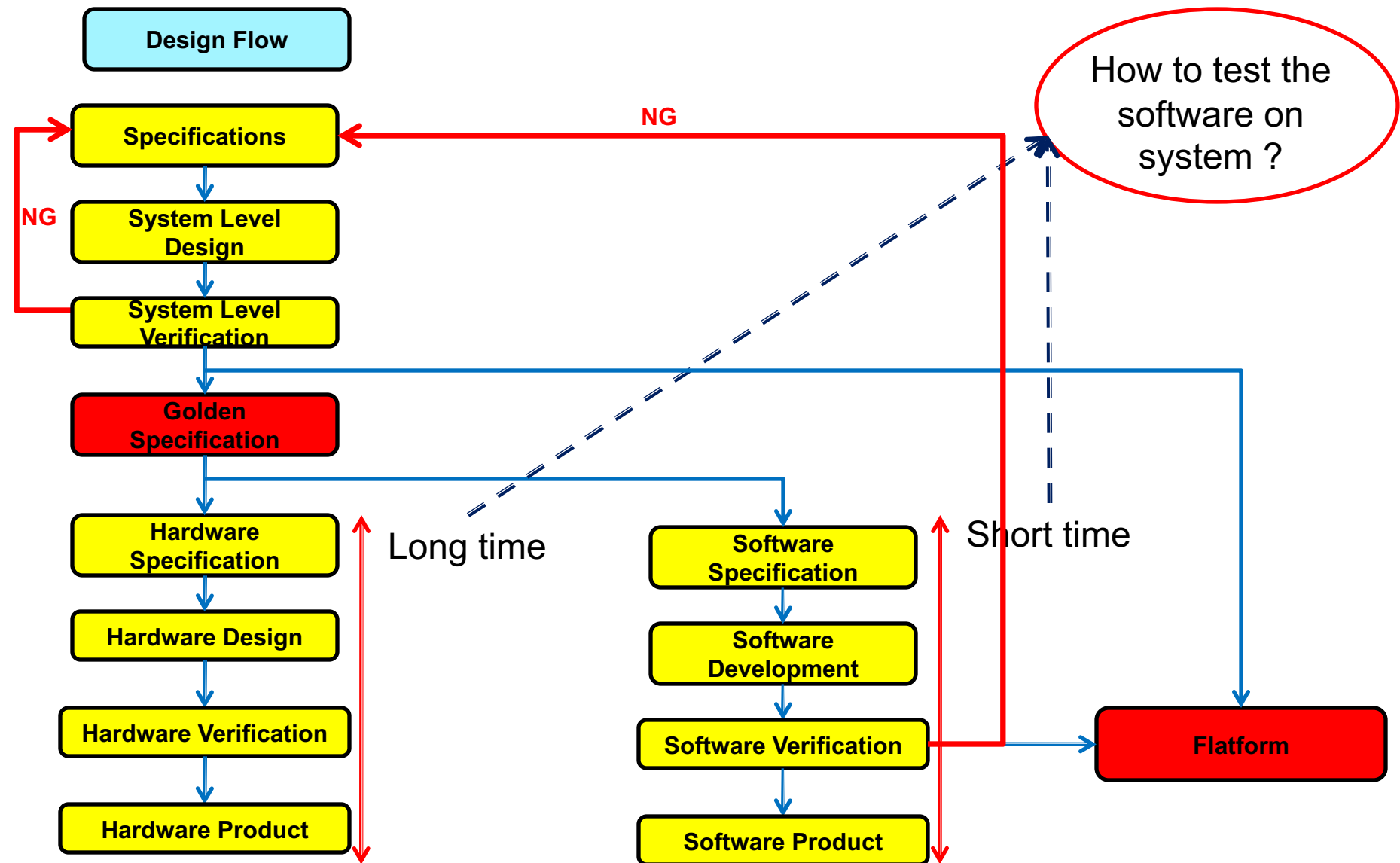


Platform

IP models

TLM model

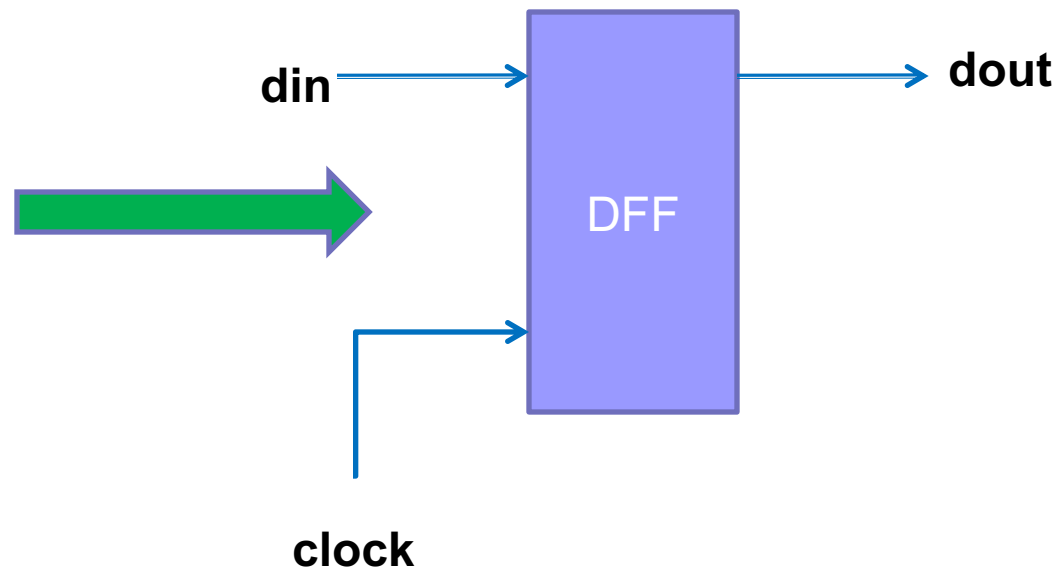
System Level Design Step



System Level Design Step

```
#include "systemc.h"

SC_MODULE(d_ff) {
    sc_in<bool> din;
    sc_in<bool> clock
    sc_out<bool> dout;
    void doit() {
        dout = din;
        cout << dout;
    };
    SC_CTOR(d_ff) {
        SC_METHOD(doit);
        sensitive_pos << clock;
    }
}
```



Q & A