15:13	12:11	10:8	7:5	4:2	1:0	Mnemonic	Functional description	Assembly Code
000	00	rd	r0	r1	00	ADD	rd= r0 + r1	add, rd, r0, r1
					01	SUB	rd = r0 - r1	sub, rd, r0, r1
					10	MUL	rd = r0 * r1	mul, rd, r0, r1
	01				00	AND	rd = rd & r1	and, rd, r0, r1
					01	OR	rd = r0 | r1	or, rd, r0, r1
					10	XOR	rd = r0 ^ r1	xor, rd, r0, r1
	10				00	SLL	rd = r0 << r1	sll, rd, r0, r1
					01	SRL	rd = r0 >> r1	srl, rd, r0, r1
	11			imm	00	SLLI	rd = r0 << imm	slli, rd, r0, imm
					01	SRLI	rd = r0 >> imm	srli, rd, r0, imm
001	00			imm		ANDI	rd = r0 & imm	andi, rd, r0, imm
	01					ORI	rd = r0 | imm	ori, rd, r0, imm
	10					XORI	rd = r0 ^ imm	xori, rd, r0, imm
	11					ADDI	rd = r0 + imm	addi, rd, r0, imm
010	00	imm[4:2]		r1	imm[1:0]	BEQ	if (r0 == r1) PC = PC + imm	beq, r0, r1, imm
	01					BLT	if (r0 < r1) PC = PC + imm	blt, r0, r1, imm
	10					BNE	if (r0 != r1) PC = PC + imm	bne, r0, r1, imm
011	00	rd	imm			JAL	rd = PC + 4, PC = PC + imm	jal, rd, imm
100	00					LD	rd = MEM[imm]	ld, rd, imm
	01	imm[7:2]		r1	imm[1:0]	SD	MEM[imm] = r1	sd, rd, imm