Fall
2014

# INVERTER Design

PROJECT 3 CE6325 VLSI DESIGN: INVERTER DESIGN

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## Project Description:

In this project an Inverter is designed using Cadence Virtuoso. The inverter has two transistors, NMOS and PMOS. The inverter layout and the schematic were designed using the given specification and source files. The width of the transistor is 1.8um and 1.7um for the PMOS and NMOS respectively. After the design layout and schematic several Rules were used to evaluate the design, and the netlist was exported to be used with HSPICE.

## Design tools used:

- Cadence Virtuoso: to perform layout and schematic drawing
- HSPICE: to simulate the circuit or design and validate the design performance

## Design Specification:

- Slew rate = 30ps
- Width of PMOS (Wp) = 1.8µm
- Width of NMOS (Wn) = 1.7µm
- Length of (L) = 65nm
- Load Capacitance (C_load) = 27fF

**Design Layout**

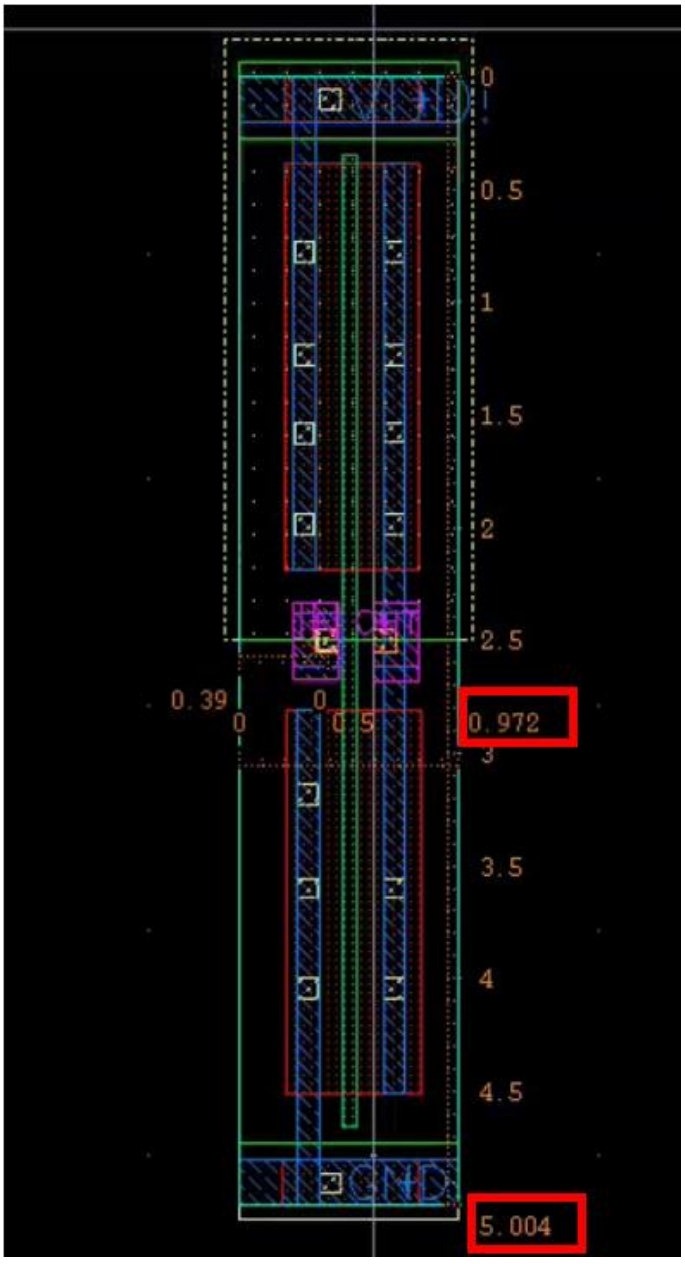


Figure2: INV layout showing H x W as 0.972µm and 5.004µm

Design Pitch and offset: the Project requires certain pitch and offset

$$pitch = 0.26 * n \qquad where = 1,2,3, \ldots$$

$$offset = 0.13 + pitch \qquad where\ offset = 0.13, 0.39, 0.65, \ldots.$$

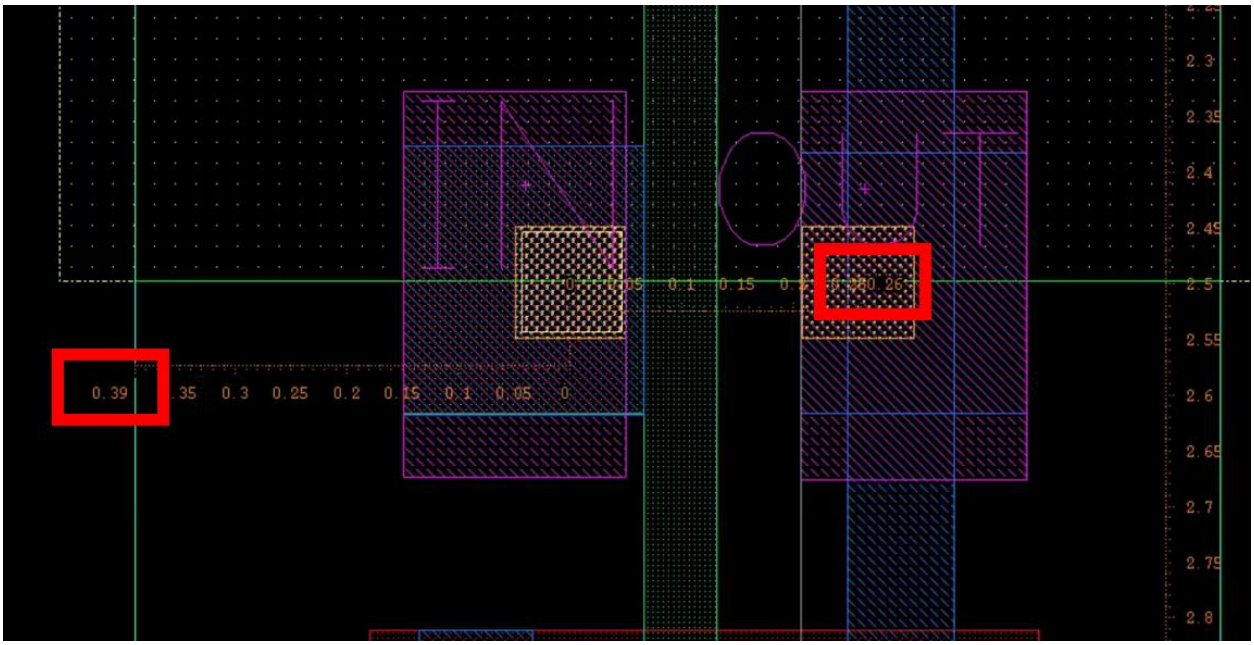


Figure3: INV layout showing pitch and offset as 0.39µm and 0.26µm

**Design schematic**

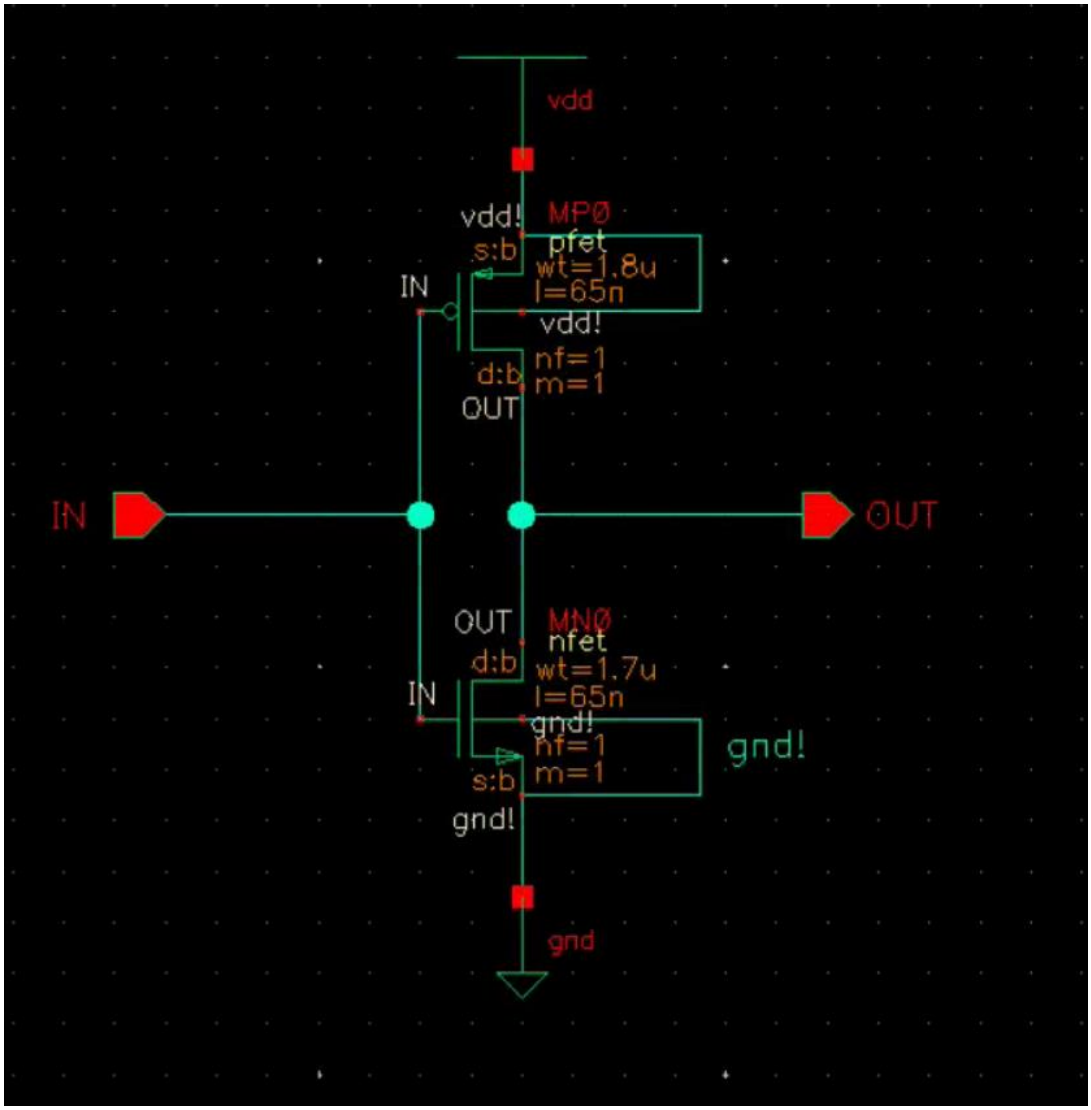


Figure4: INV schematic showing Wp=1.8µm, Wn=1.7µm, and L = 65nm

**Results from Cadence Virtuoso:**

After the Layout and Schematic drawing. The design rule check (DRC) and the layout vs schematic rule (LVS) were ran to make sure the both layout and schematic matched, this ensures the circuit to behave as close to ideal as possible if there are no fabrication issues.

## DRC check Result:


Figure4: DRC results showing 0 errors and file path to DRC rules

## LVS results:


Figure5: LVS results showing 0 errors and Design Specs

**HSPICE Simulation:**

after the layout and schematic rule check a Parasitic extraction (PEX) was performed to extract the netlist file. A Hspice script was written to perform use the extracted netlist for simulation.

**V(in) Results**

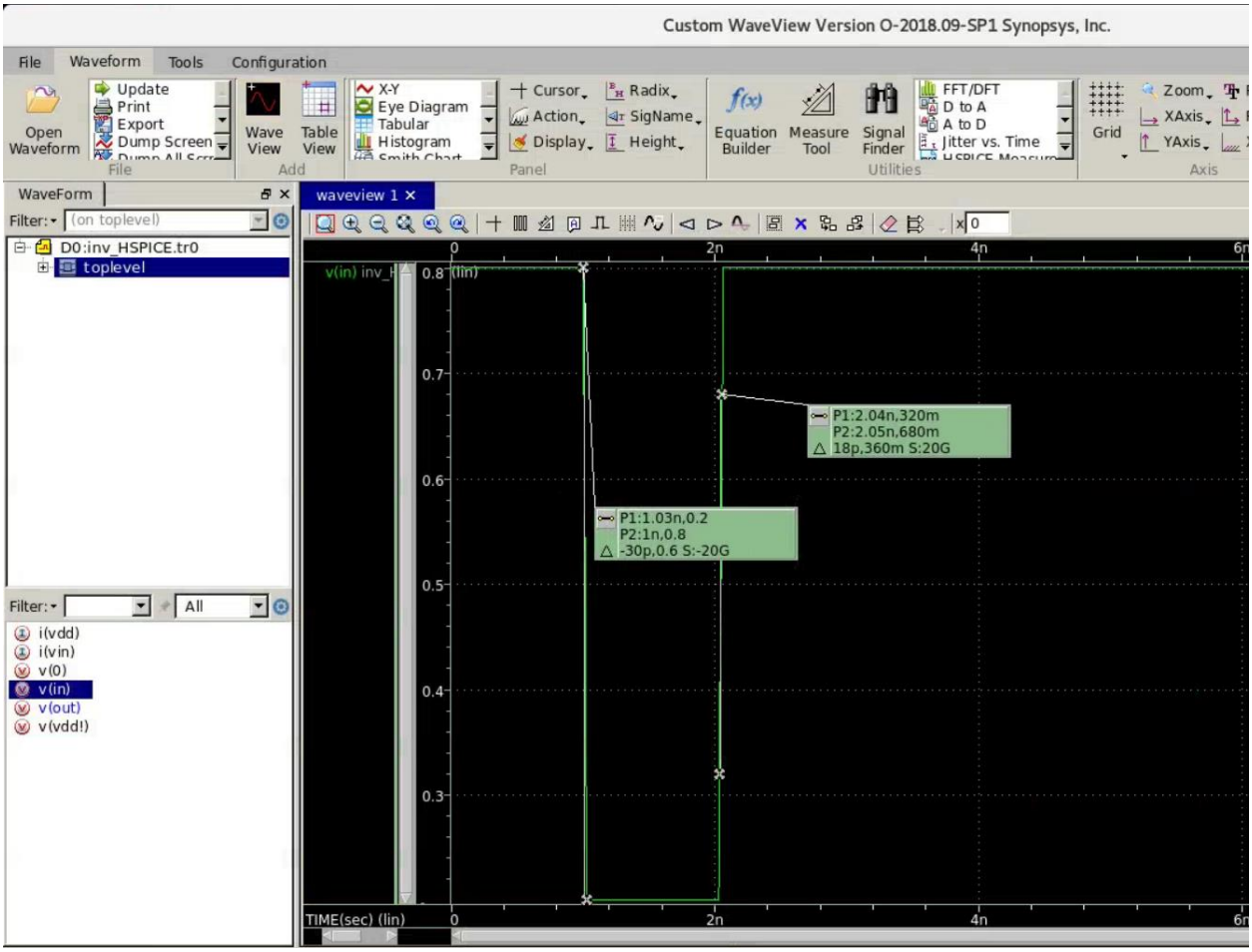


Figure 6: V(in) wave showing 30ps as slew rate for 0.8Vdd to 0.2Vdd and 18ps for 02Vin to 0.8Vin

**V(out) Results:**

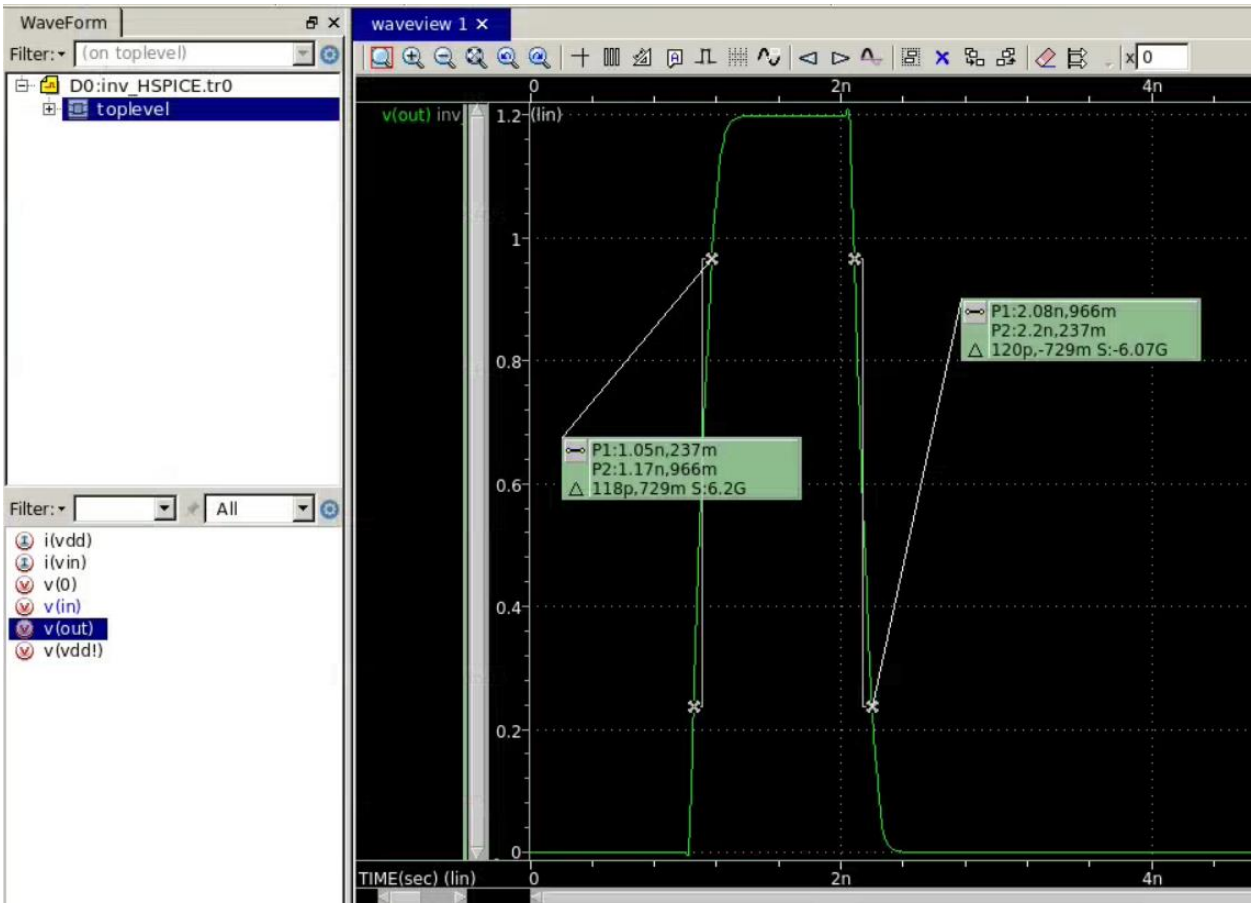


Figure 7: V(out) showing trise and tfall

The result shows that:

- trise for V(out) from 20% to 80% = 118ps
- tfall for V(out) from 80% to 20% = 120ps
- the design requirement for difference between trise and tfall ≤ 5ps
- from above tfall – trise = 2ps

**Delay of the design:**

In this design the delay will be measured using the time difference between 50% of Vin and 50% of V(out). The aim is to make the delay as low as possible.

$$delay = abs((0.5 * Vin_{tHL}) - (0.5 * Vout_{tLH}))$$

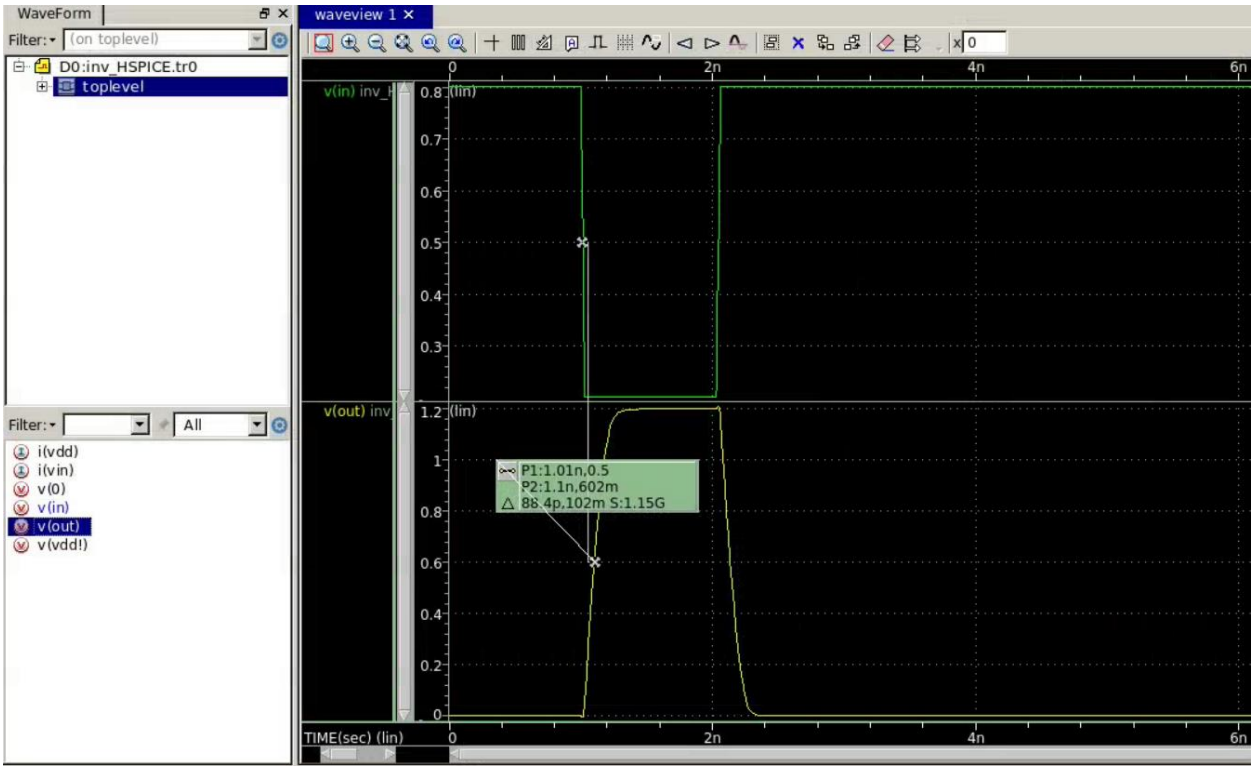


Figure 8: Vin vs Vout showing a delay of 88.4ps

**Energy Dissipation and calculated Delay from HSPICE script:**

$$edp = abs(delay * energy)$$

Edp1 using method 1 of the Hspice script:

```
$DATA1 SOURCE='HSPICE' VERSION='O-2018.09-2 linux64' PARAM_COUNT=1
.TITLE '$ hspice setup file for proj3'
 wp                trise             tfall             tavg
                   tdiff             delay             iavg
                   energy            edp1              temper
                   alter#
  1.000e-07         9.319e-11         8.527e-11         8.923e-11
                    7.913e-12         9.319e-11        -4.257e-06
                   -5.108e-14         4.760e-24          25.0000
                  1
  1.700e-06         9.319e-11         8.527e-11         8.923e-11
                    7.913e-12         9.319e-11        -4.257e-06
                   -5.108e-14         4.760e-24          25.0000
                  1
  1.800e-06         9.319e-11         8.527e-11         8.923e-11
                    7.913e-12         9.319e-11        -4.257e-06
                   -5.108e-14         4.760e-24          25.0000
                  1
```

Figure 9: method 1 results show delay of 93ps and edp1 = $4.7 * 10^{-24}$

**Summary:**

In the design the following were done to minimize Area and energy dissipation

The Diffusion rectangle for the PMOS and NMOS were brought close together while avoiding breaking any Design rule Check. This helps reduce the width of the overall design from Highest point of metal 1 (M1) to lowest point of metal 1 (M1) to 5.004nm.

The length of the design was also reduced while keeping the required pitch and pin offset. These reductions made the overall design Area to be 4.863$\mu m^2$