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1  /*-----------------------------------------------------------------------------------------
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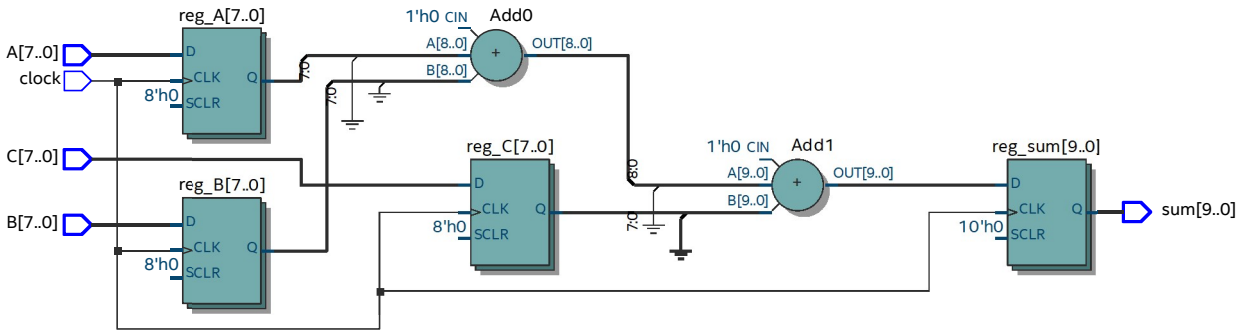
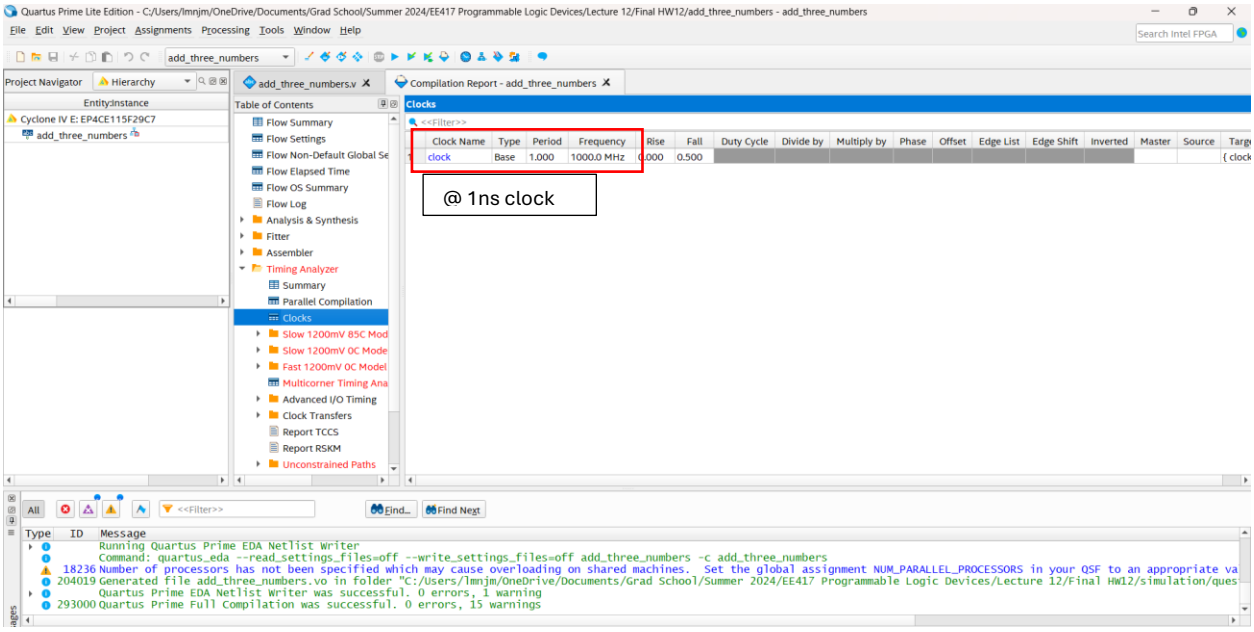
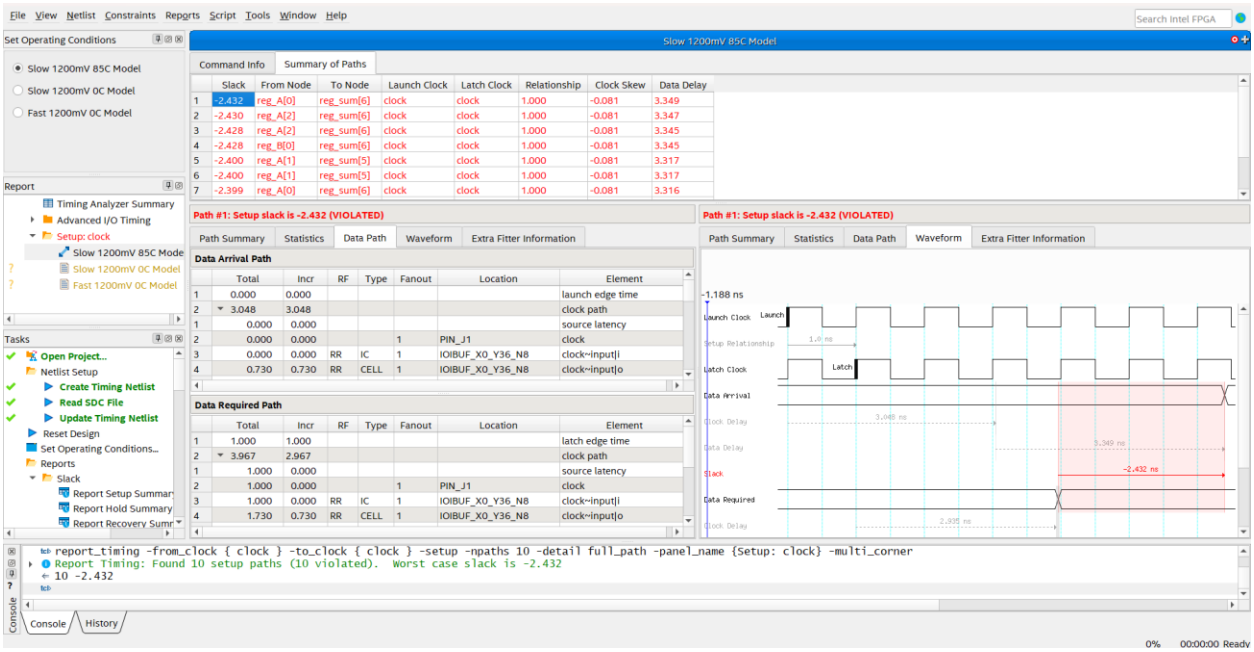
2  Name Lamin Jammeh
3  CLass: EE417 Summer 2024
4  Lesson 12 HW Question 1
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: Simple Timing analysis using an Synopsus Design Constraint ((SDC) file
   in Quartus
7  the circuit is run by a single clock name clock which has timing cntraints change from 1ns
   to 4ns
8  -----------------------------------------------------------------------------------------
   --------*/
9
10 module add_three_numbers (clock, A, B, C, sum);
11
12 //define the inputs and outputs
13 input          clock;
14 input [7:0]    A, B, C;
15 output   [9:0]    sum;
16
17 //define the internal registers
18 reg      [7:0]    reg_A, reg_B, reg_C;    //synthesis keep
19 reg      [9:0]    reg_sum;             //synthesis keep
20
21 //combination logics
22 always @(posedge clock)
23    begin
24       reg_A <= A;
25       reg_B <= B;
26       reg_C <= C;
27       reg_sum  <= reg_A + reg_B + reg_C;
28    end
29
30 //assign the reg_sum to the output
31 assign      sum = reg_sum;
32 endmodule
```


reg_A[7..0]
A[7..0]
clock
D
CLK
Q
8'h0
SCLR
7:0
1'h0 CIN
Add0
A[8..0]
B[8..0]
OUT[8..0]
C[7..0]
reg_C[7..0]
8'h0
reg_B[7..0]
B[7..0]
8:0
1'h0 CIN
Add1
A[9..0]
B[9..0]
OUT[9..0]
reg_sum[9..0]
10'h0
sum[9..0]

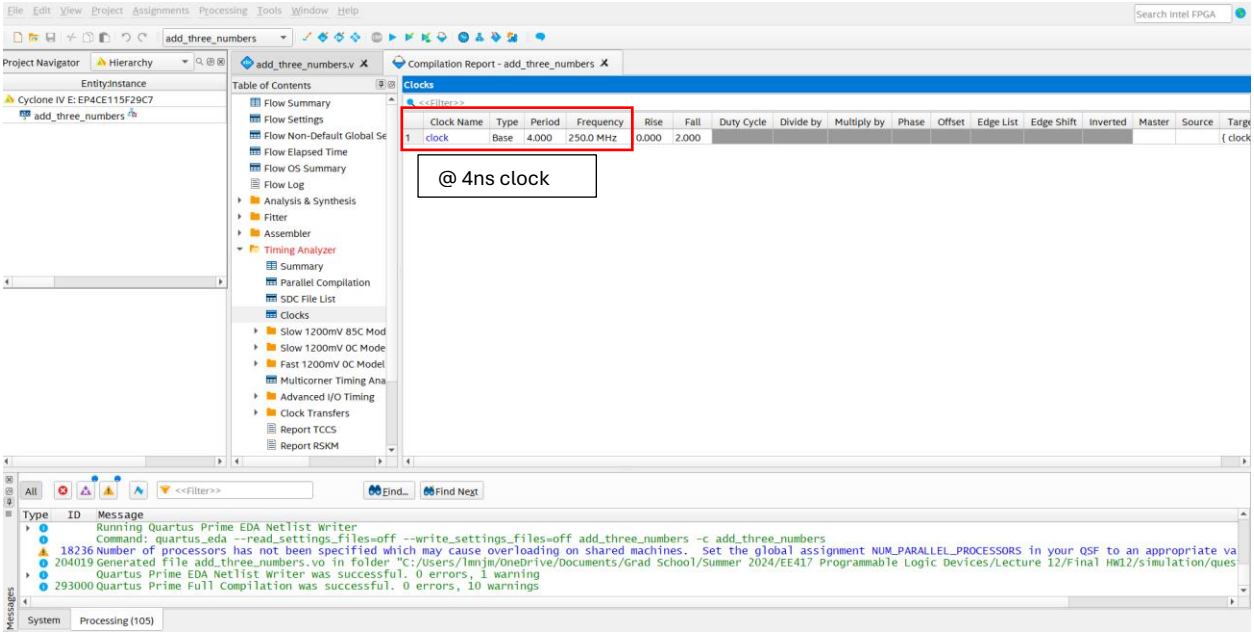
Timing Analysis at 1ns clock period



Summary of Paths and Waveform @clock period of 1ns



Timing Analysis at 4.00ns clock period



Summary of Paths and Waveform @clock period of 4.000ns