**EECT/CE 6325 VLSI Design**
Fall 2024

# PROJECT #4: Cell Library
**Due: Friday Nov. 1 at 5pm**

**Project Introduction**

For this project you will be creating your standard library of cells (without D-Flip Flop), which will be used for your final project. **NOTE: The poly width (length of the channel) must be 62nm for this project. No points for other sizes.**

**Project Goals**

1) You must design, layout and verify at least 8 different combinational standard cells. Note that the following are required by Synopsys.
   - INV
   - NAND2
   - NOR2
2) It will be graded competitively, so the more cells you have and the more complex they are, the more points. However, be realistic with the time you have available!
3) Try not to have the same cells as another group; if you do, TAs will check more closely for copying.
4) All your cells should be placed side by side, next to each other, and have no DRC errors. All pins must be aligned horizontally with uniform spacing.
5) Do not use the library.lib provided for Project 2, instead generate a .lib file for the given set of cells using *PrimeLib*. For generating a library follow the instructions given in *PrimeLib by Synopsys* document uploaded on eLearning in Project 4 folder.
6) The height of the pMOS diffusion (RX drw layer) must accommodate 4 contacts and the height of the nMOS diffusion (RX drw layer) must accommodate 3 contacts.
7) Generate abstract views of your cells, use instructions given in *Abstract View Generation* document uploaded on eLearning in Project 4 folder)

**Project Rules & Requirements**

1) All the cells should have the same height with VDD & GND rails aligned horizontally.
2) **NOTE: The poly width (length of the channel) must be 62nm for this project. No points for other sizes.**
3) The input slew rate is 30 ps (0.2*Vdd to 0.8*Vdd and vice versa)
4) Assume a 55 fF load capacitance when simulating.

**What to Turn In** (points are deducted for anything missing)

1) A cover page containing all the following information.
   - Name, NetID and project title
2) Each cell layout with **rulers** showing the dimensions of the cell. Part of grade depends on the clarity of your ***report***.
   - Show the distance between your pins
   - Show the length of the channel
   - Show the height & width of entire cell.
3) Also turn in the following for each cell in your library:
   - Simulation data that shows each transistor works in each cell
4) Please also hand in a layout showing all your cells lined up in a row with the boundary layers touching to demonstrate that they can be placed next to each other with no problems (yes, that means run DRC).
   - Show distance between pins to verify that they have a uniform pitch.
5) Upload the project report on eLearning.
6) Upload the zipped folder containing all layouts and schematics on eLearning

**Grading Breakdown**

| | |
|---|---|
| Correct functionality of all cells | 40% |
| Number and complexity of cells | 20% |
| Correct pin spacing and sizing | 20% |
| Report | 20% |