PennState

Logic Design using FPGAs

Assignment – lesson 2
Structural Design

Objective:

- Designing Verilog modules using the instantiation of primitive modules and using structural design to build larger modules with more inputs and outputs.

- Creating testbenches that verify the functionality of the modules designed

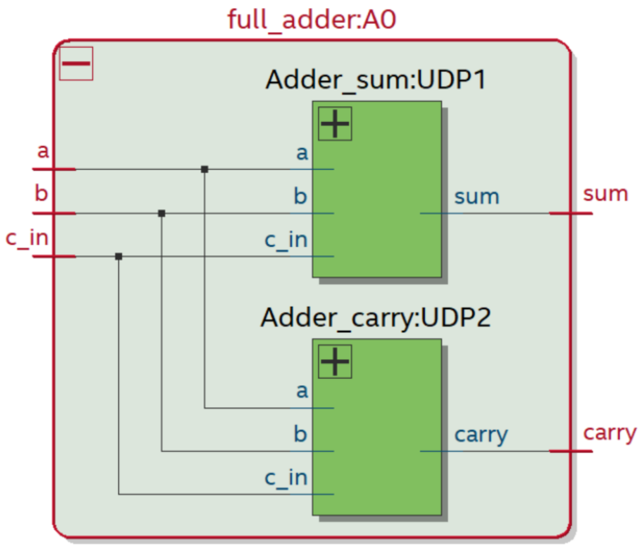
Assignment I:

Design a T**wo-8bit-input** adder using primitive full adders and structural hierarchical design.

(a) Design a primitive **Adder_sum** with 3 inputs for a, b, and c_in that finds the LSB of the sum of the three inputs.

(b) Design a primitive **Adder_carry** with 3 inputs for a, b, and c_in that finds the MSB or carry_out of the sum of the three inputs.

(c) Design a **full_adder** top module that instantiates the two primitives created in parts (a) and (b) as shown in the given netlist viewer.



(d) Create a higher level two-4bit_input adder by instantiating the single-bit full adder 4 times as follows as indicated in the book and the PowerPoint document.

(e) Design you top module **Two-8bit-input (sum_out, a_in, b_in)** that add two 8-bit inputs. Make sure that the size of the output sum can accomodate the maximum numbers that can be reached by the inputs a_in and b_in without any overflow.

(f) Create a testbench that tests the functionality of the single building blocks of the design as well as the interconnections.

Assignment II:

Design a module using the structural design of simple logic gates that takes as an input a 4bit word and has two single-bit outputs divBy3 and divBy5:
divBy3 is raised to a logic high if the 4-bit input is divisible by 3 including 0.
divBy5 is raised to a logic high if the 4-bit input is divisible by 5 including 0.

- Use Karnaugh map to derive the switching function for the two output bits.
- Use simple logic gates and internal wires to build the structural design for the module.
- Create a testbench to verify the functionality of your design.