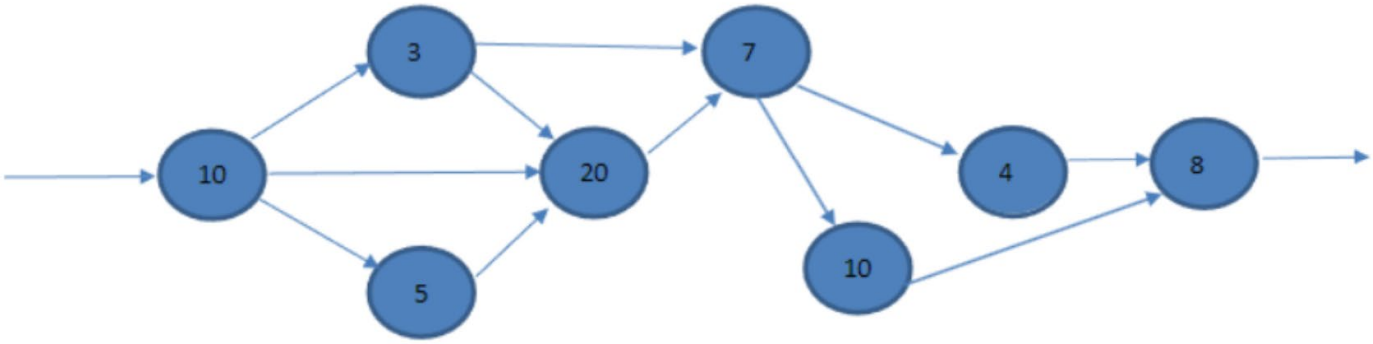
Assignment 10: Pipelining

Question 1: (20 points)

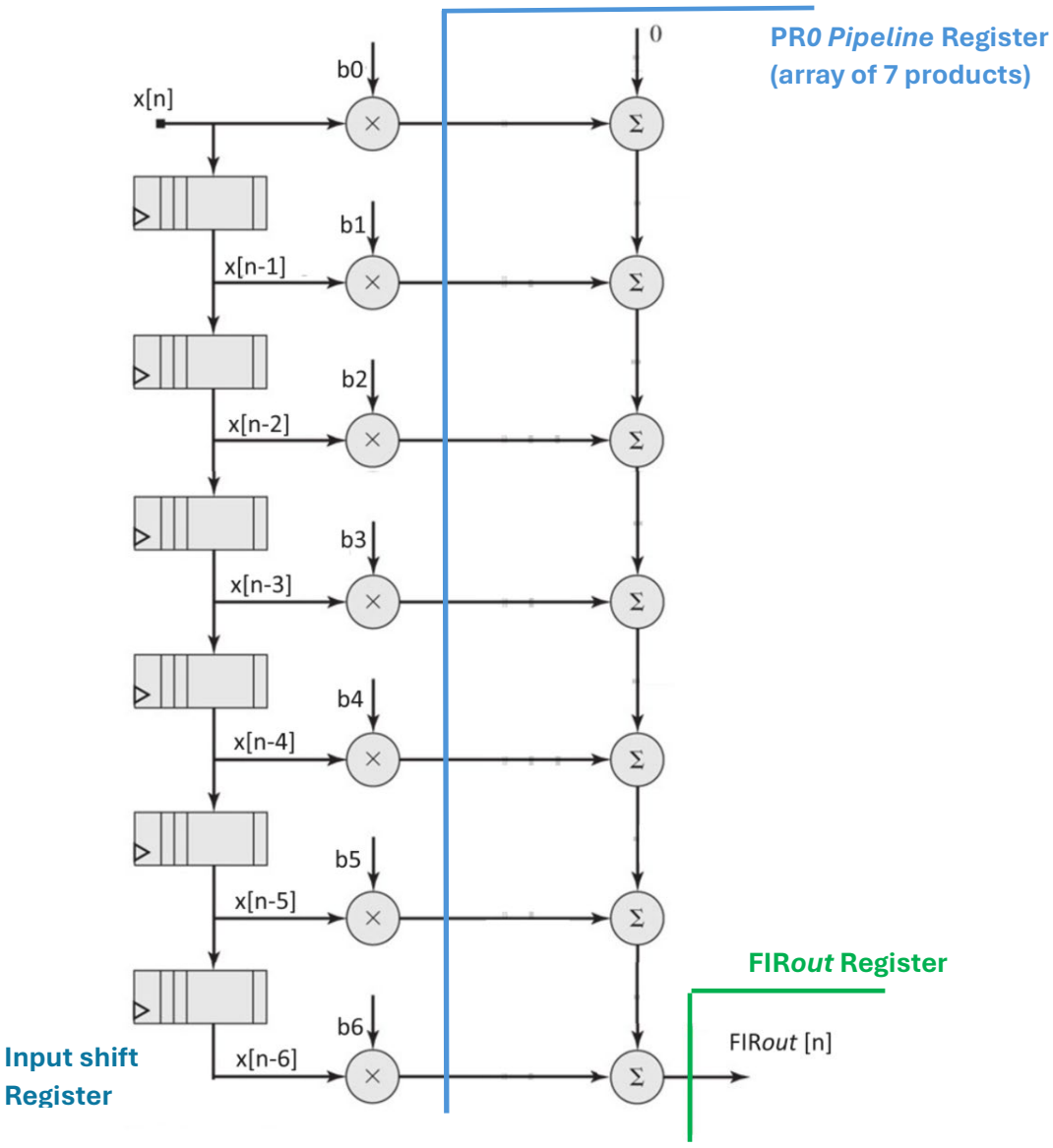
The nodes of the DFG (Data Flow Graph) shown in figure has been annotated with propagation delays. Find the optimal placement of pipeline registers in the circuit. Make a list with the number of cut-sets and their locations and the corresponding latencies and throughput. What is the maximum clock frequency that can be used?



Assignment Question 2: (40 points)

Consider the following 6th order FIR filter. The filter coefficients are given in 4bit numbers as follows: b0 = 2, b1 = 5, b2 = 9, b3 = 14, b4 = 9, b5 = 5, and b6 = 2. The input samples are also 4 bits wide with positive values. The output of the FIR filter is assigned 11 parallel bits. The output FIRout should be a registered output.

It is required to add one pipeline register PR0 as shown in figure. Design the module and verify its functionality and the data coherence and compare it to a design with the same FIR filter coefficients but without any pipelining. Comment on the latency and throughput. (see example posted for thourough guidelines)



Assignment Question 3: (40 points)

Consider the following 6th order FIR filter. The filter coefficients are given in 4bit numbers as follows: b0 = 2, b1 = 5, b2 = 9, b3 = 14, b4 = 9, b5 = 5, and b6 = 2. The input samples are also 4 bits wide with positive values. The output of the FIR filter is assigned 11 parallel bits. The output FIRout should be a registered output.

It is required to add pipeline registers PR0, PR1, PR2 as shown in figure. Design the module and verify its functionality and the data coherence and compare it to a design with the same FIR filter coefficients but without any pipelining. Comment on the latency and throughput. (see example posted for thourough guidelines)