Logic Design using FPGAs **Spring 2024**
Assignment 2
Structural Design - Comparator

Objective: Structural Design using Verilog modules and using the RTL viewer to verify the nested structure of the design.

Design:

(a) Write a gate-level model describing the operation of a TwoBit comparator. The module will have 2 Two-bit inputs: **a**, and **b**. Three outputs indicate whether a equals b, a is less than b, or a is greater than b. Create the Karnaugh map and find the expression for the switching function for **the three outputs**.

(b) Use the TwoBit comparator to design a FourBit comparator. Add any additional logic needed.

(c) Verify the connection using the RTL Viewer, and verify the interconnections of the instantiated module.

(d) The Verilog Code should be well documented.