```
1  /*-------------------------------------------------------------------------------
2  Name Lamin Jammeh
3  CLass: EE417 Summer 2024
4  Lesson 07 HW Question 2
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: This is testbench shows the outputs and how the value 1 is shifting
7  -------------------------------------------------------------------------------*/
8
9  /*-----------------------TestBench for up/down count---------------*/
10 module DataPath_controller_tb ();
11
12 //define registers and wires
13 reg clk;
14 reg reset;
15 reg  [7:0] data_in;
16 wire [7:0] count;
17 wire shift_left;
18 wire shift_right;
19
20 //define the units under test UUT
21 DataPath_controller #(8, 18) UUT (
22                                    .clk(clk),
23                                    .reset(reset),
24                                    .data_in(data_in),
25                                    .count(count)
26                                    );
27
28 //monitor internal probe
29 assign count_up   = UUT.controller.shift_left;
30 assign count_down = UUT.controller.shift_right;
31 //clock cycle
32 initial
33    begin
34       clk = 0;
35       forever #10 clk = ~clk;
36    end
37
38 //count output is base on posedge of clk and reset
39 //initialie reset and run enough clk cycle to get all desired counts
40 initial
41    begin
42       reset = 1;
43       data_in = 8'b00000001;  //load initial value
44       #10 reset = 0;
45       #800 $stop;          //run clk for 100 time units change if necessary
46    end
47
48 //display results for each change in count
49 initial
50    begin
51       $monitor ("Time: %0t |  Count_up: %b | Count_down: %b |  count: %b", $time, count_up,
   count_down, count);
52    end
53 endmodule
```