Write a Verilog module that detects whether an input word has its majority of bits equal to 1s or not. The module should be parametrized, and should use the 'disable' command.

```
module majority_bits_are_1s   #(
                        parameter    word_size = 8,
                        parameter    majority = 5
                                    ) (
                        input       [word_size -1 : 0]      data_in,
                        output                              majority_ones_out

                                    );

integer                             index;
parameter                           count_size = 3,      // Should accommodate a count of 101 for majority
reg             [count_size – 1: 0]    count;

assign      majority_ones_out = (count>=majority);

always @ (data_in)    begin: count_ones
        count = 0;
        for ( index = 0;   index < word_size;  index = index+1)
            begin
                count = count + data_in[index];
                if (count >= majority)
                    disable count_ones;
             end
        end

endmodule
```

```
module majority_bits_are_1s    #(
                                    parameter     word_size = 8,
                                    parameter     majority = 5,
                                    parameter     count_size = 3
                               )(
                                    input         [word_size  -1: 0]        data_in,
                                    output                                  majority_ones_out,
                                    output reg    [count_size -1: 0]        count
                                 );

//parameter                         count_size = 3;
//reg      [count_size-1:0]         count;
integer                           index;

assign        majority_ones_out = (count>=majority);

always @ (data_in)     begin: count_ones
    count = 0;
    for ( index = 0;   index < word_size;  index = index+1)
         begin
              count = count + data_in[index];
              if (count >= majority)
                   disable count_ones;
        end
end

endmodule


module  majority_1s_tb ();
 parameter                      word_size = 8;
 parameter                      count_size = 3;
 reg        [word_size -1:0]    data_in;
 wire                           majority_ones_out;
 wire       [count_size-1:0]    count;


 majority_bits_are_1s    UUT     (data_in, majority_ones_out,count);

 initial
 begin
 #0      data_in = 8'b0000_0000;
 #10     data_in = 8'b1111_0001;    // Expected high out
 #10     data_in = 8'b0000_1111;
 #10     data_in = 8'b1111_1111;    // Expected high out
 #10     data_in = 8'b1010_1010;
 #10     data_in = 8'b0111_1111;    // Expected high out
 #10     data_in = 8'b1100_0001;
 #10     data_in = 8'b1111_0011;    // Expected high out
 #10     data_in = 8'b0000_0011;
 #10     data_in = 8'b1010_1111;    // Expected high out
 end

 // Using the disable command, the count should not exceed 5.
 // majority_ones_out should only be high when the majority of bits are ones.

 endmodule
```