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1  /*-------------------------------------------------------------------------------------------
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2  Name Lamin Jammeh
3  CLass: EE417 Summer 2024
4  FINAL PROJECT: Controller
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: The Controller module drives the enable signal. This signal will
   enable the
7  computation of the FIR_MAC
8  -------------------------------------------------------------------------------------------
   --------*/
9
10 module Pipeline_FIR_Controller (
11                                  input clock,
12                                  input reset,
13                                  output reg enable
14                                 );
15
16 // Control logic for the FIR filter
17 always @ (posedge clock or posedge reset)
18 begin
19    if (reset)
20       begin
21         enable <= 0;
22       end
23       else
24       begin
25         enable <= 1;
26       end
27 end
28
29 endmodule
30
```