Fall
2024

D_Flip-Flop

Tsu_dd = 80ps Tsu_opt = 254ps Thold = 70ps Tclk->Q = 165ps Width = 11.427µm height = 7.099µm

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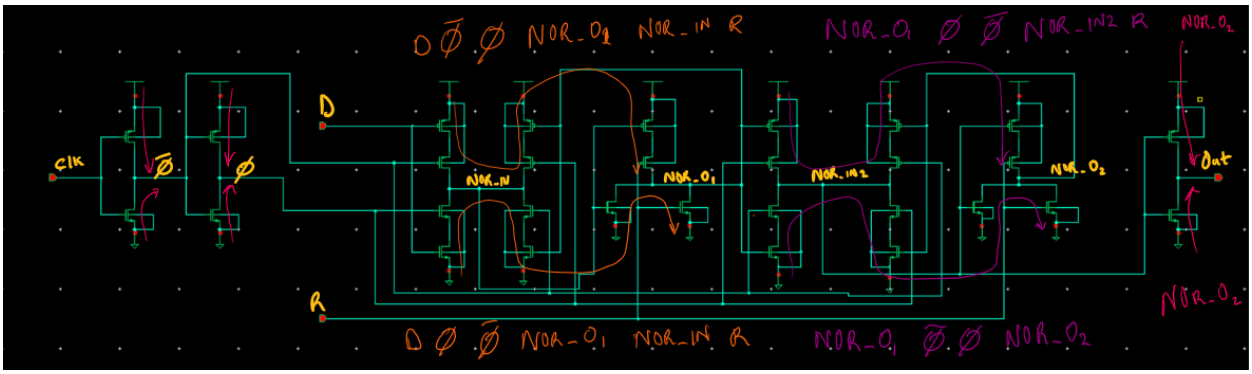
Pirpose:

In this project a D_Flip-Flop was design using two Tri-state inverters with a NOR2 gate to form a latch. The Flip-Flop has one output which is Q and a D input with the clk signal to drive the output

Schematic and Layout Trails:



obtain the trail for the stick diagram the circuit was divided into 4 sections. The first section consists of the clk, the second and third section consist of the latches and the fourth section is the Inverter for the Q output.

$$clk = \sim\emptyset$$

$$\sim\emptyset = \emptyset$$

The Clk section consist of an inverter with clk input which outputs the ~ø, and another inverter with input as ~ø and output is ø

Second section is the latch_1 which consists of the Tri-state inverter and the first NOR2 gate. Below is the equation from the upper trail1.

$$Trail1 = D \begin{pmatrix} \sim\emptyset & \emptyset \\ \emptyset & \sim\emptyset \end{pmatrix} NOR_{out1}\, NOR_{IN1}\, R$$

Third section is the latch_2 which is similar to the latch_1 with a mirrored Tri-states. Below is the equation for trail2.

$$Trail2 = NOR_{out1} \begin{pmatrix} \emptyset & \sim\emptyset \\ \sim\emptyset & \emptyset \end{pmatrix} NOR_{IN2}\, R$$

For the fourth section the input of the second NOR2 is also going to the output inverter.

$$Q = \sim NOR_{IN2}$$

Layout:

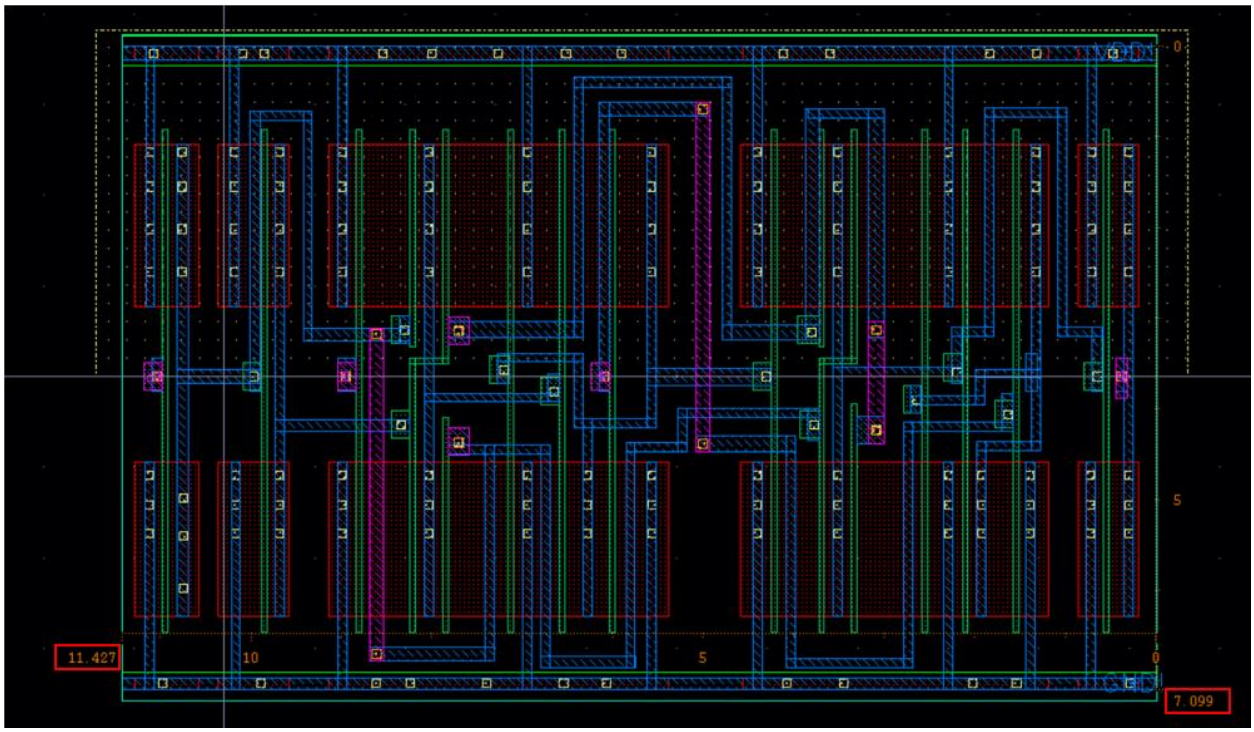


Figure showing the layout with Area = 11.427µm x 7.099µm

Pitch and Offset:

$$\boldsymbol{pitch = 0.26 * n} \quad [\boldsymbol{n = 1, 2, 3, 4, \ldots\ldots}]$$

$$\boldsymbol{offset = 0.13 + (0.26 * n)} \qquad [\boldsymbol{n = 1, 2, 3, 4, \ldots\ldots}]$$

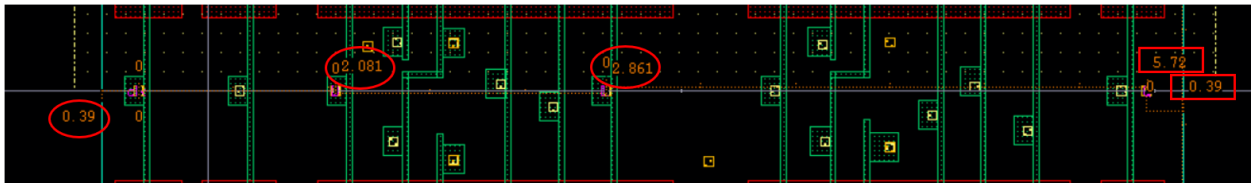


Figure showing the pin offsets and pitch

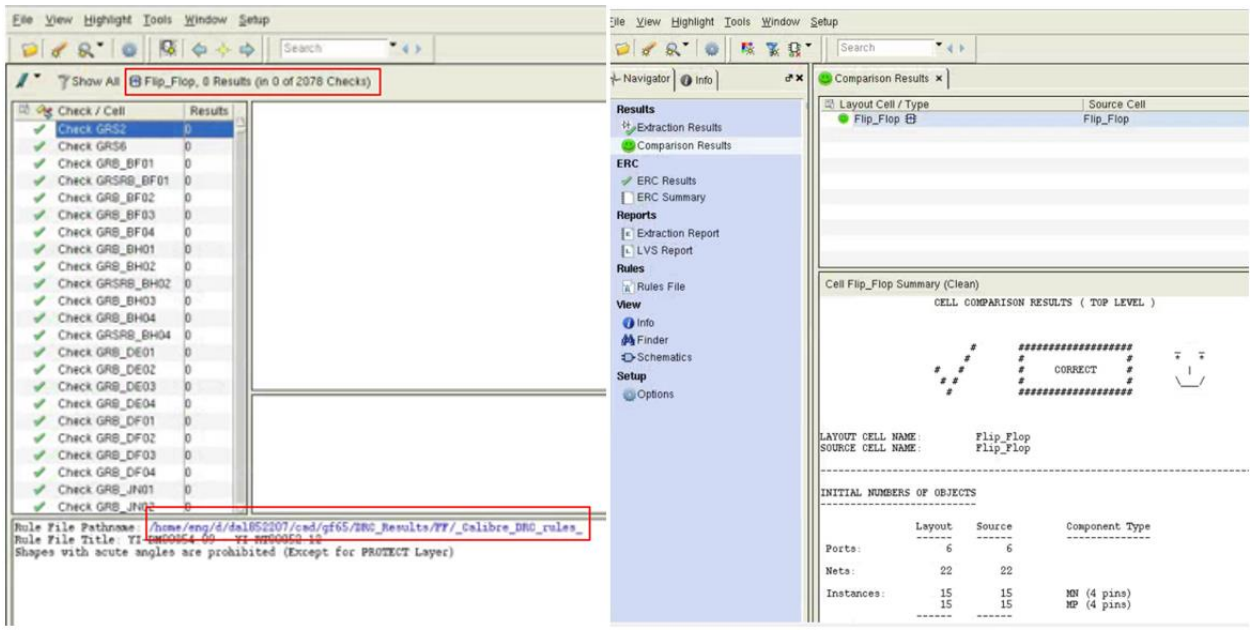
The offset from the edge to the clk input pin and from the edge to the Q output pins are both 0.39µm

clk to D pitch = 2.08µm = 0.26µm*8

D to R pitch = 2.86µm = 0.26µm*11

R to Q pitch = 5.72µm = 0.26µm*22

DRC and LVS results:

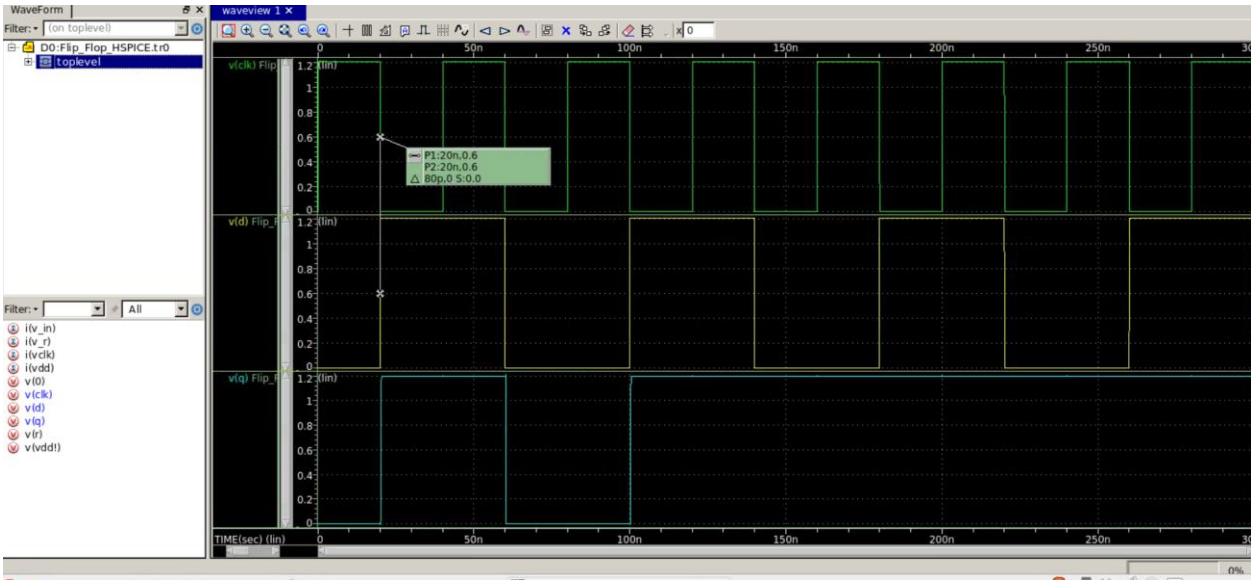


Timing measurement:

T_{su_dd}: the setup time drop dead was determined using the initial delay time of input D (T_DI) with first point of the input signal. The FP and the T_DI were changed until the output Q stopped changing. Once the Output Q stops changing the last clk to D delay ($Td_{clk->D}$) before the output stops changing was obtained as the T_{su_dd}

$$T_{DI} + FP = constant \ldots\ldots use\ this\ equation\ to\ chnage\ the\ initial\ delay\ of\ input\ D$$

T_{su_dd} = 80ps



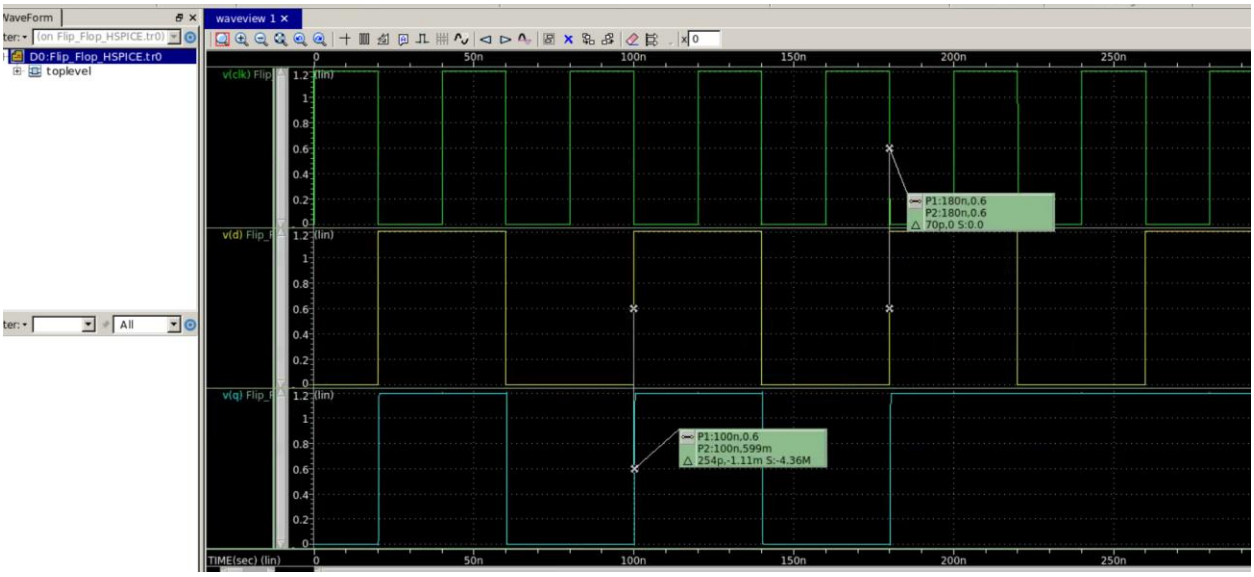
T_{su_opt} is the lowest input to output delay ($Td_{D->Q}$) before the setup drop dead time

T_{hold} : this is the clk to input D delay at the point when the output stops changing

T_{su_opt} = 254ps

T_{hold} = 70ps

$T_{clk->Q}$ = 165ps



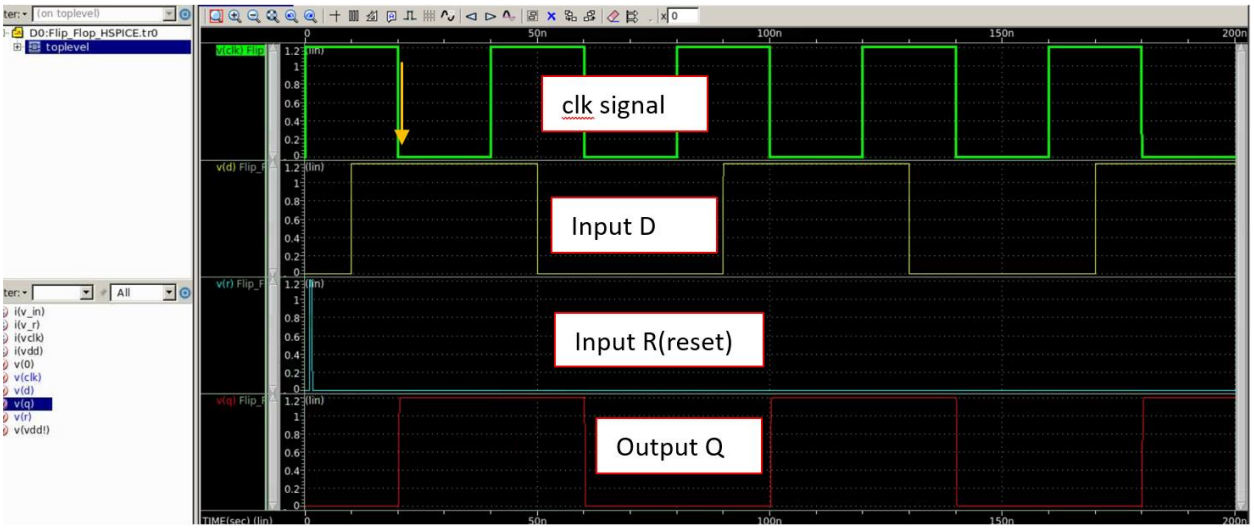
The equation below is used to determine the delay of the Flip-flop

$$T_D = T_{su} + T_{clk \rightarrow Q}$$

T_D = 254ps + 165ps = 419ps

Cell Behavior

The overall Flip-Flop behave as expected the input D equal to the output Q. the Flip-Flop is a negative edged trigger, since the output is changing at the falling edge of the clock signal. The reset changes the output to zero regardless of the input signal.



HSPICE setup script

```
HSPICE setup file for 3 Input cells
$ Name: Lamin Jammeh
$ UTD_ID: dal852207
$ CE6325 Proj4 Fall2024

$ transistor model this includes files generated from cadence virtuoso with the run.pex
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "Flip_Flop.pex.sp"

.option post runlvl=5

$ define the name for the circuit under test and ports
xi GND! Q VDD! CLK D R Flip_Flop

$define Power Supply as Vdd = 1.2
Vdd VDD! GND! 1.2v
Vss GND! 0 0



$ define Simulation parameters


.PARAM SR = 30ps                                                    $ Slew Rate
.PARAM Tclk = 20ns                                                  $ clk high and low time
.PARAM T_D = 40.01ns                                                $ D input high and low time
.PARAM T_R1 = 2ns                                                   $ initial low time
.PARAM T_R2 = 3ns                                                   $ High time
.PARAM PERIOD1 = '2*Tclk'
.PARAM PERIOD2 = '2*T_D'
.PARAM PERIOD3 = '2*T_R1'
.PARAM T_DI = 19.5ns                                                $inital Delay for input D

$generate a clk signal using the pulse function
VCLK CLK 0 PULSE (0 1.2 0 SR SR Tclk PERIOD1)

$generate a D input signal using the pulse function
V_IN D 0 PULSE (0 1.2 T_DI  SR SR T_D PERIOD2)
```

```
$generate a R input signal using the pulse function
V_R R 0 PWL (0 0 0.9n 0 1n 1.2 1.5n 1.2 1.6n 0 )

$ Load capacitance = 55pFarad
Cout Q GND! 55f

$ Type of HSPICE Simulation = Transient Analysis with 1ps step for 20ns durationF
.tran 1ps 300ns

$ Adding a sweep of 0.1u to 1.8u in steps of 0.1u the Transient analysis
$ .tran 1ps 400ns sweep WP 0.1u 1.8u 0.1u

.measure tran trise trig v(V_IN) val = 0.6 fall=1 targ v(Q) val = 0.6 rise=1                $measure thl at
0.6v
.measure tran tfall trig v(V_IN) val = 0.6 rise=1 targ v(Q) val = 0.6 fall=1                $measure tpl at
0.6v
.measure tran tfall trig v(V_IN) val = 0.6 rise=1 targ v(Q) val = 0.6 fall=1                $measure tpl at
0.6v
.measure tavg param  = '(trise + tfall)/2'
            $calculate average delay
.measure tdiff param = 'abs(trise - tfall)'
            $calculate delay difference
.measure delay param = 'max(trise, tfall)'
                        $calculate worst delay

$Calculate the energy dessipated during the delay
$method1
.measure tran iavg avg i(vdd) from=0  to=20n
            $average current in one clock cycle
.measure energy param = '1.2 * iavg * 300n'
                        $calculate energy in one clock cycle
.measure edp1   param = 'abs(delay * energy)'


.end
```