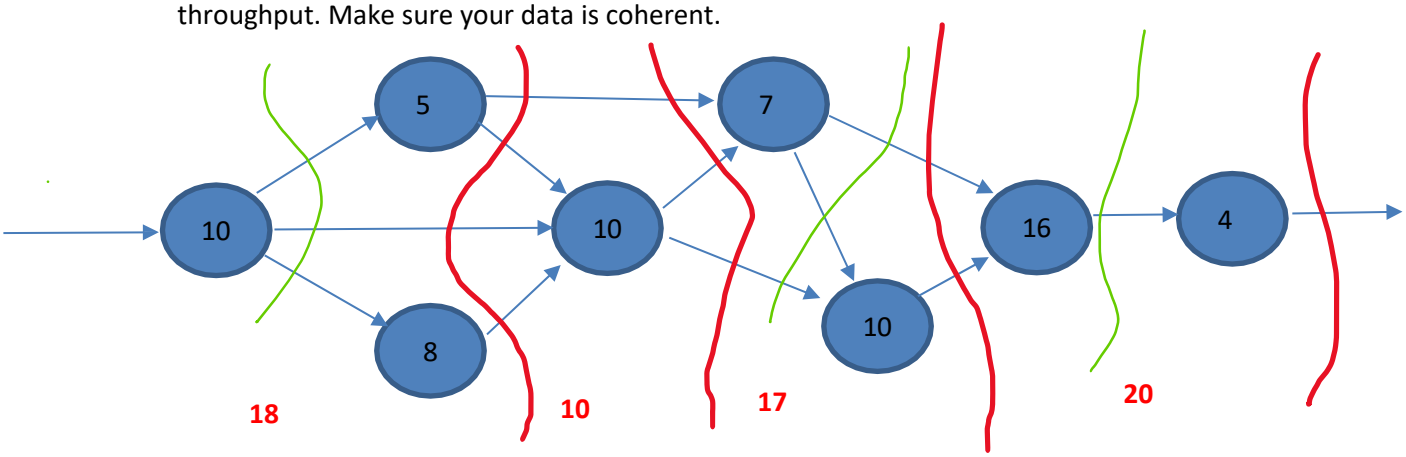
Example Pipelining Problem:

1. The nodes of the DFG shown in figure have been annotated with propagation delays. Find the optimal placement of pipeline registers in the circuit. Calculate the throughput and the latency. The latency should not exceed 80ns, and the design should give the maximum possible throughput. Make sure your data is coherent.



Pipelining Cut-sets	Minimum clock period	Latency	Throughput
1 output register	65ns	65ns	15.4 MHz
2 cut-sets	35ns	70ns	28.6 MHz
3 cut-sets	27ns	81ns	37.0 MHz
4 cut-sets	20ns	80ns	50 MHz
5 cut-sets	18ns	90ns	55.6 MHz
6 cut-sets	17ns	102ns	58.8 MHz
7 cut-sets	16ns	112ns	62.5 MHz

2. If there was no restriction on the latency, where would you locate your cut-sets to obtain the maximum possible throughput?

   The maximum possible throughput is determined by the process unit with the maximum delay. In this example the 16ns unit defines the throughput as 1/16ns = 62.5 MHz.