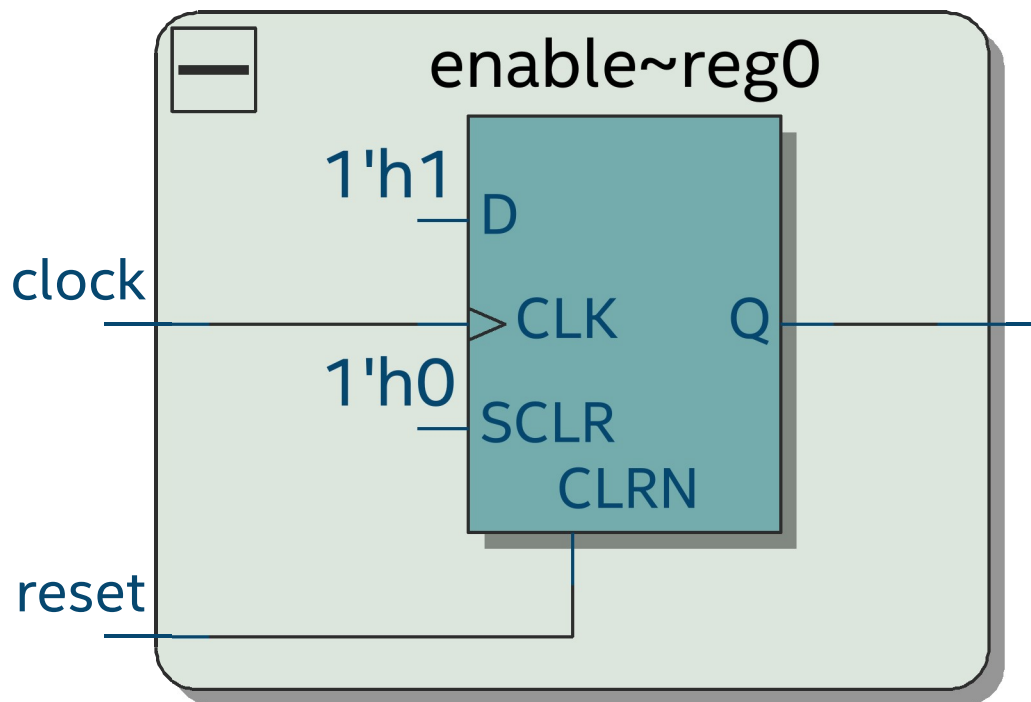


```
1  /*-----
2  Name Lamin Jammeh
3  Class: EE417 Summer 2024
4  FINAL PROJECT: Controller
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: The Controller module drives the enable signal. This signal will
7  enable the
8  computation of the FIR_MAC
9  -----*/
10 module Pipeline_FIR_Controller (
11     input clock,
12     input reset,
13     output reg enable
14 );
15
16 // Control logic for the FIR filter
17 always @ (posedge clock or posedge reset)
18 begin
19     if (reset)
20     begin
21         enable <= 0;
22     end
23     else
24     begin
25         enable <= 1;
26     end
27 end
28
29 endmodule
30
```

## Pipeline\_FIR\_Controller:controller



```

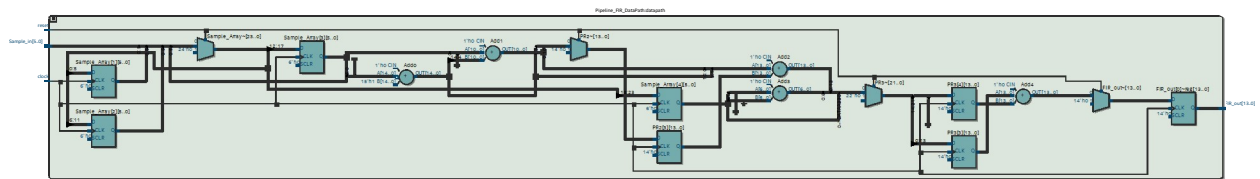
1  /*-----
2  Name Lamin Jammeh
3  Class: EE417 Summer 2024
4  FINAL PROJECT: Datapath
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: The Datapath module computes Filters the input Sample by Multiplying
   and Accumulating
7  -----*/
8
9  module Pipeline_FIR_DataPath (FIR_out, Sample_in, clock, reset);
10
11  //define the parameter sets for the design
12  parameter FIR_order      = 4;
13  parameter Sample_size    = 6;           //maximum sample value is 63
14  parameter weight_size    = 5;           //maximum value may be 31
15  parameter word_size_out  = Sample_size + weight_size + 3; //log2(2^2 * 2^5 * (order+1))
16
17  //define output
18  output reg [word_size_out-1:0] FIR_out;
19
20  //define inputs
21  input [Sample_size-1:0] Sample_in;
22  input clock, reset;
23
24  //define the filter coefficients
25  parameter b0 = 5'd3;
26  parameter b1 = 5'd7;
27  parameter b2 = 5'd20;
28  parameter b3 = 5'd7;
29  parameter b4 = 5'd3;
30
31  reg [Sample_size-1:0] Sample_Array[1:FIR_order]; //5th coefficient
   multiplied by Data_in
32  integer k;
33
34  //define PR0 to PR3 as registers
35  reg [word_size_out-1:0] PR0 [0:FIR_order];
36  reg [word_size_out-1:0] PR1 [1:FIR_order];
37  reg [word_size_out-1:0] PR2 [2:FIR_order];
38  reg [word_size_out-1:0] PR3 [3:FIR_order];
39
40  //define the transition logic
41  always @ (posedge clock)
42  if (reset == 1)
43  /*-----
44  if reset is high do the following
45  ***set all Pipeline registers to zero
46  *****IR = 0      Input register
47  *****PR[0:order-1] = 0      Pipeline register
48  *****OR = 0      Output register
49  -----*/
50  begin
51  //The input shift register
52  for (k=1; k <= FIR_order; k = k + 1)
53  Sample_Array[k] <= 0;
54
55  //The pipeline register
56  for (k = 0; k <= FIR_order; k = k + 1)
57  PR0[k] <= 0;
58  //The pipeline register
59  for (k = 1; k <= FIR_order; k = k + 1)
60  PR1[k] <= 0;
61
62  //The pipeline register
63  for (k = 2; k <= FIR_order; k = k + 1)
64  PR2[k] <= 0;
65  //The pipeline register

```

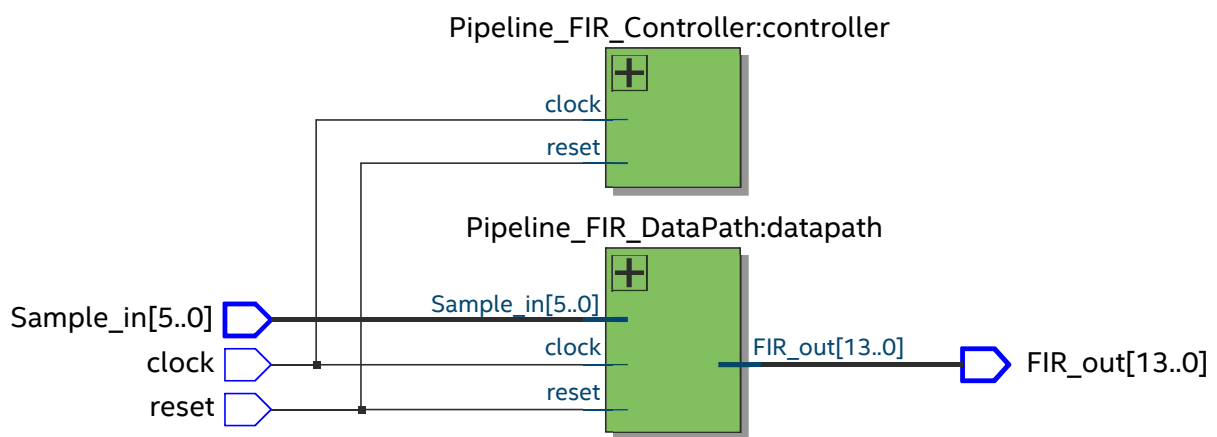
```

66         for (k = 3; k <= FIR_order; k = k + 1)
67             PR3[k] <= 0;
68
69         //The output register
70         FIR_out <= 0;
71     end
72 else
73     /*-----
74     if reset is low do the following
75     *****1 => move the Sample in into a cutset (Input register) to reduce idle time
of the input
76     *****2 => insert the PR at the input of the add and perform  $x[n] * b(n)$  and save
in Pipeline register (PR[n-1])
77     *****3 => add all the PR registers at the input of the output register and save
in the Output register
78     -----*/
79     begin
80         //The input shift register
81         Sample_Array[1] <= Sample_in;
82         for (k = 2; k <= FIR_order; k = k + 1)
83             Sample_Array[k] <= Sample_Array[k-1];
84
85         //The pipeline register at PR0
86         PR0[0] <= b0 * Sample_in;
87         PR0[1] <= b1 * Sample_Array[1];
88         PR0[2] <= b2 * Sample_Array[2];
89         PR0[3] <= b3 * Sample_Array[3];
90         PR0[4] <= b4 * Sample_Array[4];
91
92         //The pipeline register at PR1
93         PR1[1] <= b1 * Sample_Array[1] + PR0[1];
94         PR1[2] <= b2 * Sample_Array[2];
95         PR1[3] <= b3 * Sample_Array[3];
96         PR1[4] <= b4 * Sample_Array[4];
97
98         //The pipeline register at PR2
99         PR2[2] <= b2 * Sample_Array[2] + PR1[2];
100        PR2[3] <= b3 * Sample_Array[3];
101        PR2[4] <= b4 * Sample_Array[4];
102
103        //The pipeline register at PR3
104        PR3[3] <= b3 * Sample_Array[3] + PR2[3];
105        PR3[4] <= b4 * Sample_Array[4];
106
107        //The output register
108        FIR_out <= PR3[3] + PR3[4];
109    end
110 endmodule
111
112

```



```
1  /*-----
2  Name Lamin Jammeh
3  Class: EE417 Summer 2024
4  FINAL PROJECT: FIR MAC module
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: This Module combines the Datapath with the controller to form a
7  FIR_MAC.
8  -----*/
9  module Pipeline_FIR_MAC (FIR_out, Sample_in, clock, reset);
10
11  // Define the parameter sets for the design
12  parameter FIR_order      = 4;
13  parameter Sample_size    = 6; // Maximum sample value is 63
14  parameter weight_size    = 5; // Maximum value may be 31
15  parameter word_size_out  = Sample_size + weight_size + 3; // log2(2^2 * 2^5 * (order+1))
16
17  //define the outputs
18  output [word_size_out - 1:0] FIR_out;
19
20  //define the inputs
21  input [Sample_size - 1:0] Sample_in;
22  input clock, reset;
23
24  // Internal signals
25  wire enable;
26
27  // Instantiate the DataPath module
28  Pipeline_FIR_DataPath #(FIR_order, Sample_size, weight_size, word_size_out) datapath (
29      .FIR_out(FIR_out),
30      .Sample_in(Sample_in),
31      .clock(clock),
32      .reset(reset)
33  );
34
35  // Instantiate the Controller module
36  Pipeline_FIR_Controller controller (
37      .clock(clock),
38      .reset(reset),
39      .enable(enable)
40  );
41
42  endmodule
43
```



```

1  /*-----
2  Name Lamin Jammeh
3  Class: EE417 Summer 2024
4  FINAL PROJECT: FIR MAC module
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: testbench for the FIR_MAC with Pipelining
7  -----*/
8
9  module Pipeline_FIR_MAC_tb;
10
11  // Define the parameter sets for the design
12  parameter FIR_order      = 4;
13  parameter Sample_size    = 6; // maximum sample value is 63
14  parameter weight_size    = 5; // maximum value may be 31
15  parameter word_size_out  = 2 * Sample_size + 2; // maximum possible output 63*31*(4+1)
16
17  // Define the wires and registers for the test bench
18  wire [word_size_out-1:0] FIR_out;
19  reg [Sample_size-1:0] Sample_in;
20  reg clock, reset;
21
22  // Define the unit under test UUT
23  Pipeline_FIR_MAC UUT (FIR_out, Sample_in, clock, reset);
24
25  // Define Probes to observe the Pipeline register PR0
26  wire [word_size_out-1:0] PR00; assign PR00 = UUT.datapath.PR0[0];
27  wire [word_size_out-1:0] PR01; assign PR01 = UUT.datapath.PR0[1];
28  wire [word_size_out-1:0] PR02; assign PR02 = UUT.datapath.PR0[2];
29  wire [word_size_out-1:0] PR03; assign PR03 = UUT.datapath.PR0[3];
30  wire [word_size_out-1:0] PR04; assign PR04 = UUT.datapath.PR0[4];
31
32  // Define Probes to observe the Pipeline register PR1
33  wire [word_size_out-1:0] PR11; assign PR11 = UUT.datapath.PR1[1];
34  wire [word_size_out-1:0] PR12; assign PR12 = UUT.datapath.PR1[2];
35  wire [word_size_out-1:0] PR13; assign PR13 = UUT.datapath.PR1[3];
36  wire [word_size_out-1:0] PR14; assign PR14 = UUT.datapath.PR1[4];
37
38  // Define Probes to observe the Pipeline register PR2
39  wire [word_size_out-1:0] PR22; assign PR22 = UUT.datapath.PR2[2];
40  wire [word_size_out-1:0] PR23; assign PR23 = UUT.datapath.PR2[3];
41  wire [word_size_out-1:0] PR24; assign PR24 = UUT.datapath.PR2[4];
42
43  // Define Probes to observe the Pipeline register PR3
44  wire [word_size_out-1:0] PR33; assign PR33 = UUT.datapath.PR3[3];
45  wire [word_size_out-1:0] PR34; assign PR34 = UUT.datapath.PR3[4];
46
47  // Instantiate the clock signal
48  initial
49  begin
50      clock = 0;
51      forever #5 clock = ~clock;
52  end
53
54  // Instantiate and toggle the reset signal
55  initial
56  begin
57      reset = 1;
58      #10 reset = 0;
59  end
60
61  // Integer for file handle
62  integer f;
63  integer i;
64
65  // Apply different input samples and observe the outputs
66  initial
67  begin

```



```
68     f = $fopen("output.txt", "w");
69     $fwrite(f, "\t\tTime\tSample_in\tFIR_out\n");
70
71     // Apply the input samples and log the output
72     for (i = 0; i < 10; i = i + 1)
73     begin
74         case (i)
75             0: Sample_in = 0;
76             1: Sample_in = 1;
77             2: Sample_in = 0;
78             3: Sample_in = 10;
79             4: Sample_in = 0;
80             5: Sample_in = 1;
81             6: Sample_in = 2;
82             7: Sample_in = 8;
83             8: Sample_in = 2;
84             9: Sample_in = 1;
85             10: Sample_in = 0;
86             11: Sample_in = 63;
87             12: Sample_in = 0;
88             default: Sample_in = 0;
89         endcase
90         #10; // wait for the output to settle
91         $fwrite(f, "%d\t\t%d\t\t\t%d\n", $time, Sample_in, FIR_out);
92     end
93
94     $fclose(f);
95     #100 $stop;
96 end
97
98 endmodule
99
```

Time	Sample_in	FIR_out
10	0	0
20	1	0
30	0	0
40	10	0
50	0	0
60	1	7
70	2	10
80	8	70
90	2	100
100	1	7

## Timing Analysis for the clock signal

@ default time when clock period is 1ns

The screenshot shows the Quartus Prime IDE with the Timing Analyzer results for the clock signal. The Project Navigator on the left lists the files: `Controller/Pipeline_FIR_Controller.v`, `DataPath/Pipeline_FIR_DataPath.v`, `Pipeline_FIR_MAC.v`, and `Pipeline_FIR_MAC_tb.v`. The Table of Contents in the center lists the analysis steps: Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, Flow Log, Analysis & Synthesis, Fitter, Assembler, Timing Analyzer (selected), Summary, Parallel Compilation, and Clocks. The Messages window at the bottom displays the following information:

```
System (6) Processing (126)
100% 00:02:01
```

Messages:

- 332146 worst-case minimum pulse width slack is -0.080
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus\_edo --read\_settings\_files=off --write\_settings\_files=off Pipeline\_FIR\_MAC -c Pipeline\_FIR\_MAC
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value
- 204019 Generated File Pipeline\_FIR\_MAC.vo in folder "C:/Users/lanjg/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/FINAL PROJECT/FIR\_MAC/simulation"
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings

## Time report at a slack of -1.790

The screenshot shows the Quartus Prime IDE with the Timing Analyzer results for the clock signal at a slack of -1.790. The Set Operating Conditions window on the left shows the selected model: Slow 1100mV 85C Model. The Command Info window in the center displays the command: `quartus_edo --read_settings_files=off --write_settings_files=off Pipeline_FIR_MAC -c Pipeline_FIR_MAC`. The Path Summary window on the right shows the path summary for the clock signal, including the path name, statistics, data path, waveform, and extra filter information. The Path Summary table shows the following data:

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
-1.790	Pipeline_F_rray3[0]	Pipel_3[8]	clock	clock	1.000	-0.074	2.546
-1.786	Pipeline_F_rray3[2]	Pipel_3[8]	clock	clock	1.000	-0.078	2.538
-1.729	Pipeline_F_rray3[0]	Pipel_3[8]	clock	clock	1.000	-0.074	2.485
-1.716	Pipeline_F_rray3[3]	Pipel_3[8]	clock	clock	1.000	-0.073	2.473
-1.692	Pipeline_F_rray3[0]	Pipel_3[9]	clock	clock	1.000	-0.069	2.453
-1.690	Pipeline_F_rray3[2]	Pipel_3[9]	clock	clock	1.000	-0.073	2.447
-1.668	Pipeline_F_rray3[0]	Pipel_3[6]	clock	clock	1.000	-0.071	2.427

The Path Summary table also shows the path name, statistics, data path, waveform, and extra filter information. The Path Summary table shows the following data:

Path Name	Statistics	Data Path	Waveform	Extra Filter Information
Path #1: Setup slack is -1.790 (VIOLATED)				
Path Summary	Statistics	Data Path	Waveform	Extra Filter Information
Data Arrival Path				
1	0.000	0.000		launch edge time
2	4.097	4.097		clock path
3	0.000	0.000		source latency
4	0.000	0.000		clock
5	0.000	0.000		clock-input[i]
6	0.650	0.650		clock-input[o]
Data Required Path				
1	1.000	1.000		latch edge time
2	5.023	4.023		clock path
3	1.000	0.000		source latency
4	1.000	0.000		clock
5	1.000	0.000		clock-input[i]
6	1.650	0.650		clock-input[o]

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3	0.000	0.000		source latency
4	0.000	0.000		clock
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The Path Summary table also shows the path name, statistics, data path, waveform, and extra filter information. The Path Summary table shows the following data:

Path Name	Statistics	Data Path	Waveform	Extra Filter Information
Path #1: Setup slack is -1.790 (VIOLATED)				
Path Summary	Statistics	Data Path	Waveform	Extra Filter Information
Data Arrival Path				
1	0.000	0.000		launch edge time
2	4.097	4.097		clock path
3	0.000	0.000		source latency
4	0.000	0.000		clock
5	0.000	0.000		clock-input[i]
6	0.650	0.650		clock-input[o]
Data Required Path				
1	1.000	1.000		latch edge time
2	5.023	4.023		clock path
3	1.000	0.000		source latency
4	1.000	0.000		clock
5	1.000	0.000		clock-input[i]
6	1.650	0.650		clock-input[o]

The Path Summary table also shows the path name, statistics, data path, waveform, and extra filter information. The Path Summary table shows the following data:

Path Name	Statistics	Data Path	Waveform	Extra Filter Information
Path #1: Setup slack is -1.790 (VIOLATED)				
Path Summary	Statistics	Data Path	Waveform	Extra Filter Information
Data Arrival Path				
1	0.000	0.000		launch edge time
2	4.097	4.097		clock path
3	0.000	0.000		source latency
4	0.000	0.000		clock
5	0.000	0.000		clock-input[i]
6	0.650	0.650		clock-input[o]
Data Required Path				
1	1.000	1.000		latch edge time
2	5.023	4.023		clock path
3	1.000	0.000		source latency
4	1.000	0.000		clock
5	1.000	0.000		clock-input[i]
6	1.650	0.650		clock-input[o]

The Path Summary table also shows the path name, statistics, data path, waveform, and extra filter information. The Path Summary table shows the following data:

Path Name	Statistics	Data Path	Waveform	Extra Filter Information
Path #1: Setup slack is -1.790 (VIOLATED)				
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Data Arrival Path				
1	0.000	0.000		launch edge time
2	4.097	4.097		clock path
3	0.000	0.000		source latency
4	0.000	0.000		clock
5	0.000	0.000		clock-input[i]
6	0.650	0.650		clock-input[o]
Data Required Path				
1	1.000	1.000		latch edge time
2	5.023	4.023		clock path
3	1.000	0.000		source latency
4	1.000	0.000		clock
5	1.000	0.000		clock-input[i]
6	1.650	0.650		clock-input[o]

The Path Summary table also shows the path name, statistics, data path, waveform, and extra filter information. The Path Summary table shows the following data:

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Path #1: Setup slack is -1.790 (VIOLATED)				
Path Summary	Statistics	Data Path	Waveform	Extra Filter Information
Data Arrival Path				
1	0.000	0.000		launch edge time
2	4.097	4.097		clock path
3	0.000	0.000		source latency
4	0.000	0.000		clock
5	0.000	0.000		clock-input[i]
6	0.650	0.650		clock-input[o]
Data Required Path				
1	1.000	1.000		latch edge time
2	5.023	4.023		clock path
3	1.000	0.000		source latency
4	1.000	0.000		clock
5	1.000	0.000		clock-input[i]
6	1.650	0.650		clock-input[o]

The Path Summary table also shows the path name, statistics, data path, waveform, and extra filter information. The Path Summary table shows the following data:

Path Name	Statistics	Data Path	Waveform	Extra Filter Information

@ default time when clock period is 4ns

Quartus Prime Lite Edition - C:/Users/Imnjm/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/FINAL PROJECT/FIR\_MAC/Pipeline\_FIR\_MAC - Pipeline\_FIR\_MAC

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Project Navigator Files

Files

- Pipeline\_FIR\_MACOut.sdc
- \_Controller/Pipeline\_FIR\_Controller.v
- \_DataPath/Pipeline\_FIR\_DataPath.v
- Pipeline\_FIR\_MAC.v
- Pipeline\_FIR\_MAC\_tb.v

Table of Contents

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  - Parallel Compilation
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    - Slow 1100mV 85C Model
    - Slow 1100mV OC Model
    - Fast 1100mV 85C Model
    - Fast 1100mV OC Model

Messages

System (6) Processing (118)

100% 00:01:35

Time report at a slack of 1.096

Timing Analyzer - C:/Users/Imnjm/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/FINAL PROJECT/FIR\_MAC/Pipeline\_FIR\_MAC - Pipeline\_FIR\_MAC

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Set Operating Conditions

Slow 1100mV 85C Model

Command Info

Summary of Paths

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1.096	Pipeline_F_array[3][1]	Pipel_3[8]	clock	clock	4.000	-0.080	2.654
1.108	Pipeline_F_array[3][2]	Pipel_3[8]	clock	clock	4.000	-0.074	2.648
1.111	Pipeline_F_array[3][0]	Pipel_3[8]	clock	clock	4.000	-0.074	2.645
1.131	Pipeline_F_array[3][3]	Pipel_3[8]	clock	clock	4.000	-0.079	2.620
1.136	Pipeline_F_array[3][2]	Pipel_3[8]	clock	clock	4.000	-0.074	2.620
1.138	Pipeline_F_array[3][0]	Pipel_3[8]	clock	clock	4.000	-0.074	2.618
1.148	Pipeline_F_array[3][1]	Pipel_3[8]	clock	clock	4.000	-0.080	2.602

Path #1: Setup slack is 1.096

Path Summary

Total	Incr	RF	Type	Fanout	Location	Element
0.000	0.000					launch edge time
4.104	4.104					clock path
0.000	0.000					source latency
0.000	0.000	RR	IC	1	IOIBUF_X89_Y25_N21	clock-input[1]
0.650	0.650	RR	CELL	1	IOIBUF_X89_Y25_N21	clock-input[0]

Data Required Path

Total	Incr	RF	Type	Fanout	Location	Element
4.000	4.000					latch edge time
8.024	4.024					clock path
4.000	0.000					source latency
4.000	0.000	RR	IC	1	IOIBUF_X89_Y25_N21	clock-input[1]
4.650	0.650	RR	CELL	1	IOIBUF_X89_Y25_N21	clock-input[0]

Waveform

Setup Relationship

Latch Clock

Data Arrival

Clock Delay

Data Delay

Slack

Data Required

Console

History

0% 00:00:00 Ready



```
%  
-----  
% Name Lamin Jammeh  
% Class: EE417 Summer 2024  
% Lesson 10 HW Question 3  
% Group: Ron Kalin/ Lamin Jammeh  
% Project Description: The Testbench results are plotted to show the filtered and  
unfiltered signals  
%  
-----  
  
%Step1 define the TestBench result  
time = 10:10:100;  
Sample_in = [0, 1, 0, 10, 0, 1, 2, 8, 2, 1];  
FIR_out = [0, 0, 0, 0, 0, 7, 10, 70, 100, 7];  
  
%Step2 plot the TestBench results  
plot(time, Sample_in, 'LineWidth',2);  
hold on;  
plot(time, FIR_out, 'LineWidth',2);  
grid on;  
legend('Unfiltered Signal','Filtered Signal', 'Location','north');  
  
title('FIR_MAC Filtered vs Unfiltered Results');  
xticks(0:5:100);  
yticks(0:5:100);  
xlabel('time in nanoSec');  
ylabel('Signal values');  
hold off;
```

