**EECT/CE 6325 VLSI Design**

Fall 2024

**PROJECT #5: D Flip-Flop**

**Due: Fri. November 15**

**Project Introduction**

For this project you will be using the Cadence Design tools to design, layout and characterize the D-Flip-Flop as designed in class (no other FF allowed!). **NOTE: The poly width (length of the channel) must be 62nm for this project, as in Project 4. No points for other sizes.**

**Project Goals**

1) Minimize diffusion breaks and cell width.
2) Match the cell height to that of your cells in Project 4, given that the height of the pMOS must accommodate 4 contacts and nMOS must accommodate 3 contacts.

**Project Rules & Requirements**

1) Use exactly the DFF design shown in class.
2) Input/output pins must lie on a grid (an integer multiple of the grid spacing)
3) Minimize the use of vertical metal2, and no horizontal metal2.
   EACH USE of vertical M2 COUNTS AGAINST You!!
4) Minimize the use of horizontal poly, no longer than 4 poly pitches.
5) The input slew rate is 30 ps (the slew rate, for this problem, is defined as the time for the input to go from low (.2 Vdd) to high (.8 Vdd) and vice versa).
6) Assume a 55fF load capacitance when simulating.
7) The DFF cell has 4 pins: D, CLK, R (reset, active high) and Q (output pin).
8) Characterize the DFF using **PrimeLib**. Use the DFF.inst file provided on eLearning.

**What to Turn In** (points are deducted for anything missing)

1) A cover page containing all the following information.
   - Name, NetID and project title
   - D Flip-Flop times: $T_{su\_dd}$, $T_{su\_opt}$, $T_{hold}$, $T_{clk->Q}$, and $t_D$
   - Clearly state your width and height on the front.
2) Please include a short report describing the following
   - How you found your D Flip-Flop times
   - How you came up with your layout
3) D Flip-Flop layout with rulers showing the dimensions of the cell.
   - Show the uniform distance of your pin grid
   - Show height & width of entire cell
4) Waveforms and explanation showing how you computed $T_{su\_dd}$, $T_{su\_opt}$, $T_{hold}$, $T_{clk->Q}$, and $t_D$.
5) Spice testing setup file (Don't include any spice netlist)
6) Upload the project report on eLearning.
7) Upload the zipped folder containing your DFF layout and schematic on eLearning

**Grading Breakdown**

- Correct functionality 30%
- Cell Area 25%
- Number of M2 used 25%
- Report 20%