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1   //ee417 lesson 5 Assignment 1, L5A1
2   // Name: Ron Kalin, Date: 06-13-24  Group: Kalin/Jammeh
3   // Testbench for Design: manchester to PAM4 converter using
4   // manchester to NRZ converter then NRZ to PAM4 converter
5   //Step1 define test bench name
6   module manchester_to_pam4_tb();
7
8   /*original module declaration
9   module manchester_to_pam4 (
10      output[2:0] PAM_out, // 3-bit PAM4 output
11      input clk, // Clock for sampling
12      input rst, // Reset
13      input manchester_in); // Manchester-encoded 1bit serial input*/
14  //Step2 define inputs as registers, outputs as wires
15  reg clk, rst, manchester_in;
16  reg [3:0] a;
17  wire [1:0] PAM_out;
18  //internal probe wires: observe change in state..Questa error if not correct no. of
    bits
19  wire NRZ_out;
20
21  //Step3 define unit under test
22  manchester_to_pam4 UUT (PAM_out,clk,rst,manchester_in);
23
24  //internal probes to track logic and troubleshoot
25  assign NRZ_out= UUT.NRZ_out;
26
27  //Step4 open initial block, define all possible input combinations
28  // Clock generation (adjust the period as needed)
29  initial begin
30    clk=0;
31    forever
32    #5 clk = ~clk;
33  end
34
35  initial  //reset is active high, longer time to count when reset is inactive (low)
36   begin   //4 cases with two selects
37    rst  = 1'b1; //reset on
38    a=4'b0000;
39    # 10 rst = 1'b0;  //reset off
40  //start manchester sequence
41    repeat (2) begin  // repeat x times
42    #5   manchester_in=1'b1;
43    #10  manchester_in=1'b0;
44    #10  manchester_in=1'b0;
45    #10  manchester_in=1'b1;  //PAM 4=2
46
47    #10  manchester_in=1'b1;
48    #10  manchester_in=1'b0;
49    #10  manchester_in=1'b1;
50    #10  manchester_in=1'b0; //PAM 4=3
51
52    #10  manchester_in=1'b0;
53    #10  manchester_in=1'b1;
54    #10  manchester_in=1'b0;
55    #10  manchester_in=1'b1; //PAM 4=0
56
57    #10  manchester_in=1'b0;
58    #10  manchester_in=1'b1;
59    #10  manchester_in=1'b1;
60    #10  manchester_in=1'b0; //PAM 4=1
61    #10;
62    end
63
64    rst = 1'b1;
65    #20 rst=1'b0;
66
67    repeat (15) begin //cycle thru every possible combination of four series inputs
68      #10 manchester_in=a[3];
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69        #10 manchester_in=a[2];
70        #10 manchester_in=a[1];
71        #10 manchester_in=a[0];
72        a=a+1;
73      end
74
75      #100 $stop; //close debug window to view waveform viewer
76     end
77
78    //Step5 Display the results
79    initial begin //monitor counter value
80      $display("_____________________________output_PAM_out = -PAM4-");
81      $monitor("clk_in = %b: rst_in = %b:  output_PAM_out = %d ",
82      clk, rst, PAM_out);
83     end
84    endmodule
```