

# Cell Library

PROJECT 4 CE6325 VLSI DESIGN: CELL LIBRARY

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## **Project Description:**

The project library was built using 11 different cells. Both the cell schematic and layout were designed in cadence virtuoso. Using the design specs for the project, each cell is evaluated independently using calibre rules script provided for this course. A design rule check (DRC) and a layout vs schematic (LVS) evaluation were performed to make sure the schematic and layout have no discrepancies. A parasitic extraction was performed to be able to analyze the circuit behavior in simulation tools like HSPICE, this makes sure the designed cell will behave as intended (a form of verification step). The abstract view of each cell was made and a primelib was compiled using Synopsys.

## **Design tools used**

- Cadence Virtuoso: to perform layout and schematic drawings
- HSPICE: to simulate the circuit and validate the design performance
- SYNOPSIS: to perform the PrimeLib compilation

## **Design Specification:**

Slew rate = 30ps [this spec is required for this project]

Width of PMOS ( $W_p$ ) = 1.8 $\mu$ m [this spec is not required but was used for all cells]

Width of NMOS ( $W_n$ ) = 1.7 $\mu$ m [this spec is not required but was used for all cells]

Length ( $L$ ) = 62nm [this is required for this project]

Load Capacitance ( $C_{load}$ ) = 55fF

## **INV Cell:**

### **Layout**

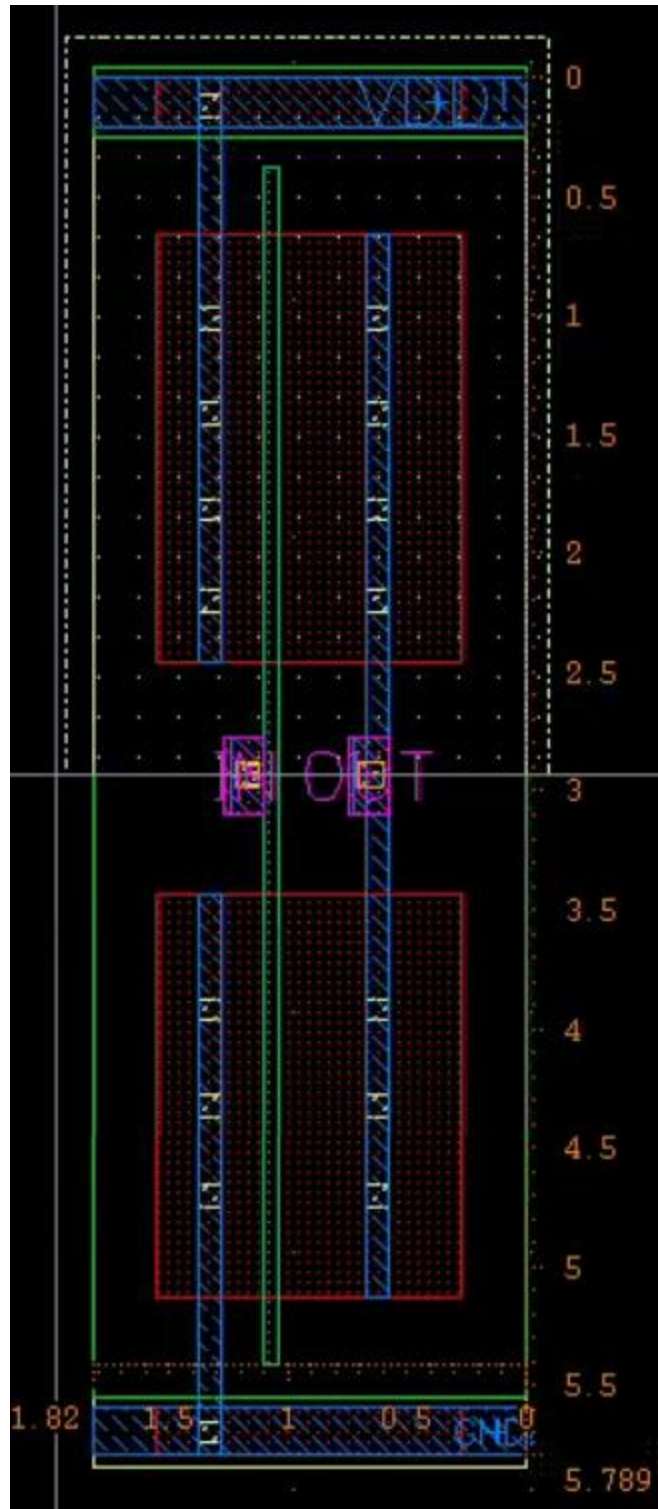


Figure NOR2 layout with size = [5.789um X 1.82um]

**Abstract View:**

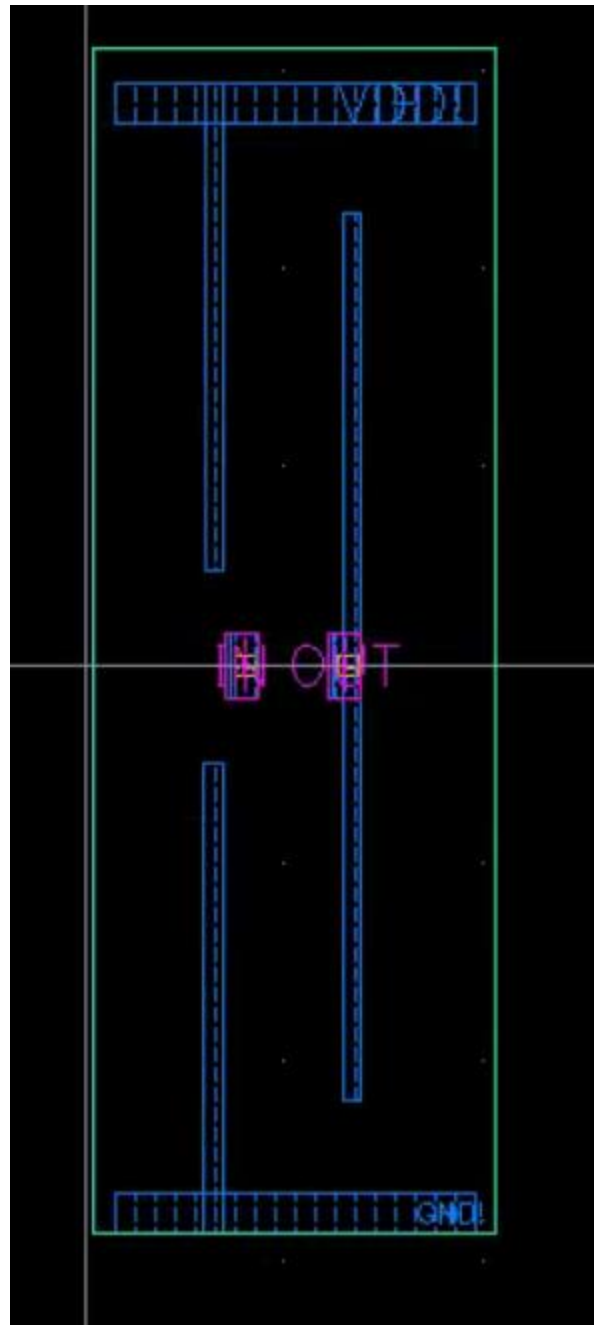


Figure Abstract View

Pitch

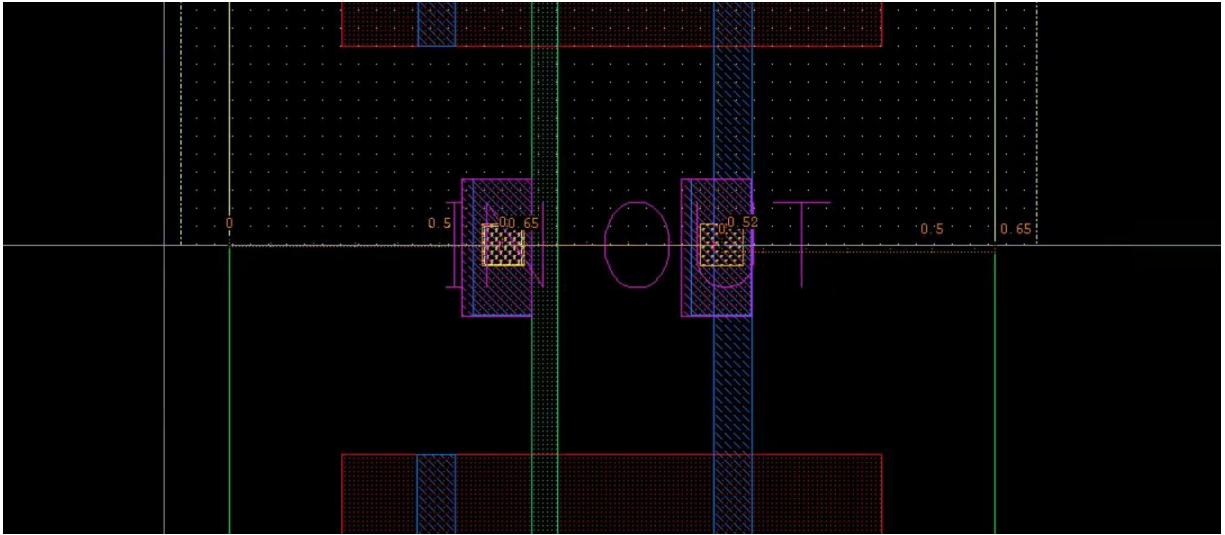


Figure showing 0.65um offset and 0.52um pitch

### Boolean Table

INV	
IN	OUT
0	1
1	0

Table showing the expected INV behavior

### Waveform view

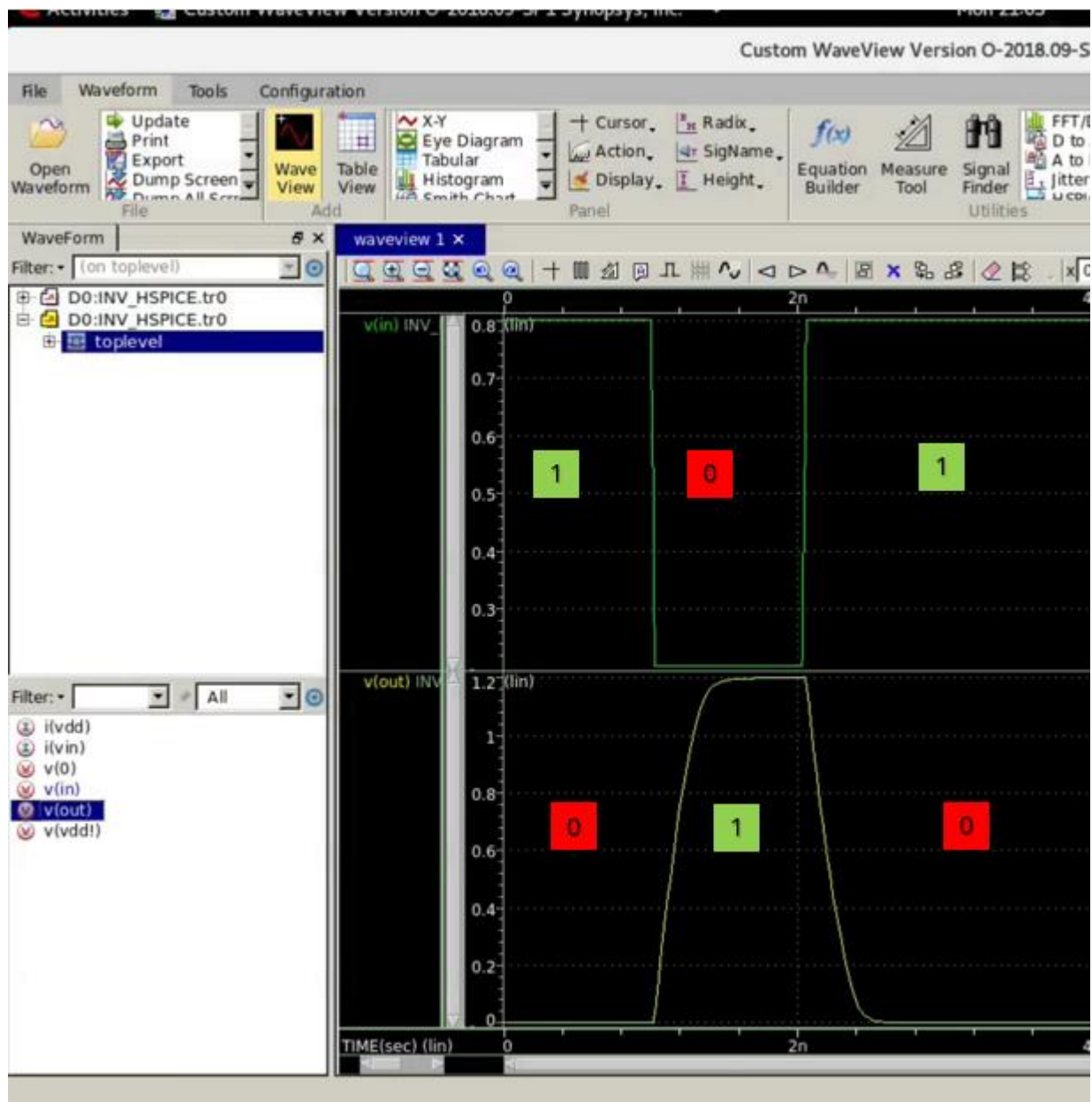


Figure waveform of Input Vs OUT for INV

**NOR2 Cell:**

**Layout**

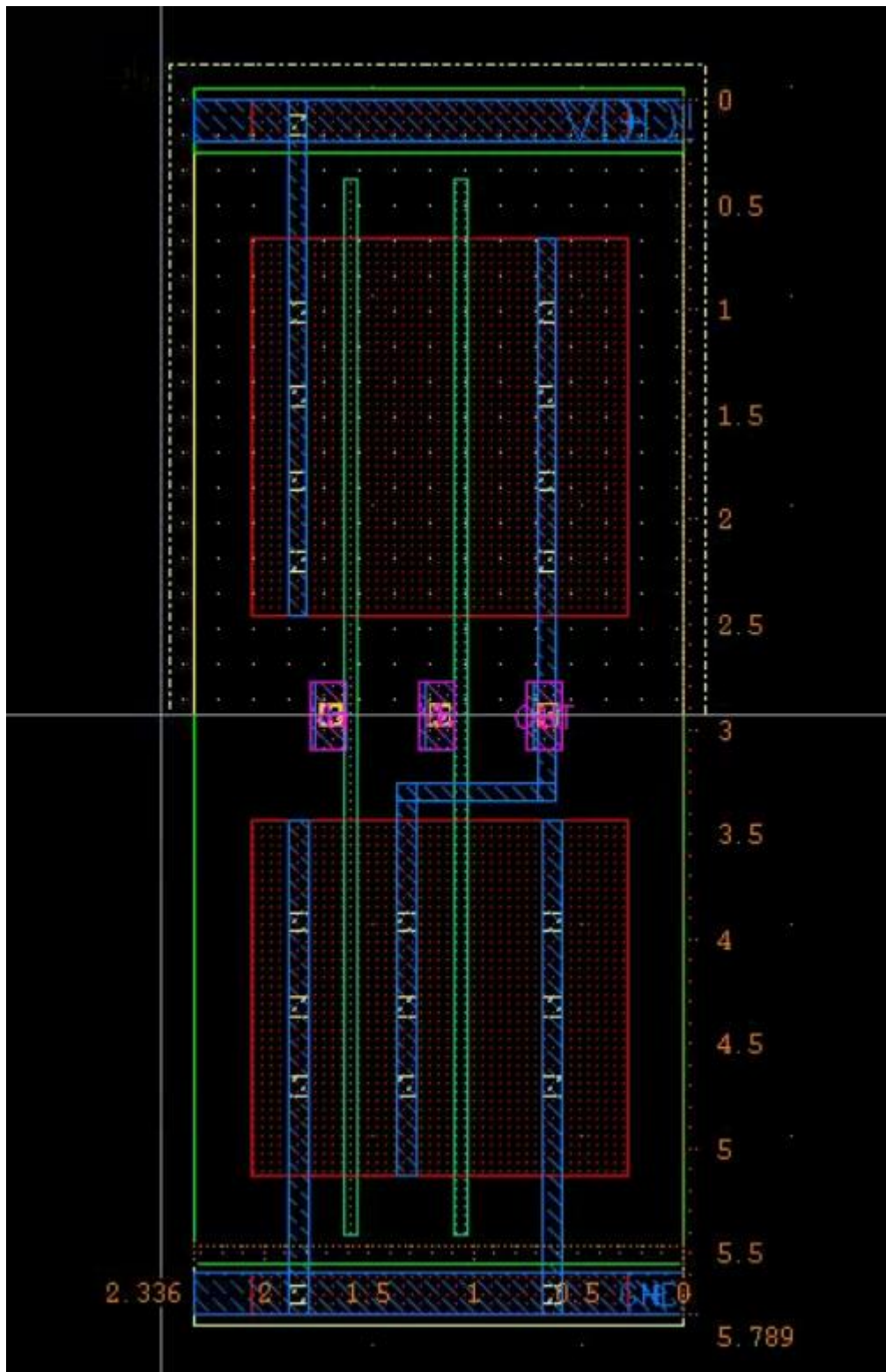


Figure NOR2 layout with size = [5.789um X 2.336um]

**Abstract View:**

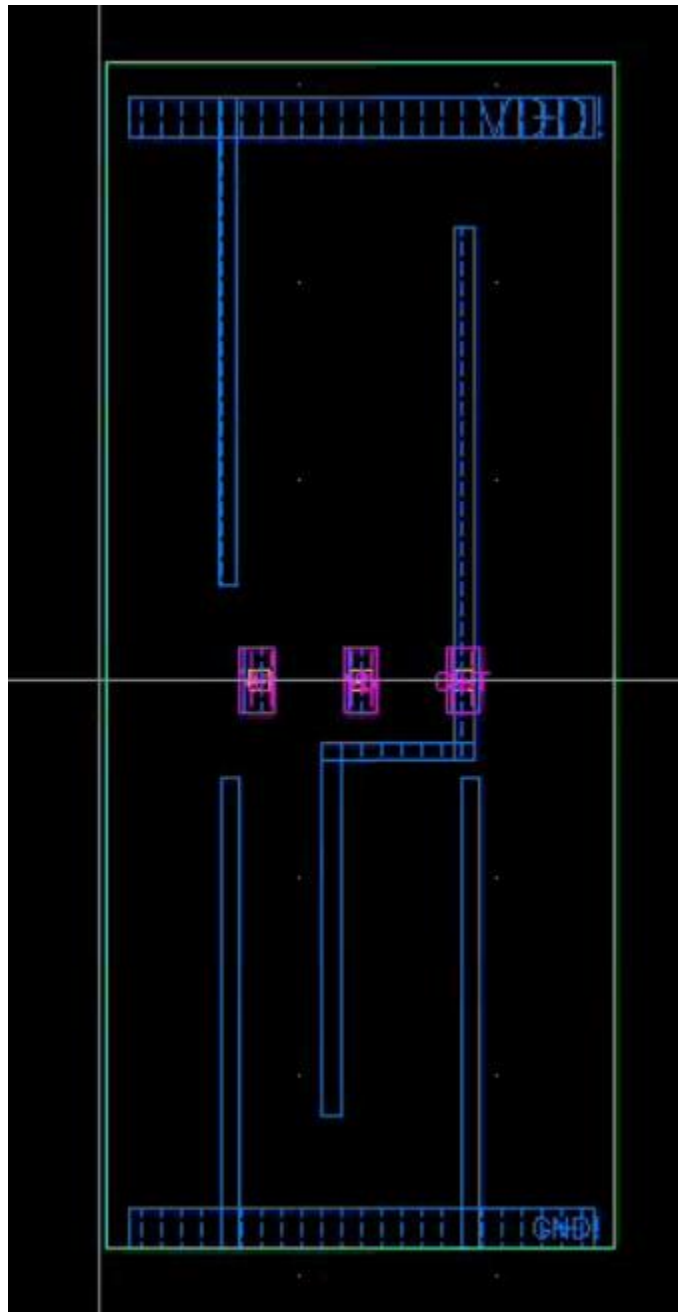


Figure Abstract View

**Pitch**



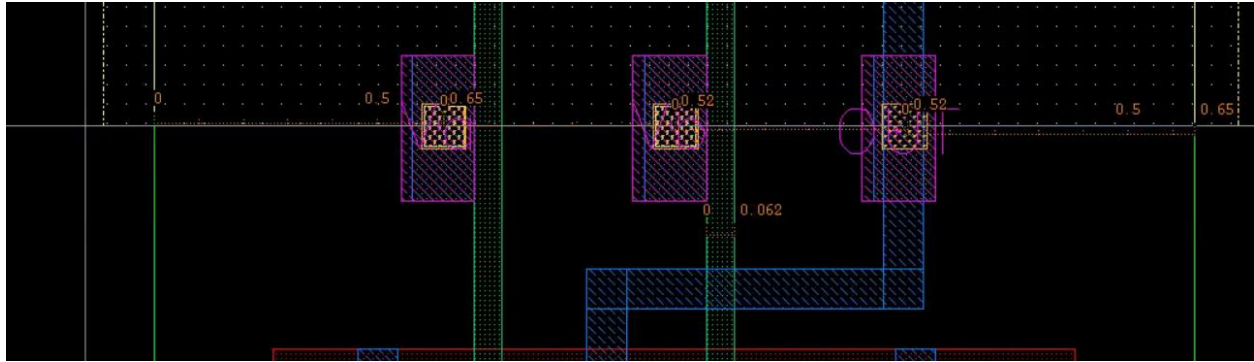


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

### Boolean Table

NOR2		
VA	VB	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Table showing the expected NOR2 behavior

### Waveform view:

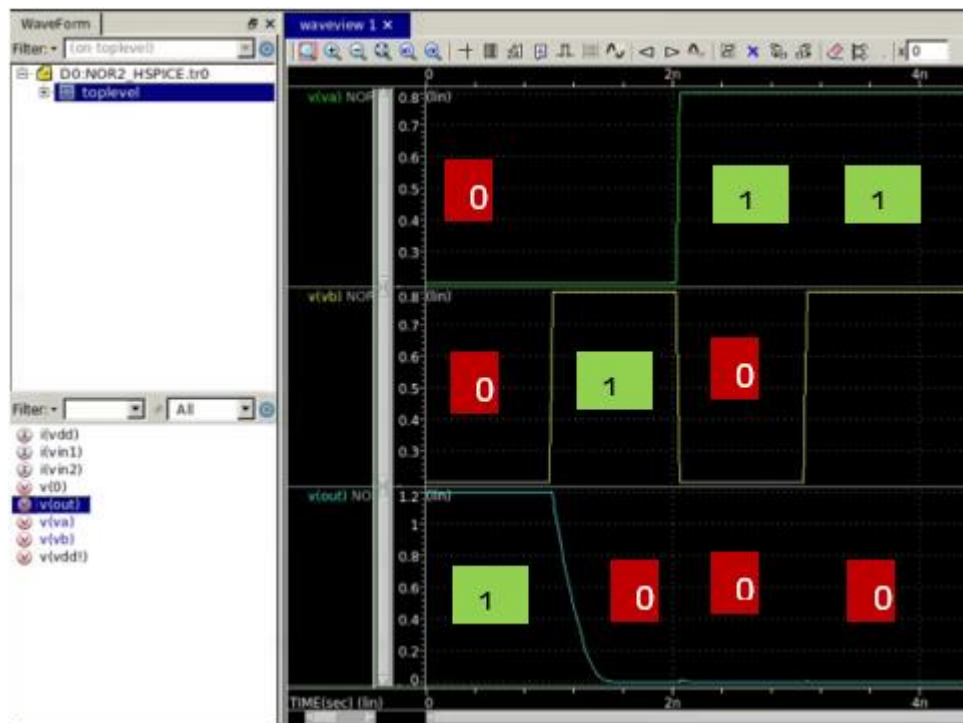


Figure waveform of Input Vs OUT for NOR2

**NOR3 Cell:**

**Layout:**

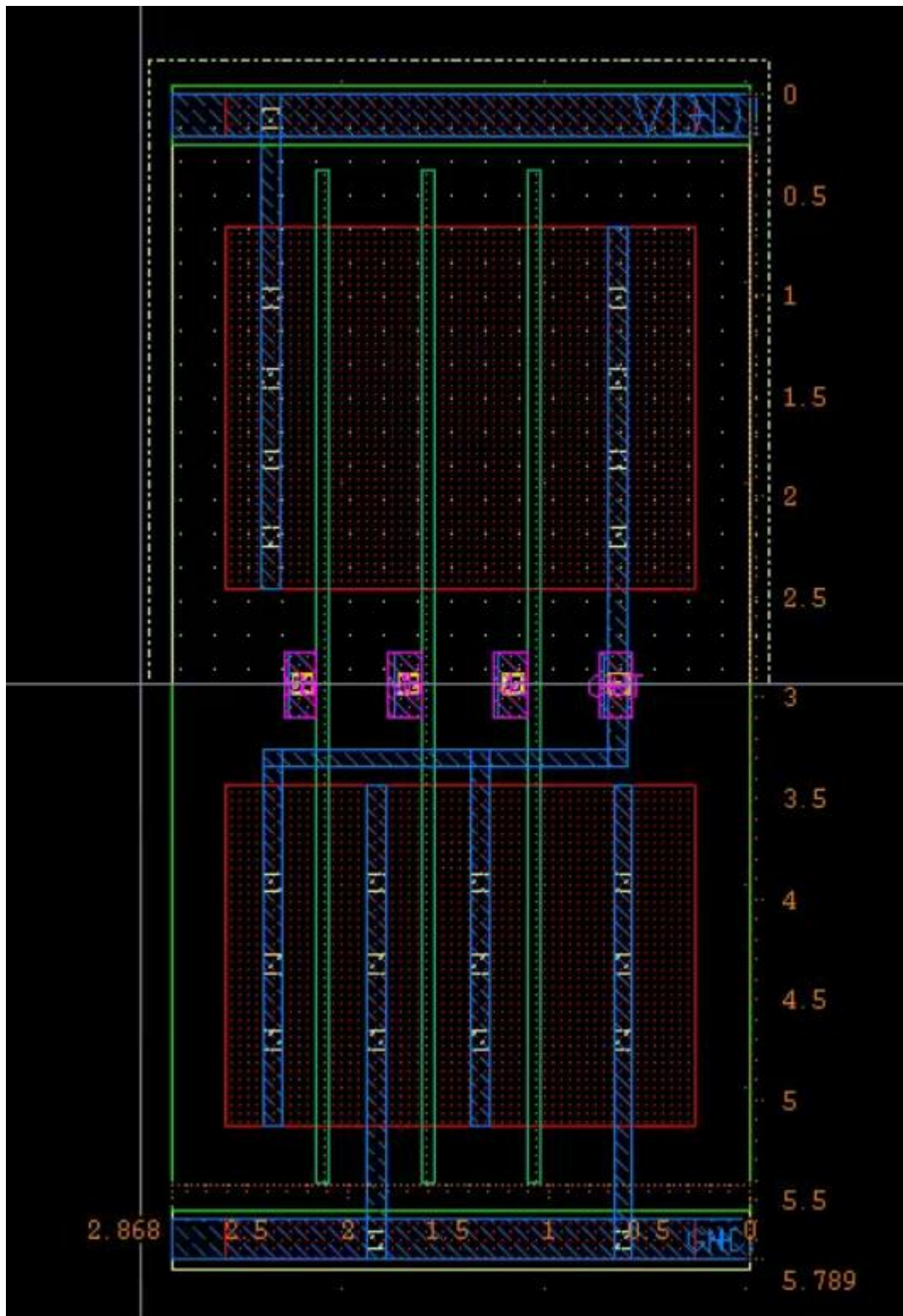


Figure NOR3 layout with size = [5.789um X 2.868um]

**Abstract View:**

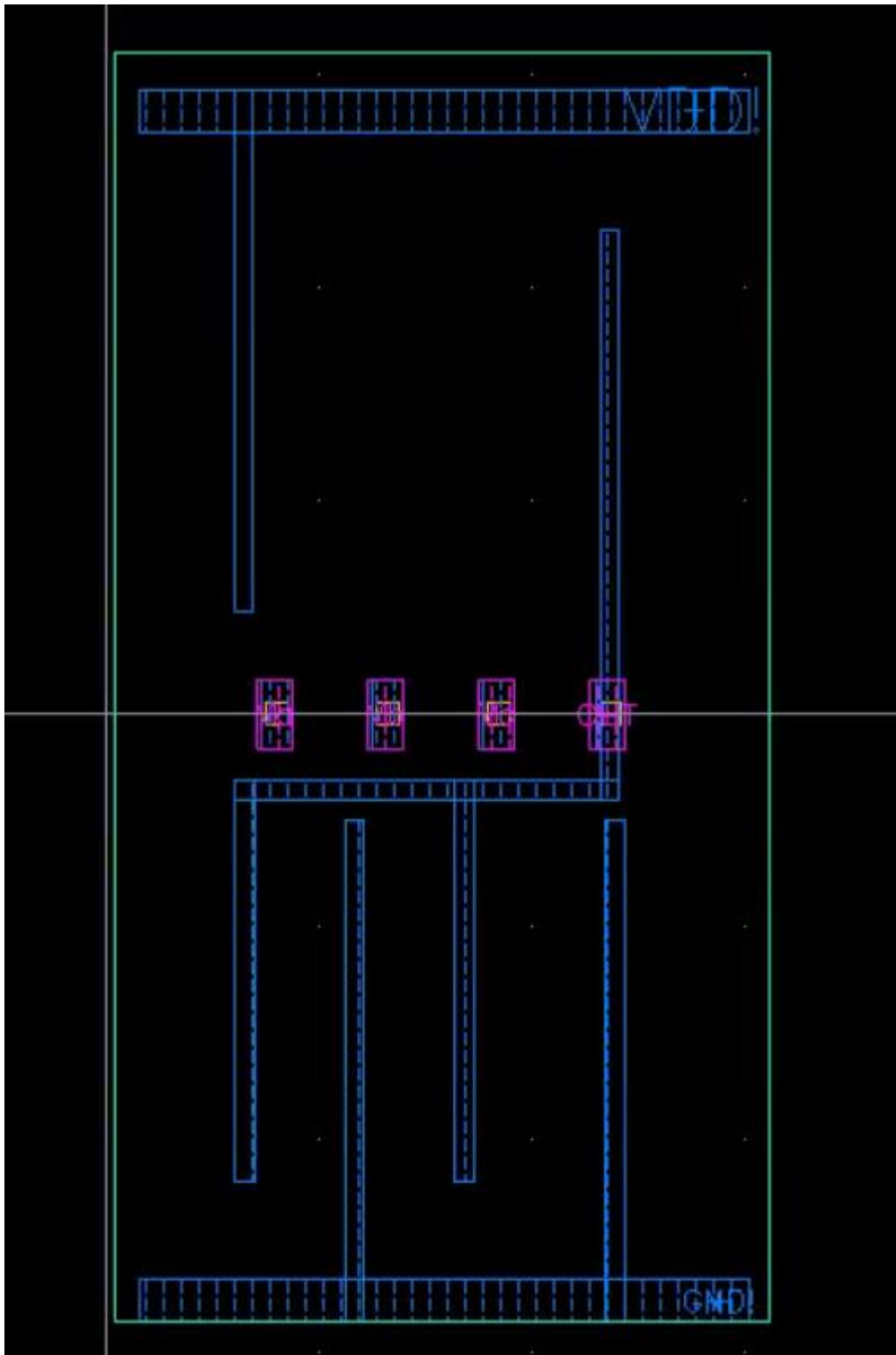


Figure Abstract View

### Pitch:

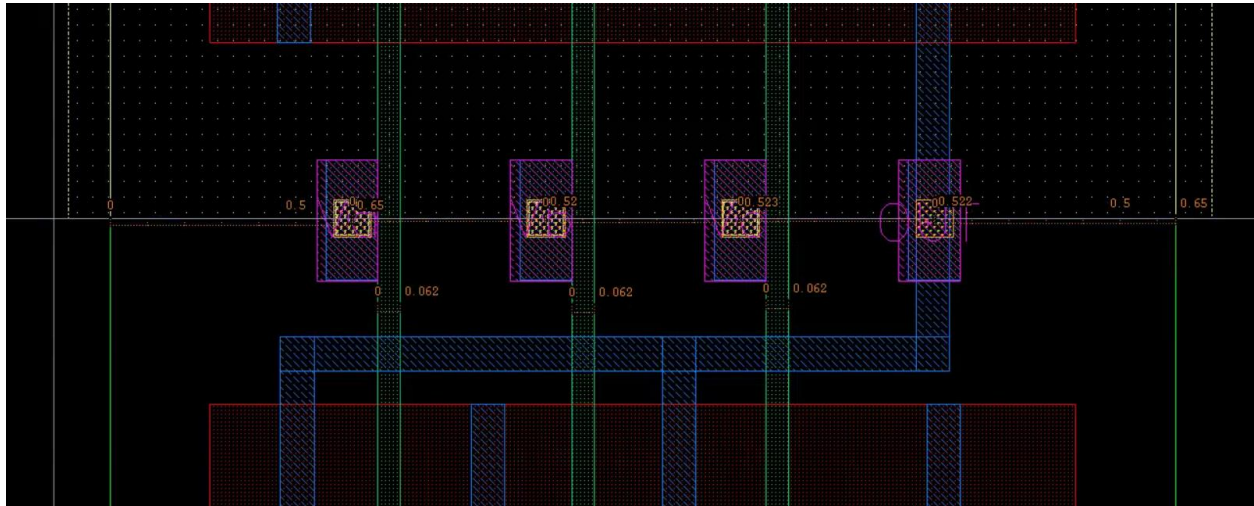


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

### Boolean Table:

NOR3			
VA	VB	VC	OUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Table showing the expected NOR3 behavior

### Waveform view:

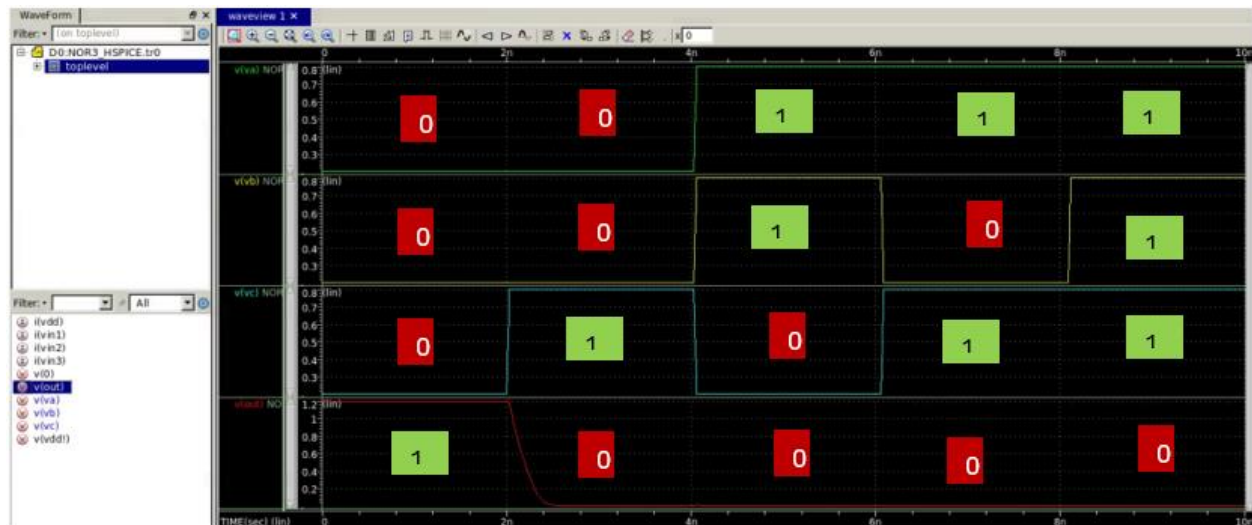


Figure waveform of Input Vs OUT for NOR3

**NAND2 Cell:**

**Layout:**



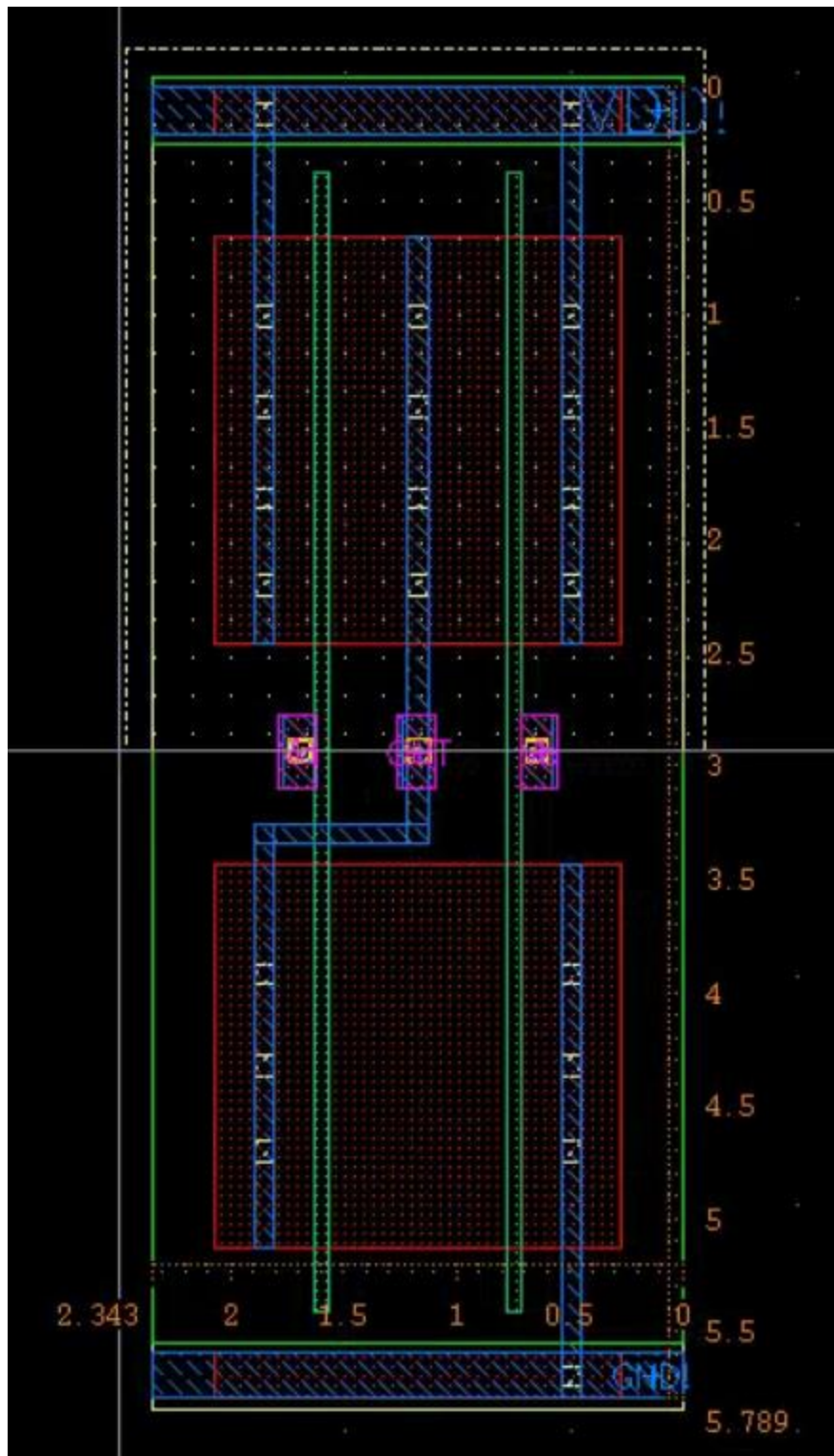


Figure NAND2 layout with size = [5.789um X 2.343um]

**Abstract View:**

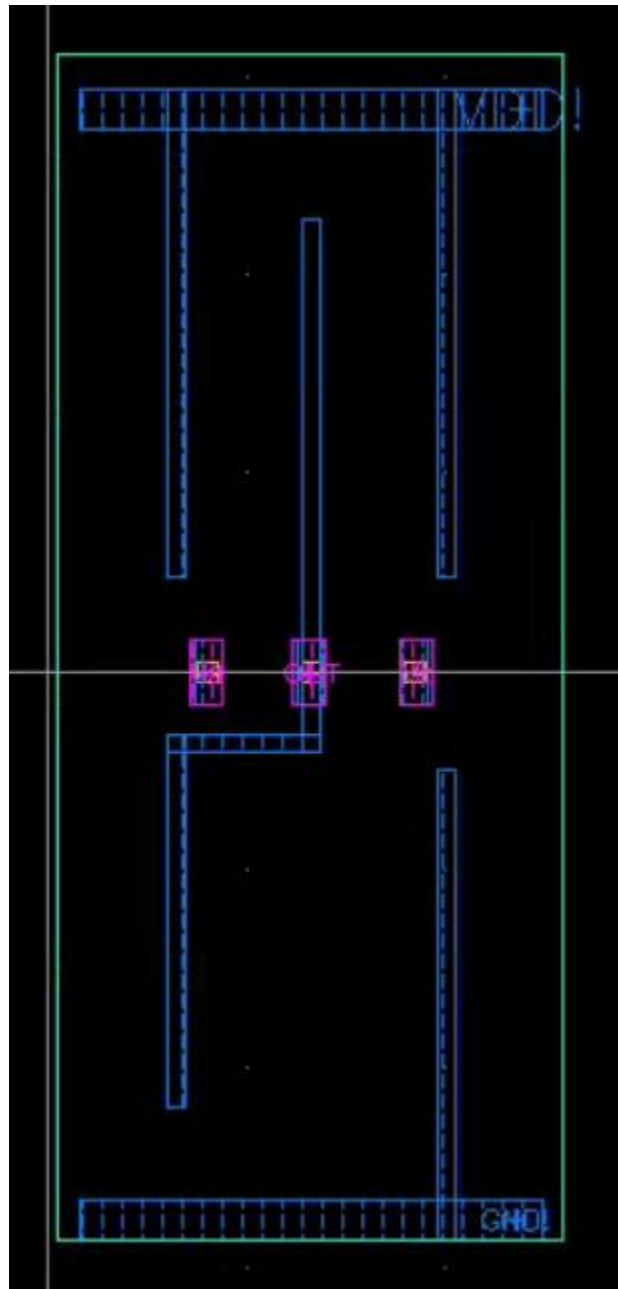


Figure Abstract View

**Pitch:**



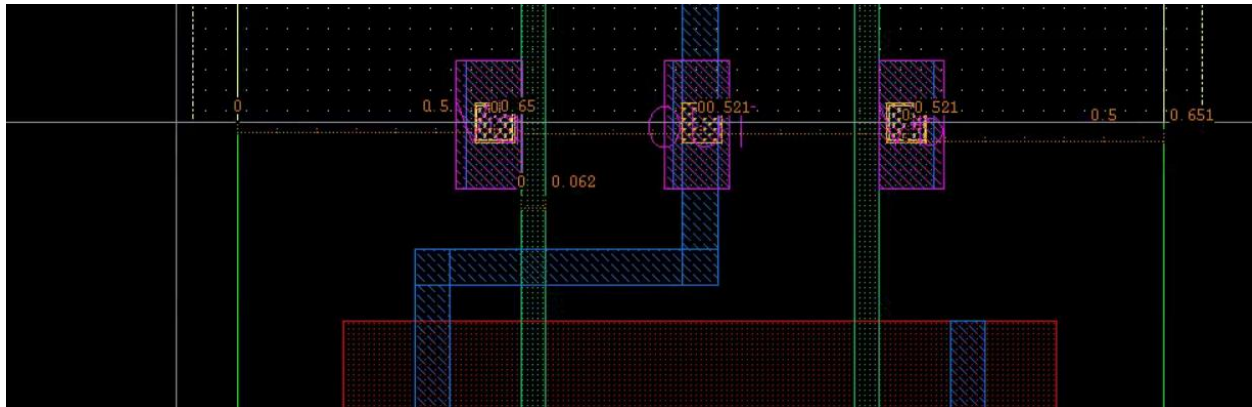


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

### Boolean Table

NAND2		
VA	VB	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Table showing the expected NAND2 behavior

### Waveform view:

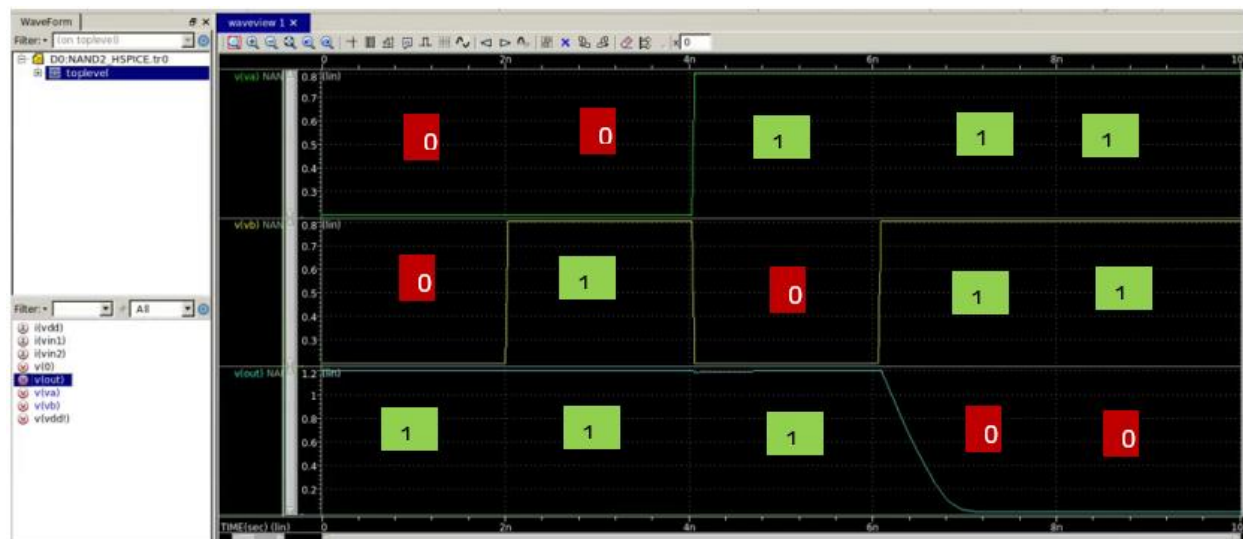


Figure waveform of Input Vs OUT for NAND2

**NAND3 Cell:**

**Layout:**

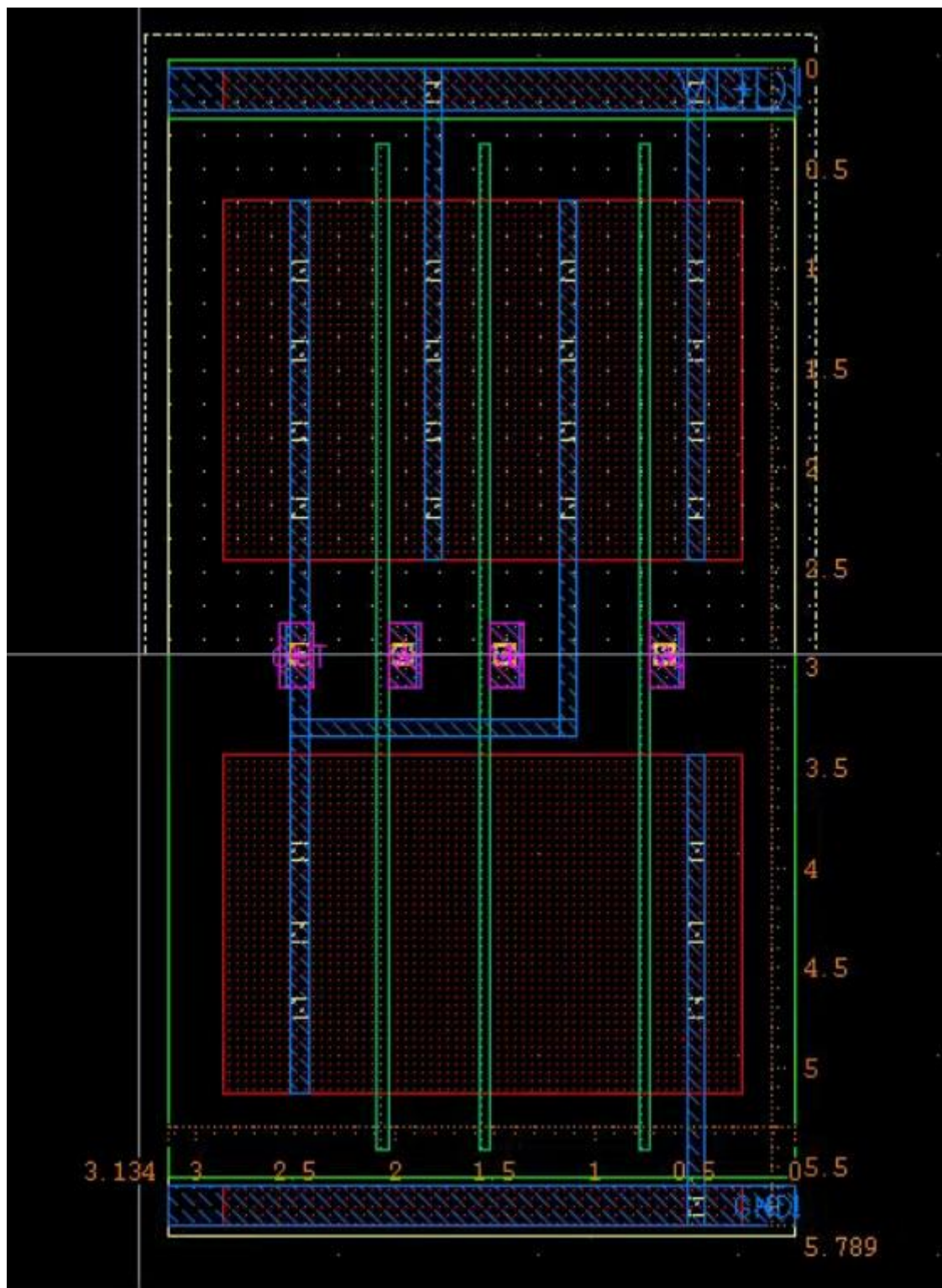


Figure NAND3 layout with size = [5.789um X 3.134um]

**Abstract View:**

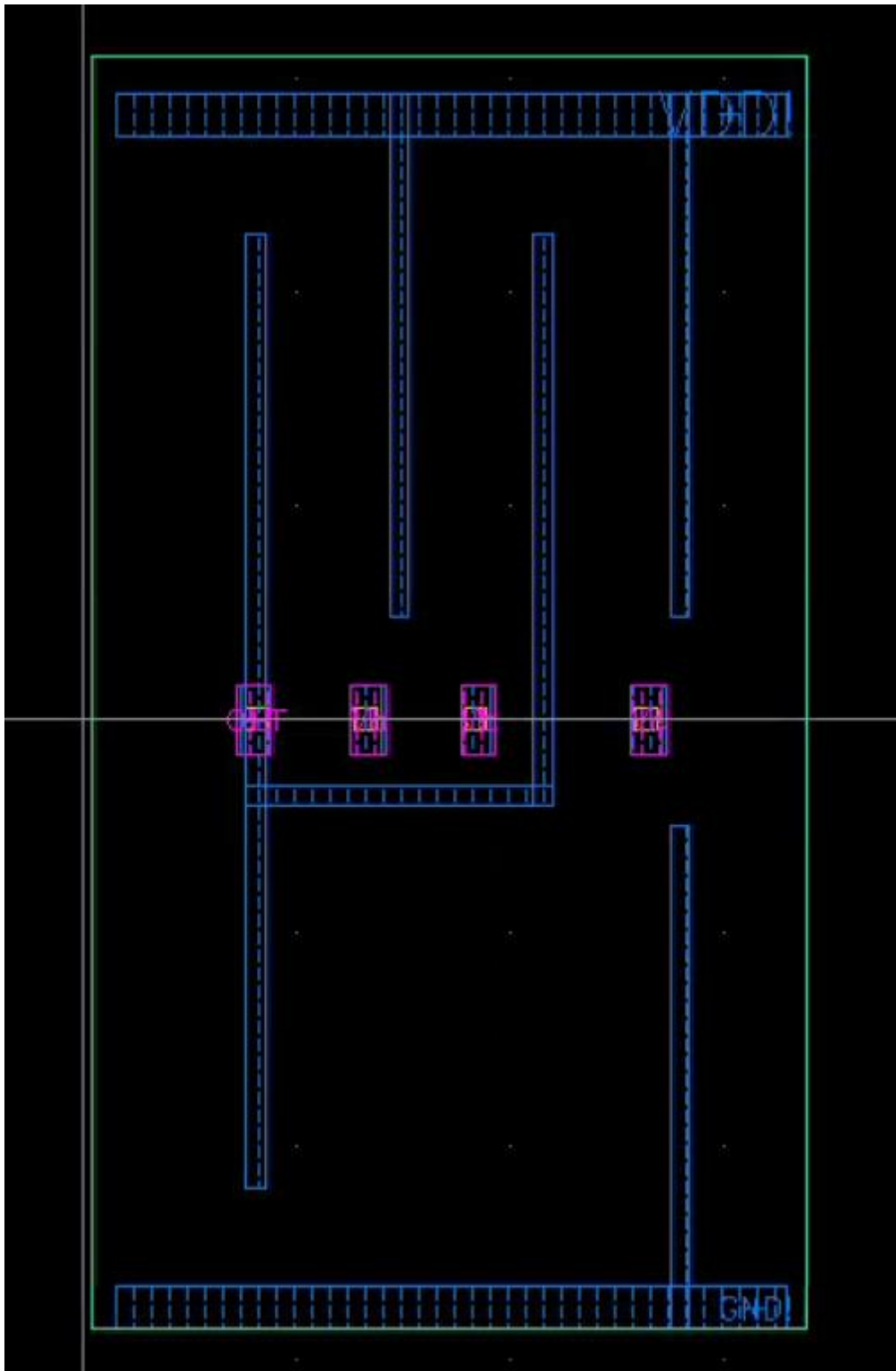


Figure Abstract View

Pitch:

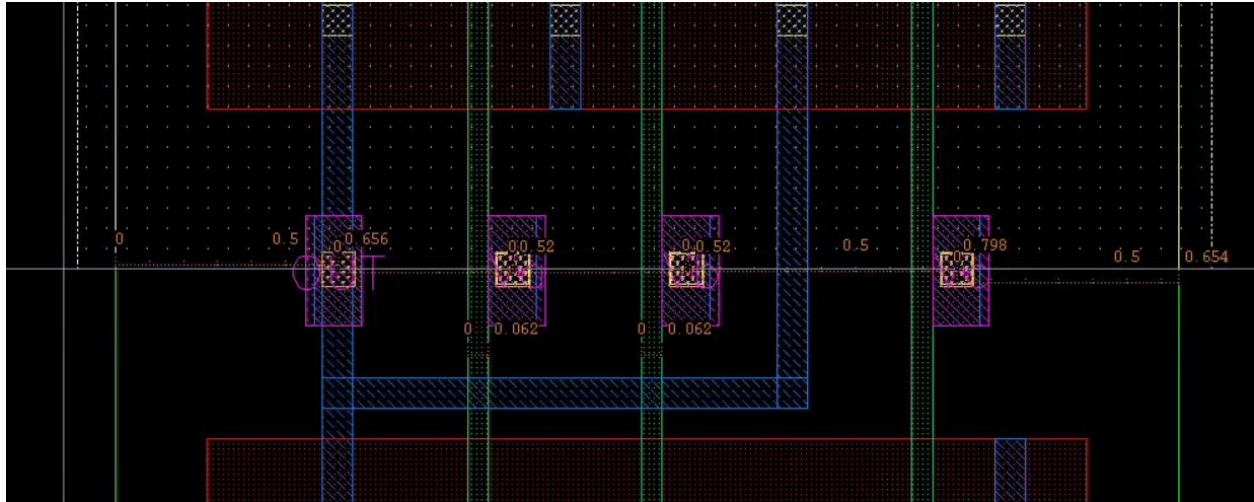


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

#### Boolean Table:

NAND3			
VA	VB	VC	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table showing the expected NAND3 behavior

#### Waveform view:

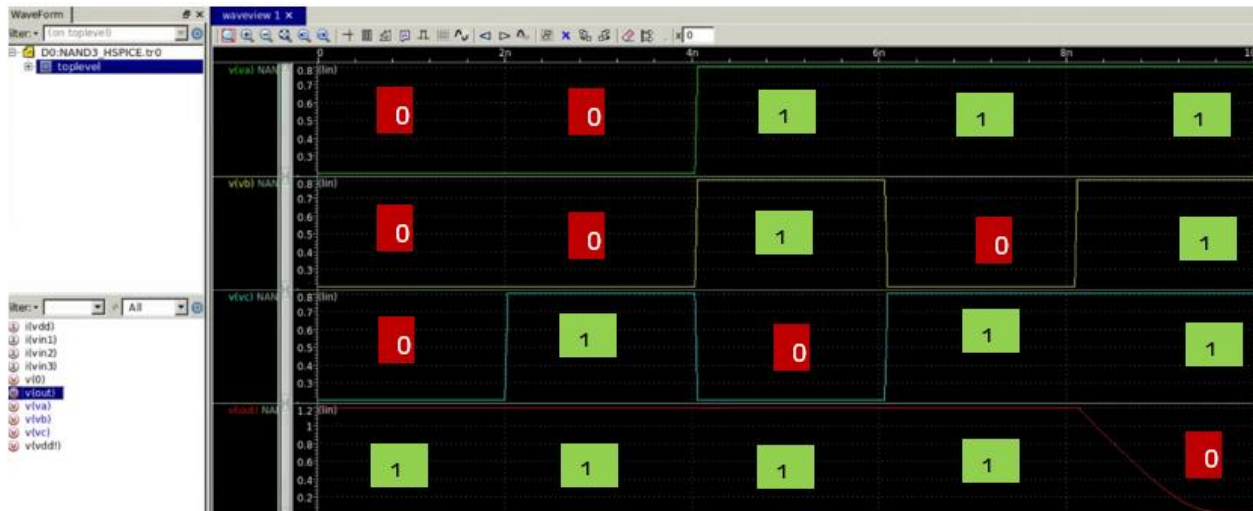


Figure waveform of Input Vs OUT for NAND3

**NAND4 Cell:**

**Layout:**



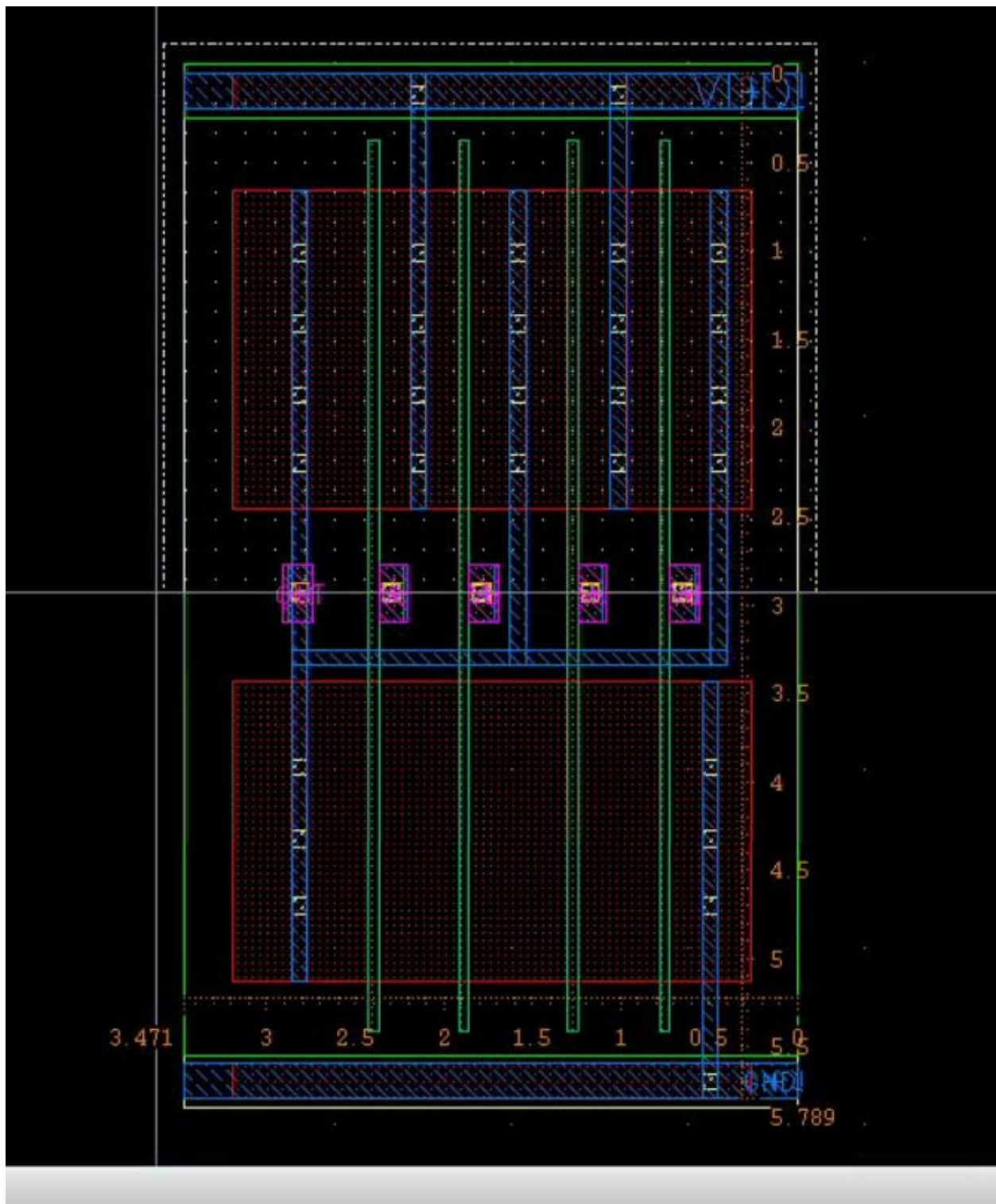


Figure NAND4 layout with size = [5.789um X 3.471um]

**Abstract View:**

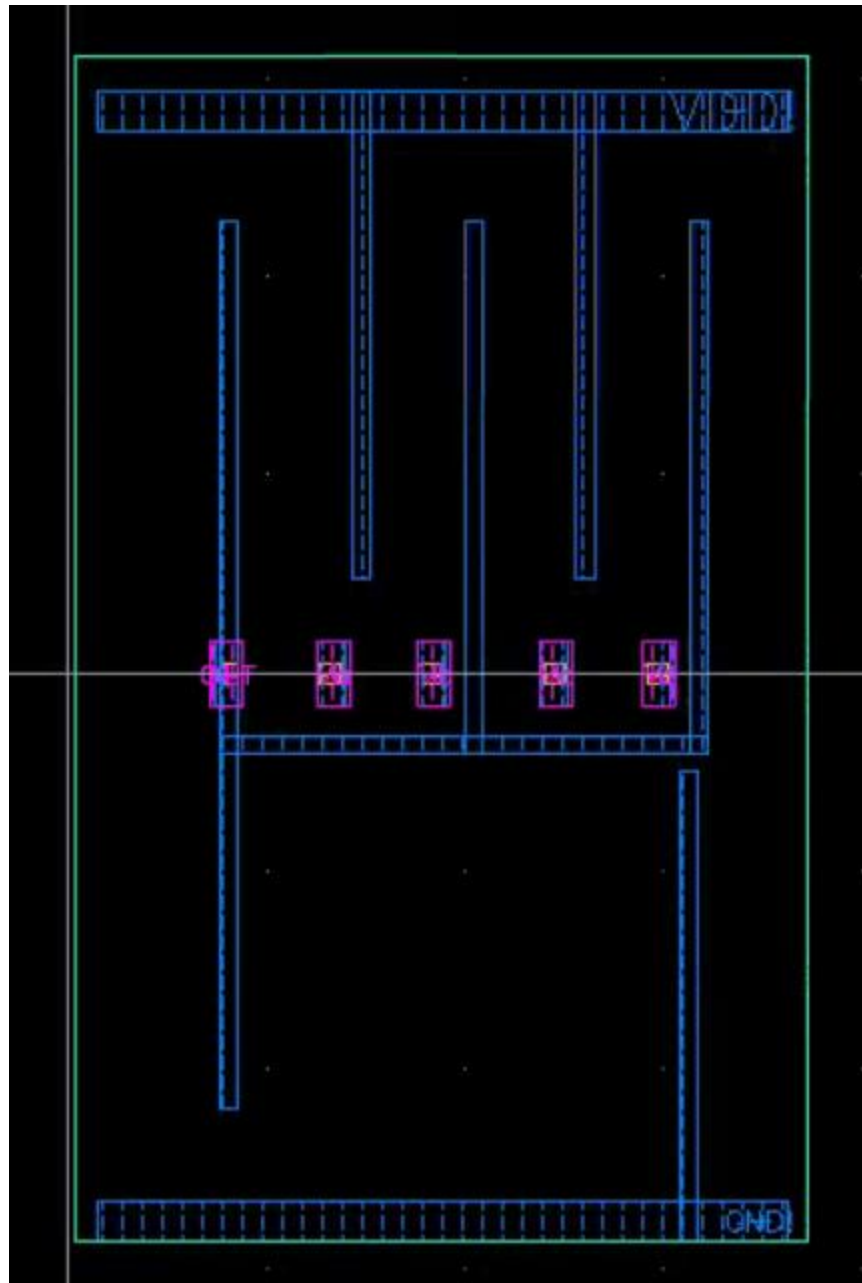


Figure Abstract View

Pitch:



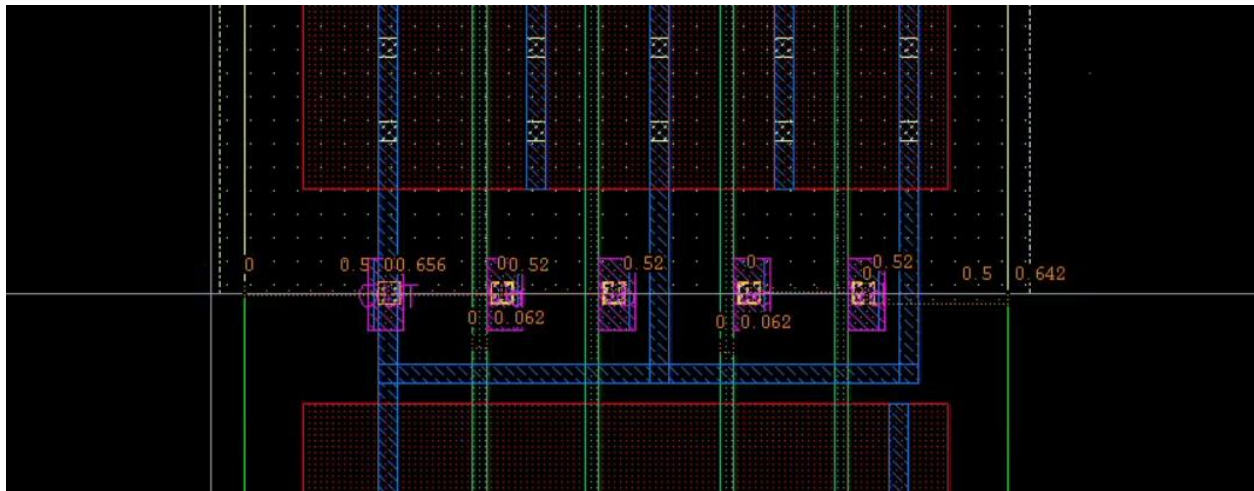


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

### Boolean Table:

NAND4				
VA	VB	VC	VD	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Table showing the expected NAND4 behavior

### Waveform view:

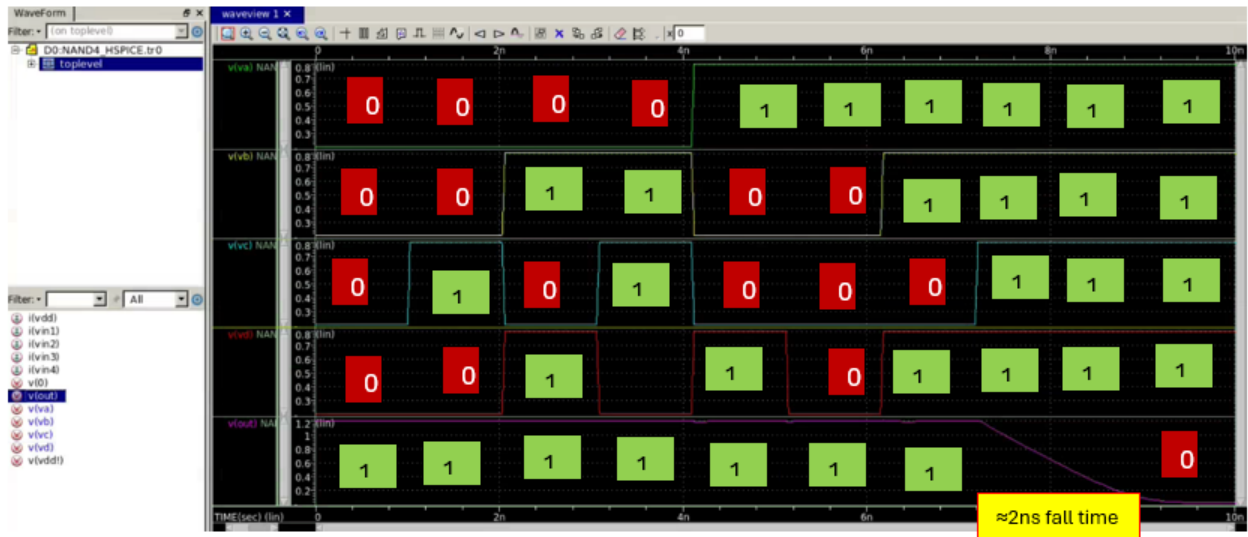


Figure waveform of Input Vs OUT for NAND4

**AOI12 Cell:**

**Layout:**

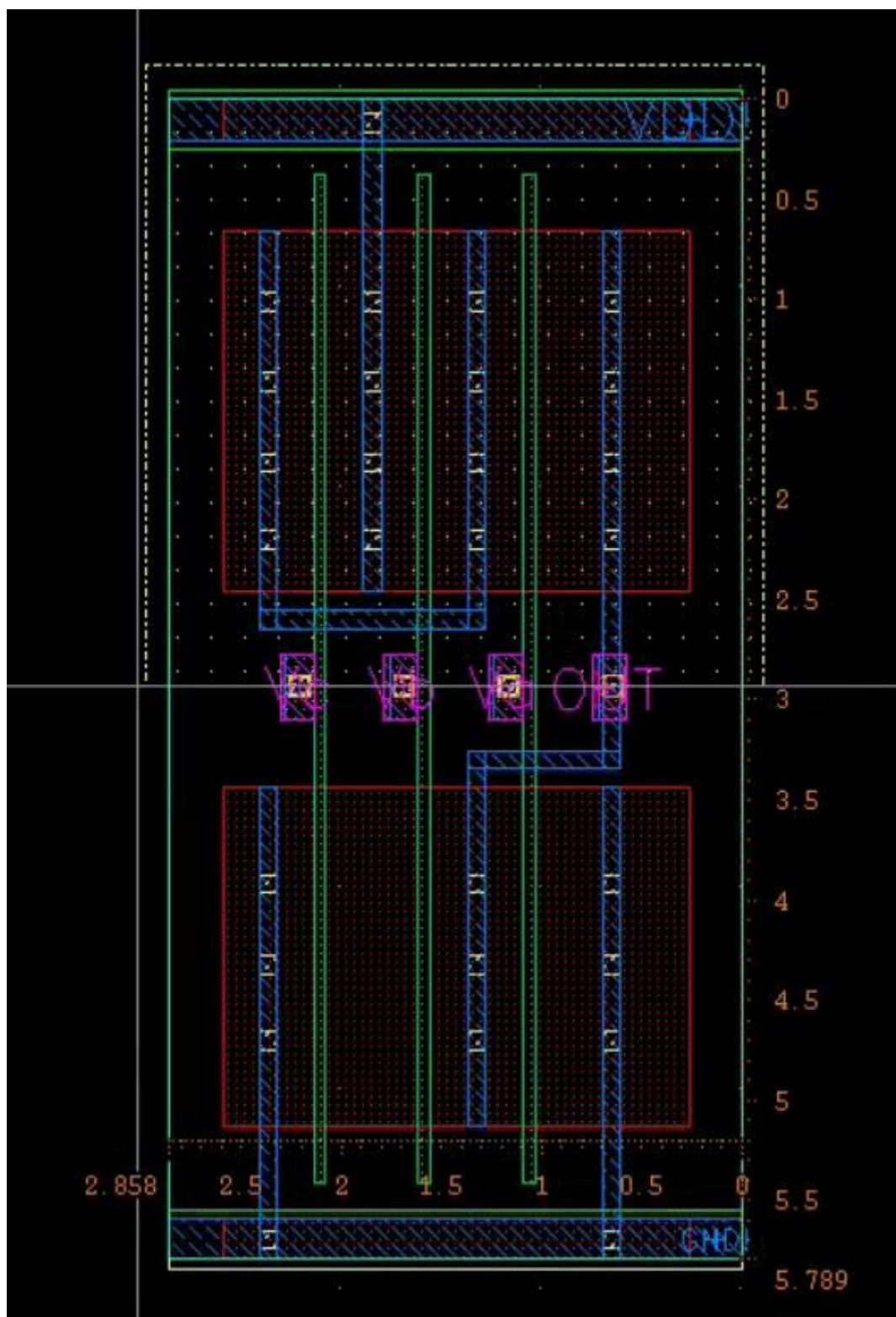


Figure AOI12 layout with size = [5.789um X 2.858um]

**Abstract View:**

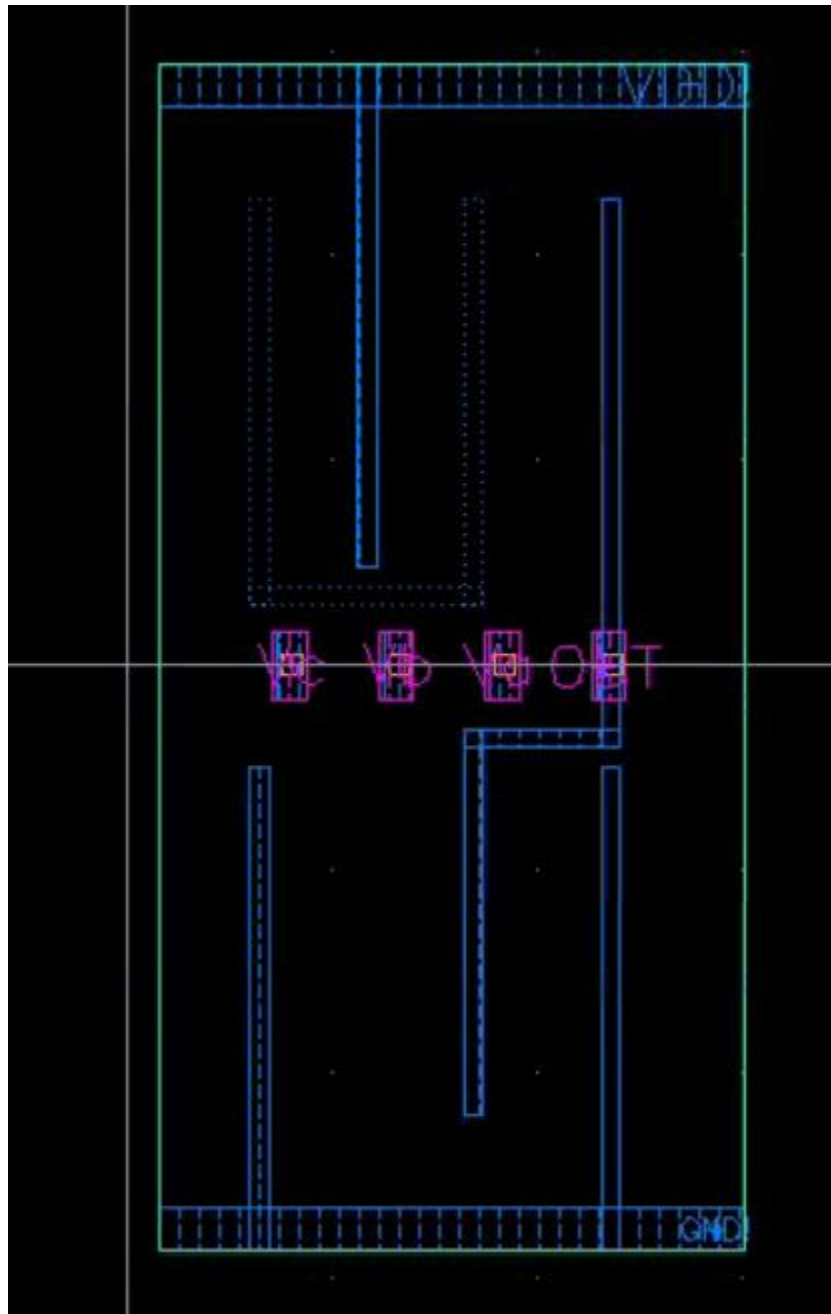


Figure Abstract View

**Pitch:**

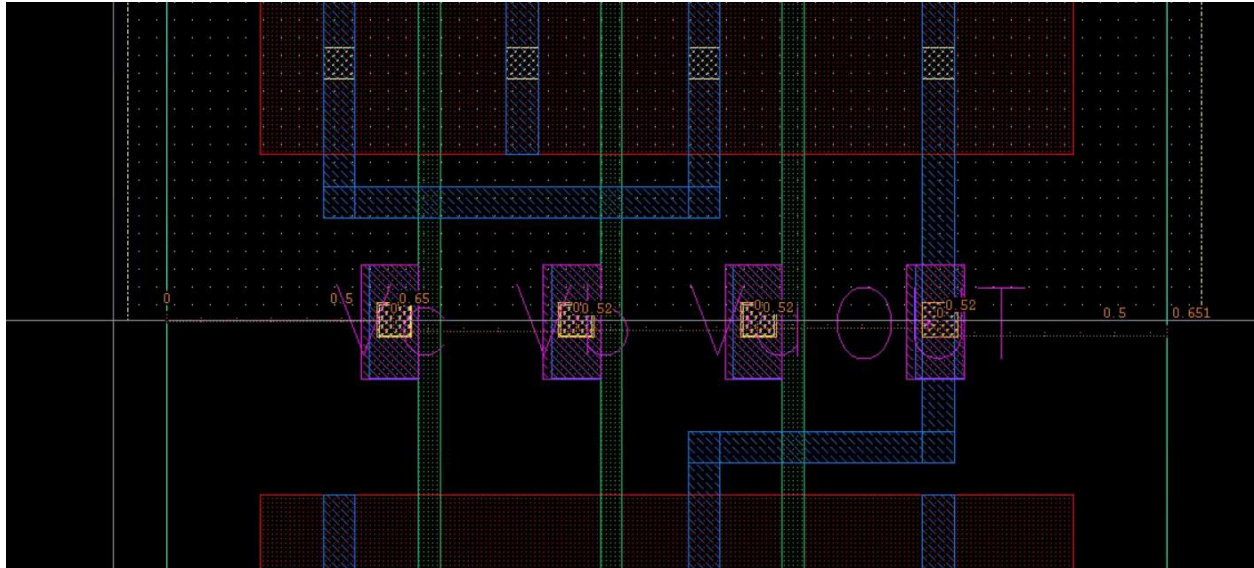


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

#### Boolean Table:

AOI12 = $\sim[(a+b).c]$			
VA	VB	VC	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Table showing the expected AOI12 behavior

#### Waveform view:

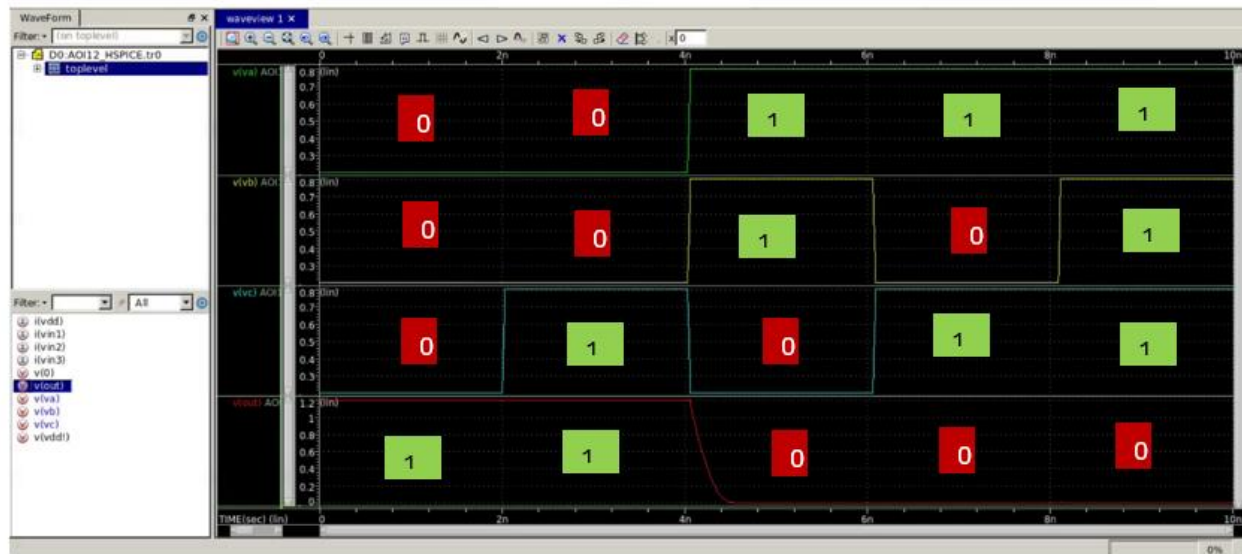


Figure waveform of Input Vs OUT for AOI12

**AOI22 Cell:**

**Layout:**



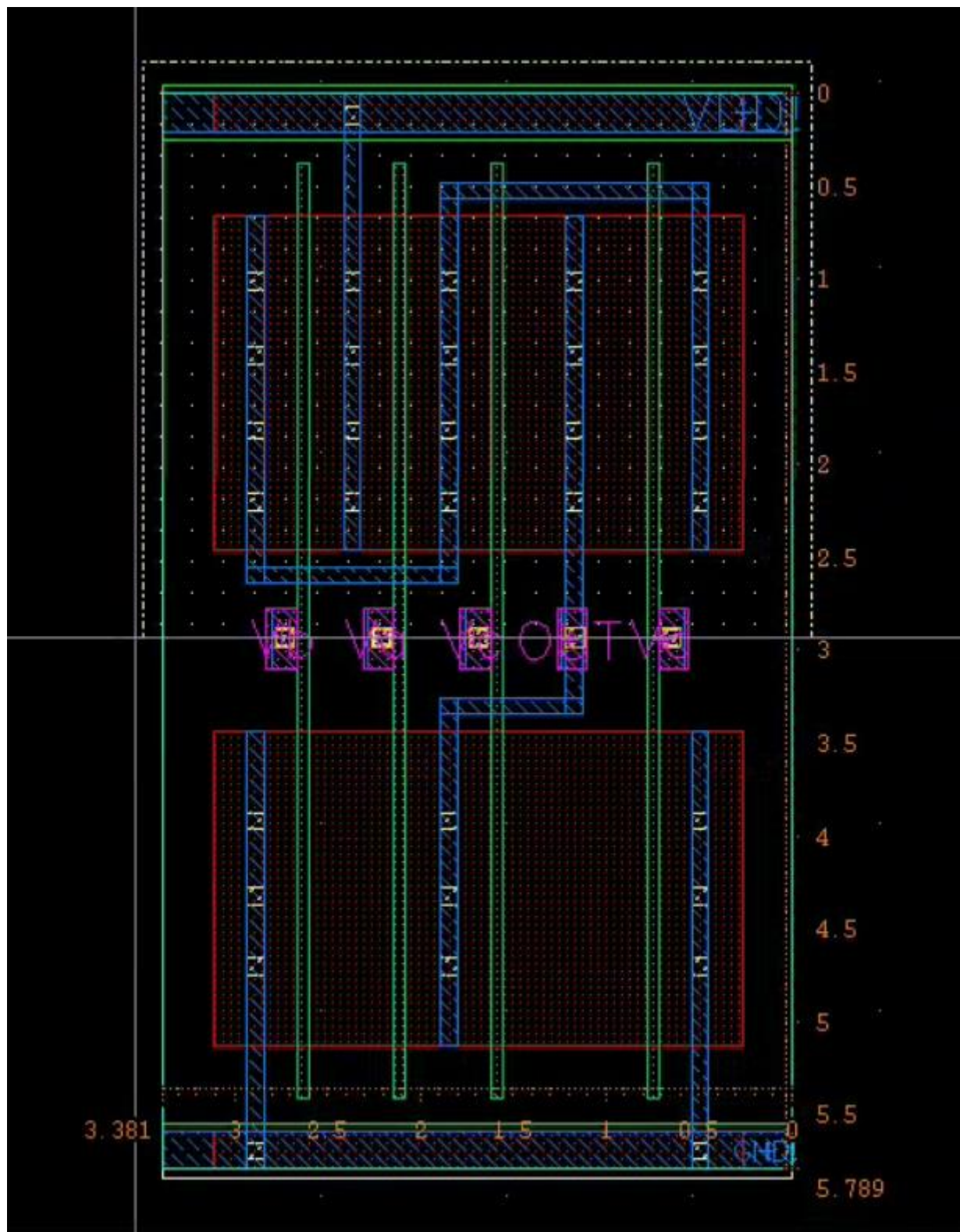


Figure AOI22 layout with size = [5.789um X 3.381um]

**Abstract View:**

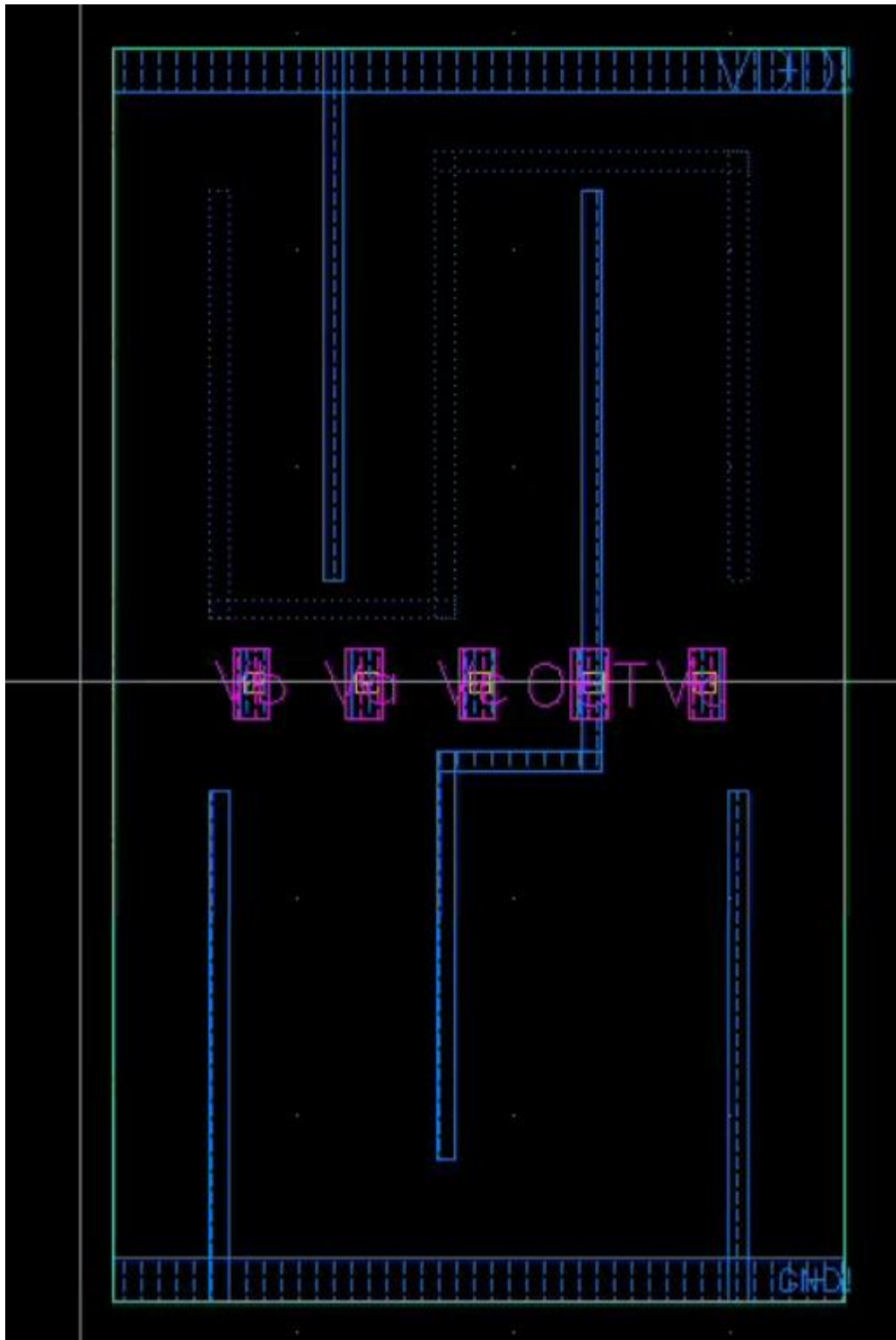


Figure Abstract View



**Pitch:**

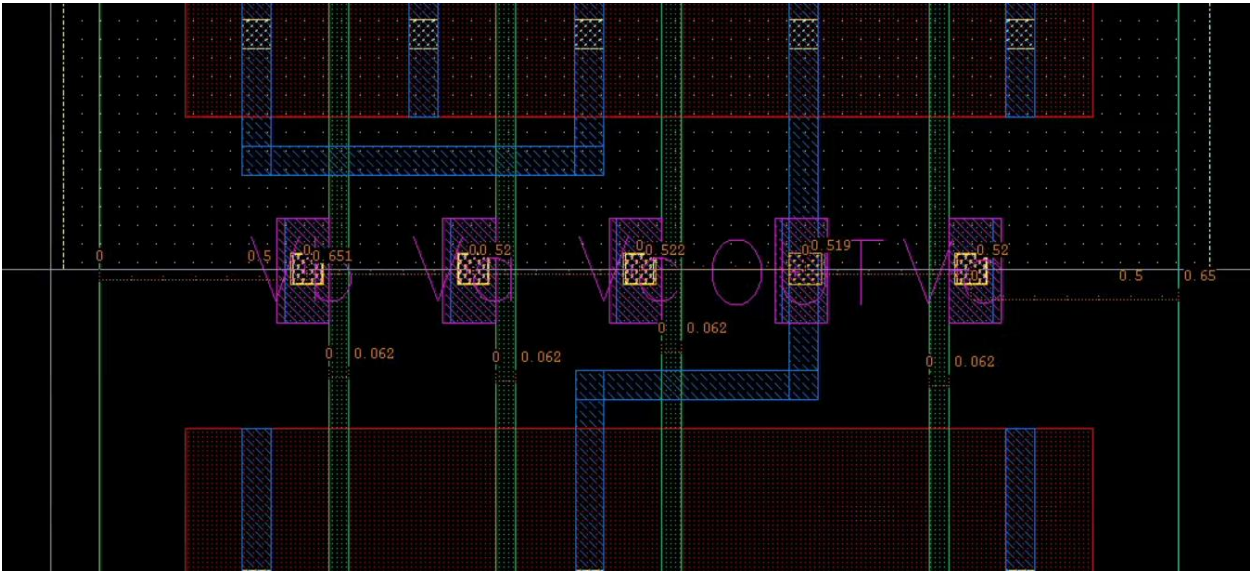


Figure showing Length of 0.062μm, Pitch of 0.52μm and offset of 0.65μm

**Boolean Table:**

AOI22 = ~(a.b + c.d)				
VA	VB	VC	VD	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Table showing the expected AOI22 behavior

**Waveform view:**

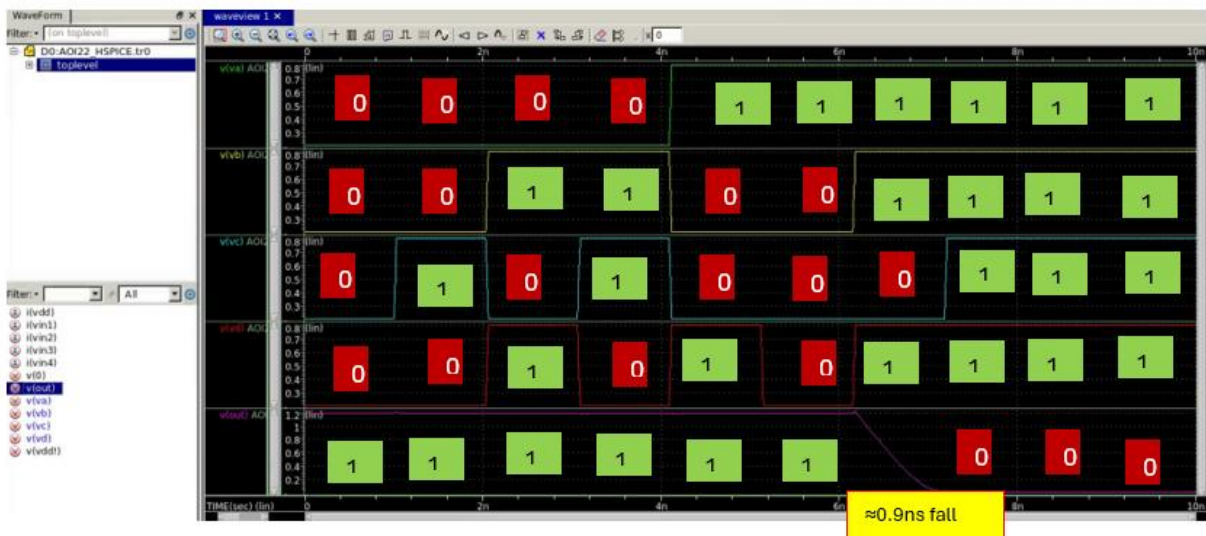


Figure waveform of Input Vs OUT for AOI22

**OAI12 Cell:**

**Layout:**

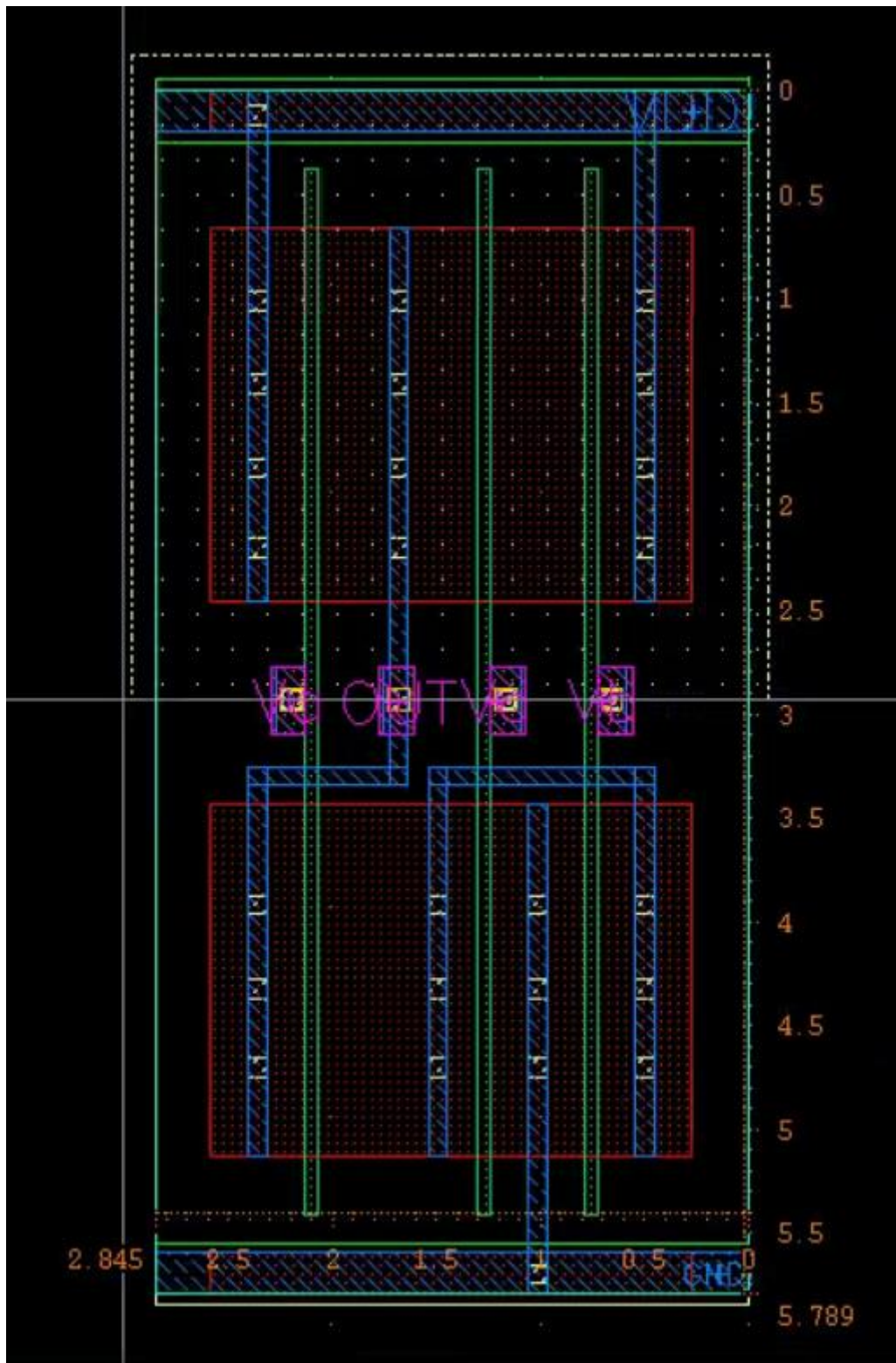


Figure OAI12 layout with size = [5.789um X 2.845um]

**Abstract View:**

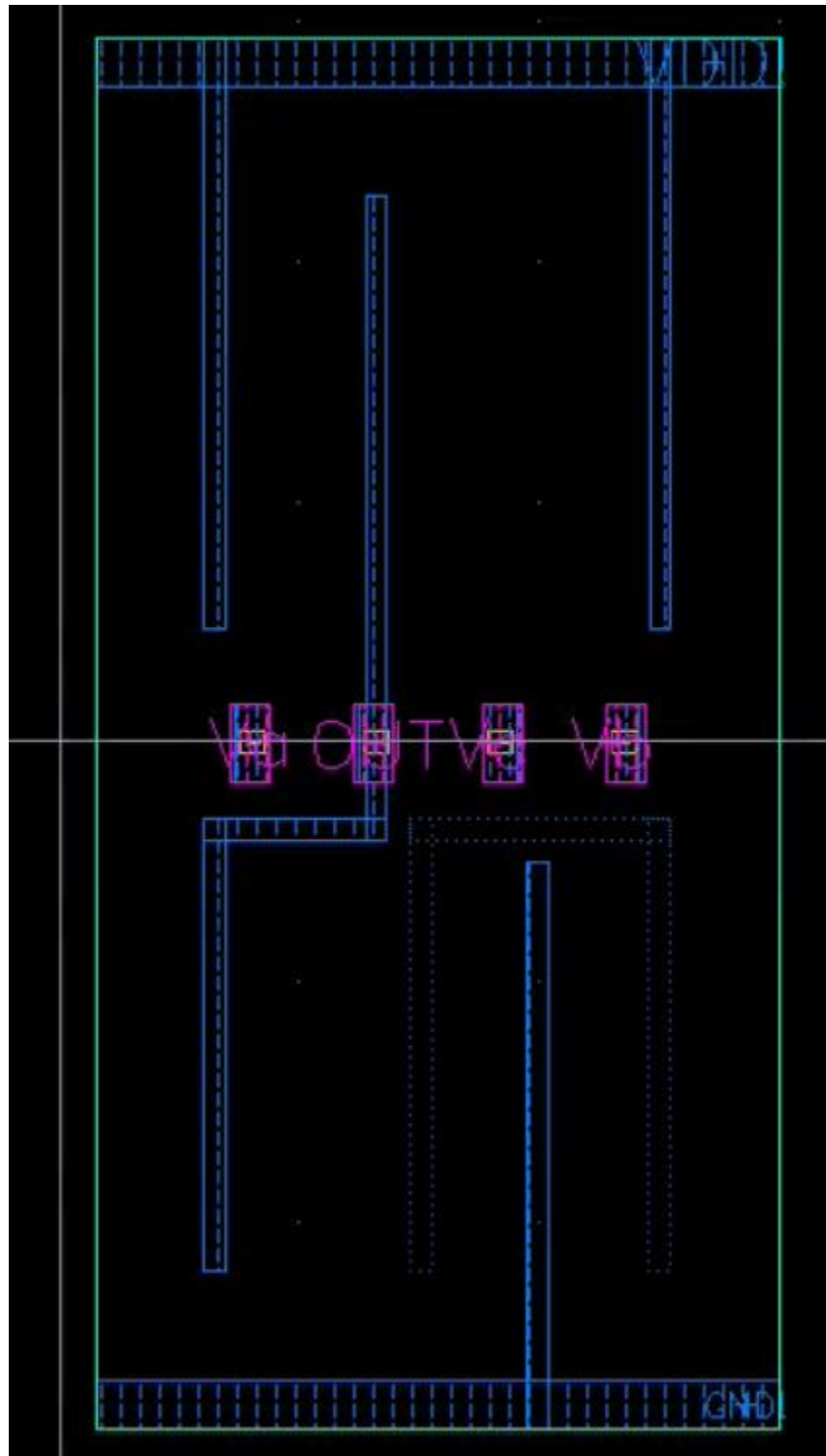


Figure Abstract View

### Pitch:

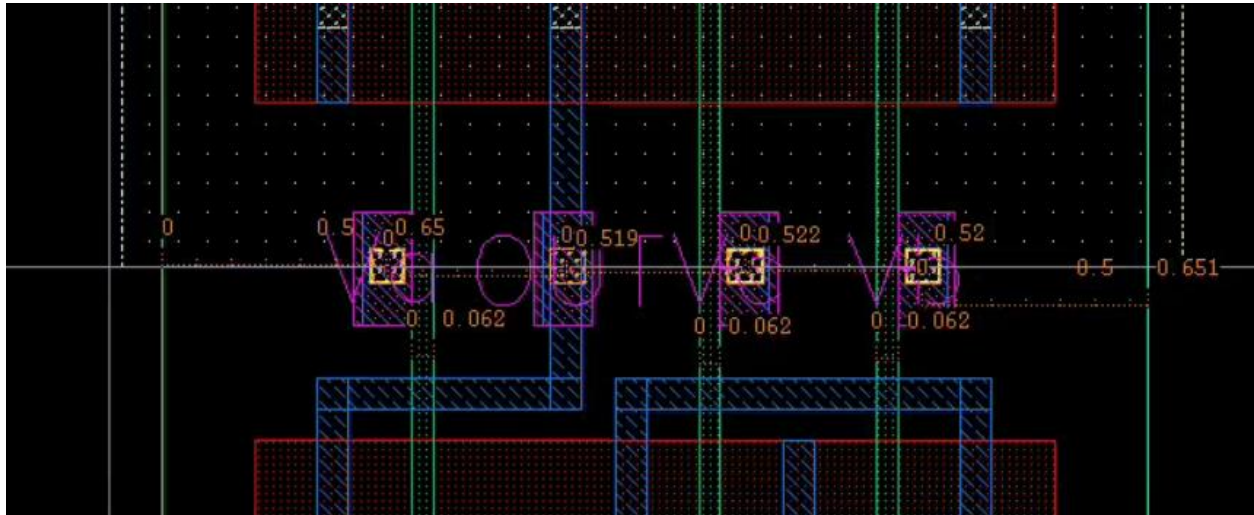


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

### Boolean Table:

OAI12 = $\sim(a.(b+c))$			
VA	VB	VC	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Table showing the expected OAI12 behavior

### Waveform view:

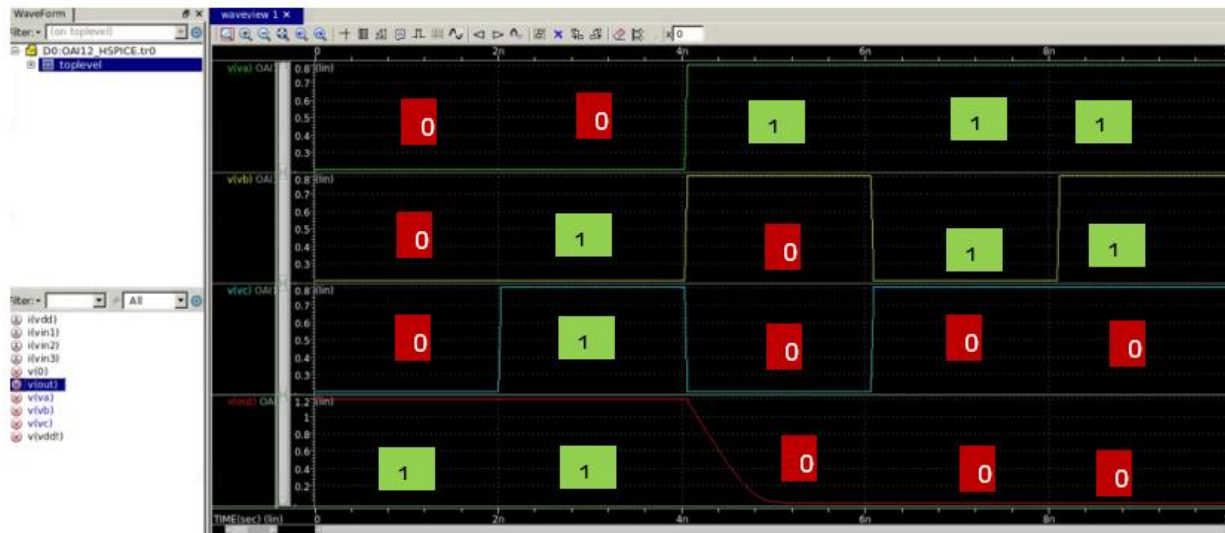


Figure waveform of Input Vs OUT for OAI12

**OAI22 Cell:**

**Layout:**



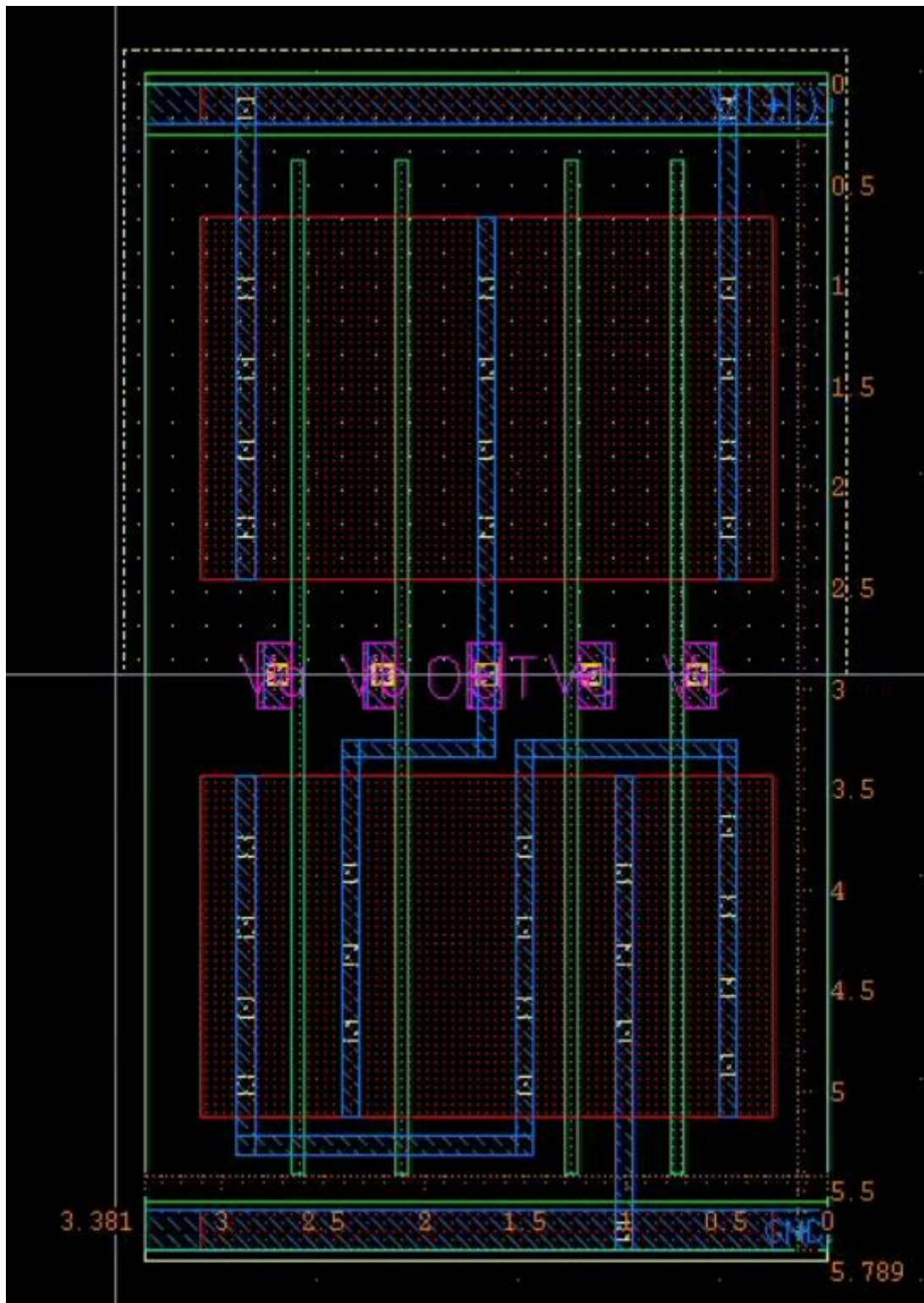


Figure OAI22 layout with size = [5.789um X 3.381um]

**Abstract View:**

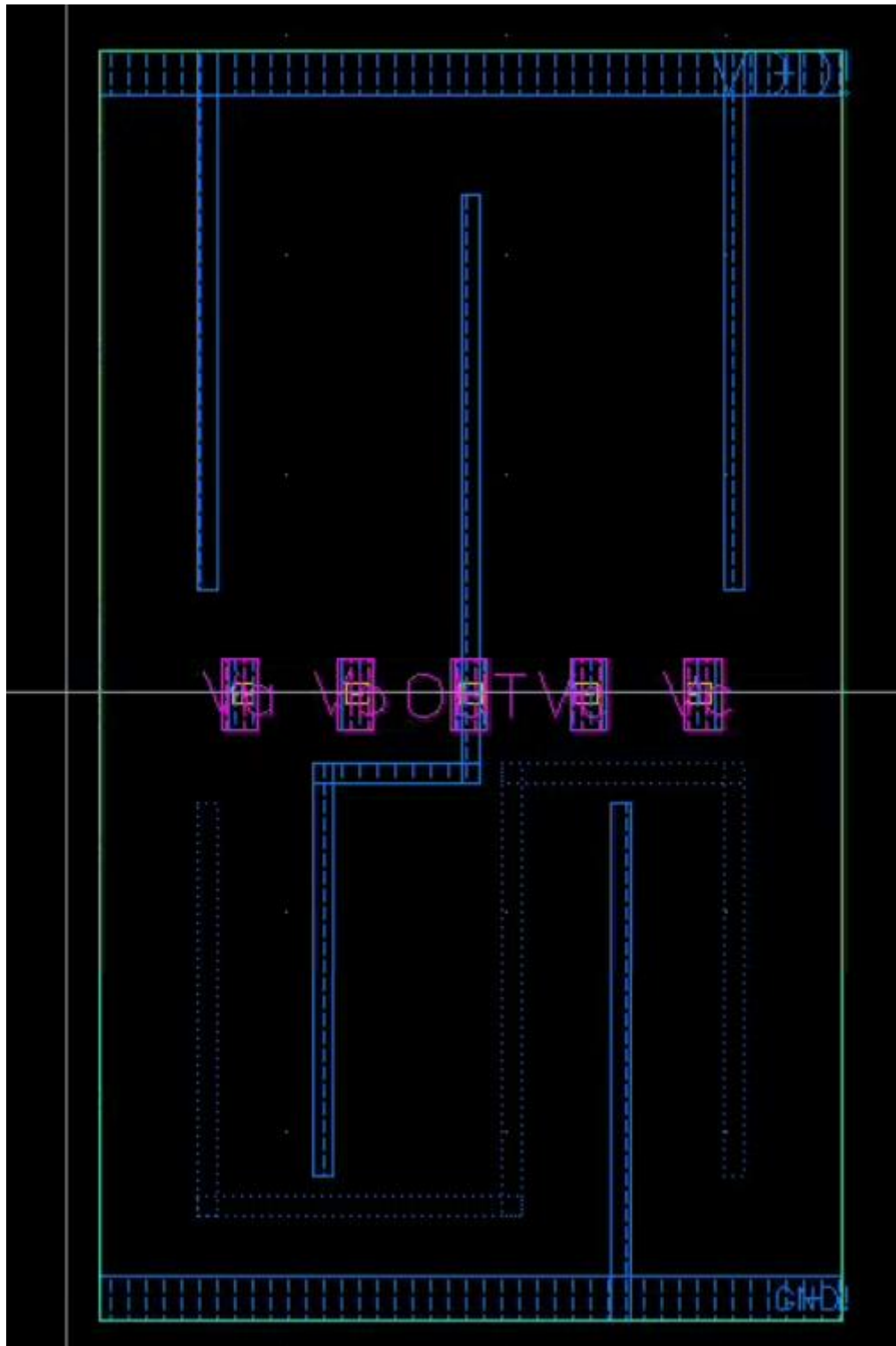


Figure Abstract View

Pitch:



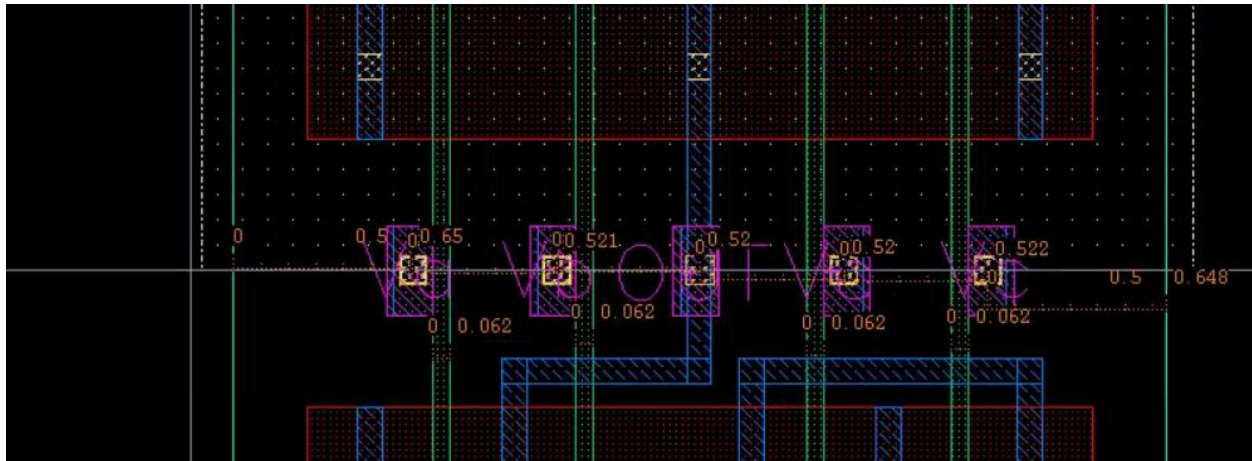


Figure showing Length of 0.062um, Pitch of 0.52um and offset of 0.65um

### Boolean Table:

AOI22 = $\sim((a+b) \cdot (c+d))$				
VA	VB	VC	VD	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Table showing the expected OAI22 behavior

### Waveform view:

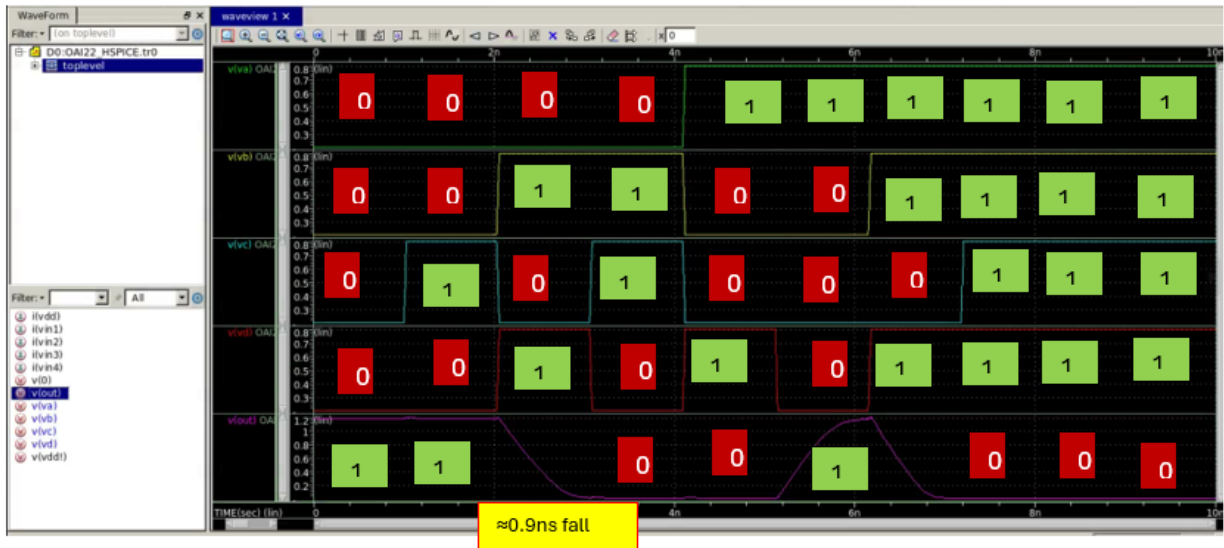


Figure waveform of Input Vs OUT for OAI22

**Combined Cell:**

**Layout:**

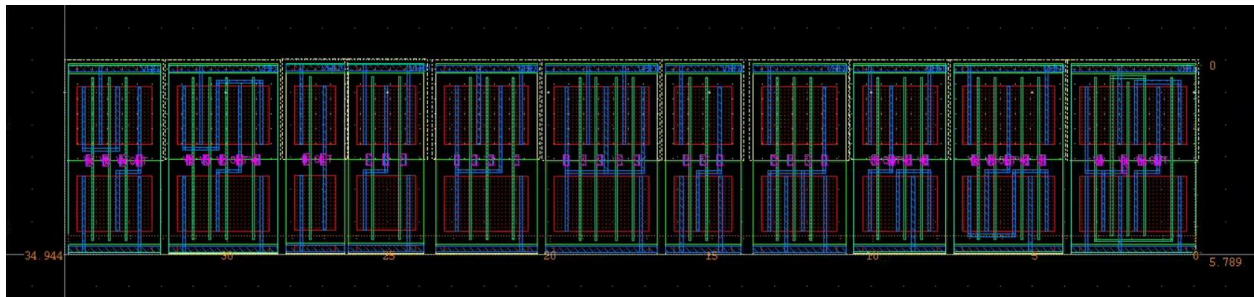
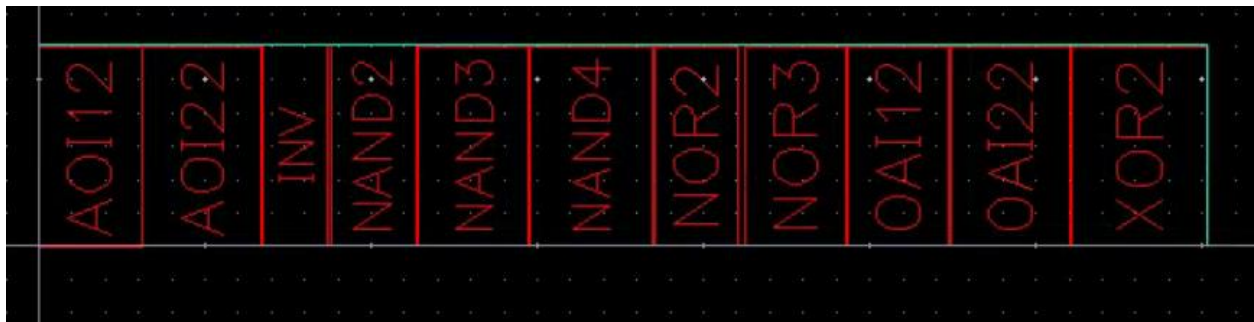
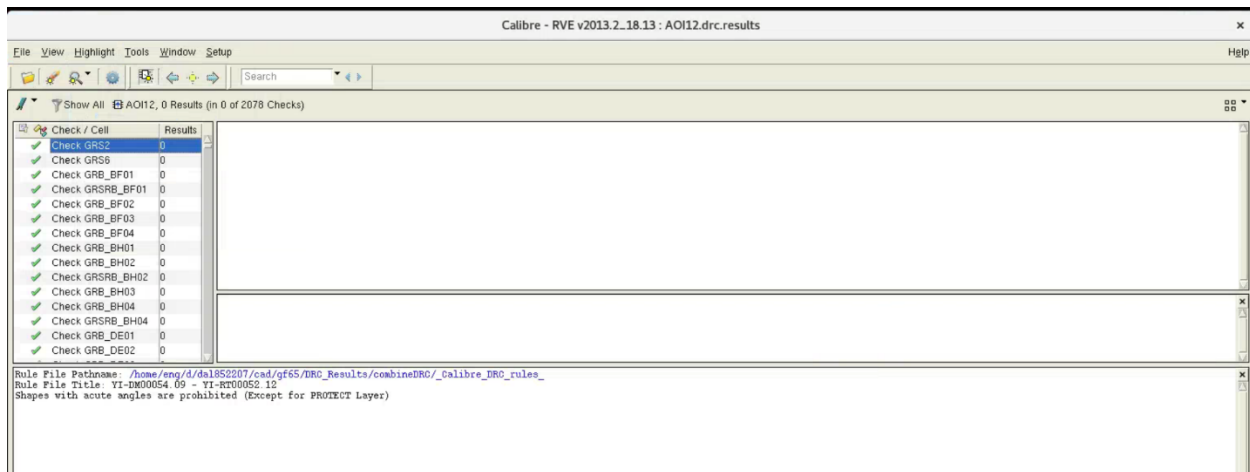


Figure Combined Cell layout with size = [5.789um X 34.944um]

**Cell Alignment:**



**DRC Result:**



## Abstract Generation:

The final library was loaded into abstract View generation tool to extract the abstract view s from each cell using the layout, Pin, extract, and Abstract. This added extra views to each cell.

