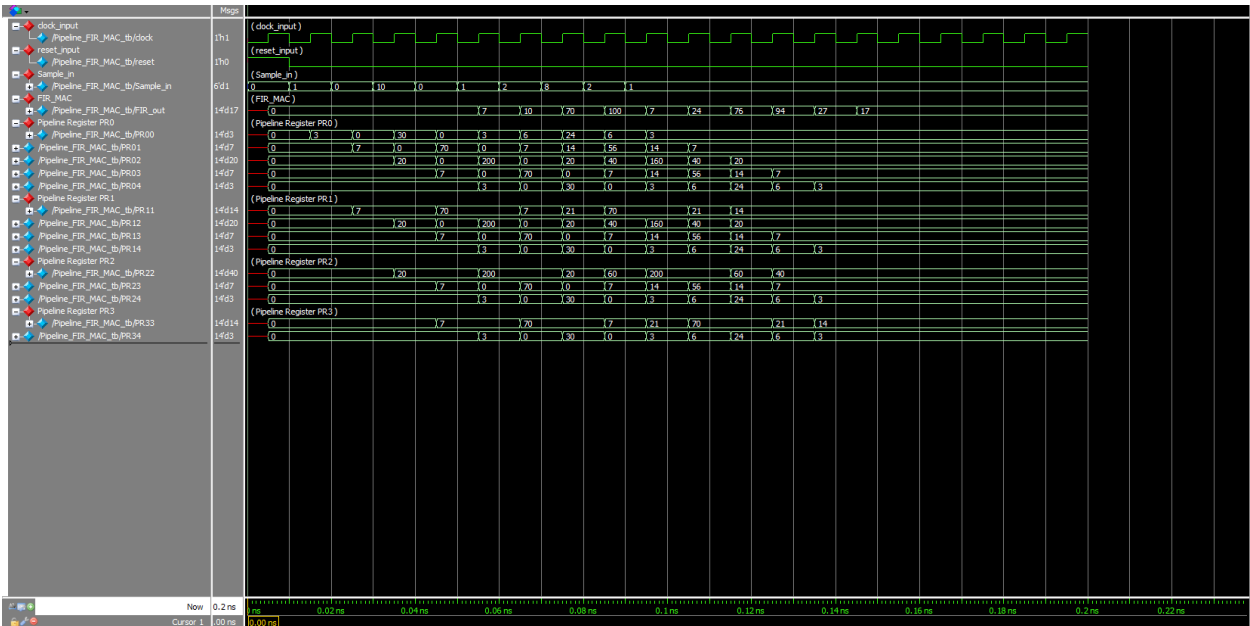


Bitwave



Testbench results from the text file

Time	Sample_in	FIR_out
10	0	0
20	1	0
30	0	0
40	10	0
50	0	0
60	1	7
70	2	10
80	8	70
90	2	100
100	1	7

## Timing Analysis for the clock signal

@ default time when clock period is 1ns

The screenshot shows the Quartus Prime IDE with the Timing Analyzer results for the clock signal. The Project Navigator on the left lists the files: `Controller/Pipeline_FIR_Controller.v`, `DataPath/Pipeline_FIR_DataPath.v`, `Pipeline_FIR_MAC.v`, and `Pipeline_FIR_MAC_tb.v`. The Table of Contents in the center lists the analysis steps: Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, Flow Log, Analysis & Synthesis, Fitter, Assembler, Timing Analyzer (Summary, Parallel Compilation, Clocks), Slow 1100mV 85C Model, Slow 1100mV OC Model, Fast 1100mV 85C Model, Fast 1100mV OC Model, Multicorner Timing Analysis, and Advanced I/O Timing.

The Messages window at the bottom displays the following information:

- 332146 worst-case minimum pulse width slack is -0.080
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: `quartus_eda --read_settings_files=off --write_settings_files=off Pipeline_FIR_MAC -c Pipeline_FIR_MAC`
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment `NUM_PARALLEL_PROCESSORS` in your QSF to an appropriate value
- 204019 Generated File `Pipeline_FIR_MAC.vo` in folder `"C:/Users/lmjn/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/FINAL PROJECT/FIR_MAC/simulation"`
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings

The status bar at the bottom indicates the system is processing 126 items, with a progress of 100% and a time of 00:02:01.

## Time report at a slack of -1.790

The screenshot shows the Quartus Prime IDE with the Timing Analyzer results for the clock signal at a slack of -1.790. The Set Operating Conditions window on the left shows the selected model: Slow 1100mV 85C Model. The Command Info window in the center displays the command: `quartus_eda --read_settings_files=off --write_settings_files=off Pipeline_FIR_MAC -c Pipeline_FIR_MAC`.

The Path Summary window on the right shows the results for the clock signal. The Path Summary table lists the following data:

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
-1.790	Pipeline_F_rray3[0]	Pipel_3[8]	clock	clock	1.000	-0.074	2.546
-1.786	Pipeline_F_rray3[2]	Pipel_3[8]	clock	clock	1.000	-0.078	2.538
-1.729	Pipeline_F_rray3[0]	Pipel_3[8]	clock	clock	1.000	-0.074	2.485
-1.716	Pipeline_F_rray3[3]	Pipel_3[8]	clock	clock	1.000	-0.073	2.473
-1.692	Pipeline_F_rray3[0]	Pipel_3[9]	clock	clock	1.000	-0.069	2.453
-1.690	Pipeline_F_rray3[2]	Pipel_3[9]	clock	clock	1.000	-0.073	2.447
-1.668	Pipeline_F_rray3[0]	Pipel_3[6]	clock	clock	1.000	-0.071	2.427

The Path Summary window also displays the Data Arrival Path and Data Required Path. The Data Arrival Path table lists the following data:

Total	Incr	RF	Type	Fanout	Location	Element
0.000	0.000					launch edge time
4.097	4.097					clock path
0.000	0.000					source latency
0.000	0.000	RR	IC	1	IOIBUF_X89_Y25_N21	clock-input[1]
0.650	0.650	RR	CELL	1	IOIBUF_X89_Y25_N21	clock-input[0]

The Data Required Path table lists the following data:

Total	Incr	RF	Type	Fanout	Location	Element
1.000	1.000					latch edge time
5.023	4.023					clock path
1.000	0.000					source latency
1.000	0.000					clock
1.000	0.000	RR	IC	1	IOIBUF_X89_Y25_N21	clock-input[1]
1.650	0.650	RR	CELL	1	IOIBUF_X89_Y25_N21	clock-input[0]

The Path Summary window also displays the Waveform and Extra Filter Information. The Waveform shows the clock signal and the data path. The Extra Filter Information shows the clock signal and the data path.

The Console window at the bottom displays the following command:

```
report_timing -from_clock { clock } -to_clock { clock } -setup -npaths 10 -detail full_path -panel_name {Setup: clock} -multi_corner
```

The Console window also displays the following output:

```
Report Timing: Found 10 setup paths (10 violated). Worst case slack is -1.790
```

@ default time when clock period is 4ns

Quartus Prime IDE - C:/Users/Imnjm/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/FINAL PROJECT/FIR\_MAC/Pipeline\_FIR\_MAC - Pipeline\_FIR\_MAC

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator Files

Files

- Pipeline\_FIR\_MACOut.sdc
- Controller/Pipeline\_FIR\_Controller.v
- DataPath/Pipeline\_FIR\_DataPath.v
- Pipeline\_FIR\_MAC.v
- Pipeline\_FIR\_MAC\_tb.v

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Filter
- Assembler
- Timing Analyzer
  - Summary
  - Parallel Compilation
  - SDC File List
  - Clocks
    - Slow 1100mV 85C Model
    - Slow 1100mV OC Model
    - Fast 1100mV 85C Model
    - Fast 1100mV OC Model
  - Multiplatform Timing Analysis

Messages

Type ID Message

- 332146 worst-case minimum pulse width slack is 1.420
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 1 warning
- Running Quartus Prime EDA Netlist Writer
- Command: quartus\_eda --read\_settings\_files=off --write\_settings\_files=off Pipeline\_FIR\_MAC -c Pipeline\_FIR\_MAC
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value
- 204019 Generated File Pipeline\_FIR\_MAC.vo in folder "C:/Users/Imnjm/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/FINAL PROJECT/FIR\_MAC/simulation"
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 8 warnings

System (6) Processing (118)

100% 00:01:35

Time report at a slack of 1.096

Timing Analyzer - C:/Users/Imnjm/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/FINAL PROJECT/FIR\_MAC/Pipeline\_FIR\_MAC - Pipeline\_FIR\_MAC

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Set Operating Conditions

Slow 1100mV 85C Model

Command Info

Summary of Paths

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1.096	Pipeline_F_array[3][1]	Pipel_3[8]	clock	clock	4.000	-0.080	2.654
1.108	Pipeline_F_array[3][2]	Pipel_3[8]	clock	clock	4.000	-0.074	2.648
1.111	Pipeline_F_array[3][0]	Pipel_3[8]	clock	clock	4.000	-0.074	2.645
1.131	Pipeline_F_array[3][3]	Pipel_3[8]	clock	clock	4.000	-0.079	2.620
1.136	Pipeline_F_array[3][2]	Pipel_3[8]	clock	clock	4.000	-0.074	2.620
1.138	Pipeline_F_array[3][0]	Pipel_3[8]	clock	clock	4.000	-0.074	2.618
1.148	Pipeline_F_array[3][1]	Pipel_3[8]	clock	clock	4.000	-0.080	2.602

Path #1: Setup slack is 1.096

Path Summary Statistics Data Path Waveform Extra Filter Information

Data Arrival Path

Total	Incr	RF	Type	Fanout	Location	Element
0.000	0.000					launch edge time
4.104	4.104					clock path
0.000	0.000					source latency
0.000	0.000					clock
0.000	0.000	RR	IC	1	IOIBUF_X89_Y25_N21	clock-input[1]
0.650	0.650	RR	CELL	1	IOIBUF_X89_Y25_N21	clock-input[0]

Data Required Path

Total	Incr	RF	Type	Fanout	Location	Element
4.000	4.000					latch edge time
8.024	4.024					clock path
4.000	0.000					source latency
4.000	0.000					clock
4.000	0.000	RR	IC	1	IOIBUF_X89_Y25_N21	clock-input[1]
4.650	0.650	RR	CELL	1	IOIBUF_X89_Y25_N21	clock-input[0]

Waveform

Setup Relationship

Latch Clock

Data Arrival

Clock Delay

Data Required

Report Timing -from:clock { clock } -to:clock { clock } -setup -npaths 10 -detail full\_path -panel\_name {Setup: clock} -multi\_corner

Report Timing: Found 10 setup paths (0 violated). Worst case slack is 1.096

Console History

0% 00:00:00 Ready

