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1  /*-----------------------------------------------------------------------------------------
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3  CLass: EE417 Summer 2024
4  Lesson 11 HW Question 2
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: This is a RAM module where write takes priority when a read_or_write
   signal is high
7  -----------------------------------------------------------------------------------------
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8
9  module RAM  #(parameter memory_height = 8,
10               parameter data_width    = 4)
11             (
12              input                                  clock,            //one clock for read
   and write
13              input                                  reset,            //clears memory
14              input         [memory_height -1:0]     address,          //address line
15              input                                  read_or_write,    //enables read or write
16              input         [data_width -1:0]        data_in,          //input data port
17              output  reg   [data_width -1:0]        data_out          //output data port
18              );
19
20 //internal register
21 reg      [data_width -1:0] memory [memory_height -1:0];              // temp register to
   store memory data
22 integer k;
23
24 //Transition logic
25 always   @(posedge clock)
26    if (reset)
27       for (k = 0; k < memory_height; k = k+1)
28          memory[k] <= 4'b0000;               //all address lines in memory are cleared @
   reset high
29    else if (read_or_write)
30          memory[address] <= data_in;      //priority to write if we recieve both read and
   write signal at the same time
31    else if (~read_or_write)
32          data_out    <= memory[address];  // when read_or_write is low data_out=requested
   address line
33 endmodule
```