

State Table				
	next_state		output	
present_state	x_in=0	x_in=1	z1	z2
S_000	S_000	S_001	0	0
S_001	S_001	S_010	0	0
S_010	S_010	S_011	1	0
S_011	S_011	S_100	0	0
S_100	S_100	S_101	0	1
S_101	S_101	S_110	0	0
S_110	S_110	S_111	0	0
S_111	S_111	S_111	0	0

State Table				
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present_state	x_in=0	x_in=1	z1	z2
S_000	S_000	S_001	0	0
S_001	S_001	S_010	1	0
S_010	S_010	S_011	1	0
S_011	S_011	S_100	0	1
S_100	S_100	S_101	0	1
S_101	S_101	S_110	0	0
S_110	S_110	S_111	0	0
S_111	S_111	S_reset	0	0

S_reset: Needs to low for the FSM to start
if input sequence = 010 then z1=1 and z2=0
if input sequence = 100 then z1=0 and z2=1
S_000: 3Bit input sequence=000
S_001: 3Bit input sequence=001 received
S_010: 3Bit input sequence=010 received
S_011: 3Bit input sequence=011 received
S_100: 3Bit input sequence=100 received
S_101: 3Bit input sequence=101 received
S_110: 3Bit input sequence=110 received
S_111: 3Bit input sequence=111 received

