```
1
2   module selectorBlock_A_TB ();
3
4       // Inputs
5       reg sel;
6       reg clk;
7       reg reset;
8       reg enable;
9
10      //declare internal probes as wire
11      wire [3:0] count;
12      wire [3:0] upcount;
13
14      // Outputs
15      wire y;
16
17      // Instantiate the selectorBlock_A module
18      selectorBlock_A UUT (
19                           .y(y),
20                           .sel(sel),
21                           .clk(clk),
22                           .reset(reset),
23                           .enable(enable)
24                          );
25
26      //assign internal probe to count and upcount
27     assign count = UUT.count;
28     assign upcount = UUT.upcount;
29
30      //step4 Initialize clock
31  initial
32     begin
33          clk = 0;
34          forever #5 clk = ~clk; // 10ns period
35      end
36
37      //step5 initialize the sel bit for the test purpose
38      initial
39     begin
40          sel = 0;
41          forever #15 sel = ~sel; // 30ns period
42      end
43   // Initialize signals
44  initial
45     begin
46          clk = 0;
47          reset = 0;
48          enable = 1; // Enable the counter
49
50          // Apply reset
51          #10 reset = 1;
52          #10 reset = 0;
53
54          // Simulate some clock cycles
55          #50;
56
57          // Display output y
58          $display("y = %b", y);
59      end
60
61  endmodule
62
```