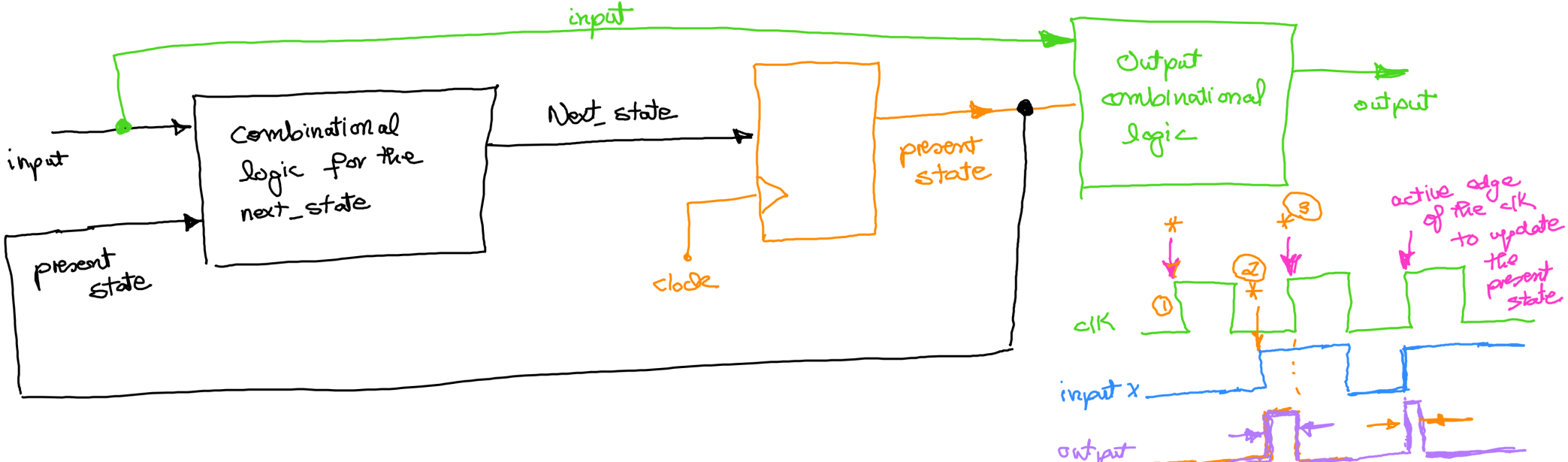
Finite State machine glitches

* Advantages
  * No delay
  * less # of states
* Disadvantages
  * may have glitches
  * Output pulses are less than one complete clock cycle.

(1) Glitches in Mealy machines

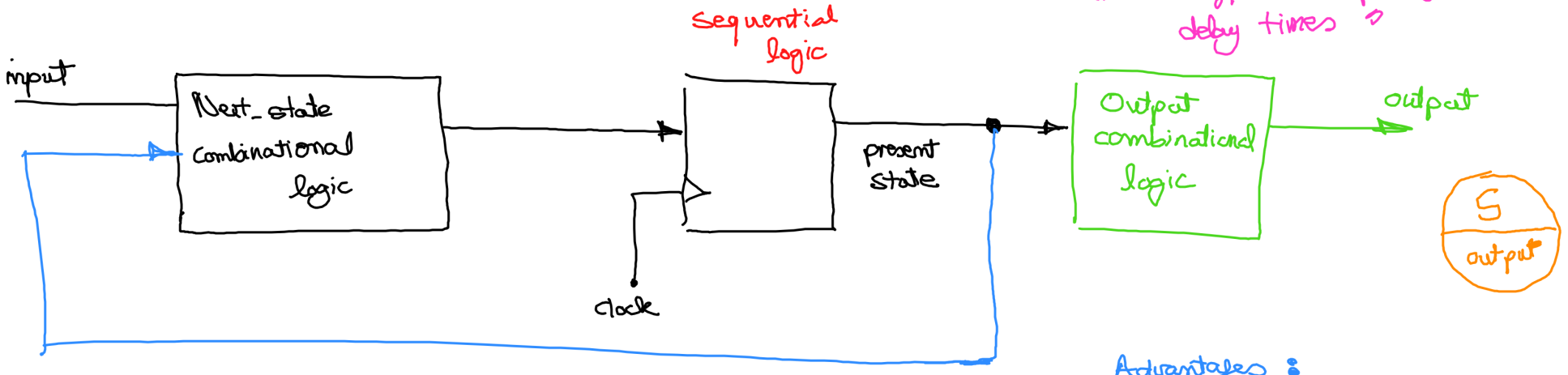
(The alignment of the output with the changes in the input signal)



Moore Machine

output glitches ?

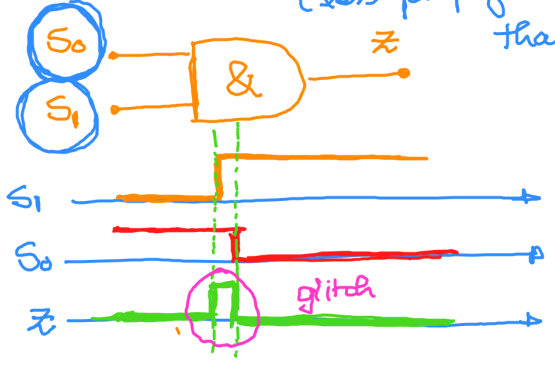
↳ due to difference in propagation delay times ↲



reg [1:0] state

present state	S_1	S_0	z
	0	1	0
next state	1	0	0

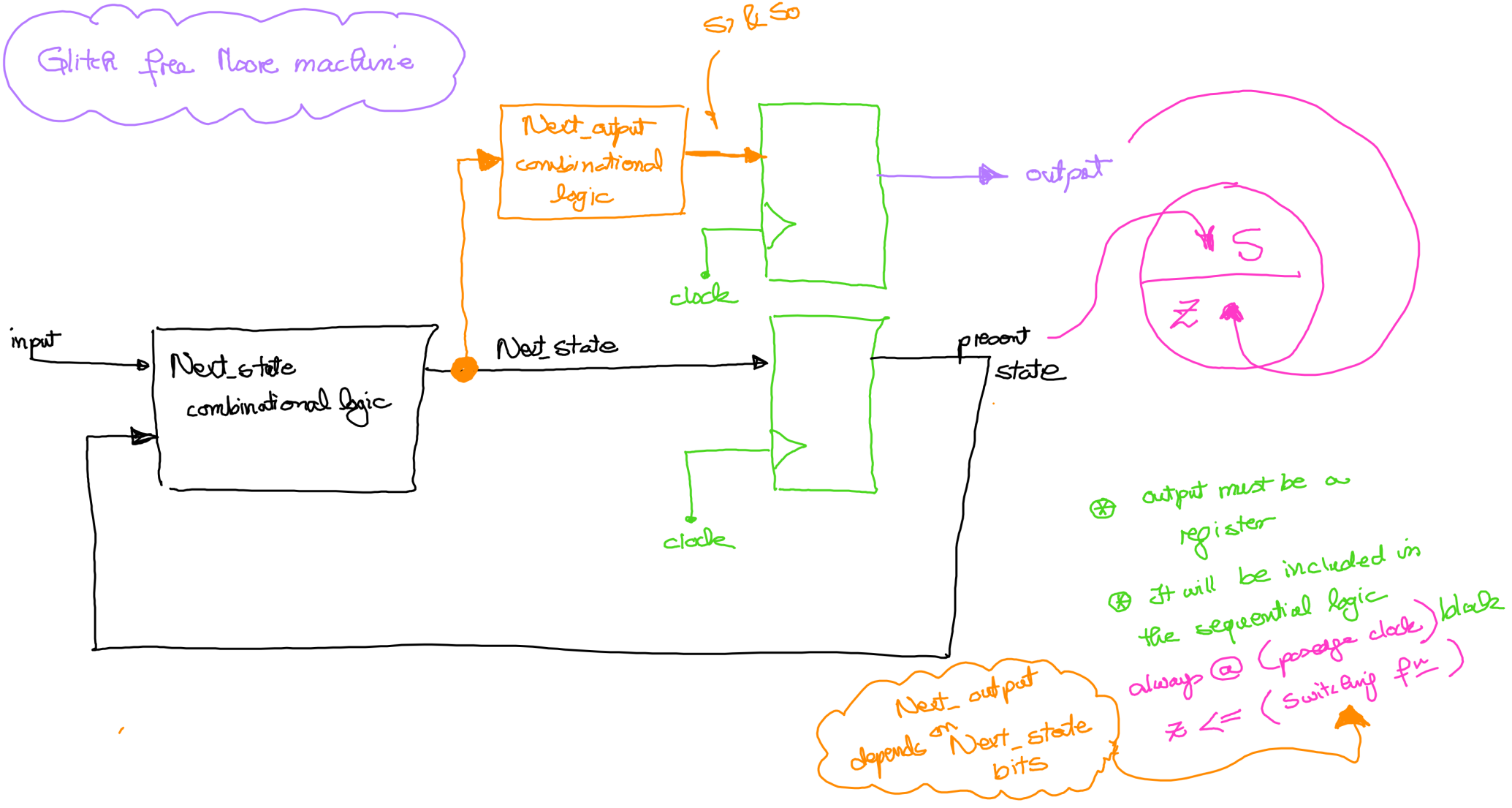
S_1 had a shorter path (less propagation delay than S_0)



Advantages :

* The output pulse width = one clock cycle. It gets updated with the present state

Disadvantages : * More states
* more delay.


Glitch free Moore machine
S1 & S0
Next_output combinational logic
output
clock
S
Z
input
Next_state combinational logic
Next_state
present state
clock
* output must be a register
* It will be included in the sequential logic always @ (passage clock) blabla
Z <= (switching fn)
Next_output depends on Next_state bits