# Course Syllabus – Fall 2024

## Course Information

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| *Course Number/Section* | EEDG/CE 5325.501 |
| *Course Title* | Hardware Modeling using HDL |
| *Term* | Fall 2024 |
| *Days and Time* | Tuesday / Thursday 5:40 – 6:45 pm |
| *Meeting Place* | *ECSW 3.210 and* eLearning Blackboard Collaborate (recorded) |

## Professor Contact Information

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| *Professor* | *William Swartz* |
| *Office Phone* | *MS Teams* |
| *Email Address* | *bill-swartz@utdallas.edu* |
| *Office Location* | *ECSN 3.210* |
| *Office Hours* | *Th 11:30am-2 pm Th 4-5 pm and by appointment in Collaborate or in office subject to COVID protocols* |

## Course Pre-requisites, Co-requisites, and/or Other Restrictions

Prerequisite: CE/EE 3320 or equivalent

## Course Description

This course introduces students to hardware description languages (HDL) beginning with simple examples and describing tools and methodologies. It covers the language, dwelling on fundamental simulation concepts. Students are also exposed to the subset of HDL that may be used for synthesis of custom logic. HDL simulation and synthesis labs and projects are performed using commercial and/or academic VLSI CAD tools.

## Student Learning Objectives/Outcomes

The following are the course learning objectives:

- **C001** Familiarization with the System Verilog language with emphasis on the synthesis of code in a Field Programmable Gate Array
- **C002** Specification, design, implementation, and test of a final project
- **C003** Interfacing a System Verilog code implementation to external logic for interaction with the real world
- **C004** Work in a team environment
- **C005** Write and follow a project plan that incorporates every step needed from concept to prototype
- **C006** Write a project report that describes the project as well as the process followed
- **C007** Present the results in an oral presentation in front of classmates and faculty

## Required Textbooks and Materials

*Required Texts*
none

*Required Materials*
none

## Suggested Course Materials

http://www.asic-world/com/
http://www.edaplayground.com/
Advanced Chip Design, Practical Examples in Verilog, Publisher: CreateSpace Independent Publishing Platform (April 16, 2013) ISBN-10: 1482593335 ISBN-13: 978-1482593334
FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version, Pong P. Chu, Publisher: Wiley-Interscience; 1st edition (February 4, 2008) ISBN-10: 0470185317 ISBN-13: 978-0470185315

*Suggested Materials*
Additional materials linked on eLearning

## Assignments & Academic Calendar

*Topics, Reading Assignments, Due Dates, Exam Dates*
Homework will be due at the beginning of class unless otherwise announced.
Midterm: Thursday October 31, 2024 during class hours (tentatively)
Project Presentation: Thursday December 5, 2024 (in class)
Cadence Certification: December 6, 2024
Final examination: TBD

Topics covered in the class include but not limited to:

- Hardware Languages
- VHDL
- Verilog
- VerilogA and VerilogAMS
- Spice
- SystemC
- System Verilog
- UVM

## Grading Policy

Homework/Project: 30%
Quizzes: 5%
Midterm: 15%
Cadence Certification: 10%
Final examination: 40% (cumulative)
Homework will be due at the beginning of class unless otherwise announced via eLearning.
Video quizzes: Announced via eLearning available all day.

*Computer resources during class*

This class will make heavy use of the NoMachine during class sessions

## Course Policies

*Make-up exams*
Only by permission of the instructor BEFORE the regularly scheduled examination date

*Extra Credit*
none

*Late Work*
Homework assignments will be considered late at 11:30 PM the Friday after they are due, and will not be graded without a valid excuse.

*Special Assignments*
none

*All-or-nothing grading*
Tests and homework will be graded as either correct for full credit or wrong with no credit. Problems with multiple steps will be graded all-or-nothing for each step. The only exception will be multiple choice questions where you may explain your reasoning.

*Class Materials*
The instructor may provide class materials that will be made available to all students registered for this class as they are intended to supplement the classroom experience. These materials may be downloaded during the course, however, these materials are for registered students' use only. Classroom materials may not be reproduced or shared with those not in class, or uploaded to other online environments except to implement an approved Office of Student AccessAbility accommodation. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

*Class Attendance*

The University's attendance policy requirement is that individual faculty set their course attendance requirements. Regular and punctual class attendance is expected. Students who fail to attend class regularly are inviting scholastic difficulty. In some courses, instructors may have special attendance requirements; these should be made known to students during the first week of classes. Faculty have the discretion to set an attendance policy for their in-person meetings, but the absences due to COVID-19 cannot be counted against a quarantined student.

*Class Participation*

*Regular class participation is expected regardless of course modality. Students who fail to participate in class regularly are inviting scholastic difficulty. A portion of the grade for this course is directly tied to your participation in this class. It also includes engaging in group or other activities during class that solicit your feedback on homework assignments, readings, or materials covered in the lectures (and/or labs). Class participation is documented by faculty. Successful participation is defined as consistently adhering to University requirements, as presented in this syllabus. Failure to comply with these University requirements is a violation of the Student Code of Conduct.*

*Class Recordings*

Students are expected to follow appropriate University policies and maintain the security of passwords used to access recorded lectures. Unless the Office of Student AccessAbility has approved the student to record the instruction, students are expressly prohibited from recording any part of this course. Recordings may not be published, reproduced, or shared with those not in the class, or uploaded to other online environments except to implement an approved Office of Student AccessAbility accommodation. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

The instructor will record meetings of this course. These recordings will be made available to all students registered for this class if the intent is to supplement the classroom experience. If the instructor or a UTD school/department/office plans any other uses for the recordings, consent of the students identifiable in the recordings is required prior to such use unless an exception is allowed by law.

*Classroom Citizenship*

## Comet Creed

This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same:

"As a Comet, I pledge honesty, integrity, and service in all that I do."

## Academic Support Resources

The information contained in the following link lists the University's academic support resources for all students.

Please see http://go.utdallas.edu/academic-support-resources.

## UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus. Please review the catalog sections regarding the credit/no credit or pass/fail grading option and withdrawal from class.

Please go to http://go.utdallas.edu/syllabus-policies for these policies.

*The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.*