65nm ProcessEECT/ CE 6325 VLSI Design
Fall 2024

PROJECT #3: INVERTER DESIGN AND LAYOUT
Due: **Fri. Oct 11 5pm**

Project Introduction

For this project you will be using the GF65nm process and Cadence Design tools to design, layout and characterize an inverter. This project will get you familiar with Cadence and also with the simulation of the layouts that you create.

Project Description/Requirements

1) Review the inverter layout tutorial: 65nm Process - VLSI tutorial.pdf
2) The input and output pin labels must be capitalized in both schematic view and layout view: IN, OUT
3) The power and ground pin labels in layout should be VDD! and GND!
4) The length of the channel (L) for this project must be ***65nm*** (not 60nm).
5) Simulate the inverter tutorial: HSPICE - VLSI tutorial.pdf
6) The input slew rate is 30ps (the slew rate, for this problem, is defined as the time for the input to go from low (0.2* Vdd) to high (0.8* Vdd) and vice versa). Use a piecewise linear input waveform or, if you dare, a pulse waveform accordingly.
7) Your group must ask the TAs for your group's unique set of Wp, Wn and C_{load}. Please email the names and the NetID of your group members to Jinkun Feng for the parameters: jinkun.feng@utdallas.edu
8) VDD is 1.2V & GND is 0V.
9) The poly gates for the two transistors must be vertically aligned.
10) ***DESIGN OBJECTIVE:*** Minimize the bounding box area (H*W) of your inverter layout.

Report Layout

1) Submit only a soft copy. Because of that, black backgrounds for waveforms are encouraged to enhance readability.
2) A cover page containing:
   - Student names, NetID and project titles
   - Clearly state your rise delay, fall delay, output rise edge rate (20% to 80%), and output fall edge rate (80% to 20%) and the area (widths & lengths are measured from highest Metal1 layer to the lowest Metal1 layer) on the front.
3) Soft copy of the report should include:
   - Spice test setup file
   - Waveforms showing how you measured the above rise/fall delays and output edge rates.
   - Inverter layout with rulers (**from cadence**)
   - Extracted Spice Netlist
4) Upload the zipped folder containing your Inverter layout, schematic on eLearning

Grading Breakdown

75% Proper layout according to given parameters; functional correctness of the inverter; proper measurement of characteristics.
25% Report clarity and completeness