EE417 Advanced Digital Logic with Verilog HDL Name: Ron Kalin / Lamin Jammeh Date: 07/17/24

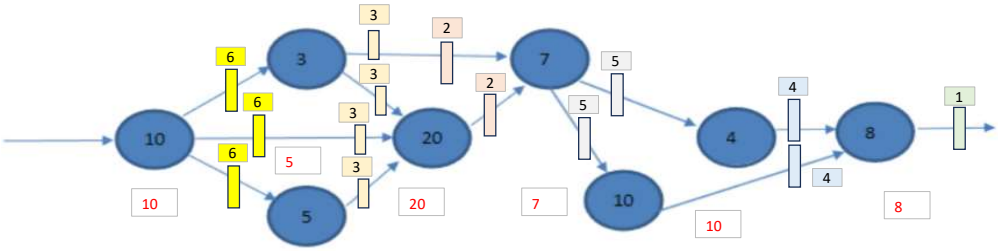
Lesson 10 **Pipelining**

Data Flow Graph

Pipelining allows for optimized usage of the hardware and the time for a given sequential logic designs with embedded combinational logic causing long propagation delay. This assignment has two questions:

(1) A theoretical example with a dataflow graph with multiple combinational logic operations with known propagation delays. With this question we practice finding the optimum locations of pipelining cut-sets to increase the clock frequency. For every set of registers inserted along a cut-set, we calculate the latency and the throughput, and make sure that data coherence is guaranteed.

The nodes of the DFG (Data Flow Graph) shown in figure has been annotated with propagation delays. Find the optimal placement of pipeline registers in the circuit. Make a list with the number of cut-sets and their locations and the corresponding latencies and throughput. What is the maximum clock frequency that can be used?



Pipelining Cut-sets	Min. clock period (ns)	Latency (ns)	Throughput (MHz)	Location of biggest delay	Rank
n	p	L=n*p	T=1/p		
1 output register	60	60	16.7	between start and reg 1	
2 cut-sets	35	70	28.6	between start and reg 2	
3	25	75	40.0	between reg 2 and 1	
4	20	80	50.0	between reg 2 and 3	minimum clock period and highest throughput with least latency
5	20	100	50.0	between reg 2 and 3	
6	20	120	50.0	between reg 2 and 3	highest latency

Optimal pipeline register placement

Since the goal is to provide the maxiumum throughput with the lowest latency, only 4 cut-sets will be used, as shown below.