Part of the Simulation transcript

```
# ________________________________output_count_out = -count-
# clk_in = 0: rst_in = 1:  enable_in=x: select_up_down=x: select_code2421_BCD=x: output_count_out =  x
# clk_in = 1: rst_in = 1:  enable_in=x: select_up_down=x: select_code2421_BCD=x: output_count_out =  x
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  x
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 15
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 15
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 14
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 14
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 13
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 13
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 12
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 12
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 11
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out = 11
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  4
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  4
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  3
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  3
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  2
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  2
# clk_in = 1: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  1
# clk_in = 0: rst_in = 0:  enable_in=1: select_up_down=0: select_code2421_BCD=0: output_count_out =  1
# ** Note: $stop    : C:/Users/lmnjm/OneDrive/Documents/Summer 2024/EE417 Programmable Logic Devices/Lecture 04/Quartu
#    Time: 940 ps  Iteration: 0  Instance: /BCD_or_2421_up_down_counter_tb
# Break in Module BCD_or_2421_up_down_counter_tb at C:/Users/lmnjm/OneDrive/Documents/Summer 2024/EE417 Programmable L
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The simulation summary shows the following

- The system takes in a code2421 and counts it down in the first block
- In the second block the output sends to code2421 upCounter and a selector block
- Block three is the selector block 1 it takes input from the downCounter and the upCounter
    - It uses a select bit to determine which input to output
- The third block is a code2421 to BCD converter
    - Takes input from the selector or third block and outputs BCD
- The final block is another selector block
    - Takes input from the first selector block and code2421 to BCD converter block
    - Outputs either a BCD code or code2421 depending on a select bit