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CLass: EE417 Summer 2024
Lesson 09 HW Question 3
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Project Description: TestBench for Interpolator Filter
module Linear_Interpolator_tb();
//define the registers and wire for the signals to monitor
             clock, reset;
       [7:0] Data_in;
reg
wire [7:0] Data_out;
//define the internal probes in the testbench for buffer1 and buffer2
wire filter; // New wire for observing filter
wire [7:0] buffer1; // New wire for observing buffer1
wire [7:0] buffer2; // New wire for observing buffer2
//Instantiate the unit under test UUT
Linear_Interpolator #(8)
                             UUT (
                           .Data_out(Data_out),
                           .Data_in(Data_in),
                           .clock(clock),
                           .reset(reset)
                           );
// Assign buffer1 and buffer2 in the testbench to buffer1 and buffer2 in the Unit under test
assign filter = UUT.filter;
assign buffer1 = UUT.buffer1;
assign buffer2 = UUT.buffer2;
//instantiate the clock cycle
initial
   begin
      clock = 0;
      forever #5 clock = ~clock;
initial
   begin
      //Initialize all the inputs
      reset = 1;
      Data_in = 8'b0;
      #20 reset = 0;
      //multiple Data_in samples and observe the buffer and Data_out
           Data_in = 8'b10101010;
      #20 Data in = 8'b01101001:
      #20 Data_in = 8'b00110011;
      #20 Data_in = 8'b11101001;
      //take everything back Data_out back to zero by setting reset to high
      #20 reset = 1;
      #20 reset = 0;
      // Final test case to ensure the interpolator works correctly after reset
           Data_in = 8'b00001001;
      #20 Data_in = 8'b01101011;
      #20 Data_in = 8'b11101011;
      #20 Data_in = 8'b11101111;
      // stop the simulation
      #20;
      $stop;
   end
// Display the results
always @(posedge clock)
```

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70 begi
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