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1  /*-----
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3  Class: EE417 Summer 2024
4  Lesson 06 HW Question 1
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: This is the test-bench for the count_0s code
7  -----*/
8
9  /*-----16 bits word_size Trial-----*/
10 module count_0s_tb ();
11
12 //define the parameters, registes and wires
13 parameter word_size = 16; //can be change to any
14 parameter count_size = 5;
15 reg [word_size -1:0] data_in;
16 wire [count_size -1:0] total_zeros;
17
18 //define the unit under test UUT
19 count_0s UUT (data_in, total_zeros);
20
21 //simulate different data_in and observe the outputs to validate the design
22
23 //-----16-bit data_in word_size-----//
24 initial
25 begin
26     #0 data_in = 16'b0000_0000_0000_0000;
27     #10 data_in = 16'b1111_0000_0000_0001;
28     #10 data_in = 16'b1111_0111_1111_1111;
29     #10 data_in = 16'b1010_1010_1000_1110;
30     #10 data_in = 16'b0111_0000_0011_1111;
31     #10 data_in = 16'b0011_1111_0011_1001;
32     #10 data_in = 16'b0000_0011_0000_0011;
33     #10 data_in = 16'b1010_1111_1101_0011;
34 end
35
36 //-----8-bit data_in word_size-----//
37 //initial
38 // begin
39 //     #0 data_in = 8'b0000_0000;
40 //     #10 data_in = 8'b1111_0001;
41 //     #10 data_in = 8'b0000_1111;
42 //     #10 data_in = 8'b1111_1111;
43 //     #10 data_in = 8'b1010_1010;
44 //     #10 data_in = 8'b0111_1111;
45 //     #10 data_in = 8'b1100_0001;
46 //     #10 data_in = 8'b1111_0011;
47 //     #10 data_in = 8'b0000_0011;
48 //     #10 data_in = 8'b1010_1111;
49 // end
50 //monitor the results
51 initial
52 begin
53     $monitor ($time,, "data_in = %b: total_zeros = %d", data_in, total_zeros);
54 end
55 endmodule

```