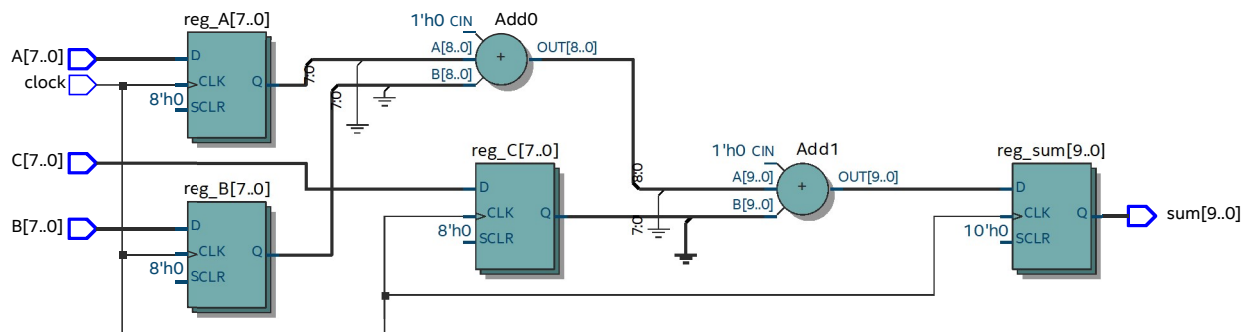


```
1  /*-----
2  Name Lamin Jammeh
3  Class: EE417 Summer 2024
4  Lesson 12 HW Question 1
5  Group: Ron Kalin/ Lamin Jammeh
6  Project Description: Simple Timing analysis using an Synopsis Design Constraint ((SDC) file
7  in Quartus
8  the circuit is run by a single clock name clock which has timing cntraints change from 1ns
9  to 4ns
10 -----*/
11
12 module add_three_numbers (clock, A, B, C, sum);
13
14 //define the inputs and outputs
15 input      clock;
16 input [7:0] A, B, C;
17 output [9:0] sum;
18
19 //define the internal registers
20 reg [7:0] reg_A, reg_B, reg_C; //synthesis keep
21 reg [9:0] reg_sum; //synthesis keep
22
23 //combination logics
24 always @(posedge clock)
25 begin
26     reg_A <= A;
27     reg_B <= B;
28     reg_C <= C;
29     reg_sum <= reg_A + reg_B + reg_C;
30 end
31
32 //assign the reg_sum to the output
33 assign sum = reg_sum;
34 endmodule
```



## Timing Analysis at 1ns clock period

Quartus Prime Lite Edition - C:/Users/Imnjm/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/Final HW12/add\_three\_numbers - add\_three\_numbers

File Edit View Project Assignments Processing Tools Window Help

add\_three\_numbers

Project Navigator

Entity/Instance

add\_three\_numbers

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Fast 1200mV 0C Model

Multicorner Timing Ana

Advanced I/O Timing

Clock Transfers

Report TCCS

Report RSKM

Unconstrained Paths

Compilation Report - add\_three\_numbers

Filter

Clock Name	Type	Period	Frequency	Rise	Fall	Duty Cycle	Divide by	Multiply by	Phase	Offset	Edge List	Edge Shift	Inverted	Master	Source	Target
clock	Base	1.000	1000.0 MHz	0.000	0.500											( clock

@ 1ns clock

Find

Find Next

Messages

Type ID Message

Running Quartus Prime EDA Netlist Writer

Command: quartus\_eda --read\_settings\_files=off --write\_settings\_files=off add\_three\_numbers -c add\_three\_numbers

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value.

204019 Generated file add\_three\_numbers.vo in folder "C:/Users/Imnjm/OneDrive/Documents/Grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/Final HW12/simulation/questions".

Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning

293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings

## Summary of Paths and Waveform @clock period of 1ns

File View Netlist Constraints Reports Script Tools Window Help

Search Intel FPGA

Set Operating Conditions

Slow 1200mV 85C Model

Slow 1200mV 0C Model

Fast 1200mV 0C Model

Report

Timing Analyzer Summary

Advanced I/O Timing

Setup: clock

Slow 1200mV 85C Model

Slow 1200mV 0C Model

Fast 1200mV 0C Model

Tasks

Open Project...

Netlist Setup

Create Timing Netlist

Read SDC File

Update Timing Netlist

Reset Design

Set Operating Conditions...

Reports

Report Setup Summary

Report Hold Summary

Report Recovery Summary

Console

History

Command Info

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
-2.432	reg_A[0]	reg_sum[6]	clock	clock	1.000	-0.081	3.349
-2.430	reg_A[2]	reg_sum[6]	clock	clock	1.000	-0.081	3.347
-2.428	reg_A[2]	reg_sum[6]	clock	clock	1.000	-0.081	3.345
-2.428	reg_B[0]	reg_sum[6]	clock	clock	1.000	-0.081	3.345
-2.400	reg_A[1]	reg_sum[5]	clock	clock	1.000	-0.081	3.317
-2.400	reg_A[1]	reg_sum[5]	clock	clock	1.000	-0.081	3.317
-2.399	reg_A[0]	reg_sum[6]	clock	clock	1.000	-0.081	3.316

Path #1: Setup slack is -2.432 (VIOLATED)

Path Summary

Statistics

Data Path

Waveform

Extra Filter Information

Data Arrival Path

Total	Incr	RF	Type	Fanout	Location	Element
0.000	0.000					launch edge time
3.048	3.048					clock path
0.000	0.000					source latency
0.000	0.000	RR	IC	1	PIN_11	clock
0.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N8	clock-input[i]
0.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clock-input[o]

Data Required Path

Total	Incr	RF	Type	Fanout	Location	Element
1.000	1.000					latch edge time
3.967	2.967					clock path
1.000	0.000					source latency
1.000	0.000	RR	IC	1	PIN_11	clock
1.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N8	clock-input[i]
1.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clock-input[o]

Waveform

Launch Clock

Launch

Setup Relationship

1.00 ns

Latch Clock

Latch

Data Arrival

3.048 ns

3.345 ns

3.347 ns

3.349 ns

2.432 ns

2.430 ns

2.428 ns

2.400 ns

2.399 ns

Report Timing -from:clock ( clock ) -to:clock ( clock ) -setup -npaths 10 -detail full\_path -panel\_name {Setup: clock} -multi\_corner

Report Timing: Found 10 setup paths (10 violated). Worst case slack is -2.432

0% 00:00:00 Ready

## Timing Analysis at 4.00ns clock period

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  - Report TCCS
  - Report RSKM

Messages

Running Quartus Prime EDA Netlist Writer

Command: quartus\_eda --read\_settings\_files=off --write\_settings\_files=off add\_three\_numbers -c add\_three\_numbers

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate va

204019 Generated File add\_three\_numbers.vo in folder "c:/users/1mjm/OneDrive/documents/grad School/Summer 2024/EE417 Programmable Logic Devices/Lecture 12/Final HW12/simulation/ques

Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning

293000 Quartus Prime Full Compilation was successful. 0 errors, 10 warnings

## Summary of Paths and Waveform @clock period of 4.000ns

Set Operating Conditions

- Slow 1200mV 85C Model
- Slow 1200mV 0C Model
- Fast 1200mV 0C Model

Report

- Timing Analyzer Summary
- Advanced I/O Timing
- Setup: clock
- Slow 1200mV 85C Mode
- Slow 1200mV 0C Model
- Fast 1200mV 0C Model

Tasks

- Report Net Delay...
- Report Metastability...
- Create Slack Histogram...
- Report Timing Closure Reco
- Macros
  - Report All Summaries
  - Report Top Failing Paths
  - Report All I/O Timings
  - Report All Core Timings
  - Create All Clock Histograms
- Write SDC File...

Console

report\_timing -setup -multi\_corner -panel\_name {Setup: clock} -from\_clock {get\_clocks { clock }} -to\_clock {get\_clocks { clock }} -npaths 10 -detail full\_path

Report Timing: Found 10 setup paths (0 violated). Worst case slack is 0.568

Summary of Paths

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
0.568	reg_A[0]	reg_sum[6]	clock	clock	4.000	-0.081	3.349
0.570	reg_A[2]	reg_sum[6]	clock	clock	4.000	-0.081	3.347
0.572	reg_A[2]	reg_sum[6]	clock	clock	4.000	-0.081	3.345
0.572	reg_B[0]	reg_sum[6]	clock	clock	4.000	-0.081	3.345
0.600	reg_A[1]	reg_sum[5]	clock	clock	4.000	-0.081	3.317
0.600	reg_A[1]	reg_sum[5]	clock	clock	4.000	-0.081	3.317
0.601	reg_A[0]	reg_sum[6]	clock	clock	4.000	-0.081	3.316

Path #1: Setup slack is 0.568

Path Summary

Total	Incr	RF	Type	Fanout	Location	Element
0.000	0.000					launch edge time
3.048	3.048					clock path
0.000	0.000					source latency
0.000	0.000					clock
0.000	0.000	RR	IC	1	PIN_11	clock-input
0.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clock-input
0.917	0.187	RR	IC	1	CLKCTRL_G2	clock-inputclkctrl[clk0]

Data Arrival Path

Path #1: Setup slack is 0.568

Path Summary

Total	Incr	RF	Type	Fanout	Location	Element
4.000	4.000					latch edge time
6.967	2.967					clock path
4.000	0.000					source latency
4.000	0.000					clock
4.000	0.000	RR	IC	1	PIN_11	clock-input
4.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clock-input
4.910	0.180	RR	IC	1	CLKCTRL_G2	clock-inputclkctrl[clk0]

Data Required Path

Waveform

Launch Clock

Setup Relationship

Latch Clock

Data Arrival

Clock Delay

Data Delay

Slack

Data Required

Clock Delay