Fall
2024

Layout & Verification

PROJECT 6 CE6325 VLSI DESIGN:

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Design Function:

The purpose of the design is to make an FIR_MAC filter that takes an input data and filters it through the different filter taps (orders) by multiplying the input data with the filter coefficients and accumulating the results down to the final output ports.

Design Specification:

Filter order: 15

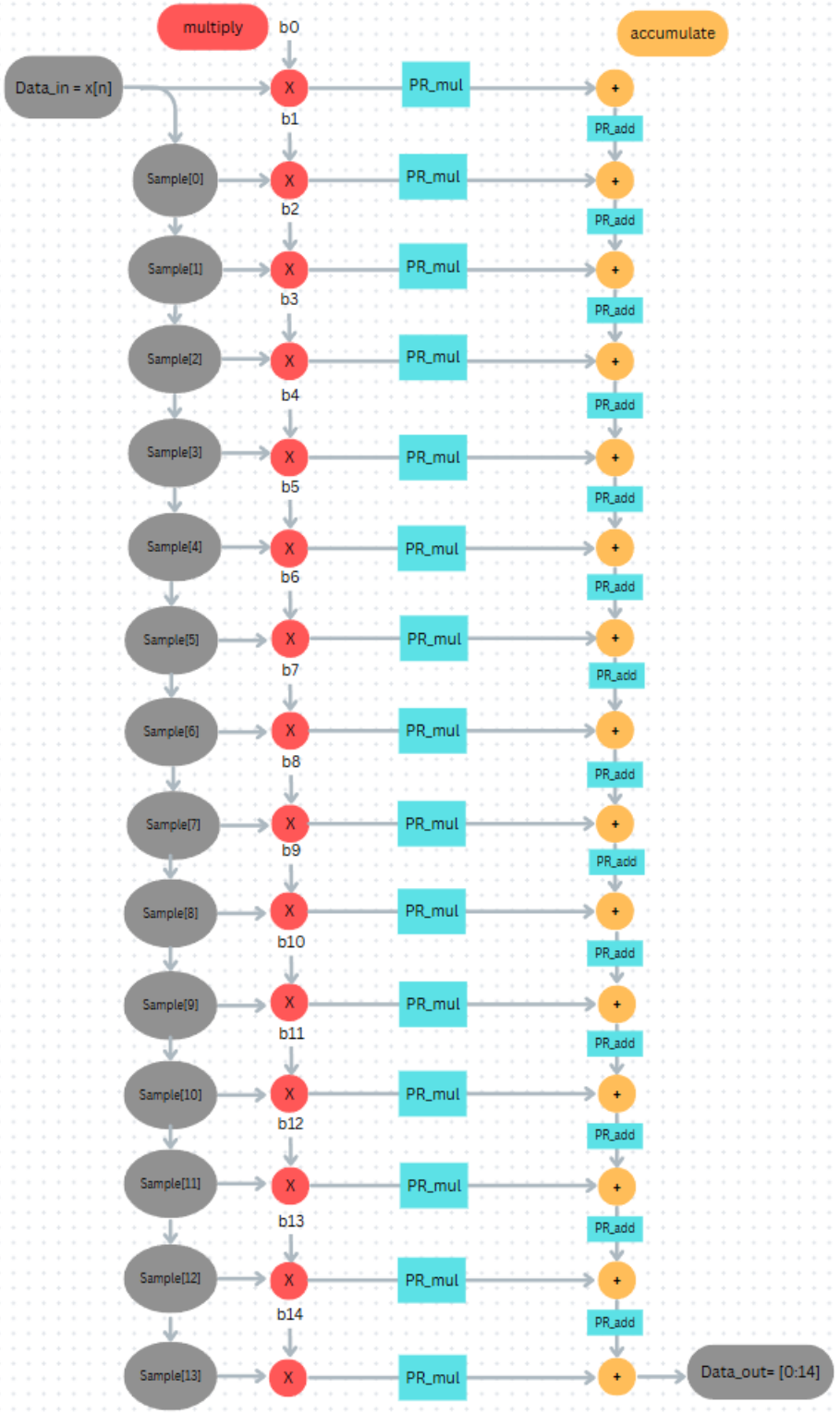
Filter coefficients: [7, 8, 9, 12, 4, 7, 8, 9, 12, 4]

Data_in size: 8

Data_out size: 20

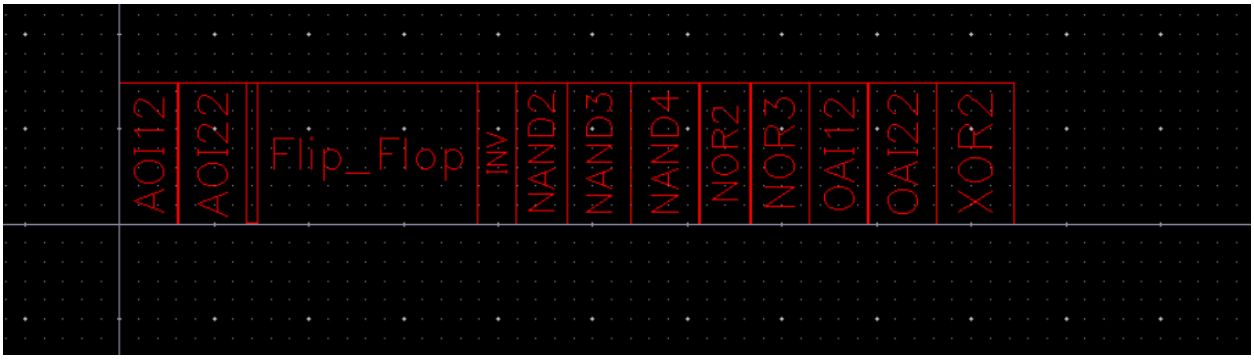
PR_mul and PR_add: Pipeline registers for multiplication results and addition results respectively

Data flow through the filter

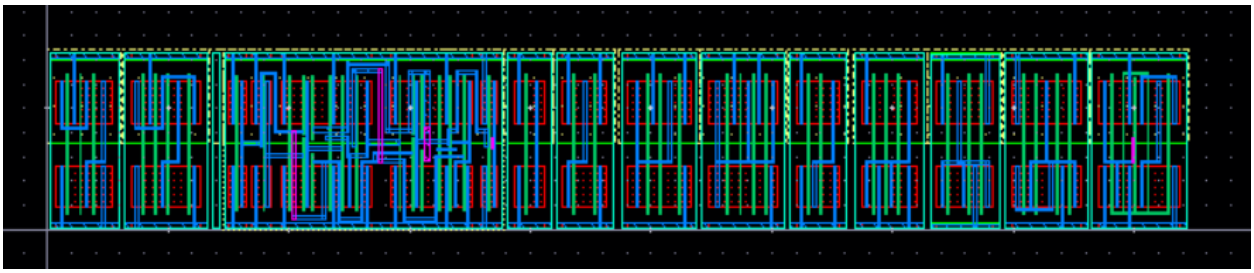

multiply
accumulate
Data_in = x[n]
Sample[0]
Sample[1]
Sample[2]
Sample[3]
Sample[4]
Sample[5]
Sample[6]
Sample[7]
Sample[8]
Sample[9]
Sample[10]
Sample[11]
Sample[12]
Sample[13]
X
b0
b1
b2
b3
b4
b5
b6
b7
b8
b9
b10
b11
b12
b13
b14
PR_mul
+
PR_add
Data_out= [0:14]

Cells used in the design

The design comprises a total of twelve cells with one filler cell. These cells were design to build a library each cell passed DRC and LVS check after which a PEX extraction was performed to obtain the netlist files for cell characterization. Each cell was place side by side to have equal height from VDD to GND and from GND to top of NW drw. A LEF file was obtain from the new library to be used with innovus later in the process development.



show they have

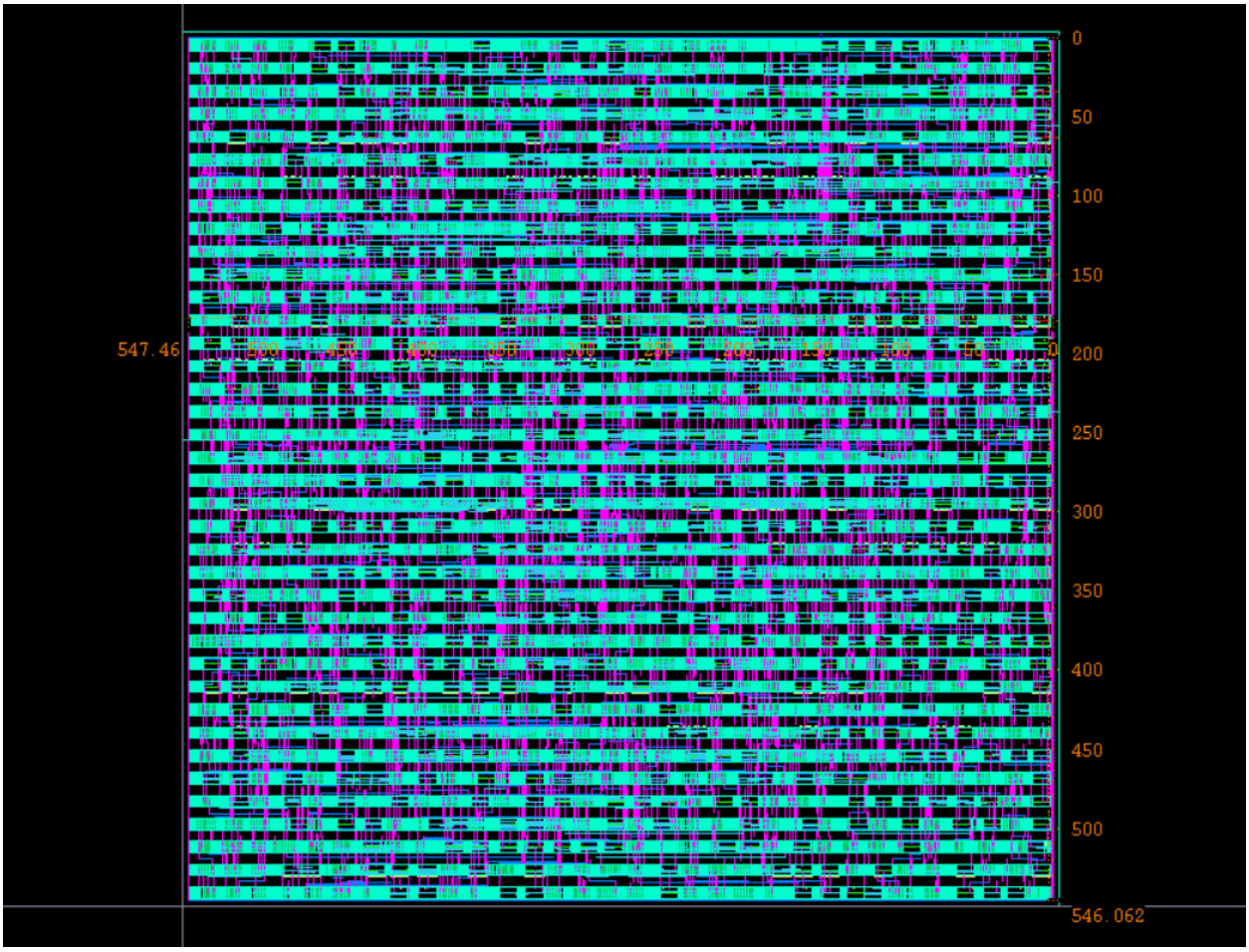


Synopsys Primlib was used to perform characterization and modeling for each cell. The operating conditions of all the cells were combined to one liberty files with power pins removed.

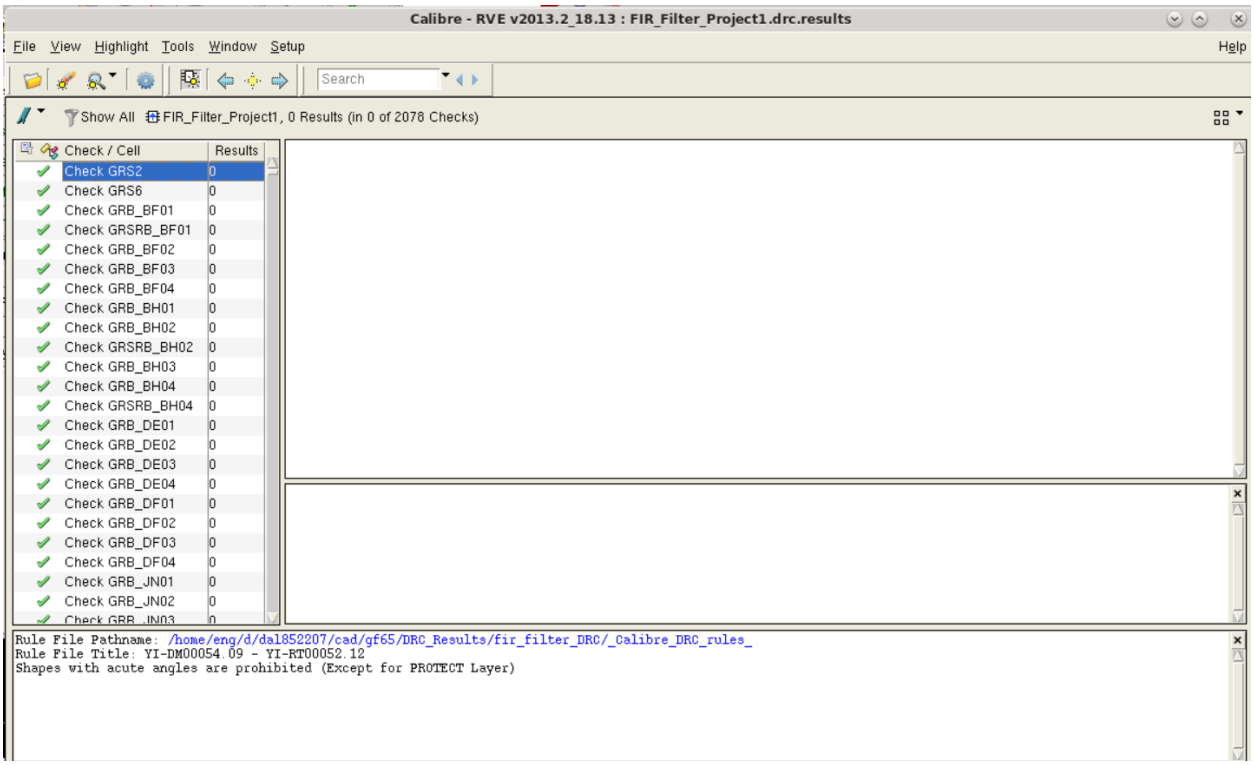
Synopsys library compiler was used to create a database file. The db file and the original Verilog code for the design were used to obtain the synthesizable Verilog file using Synopsys design vision

The synthesize Verilog file and the LEF file were used in innovus together with the cell library containing all the designed cells to perform the floor-planning, placement, and routing. The schematic and layout file (DEF file) were export out to be used in cadence virtuoso to finish the final design.

Filter layout:

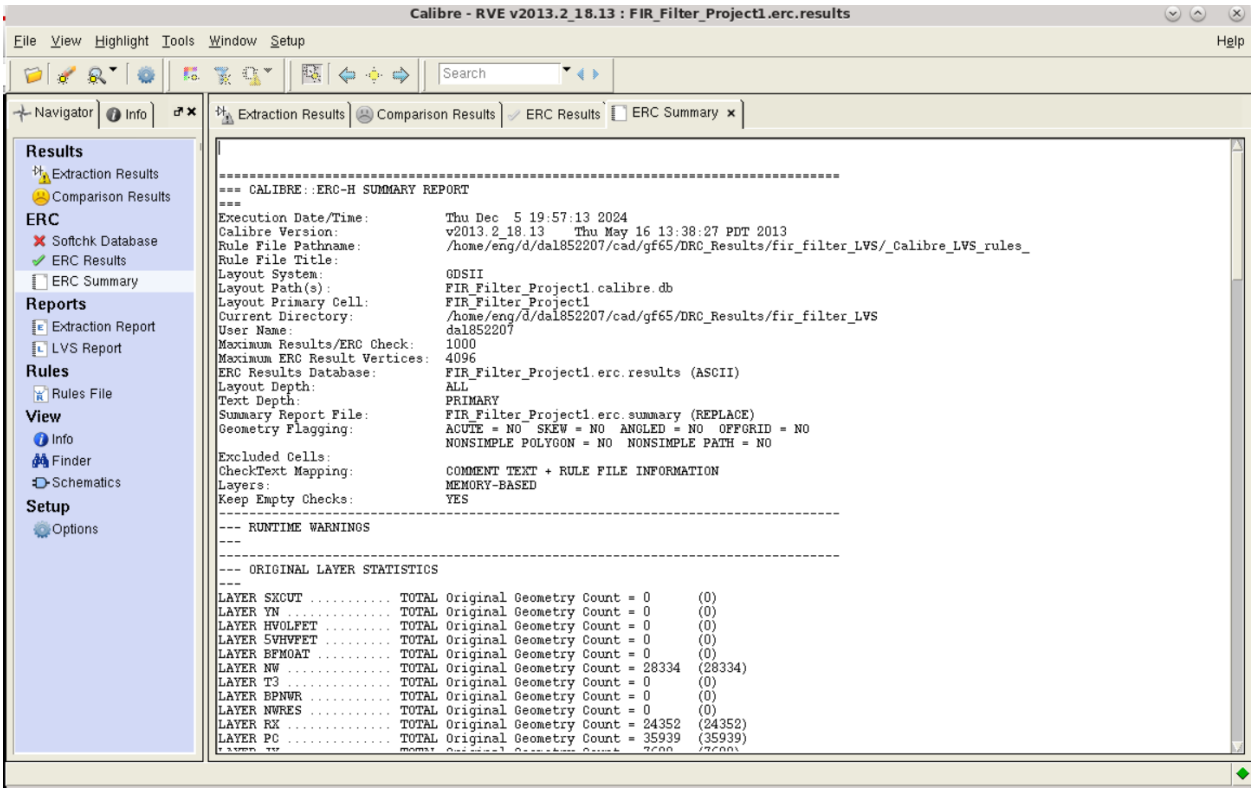


DRC results showing zero errors:



Filter schematic imported from innovus

LVS report:


Calibre - RVE v2013.2_18.13 : FIR_Filter_Project1.erc.results
File View Highlight Tools Window Setup
Help
Search
Navigator
Info
Results
Extraction Results
Comparison Results
ERC
Softchk Database
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Extraction Results
Comparison Results
ERC Results
ERC Summary
==
=== CALIBRE::ERC-H SUMMARY REPORT
===
Execution Date/Time: Thu Dec 5 19:57:13 2024
Calibre Version: v2013.2_18.13 Thu May 16 13:38:27 PDT 2013
Rule File Pathname: /home/eng/d/dal852207/cad/gf65/DRC_Results/fir_filter_LVS/_Calibre_LVS_rules_
Rule File Title:
Layout System: GDSII
Layout Path(s): FIR_Filter_Project1.calibre.db
Layout Primary Cell: FIR_Filter_Project1
Current Directory: /home/eng/d/dal852207/cad/gf65/DRC_Results/fir_filter_LVS
User Name: dal852207
Maximum Results/ERC Check: 1000
Maximum ERC Result Vertices: 4096
ERC Results Database: FIR_Filter_Project1.erc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: FIR_Filter_Project1.erc.summary (REPLACE)
Geometry Flagging: ACUTE = NO SKEW = NO ANGLED = NO OFFGRID = NO
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: YES
--- RUNTIME WARNINGS
--- ORIGINAL LAYER STATISTICS
LAYER SXCUT ..... TOTAL Original Geometry Count = 0 (0)
LAYER YN ..... TOTAL Original Geometry Count = 0 (0)
LAYER HVOLFET ..... TOTAL Original Geometry Count = 0 (0)
LAYER 5VHVFET ..... TOTAL Original Geometry Count = 0 (0)
LAYER BFMOAT ..... TOTAL Original Geometry Count = 0 (0)
LAYER NW ..... TOTAL Original Geometry Count = 28334 (28334)
LAYER T3 ..... TOTAL Original Geometry Count = 0 (0)
LAYER BPNWR ..... TOTAL Original Geometry Count = 0 (0)
LAYER NWRES ..... TOTAL Original Geometry Count = 0 (0)
LAYER RX ..... TOTAL Original Geometry Count = 24352 (24352)
LAYER PC ..... TOTAL Original Geometry Count = 35939 (35939)