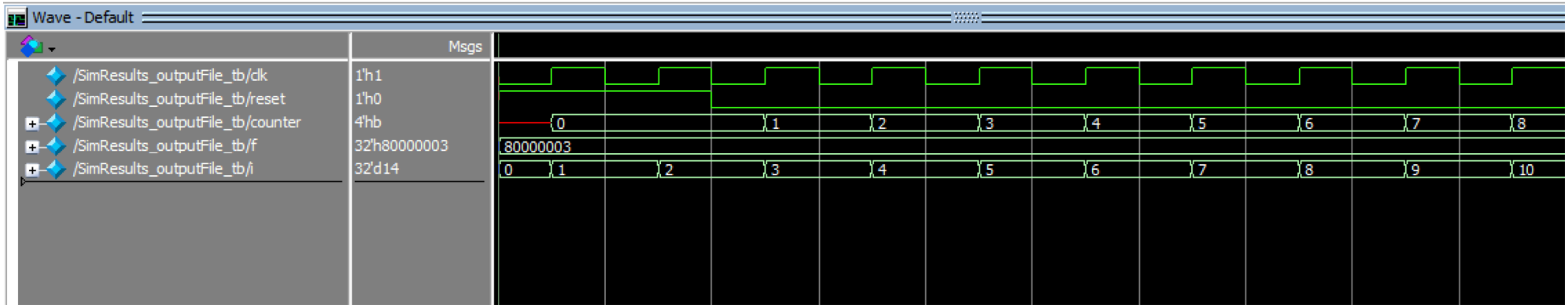
Writing the Simulation Results to a HEX file in Quartus and Questa

The simulation result data is recorded in the file at every positive edge of the clock.

```
module SimResults_outputFile_tb ();

parameter               width = 4;
reg                     clk, reset;
wire    [width-1:0]     counter;

integer   f;    // Numerical identifier for the HEX file
integer   i;    // index to use within the for loop

Counter_outputFile UUT   (clk, reset, counter);

initial   begin     clk = 0;
          forever
          #5        clk = ~clk; end

initial   begin     reset = 1;
          #20       reset = 0;   end

initial
   begin
        f = $fopen("Simulation_output.hex", "w");    // open a file for writing
        $fwrite (f,  "Simulation results for the counter @ every posedge of clock:\n\n");
        $fwrite (f,  "reset       counter\n");

        for (i=0; i<14; i=i+1)
            begin
                 @(posedge clk);
                 $fwrite (f, "%h       %h\n", reset, counter);
              end
        $fclose (f);
        $stop;
     end

endmodule
```

```
module Counter_outputFile (clk, reset, out);

   parameter               width = 4;
   input                   clk, reset;
   output reg [width-1:0]  out;

   always @ (posedge clk)
        begin
               if (reset)       out <= 0;
            else                out <= out + 1;
        end

endmodule
```



The generated simulation file: (saved under the project file > simulation > questa > simulation_output.hex

```
Simulation results for the counter @ every posedge of clock:

reset       counter
1       x
1       0
0       0
0       1
0       2
0       3
0       4
0       5
0       6
0       7
0       8
0       9
0       a
0       b
```