PennState

Digital Design Using Field Programmable Devices
E E 417

History of Programmable Logic

(1) Name two areas of application of FPGAs?
- High Definition TVs
- High-speed switching applications - Networking and communication (5)

(2) What was the main goal for basic TTL digital logic design and what were the main challenges?
- Minimize the number of chips used,
- Reduce the cost
- Minimize the space used on the board
- Design with the current device inventory. (5)

(3) What are the steps for designing basic Digital logic Designs.
(a) The creation of a truth table
(b) Karnaugh map
(c) Create boxes around the minterms
(d) Create a logic switching function using Sum of Products SOP (5)

(4) How are combinatorial logic implemented?
AND gates to create the product terms and
Or gates to create the sum terms.
Inverters can be used to create the complement of the inputs. (5)

(5) How is data synchronized and stored in logic circuits?
Registers are used to synchronize data or to store data. (5)

(6) What were the main ideas that lead to the creation of programmable devices?
- What if logic functions were fixed, but combined into a single device?
- What if we could program the routing (wiring) between the different gates or device. (5)

(7) What are the main sections of a PAL? State briefly what each section contains.
Programmable Array Logic:
- Programmable Array: The desired inputs are selected and routed to the desired AND gates.
- Product Terms: The outputs of the AND gates in the first stage forming the products of the SOP.
- Macrocell: The outputs of the OR gates of the SOP that create the final function output which is fed into a register for storage or synchronization. Some macrocells have feedback to feed into the inputs, or the registers can be completely bypassed for combinational logic realization only. (5)

(8) What are some of the advantages of PALs?

- Fewer devices required
- Less area used on the board
- lower cost
-power saving
- simpler to test and debug
- design security
- automated tools simplify the design flow
- in system programmability (for some devices)

(5)

(9) What is the key technology that was used to control the interconnection fabric in the early PAL devices? Where is this technology still used?

Floating-gate-transistors
This technology is still used in flash memory devices.

(5)

(10)What was the first version of PLDs called? What were the main differences between the PLDs and the PAL Devices?

The first PLDs: 22v10
The advantages:
- Fully programmable macrocells: Input/feedback select to product-term array
Output-select mux: true/inverted combinatorial or true/inverted registered
- variable product term distribution: different number of inputs to the AND gates.

(5)

(11) What was the innovation in CPLDs?

Increasing the amount of logic in a single device by combining multiple PLDs with programmable interconnects and I/O.

(5)

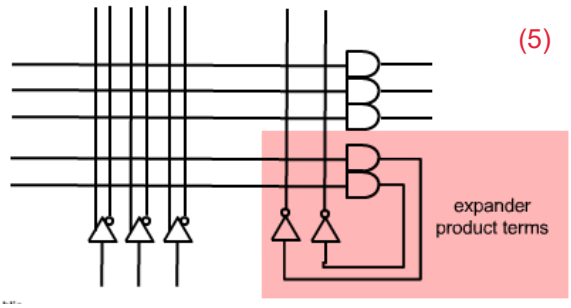
(12) What are LABs? How different is it from a PAL?

Logic Array Blocks (LABs)
The LAB in a CPLD has an expander product term, which is an extra AND gate logic that feeds directly back into the array and allows controlled product term distribution, versus the variable product term distribution found in PALs.

(5)

(13) What are the advantages and disadvantages of expander product terms?

Advantages: - expands the logic function,
- The logic is created once and shared with other macrocells as needed, which is an efficient way to minimize the circuit logic.
Disadvantages: It causes extra delay



(5)

(14) What does JTAG stand for and what is it used for?

The Joint Test Action Group (JTAG) - programming interface
- Self test
- In System programmability (ISP)

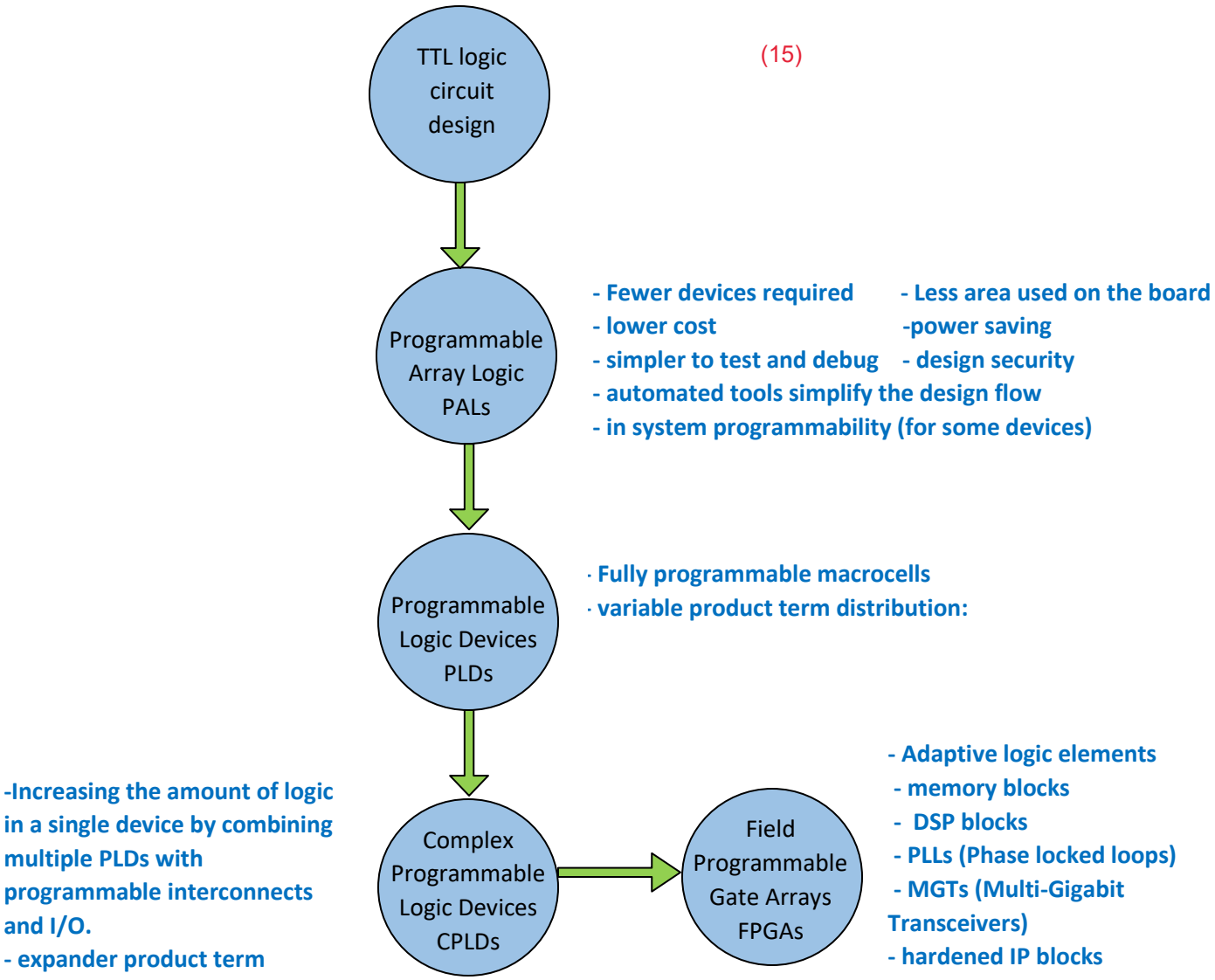
(5)

(15) What are the major additions to the FPGAs if compared to CPLDs?

- The have labs with adaptive logic elements
- They have integrated memory blocks
- They have DSP blocks
- They have PLLs (Phase locked loops)
- They have MGTs (Multi-Gigabit Transceivers)
- They have hardened IP blocks

(5)

(16) As a summary, sketch a block diagram showing the different phases of evolutions of programmable devices with the major additions for every stage.



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