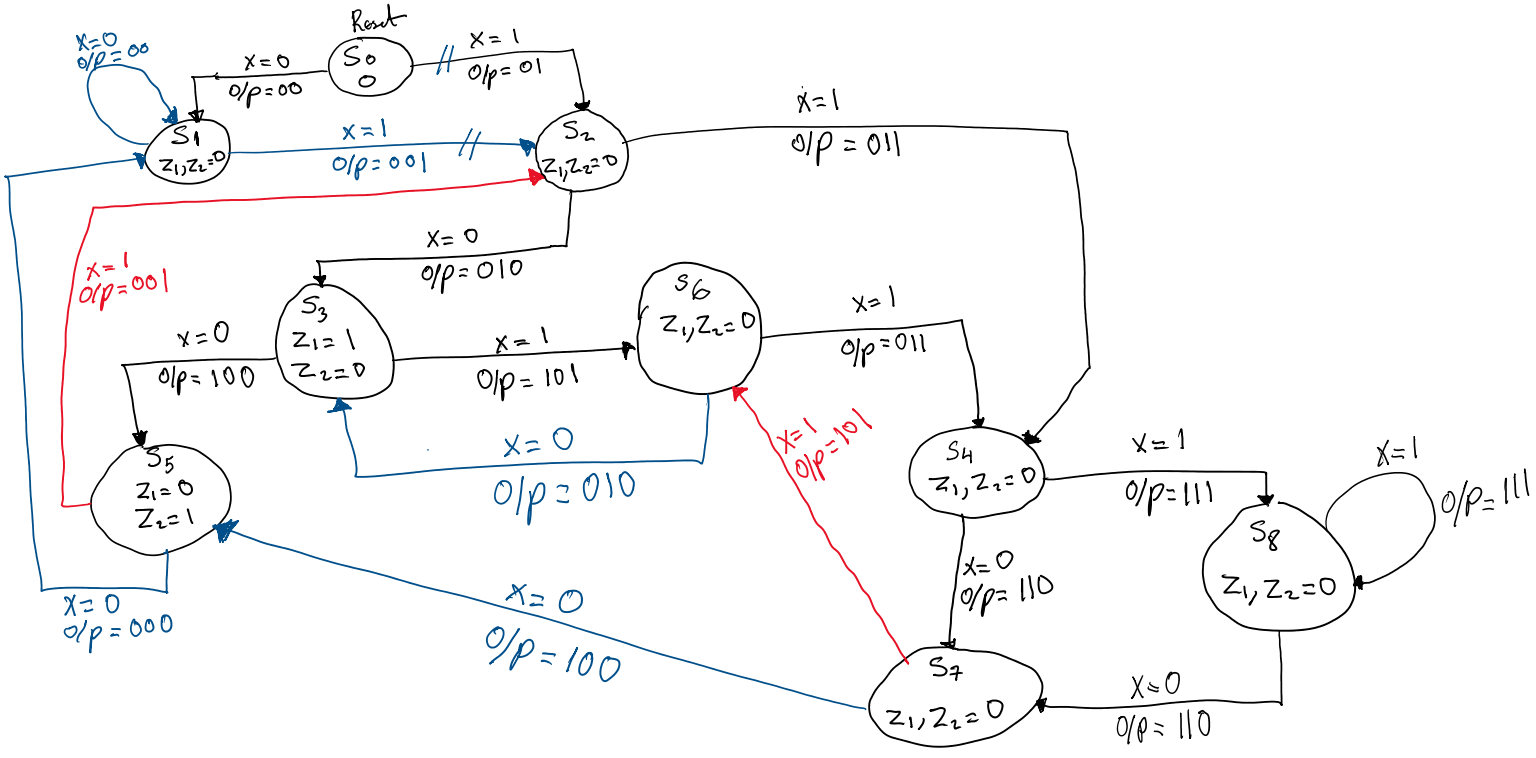
State Table			
Possible 3 bit combination logic			States
0	0	0	S0 = Reset
0	0	0	S1
0	0	1	S2
0	1	0	S3
0	1	1	S4
1	0	0	S5
1	0	1	S6
1	1	0	S7
1	1	1	S8



	Next-state_1		Output State	
Present State	x=0	x=1	Z1	Z2
S0	S1	S2	0	0
S1	S1	S2	0	0
S2	S3	S4	1	0
S3	S5	S6	0	1
S4	S7	S8	0	0
S5	S1	S2	0	0
S6	S3	S4	0	0
S7	S5	S6	0	0
S8	S7	S8	0	0