



Source State	Destination State	Condition
1 idle	starting	(Ser_in_0),(rst_b)
2 idle	idle	(!Ser_in_0) + (Ser_in_0),(rst_b)
3 receiving	receiving	(!BC_eq_8),(rst_b) + (BC_eq_8),(SC_lt_7),(rst_b)
4 receiving	idle	(!BC_eq_8),(rst_b) + (BC_eq_8),(SC_lt_7) + (BC_eq_8),(SC_lt_7),(rst_b)
5 starting	receiving	(SC_eq_3),(Ser_in_0),(rst_b)
6 starting	starting	(inc_Sample_counter),(rst_b)
7 starting	idle	(!Ser_in_0) + (Ser_in_0),(rst_b)