```verilog
 1    /*-------------------------------------------------------------------------------
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 3    Class: EE417 Summer 2024
 4    Lesson 09 HW Question 01
 5    Group: Ron Kalin/ Lamin Jammeh
 6    Project Description: test-bench for moving average FIR filter
 7    -------------------------------------------------------------------------------*/
 8    module moving_average_filter_tb ();
 9        // Parameters
10        parameter DATA_WIDTH =  8;
11        parameter FILT_LENGTH = 4;
12
13        // Signals
14        reg clk, reset, enable;
15        reg [DATA_WIDTH-1:0] sample_in;
16        wire [2*DATA_WIDTH-1:0] filtered_sample;
17
18        //wires monitor internal variables
19        wire [DATA_WIDTH-1:0] buffer0, buffer1, buffer2, buffer3;
20        wire [DATA_WIDTH-1:0] coeff0, coeff1,coeff2,coeff3;
21        wire [DATA_WIDTH-1:0] tap_outputs [0:3];
22
23        // Instantiate the moving_average_filter module
24        moving_average_filter UUT (
25            .filtered_sample(filtered_sample),
26            .sample_in(sample_in),
27            .enable(enable),
28            .clk(clk),
29            .reset(reset)
30        );
31        assign buffer0 =UUT.buffer0;
32        assign buffer1 =UUT.buffer1;
33        assign buffer2 =UUT.buffer2;
34        assign buffer3 =UUT.buffer3;
35        assign coeff0  =UUT.coeff0;
36        assign coeff1  =UUT.coeff1;
37        assign coeff2  =UUT.coeff2;
38        assign coeff3  =UUT.coeff3;
39        assign tap_outputs[0]=UUT.tap_outputs[0];
40        assign tap_outputs[1]=UUT.tap_outputs[1];
41        assign tap_outputs[2]=UUT.tap_outputs[2];
42        assign tap_outputs[3]=UUT.tap_outputs[3];
43
44        // Clock generation
45        always #5 clk = ~clk;
46
47        // Test stimulus
48        initial begin
49            clk = 0;
50            reset = 1;
51            #10 reset = 0; enable =1; // Release reset, enable
52            #20 sample_in = 8'b0000_0000;  // input sample of 0
53            #20 sample_in = 8'b0000_0000;  // input sample of 0
54            #20 sample_in = 8'b0000_0100;  // input sample of 4
55            #20 sample_in = 8'b0000_0000;  // input sample of 0
56            #20; // Wait for some cycles
57
58            // Applying additional test vectors
59            #20 sample_in = 8'b0001_0001;  // input sample of 17
60            #20 sample_in = 8'b0010_0001;  // input sample of 33
61            #20 sample_in = 8'b0011_0001;  // input sample of 49
62            #20 sample_in = 8'b0100_0001;  // input sample of 65
63            #20 sample_in = 8'b0101_0001;  // input sample of 81
64            #20 sample_in = 8'b0110_0001;  // input sample of 97
65            #20 sample_in = 8'b0111_0001;  // input sample of 113
66            #20 sample_in = 8'b1000_0001;  // input sample of 129
67            #20 sample_in = 8'b1001_0001;  // input sample of 145
68            #20 sample_in = 8'b1010_0001;  // input sample of 161
69            #20 sample_in = 8'b1011_0001;  // input sample of 177
70            #20 enable =0;
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71            #40 enable =1;
72            #20 sample_in = 8'b1100_0001;  // input sample of 193
73            #20 sample_in = 8'b1101_0001;  // input sample of 209
74            #20 sample_in = 8'b1110_0001;  // input sample of 225
75            #20 sample_in = 8'b1111_0001;  // input sample of 241
76            #20 sample_in = 8'b1000_0001;  // input sample of 129
77            #20; // Wait for some cycles
78
79            $display("Filtered Output: %h" , filtered_sample);
80            //$finish;
81        end
82
83   endmodule
```