```verilog
1    /*-----------------------------------------------------------------------------
2    Name Lamin Jammeh
3    CLass: EE417 Summer 2024
4    Lesson 07 HW Question 2
5    Group: Ron Kalin/ Lamin Jammeh
6    Project Description: This module combines submodule DataPath and Controller to perform
7    the shift functions. It is the top module for the design
8    ------------------------------------------------------------------------------*/
9
10   /*----------------------up/down counter----------------------*/
11   module DataPath_controller #(parameter WIDTH = 8, parameter CYCLES = 18) (
12       input clk,
13       input reset,
14       input  [WIDTH-1:0] data_in,
15       output [WIDTH-1:0] count
16   );
17
18   wire shift_left, shift_right, load, done;
19
20   DataPath #(WIDTH, CYCLES) datapath (
21       .clk(clk),
22       .reset(reset),
23       .shift_left(shift_left),
24       .shift_right(shift_right),
25       .load(load),
26       .data_in(data_in),
27       .count(count),
28       .done(done)
29   );
30
31   Controller controller (
32       .clk(clk),
33       .reset(reset),
34       .done(done),
35       .shift_left(shift_left),
36       .shift_right(shift_right),
37       .load(load)
38   );
39
40   endmodule
41
```