Chapter 15: Timing Constraints

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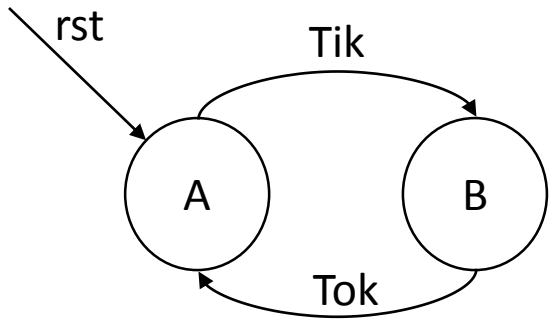
CS 4341

How fast is an FSM?

- Circuitry consists of electrons travelling at the speed of light!
- Surely, there is no lag!
- No delay!
- Urm…
- Okay, there is a *tiny* lag
- When put through the millions of logic gates in a combined circuit…
- *The lag matters*
- *Note: Traffic Lights based on states, not each other…*

Delays

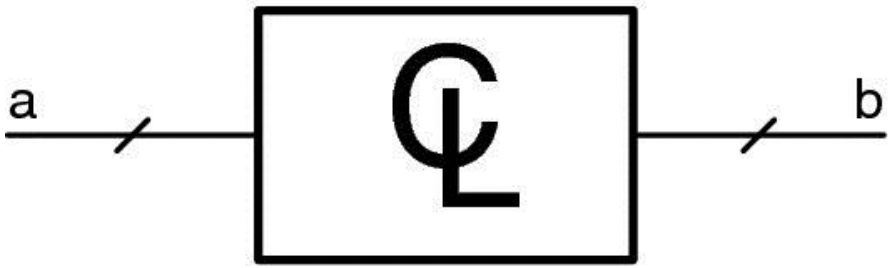
- FSM have two constraints: A maximum delay and a minimum delay
- Doesn’t have to be as fast as possible-balance
- Each flip-flop and gate has a delay
- Can continue into the next state…
- Think of a state machine,
  - running forever,
  - but with sloppy timing
  - It will fail at some point.



Propagation and Contamination Delay

- Between clock cycles, the signal can go through an arbitrary number of transitions
- How long does output retains its initial stable value from the last clock cycle *after* the input arrives with a new value. This is the *contamination delay.*
- How long does it take for the output to become the value of the input. This is the *propagation delay*.

Propagation and Contamination Delay

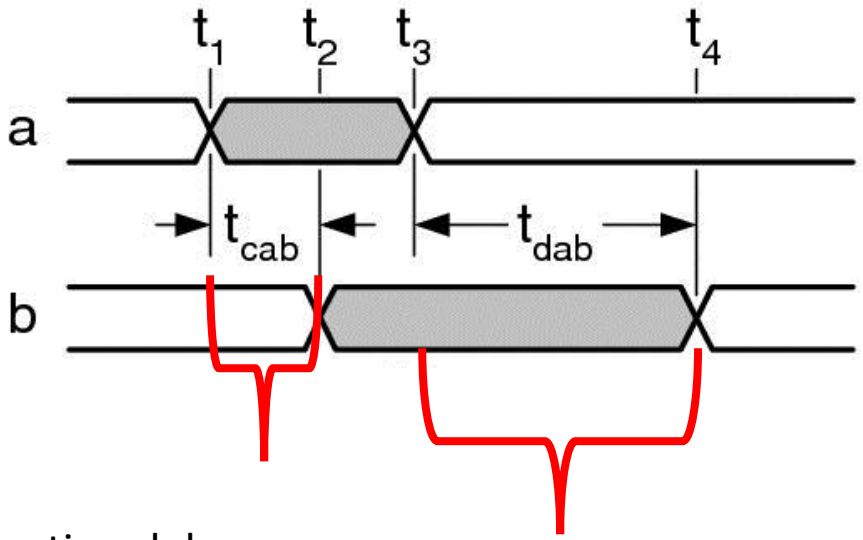


Value arrives at
t1 on wire a

Value steady
at t3 on wire a

Value changes
at t2 on wire b

Value steady
at t4 on wire b



d represents propagation
c represents contamination

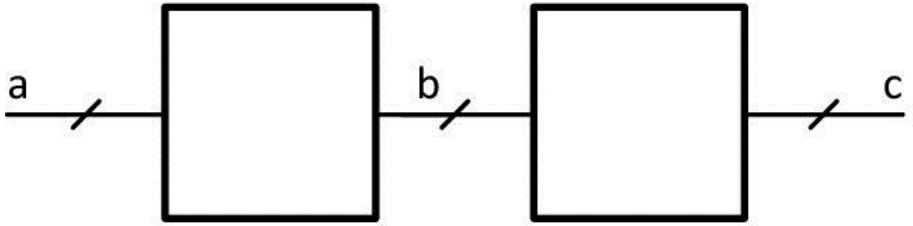
Contamination delay
(c of ab)

Propagation Delay
(d of ab)

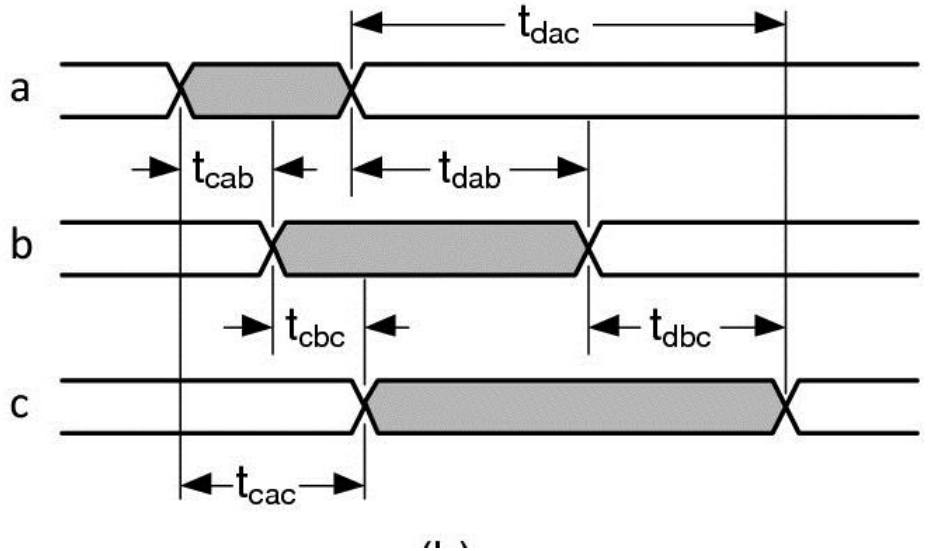
Propagation and Contamination Delay

- Notation:
- t_{dab}=time of propagation from wire *a* to wire *b*
- t_{cab}=time of contamination from wire *a* to wire *b*

Propagation and Contamination Delay

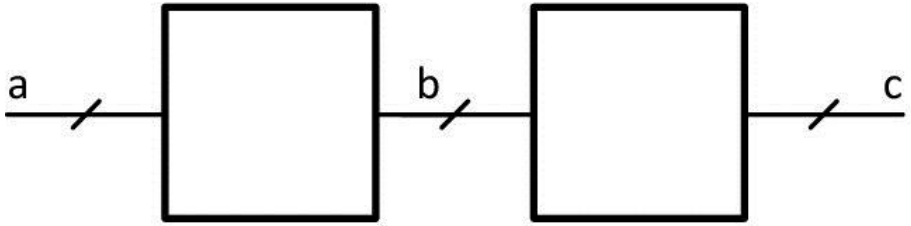


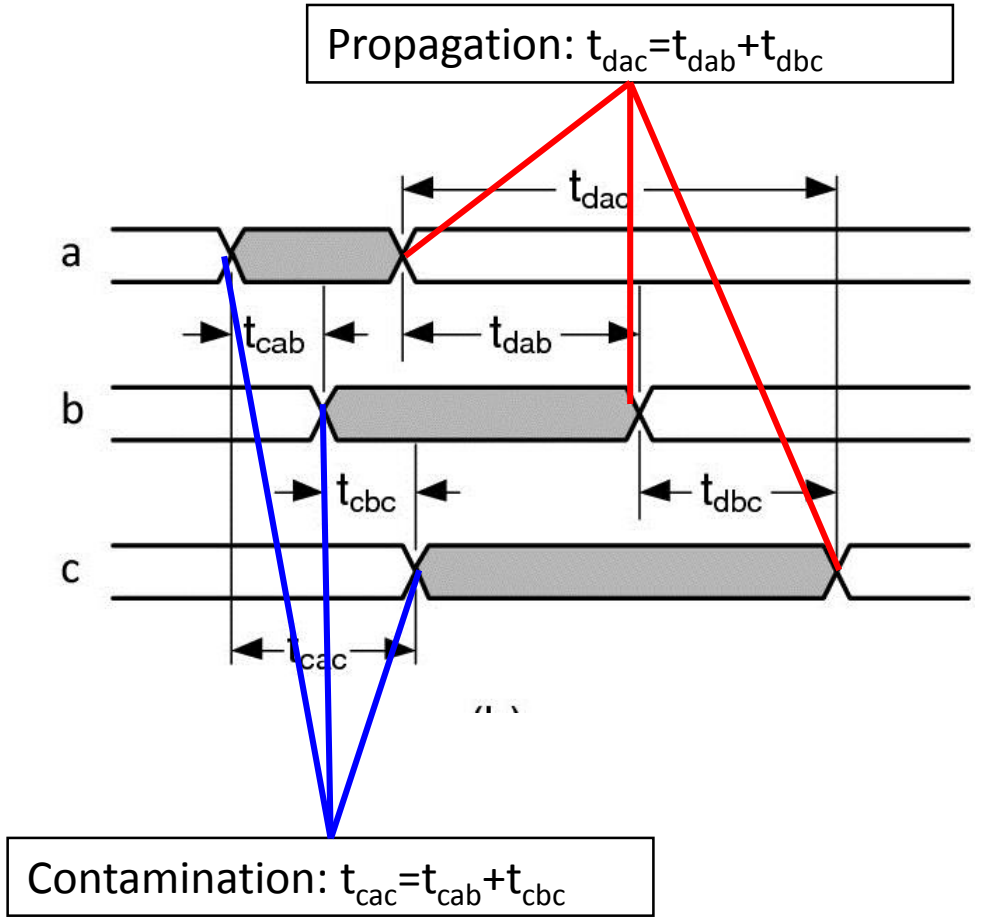
Propagation: $t_{dac}=t_{dab}+t_{dbc}$



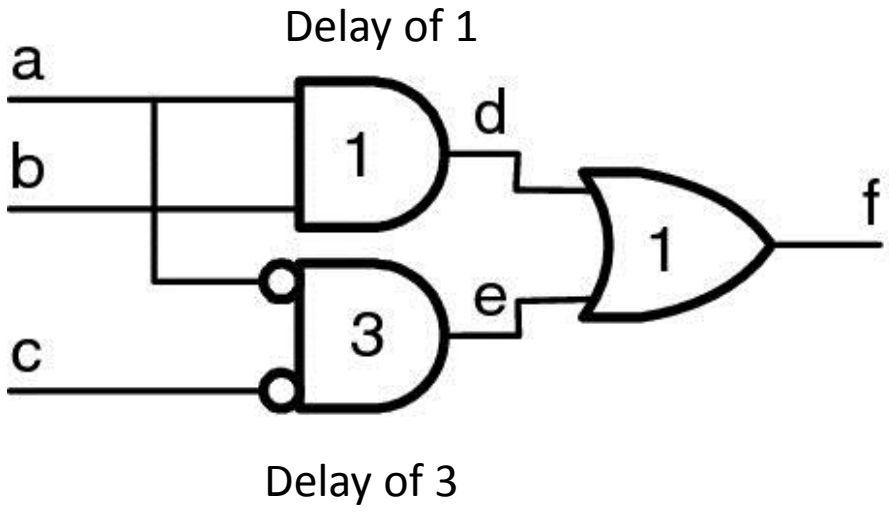
Contamination: $t_{cac}=t_{cab}+t_{cbc}$

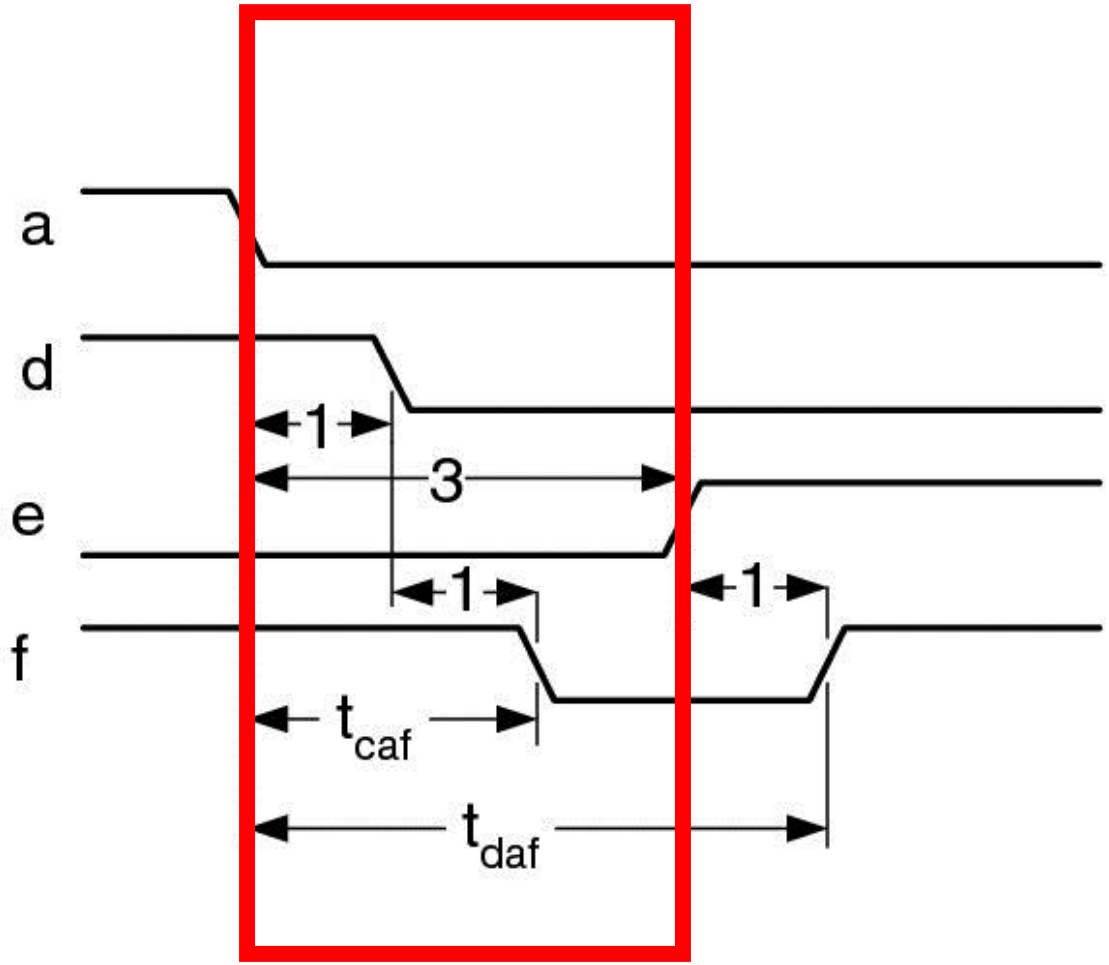
Propagation and Contamination Delay





A Hazard



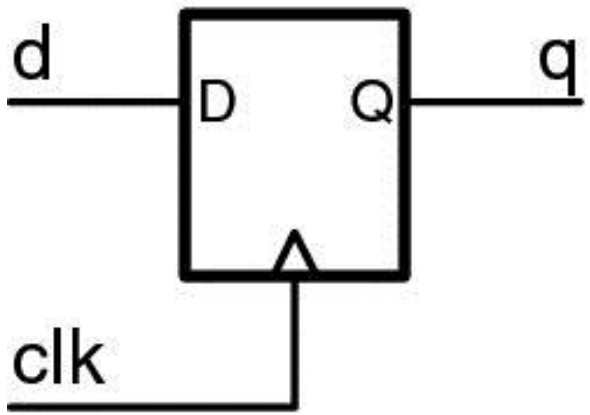


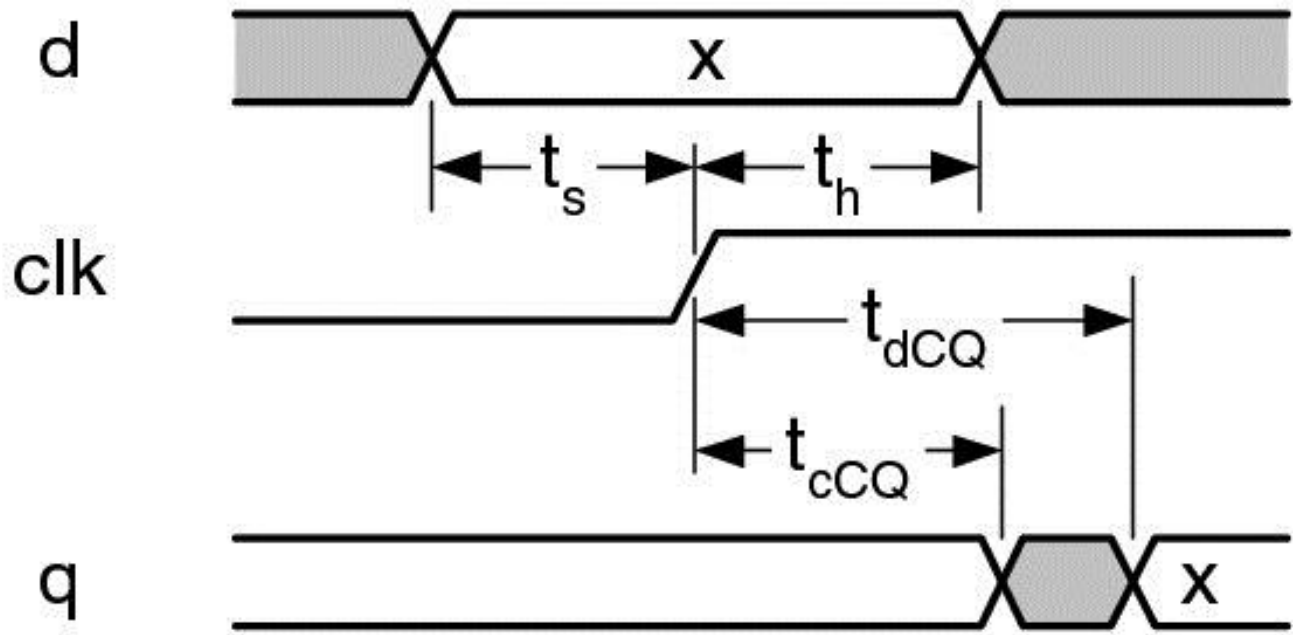
D has two values before E can finish
Cascades so F has two values in the same cycle
The *intermediate* value is not steady
Very bad for holding a steady state!

The D Flip-Flop

- A multi-bit flip-flop is a *register*
- Updates on the rising edge of the clock
- Treat D Flip-Flops as *black box*, the insides unknown
- Input must be stable for some setup time t_s
  - Before the clock cycle reaches its midpoint…
  - The data must be stable for hold time t_h
  - If the propagation delay or the contamination delay interferes with these times, the flip-flop does not keep the value

The D Flip-Flop





Huh? Need words.

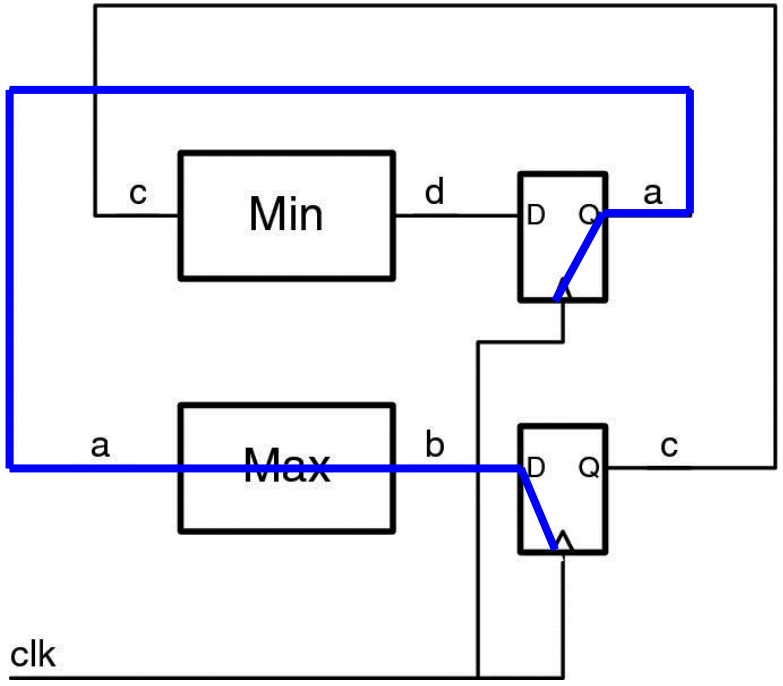
- The Flip Flop starts changing its value at the point between the setup time and the hold time.
- Starting from the setup time, the Flip Flop will hold its old value until the contamination delay has passed
- Now, the Flip Flop is unstable, and could be either the old or new value
- Once the propagation delay has passed, the Flip Flop has the new value.
- It’s a balancing act…if done correctly, the flip-flop behaves as remembering the new value

Setup Time and Hold Time Constraints

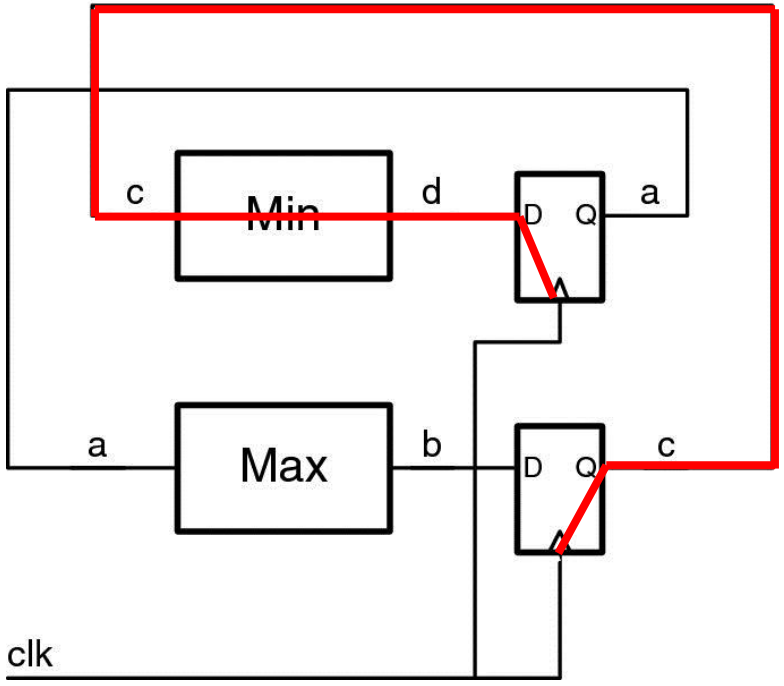
- Let t_{cy} be the time of a clock cycle. It must be long enough to work.
- $t_{cy} \geq t_{dcq} + t_{dMax} + t_s$
- Where t_{dMax} is the maximum propagation of the flip flop
- $t_h \leq t_{cCQ} + t_{cMin}$
- Where t_{cMin} is the minimum contamination of the flip-flop
- If these conditions are not met, the flip-flop cannot have a stable state.

Setup Time and Hold Time Constraints

Setup Time Constraint



Hold Time Constraint



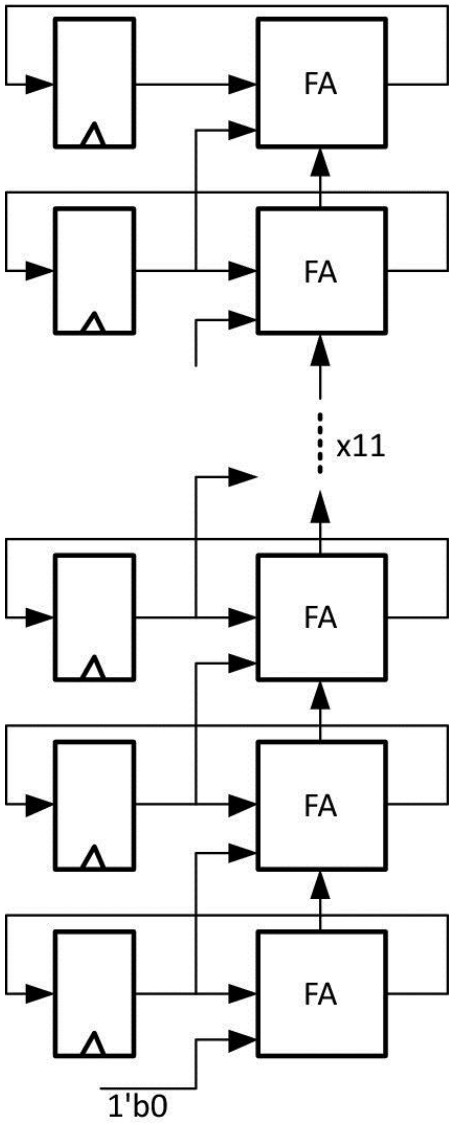
Setup Time and Hold Time Constraints

- If the path is too slow, the next clock edge may arrive at the lower flip flop before the input value b has stabilized.
- The sum of the propagation delays along the maximum path and setup time must be less than one cycle.
- If the path is too fast, the value input to the upper DFF may change before the clock signal arrives.
- The sum of the contamination delays along the minimal path must be larger than the hold time.

Clock Skew

- In an ideal case (or in a simulator like Verilog) the clock signal would change all the flip flops all at the same time.
- Not really true: length of wire, temperature, type of chip, type of gate can affect timing
- There is a slight variation…the *clock skew*
- $t_{cy} \geq t_{dcq} + t_{dMax} + t_s + t_k$
- $t_h \leq t_{cCQ} + t_{cMin} - t_k$
- Circuity needs a tolerance to handle the skew.

Example: Nothing is ever simple



Example: Nothing is simple

- Given a 16-bit state machine where the next state is the current state multiplied by 3.
- A full-Adder will compute the sum of the two values and store it in the flip-flops.
- Full Adder contamination delay is 10 ps (t_{cMin}), and a propagation delay is 30 ps
- The minimum delay between flip-flops is 10 ps
- The maximum propagation delay is 16*Full Adder is therefore 16*30 or 480 ps. (t_{dMax})

Ps?

- Post script?
- Priory of Scion?
- Nope-picosecond, or 10^{-12} seconds
- How far can light travel in one picosecond?

Unit	Measure
Speed of Light	3x108 meters per second
Milli	10^{-3}
Micro	10^{-6}
Nano	10^{-9}
Pico	10^{-12}

Example: Nothing is simple

- Given
- The flip flops have a contamination delay of 10 ps (t_{cCQ})
- The flip flops have a propagation delay of 20 ps (t_{dcq})
- The flip flops have a holding time of 10 ps (t_h)
- The flip flops have a setup time of 20 ps (t_s)

Example: Nothing is simple

- Does the hold-time constraint work?
- $t_h \leq t_{cCQ} + t_{cMin}$
- Flip-flop hold time <= flip flop contamination delay + contamination delay of one full adder
- $10 \leq 10 + 10$
- $10 \leq 20$
- Yes

Example: Nothing is simple

- Does the setup-time constraint work? What is the cycle time?
- $t_{cy} \geq t_{dcq} + t_{dMax} + t_s$
- $t_{cy} \geq 20 + 480 + 20$
- $t_{cy} \geq 520$

Example: Nothing is simple

- What if put in a clock skew(t_k) of 20?
- $t_h \leq t_{cCQ} + t_{cMin} - t_k$
- $10 \leq 10 + 10$**-20**
- $10 \leq 0$
- No, clock skew would violate constraint
- What would happen?
- Too fast-> The value arriving at the flip flop would change before becoming stable

Example: Nothing is simple

- The contamination delay has to be increased to slow down the path of the circuit.
- For example, adding in an and gate with a contamination delay of 10 ps.
- With both inputs of the and tied to the single sum of the full adder

Example: Nothing is simple

- Adding in an extra 10 ps…
- $t_h \leq t_{cCQ} + t_{cMin} - t_k + t_{andgate}$
- $10 \leq 10 + 10$**-20+10**
- $10 \leq 10$
- Working again

Example: Nothing is simple

- What about the cycle?
- $t_{cy} \geq t_{dcq} + t_{dMax} + t_s + t_k + t_{andgate}$
- $t_{cy} \geq 20 + 480 + 20 + 20 + 10$
- $t_{cy} \geq 550$ ps

Example: Nothing is simple

- So, what is the frequency of the clock?
- If a cycle is 520 ps…
  - 5.2^{-10} seconds…
  - 1.9231 GHz (Giga is 10^9)
- If a cycle is 550 ps…
  - 5.5^{-10} seconds…
  - 1.8181 GHz (Giga is 10^9)