# Sequential Circuits

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CS 4341

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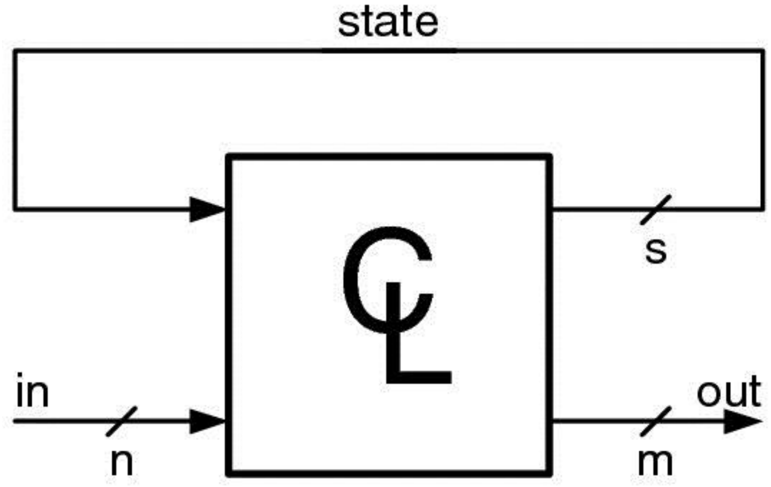
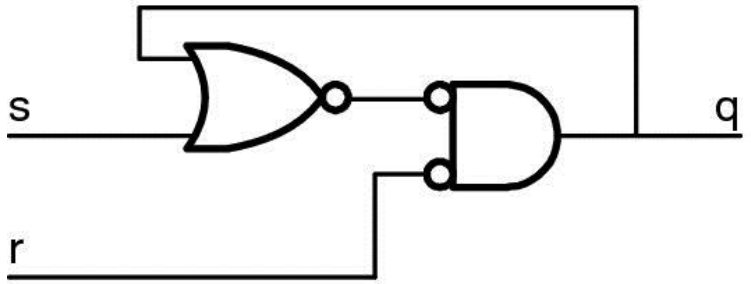
# Sequential Circuits

- Sequential Circuits have Feedback.
- Output depends on current input
- AND the history of previous inputs
- This feedback is referred to as the *state*.
- $out$ =f(in,state)
- $q_{new} = \bar{r} \wedge (s \vee q_{old})$





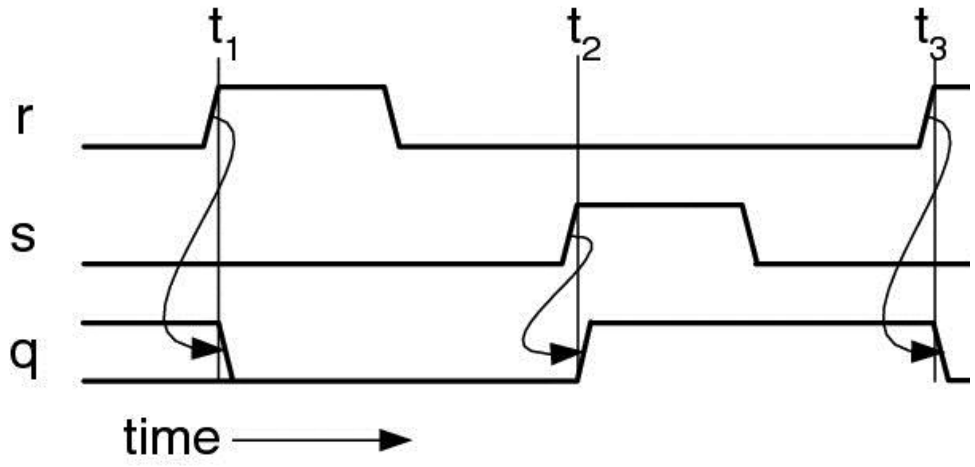
# Sequential Circuits

- This is a flip-flop
- The logic may denote the circuit change
- But the value is depended on the input history.
- If R is true, then block is reset.
- If R is false, Depends on S and Previous State.
- This is a flip-flop

| Qold | R | S | Qnew |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
|  |  |  |  |

# Sequential Circuits

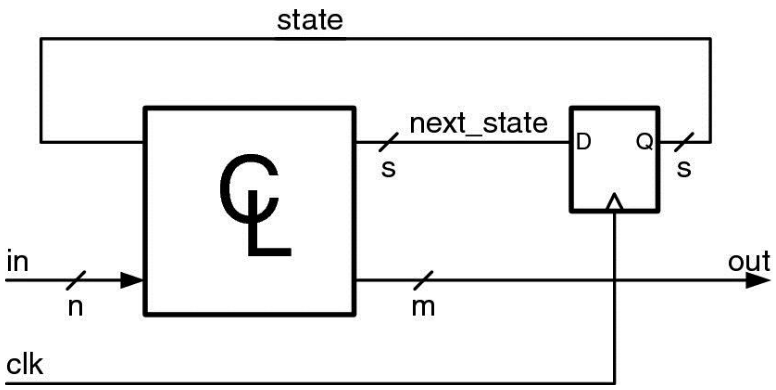
- q starts off at an unknown state
- When r resets (goes high), q will fall to 0 at t1
- When S becomes a high input at t2, q will go t o1
- At t3, reset again.
- After reset, and S is high, Q remains high until reset
- Q remembers its value
- This is called a *timing diagram*

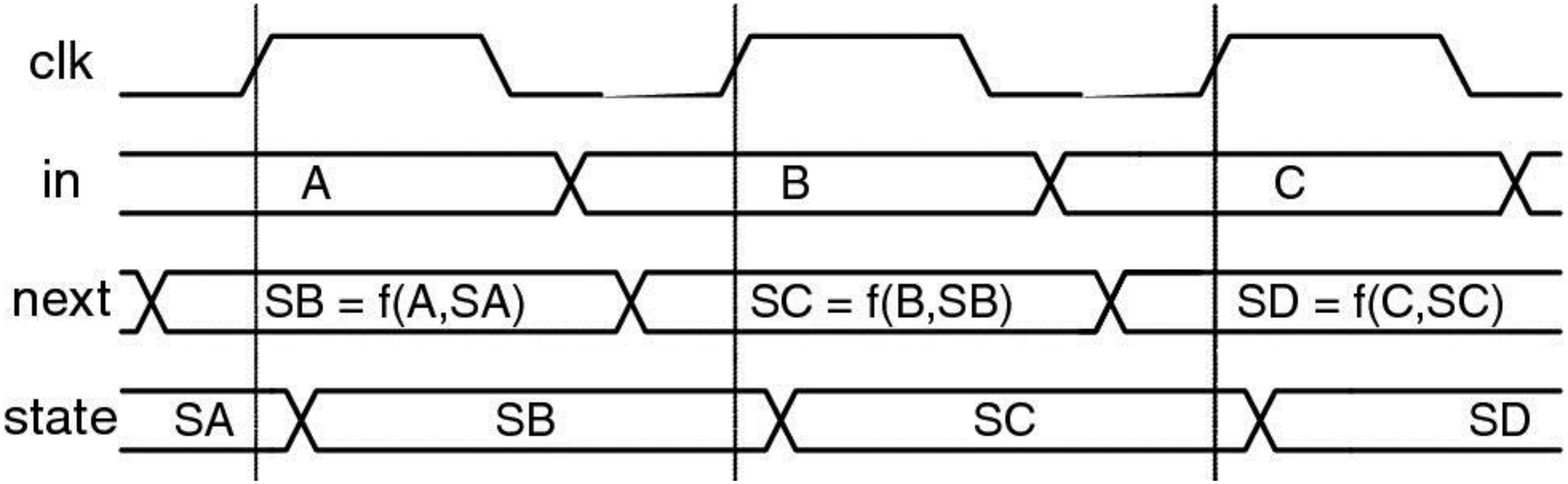


# Synchronous Sequential Circuits

- The signal for the state change can occur at any time
- These are referred to as races
- For now, sequential circuits are *synchronous* with a control clock
- State changes are only on the clock signal, and this allows sequential circuits to behave as *finite state machines*. (FSM)

# Synchronous Sequential Circuits





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# Synchronous Sequential Circuits

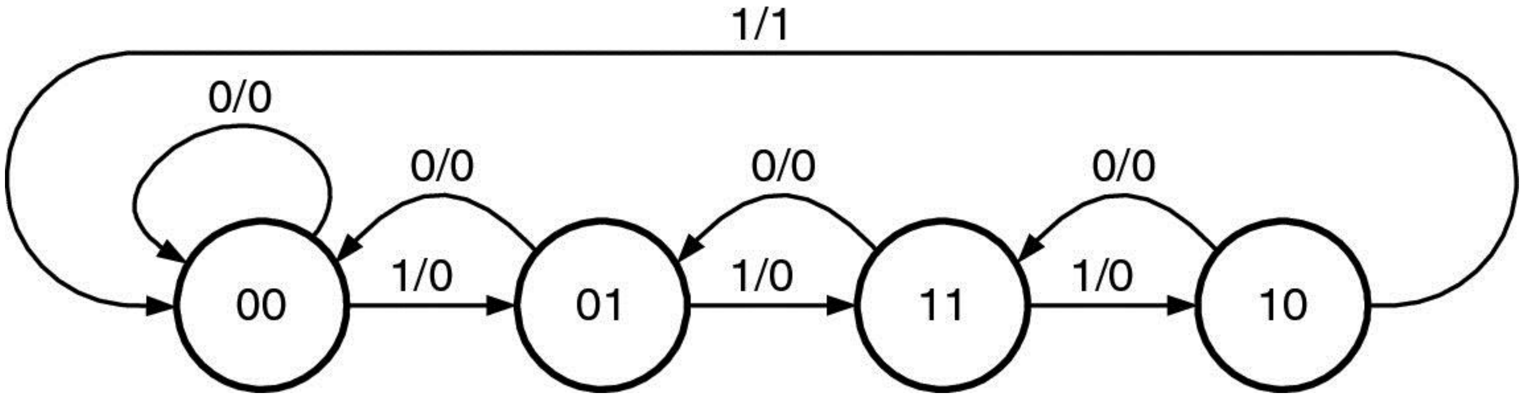
- This means that a circuit can handle a regular expression
- Can it recognize a sequence?
- Give a cycle (clock), and a set of states, can it recognize a pattern?

# 14.2

| Clk | State | In | Out |
|---|---|---|---|
| 0 | 00 | 0 | 0 |
| 1 | 00 | 1 | 0 |
| 2 | 01 | 1 | 0 |
| 3 | 11 | 0 | 0 |
| 4 | 01 | 1 | 0 |
| 5 | 11 | 1 | 0 |
| 6 | 10 | 0 | 0 |
| 7 | 11 | 1 | 0 |
| 8 | 10 | 1 | 1 |
| 9 | 00 |  | 0 |

A State Table

A State Diagram



Each circle is a state with a label.
00 Is the start state.
Each arrow is a transition
The numerator is the input signal
The denominator is the output signal
In this case, four 1,1,1,1 yields 0,0,0,1
What other patterns would be recognized?
Are there any?