CS 4341  
Fall 2017  
Homework #6

Assigned: November 28, 2017

Due: December 4, 2017, End of Day

# Breakdown:

* **Chapter 22: Interface and System-level Timing (24 points)**
* **Chapter 23: Pipelines (28 points)**
* **Chapter 24: Interconnect (24 points)**
* **Chapter 25: Memory Systems (24 points)**

## Chapter 22 (24 points)

D22.1 Define Always Valid Timing (3 points)

D22.2 Define Periodically Valid Timing (3 points)

D22.3 Define Flow-control timing (3 points)

22.1 *Always Valid Timing:* Aside from sensors and games, give three other examples of where “always valid timing” is used. (5 points)

*Note: You may refer to games and sensor sets if you include a short description.*

22.2 *Periodically valid timing* Aside from what was mentioned in the text, give three examples of where periodically valid timing is used (5 points).

*Note: You may not refer to a Data Encryption Standard (DES) Cracker*

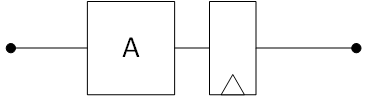
22.3 *Flow-Controlled timing.* Aside what is mentioned in the text, give three examples of where timing with flow control is used. (5 points)

*Note: You may not use a music synthesizer for an example.*

## Chapter 23 (28 points)

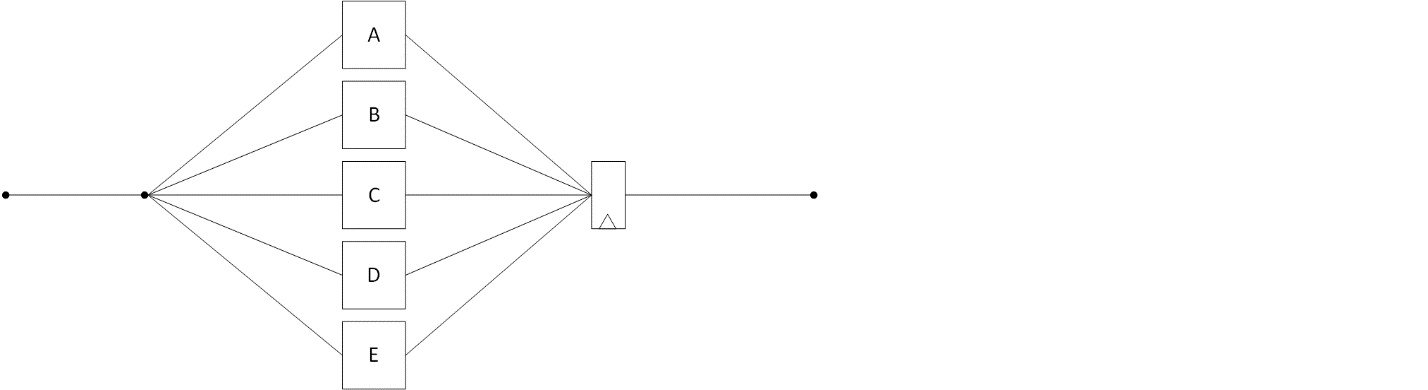
23.1 Latency and throughput, I. Assume that a module has a latency of 20 ns and that treg=500 ps. including the output register, what are the latency and throughput of this module? (6 points)

Additional: As a baseline case. One module, One Register



23.2 Latency and throughput, II. Assume that a module has a latency of 20 ns and that treg=500 ps. Including the output register, what are the latency and throughput of this module when replicated 5 times? (6 points)

Additional: As a parallel case/replicant case. Five modules, One Register



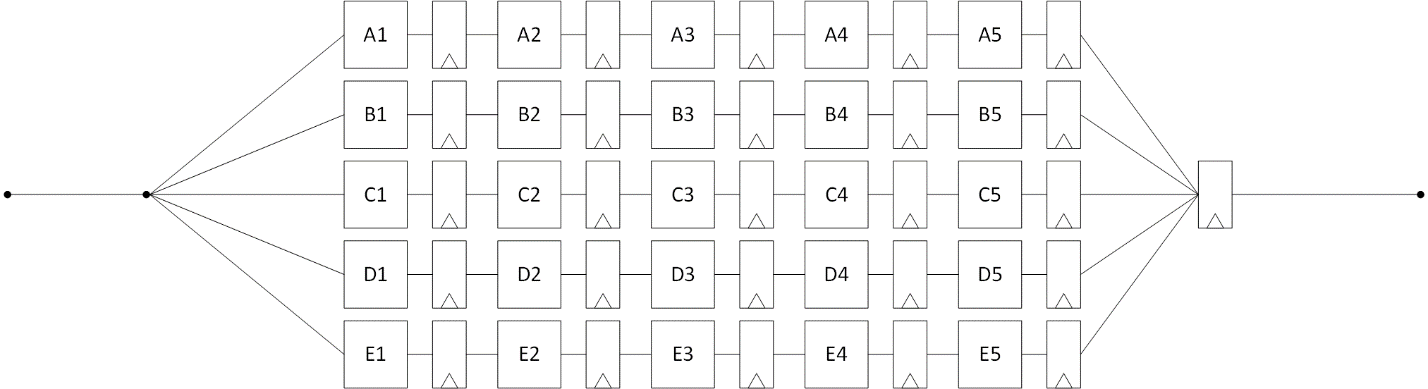
23.3 Latency and throughput, III. Assume that a module has a latency of 20 ns and that treg=500 ps. Including the output register, what are the latency and throughput of this module when pipelined into five equal stages? (6 points)

Additional: As a pipeline case, One module, Five Registers



23.4 Latency and throughput, IV. Assume that a module has a latency of 20 ns and that treg=500 ps. Including the output register, what are the latency and throughput of this module when pipelined into five equal stages, and then this pipeline is replicated five times? (10 points)

Additional: Messy. Each pipeline is one module, 5 registers. Each replicant is a pipeline. The final results are into a final register. Five Modules. Six Registers. Double form….



## Chapter 24 Interconnect (24 points)

D24.1 Define bus (3 points)

D24.2 Define crossbar-switch (3 points)

D24.3 Define interconnection network (3 points)

D23.4 Define router (3 points)

D24.5 Define channel (3 points)

D24.6 Define topology (3 points)

D24.7 Define routing algorithm (3 points)

D24.8 Define flow-control (3 points)

## Chapter 25: Memory Systems (24 Points)

D25.1Define capacity (3 points)

D25.2 Define latency (3 points)

D25.3 Define bandwidth (3 points)

D25.4 Define primitives (3 points)

D25.5 Define bit-slicing (3 points)

D25.6 Define banking (3 points)

D25.7 Define interleaving (3 points)

D25.8 Define cache (3 points)