AIP Applied Physics Letters

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Citation: Applied Physics Letters **104**, 083110 (2014); doi: 10.1063/1.4866785
View online: http://dx.doi.org/10.1063/1.4866785
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/104/8?ver=pdfcov
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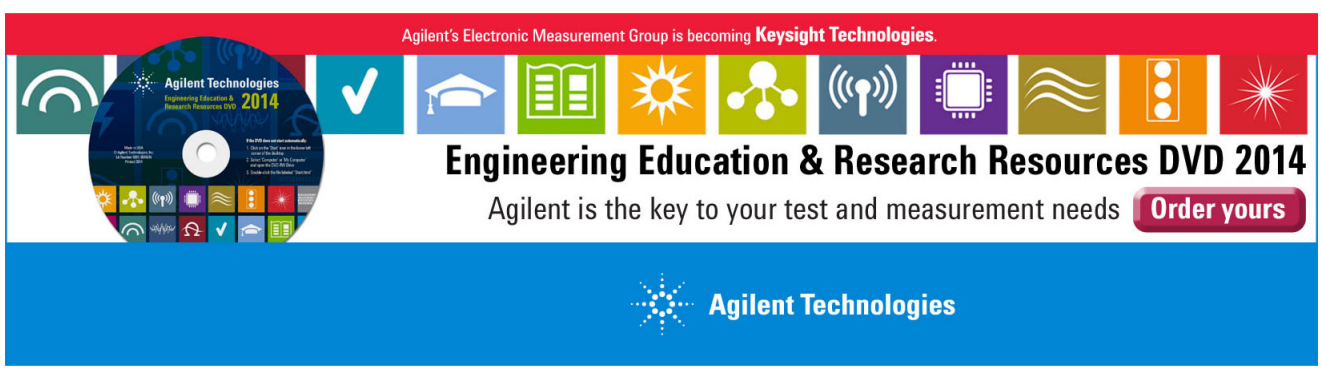

Analysis of flicker noise in two-dimensional multilayer MoS_2 transistors

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(Received 27 November 2013; accepted 6 February 2014; published online 25 February 2014)

Using low-frequency noise (LFN) analysis, we examined the quality of the semiconductor, oxide, and oxide–semiconductor interface of back-gated multilayer MoS_2 transistors. We also investigated the mechanism of the LFN and extracted γ exponents from the LFN behavior, $1/f^{\gamma}$; the value of γ was >1 at negative gate bias because of active slow traps. As V_G increased, the slow traps were filled and thus γ decreased, stabilizing at ≈0.95. Various other parameters extracted from the LFN indicated that the carrier number fluctuation (Δn) model was the dominant origin of the LFN. The multilayer MoS_2 structure had better noise immunity than a single-layer case in air. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4866785]

Much progress has been made in flexible, stretchable electronics, including human-inspired electronics, and wearable electronics. These advances are arguably most useful in displays, including televisions—the anticipated shift to flexible, stretchable displays can be considered an extension of the current trend toward miniaturization in which cathode ray tubes have been supplanted by flat-panel displays—but it continues to expand into other applications. To meet future demands, the driving electronic circuitry of displays must have high performance, low power consumption, ultra-high resolution, and high frame rate. Developing transistors with high field-effect mobility will be a key to satisfying these requirements, as increasing brightness and decreasing bus-line load power consumption.

Recently, the application of MX_2 (M = Mo, W; X = S, Se, Te) transition metal dichalcogenides (TMDs) as electronic materials has offered an exciting pathway to practical nanoscale electronics. Among the TMDs, MoS_2 is especially promising. Its properties include high carrier mobility (up to 500 $cm^2\ V^{-1}\ s^{-1}$), very thin atomic thickness (6.5 Å), and a relatively large bandgap (1.3–1.85 eV), leading to good switching behavior and mechanical flexibility.[1,2] It can be fabricated into transistors using standard top-down nano/micro-fabrication processes, and its excellent transport properties and two-dimensional (2D) nature enable strong control of its carrier density by gate bias. Therefore, 2D semiconducting MoS_2 may open a class of thin-film transistors (TFTs),[1] integrated circuits,[3] and sensors[4,5] with performance far superior to devices made from current flexible semiconductors (e.g., organic semiconductors and solution-processed inorganic semiconductors) and even silicon. In TFTs, multilayer MoS_2 may be superior to single-layer MoS_2 because of its higher density of states and the presence of multiple conducting channels.[6]

Low-frequency noise (LFN) analysis can help analyze the quality of semiconductors, oxides, and oxide–semiconductor interfaces. This technique measures conductivity fluctuations in the transistor channel; these fluctuations can be caused by mobility fluctuations from phonon scattering or/and Coulombic scattering or by carrier trapping and de-trapping.[7] Electrical noise limits the signal-to-noise ratio (SNR) of a device, particularly for the sensor applications. In such small size regimes, as the surface-to-volume ratio of 2D layered semiconductor devices increases, surface adsorbates and atomic-scale structural fluctuations greatly influence their electronic noise.[8] Many researchers have explored nanostructured devices (0D to 2D) and investigated their low-frequency electrical noise, where $1/f$ noise (also known as flicker noise) dominates.[9–12]

While $1/f$ noise has been studied in monolayer MoS_2 transistors,[13] electronic noise in devices fabricated from multilayer semiconducting MoS_2 has not yet been explored. To further optimize multilayer MoS_2-based devices, we must better understand their transport mechanisms and semiconductor/dielectric interfacial properties. In this Letter, we report on the fabrication and performance of multilayer MoS_2 field-effect transistors (FETs) and examine the quality of their interface as well as the energy distribution of carrier trapping/scattering sites by measuring LFN. Based on these observations, we discuss the origin of the $1/f$ noise in these devices.

Fig. 1(a) shows a cross-sectional schematic of a multilayer MoS_2 FET. To fabricate these FETs, a 300-nm-thick SiO_2 dielectric layer was first deposited by thermal chemical vapor deposition on a heavily doped p-type Si wafer (resistivity $< 5 \times 10^{-3}\ \Omega\cdot$cm). Bulk MoS_2 crystals (SPI Supplies, USA) were mechanically exfoliated to obtain the multilayer MoS_2 flakes. These flakes were transferred onto the SiO_2 layer to form a semiconducting channel. The source and drain were Ti/Au electrodes (10/300 nm) deposited by electron-beam evaporation at room temperature. To pattern the source and drain, conventional ultraviolet (UV) photolithography and lift-off were used. A confocal laser microscope (LEXT OLS4000, Olympus) was used to image the structure, as shown in Fig. 1(b). The thickness of the

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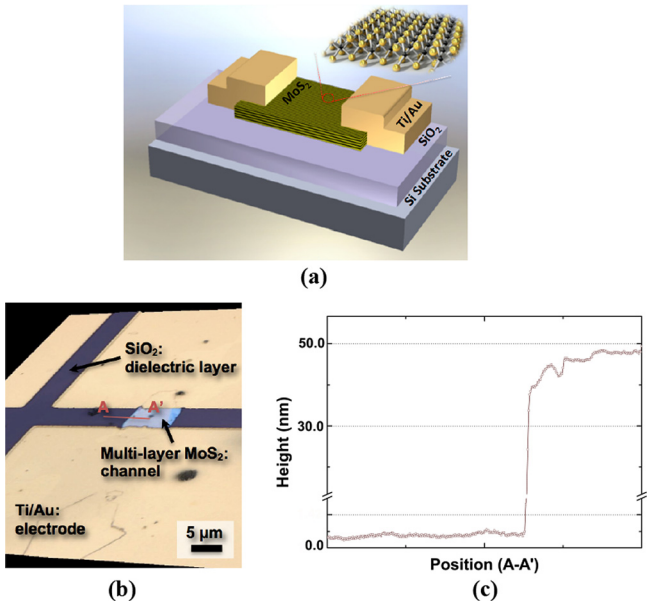

FIG. 1. Structure of the multilayer MoS_2 FET and representative characteristics: (a) cross-sectional schematic of a multilayer MoS_2 FET with a 300-nm-thick SiO_2 gate dielectric. (b) Top-view 3D confocal laser micrograph of a fabricated multilayer MoS_2 transistor ($L_{ch} = 5\,\mu$m, $W = 6.9\,\mu$m). (c) Atomic force microscopy height profile of a mechanically exfoliated multilayer MoS_2 flake (shown in (b) as the A′–A region, marked by an arrow).

exfoliated MoS_2 channel was 40–50 nm, measured by atomic force microscopy, as shown in Fig. 1(c).

We measured the 1/*f* noise in the power spectral density (PSD) of the drain current in the multilayer MoS_2 FETs in the following way. The current fluctuation across the device was amplified with a low-noise transimpedance amplifier (BTA9812B), and the 1/*f* noise was characterized by a spectrum analyzer (HP 35670A). DC bias for the TFTs during the 1/*f* noise measurement is provided by a semiconductor parameter analyzer (HP 4156) through low pass filters ($f_{3dB} = 1$ Hz). Fig. 2 shows the transfer and output characteristics of the MoS_2 FETs. The transistors exhibited good switching behavior ($I_{on}/I_{off} > 10^5$), and the linear relationship between the drain current and voltage (Fig. 2(b), inset) demonstrates that the effect of the source/drain (S/D) Schottky barrier was minimal. The PSD was measured in linear mode operation to more uniformly distribute the carriers along the channel. The measured linear mobility was 20.27 $cm^2\ V^{-1}\ s^{-1}$. All electrical measurements were performed in air at room temperature.

Fig. 3(a) shows the measured normalized drain-current PSD of the FETs after background chamber noise is subtracted. The gate bias ranged from −15 V to 25 V over 5 V increments, a wide enough range to cover various operation regions, from the subthreshold region to the fully ON region. It is important to cover these operation regions because carrier transport and noise characteristics are affected by changes in the active trap distribution, which is modulated

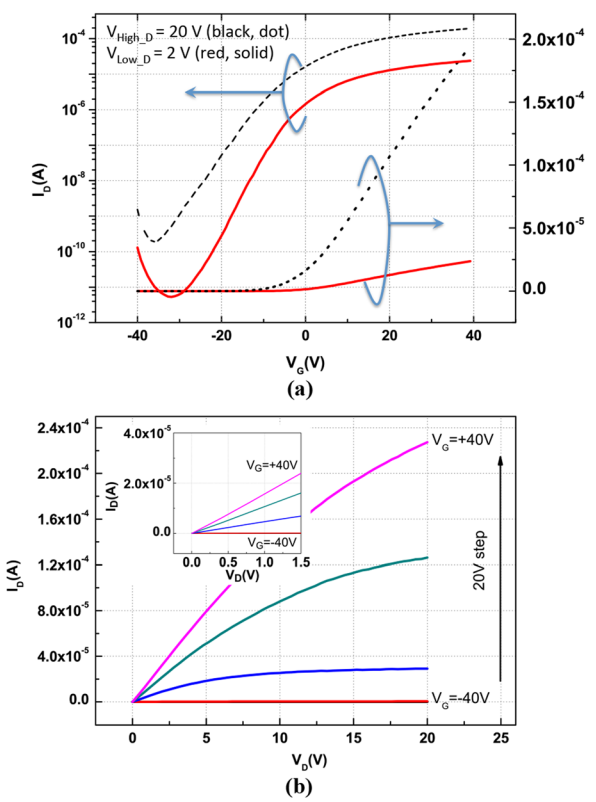

FIG. 2. Representative characteristics of the multilayer MoS_2 FETs for various drain and gate voltages: (a) transfer characteristics and (b) output characteristics; the inset shows the output characteristics in the linear region.

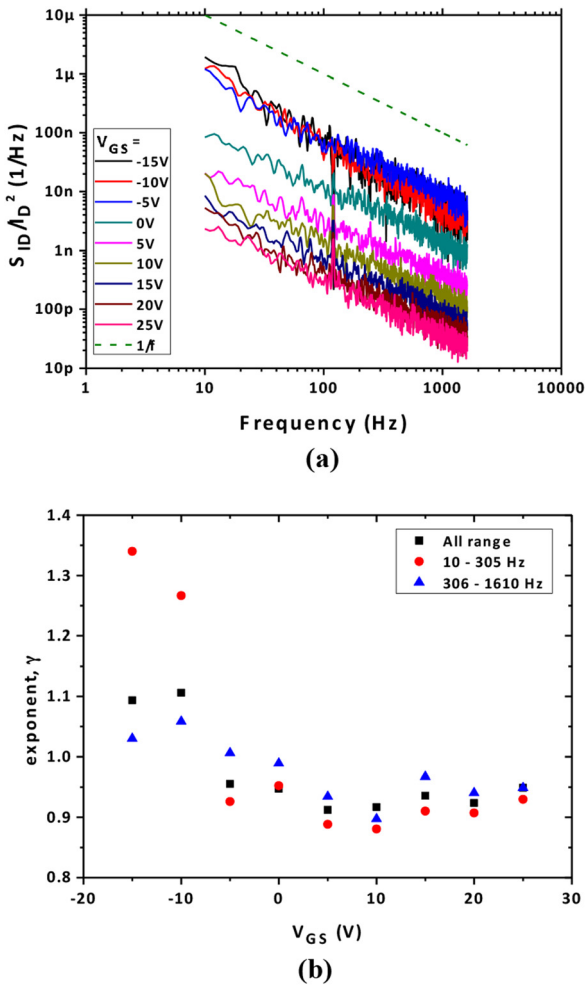

FIG. 3. (a) Normalized drain-current PSD of multilayer MoS_2 TFTs at various gate biases and a constant drain bias of 2 V, measured from 10 to 1610 Hz in 1 Hz increments. (b) Values of the γ exponent from $1/f^{\gamma}$, extracted from the PSD results in (a).

by Fermi level shifts. In these FETs the noise decreased monotonically with frequency, matching typical LFN behavior ($1/f^{\gamma}$). By carefully analyzing the measured noise, though, we found that γ depended on the gate bias, as shown in Fig. 3(b). At negative gate bias (i.e., lower than V_{th} in this device), γ was >1, but as V_{GS} increased and became greater than V_{th}, γ decreased and eventually stabilized to ≈0.9. To improve the accuracy of the extracted value, we extracted γ from the normalized PSD over full and partial ranges of the measured frequencies, but all measured data had the same trend. The γ exponent is an important parameter, that is, closely related to the trap distribution, an origin of flicker noise.[14–16] D'yakonova *et al.* showed how $1/f$ noise is connected to the structural quality of the semiconductor used; they found that, as more structural defects were introduced to GaAs by uniaxial stress, the noise level of the FET increased and the slope of the 1/f noise became steeper. Dimitriadis *et al.* showed in their LFN measurements of polycrystalline silicon TFTs that γ changes with gate bias. In McWhorter's carrier number fluctuation model (Δn) in single-crystalline silicon MOSFETs, the $1/f$ noise was computed by the summation of Lorentzian distributions at different roll-off frequencies; this noise originated from spatially uniformly distributed traps within the gate oxide with different tunneling depths during the trapping/de-trapping process, which was later observed in nanoscale silicon MOSFETs as random telegraph noise.[17–20] These results revealed that if the distribution of relaxation times is nonuniform, the overall noise deviates from the ideal $1/f$ PSD relationship. For example, if slow traps dominate, then lower frequency noise will be amplified, increasing the slope; if fast traps dominate, the reverse occurs. McWhorter's carrier number fluctuation model, modified based on the origin of traps, agrees well with the data measured in the current Letter from the multilayer MoS_2 FETs. Our device contained active slow traps at low gate bias, increasing γ, although the exact origin of these traps is unknown. As V_G increased the Fermi level shifted, filling the slow traps, and decreasing γ, which eventually saturated at ≈0.95.

This result can be supported in other ways. For example, the Hooge parameter (α_H) shown in Eq. (1) is closely related to the degree of the 1/f noise being studied

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H}{N_{total} f^{\gamma}} \frac{1}{f^{\gamma}}, \tag{1}$$

where S_{ID} is the drain-current noise PSD, I_D is drain current, and N_{total} is the total number of free carriers in the sample. Based on N_{total}, defined as $C_{ox}(V_{GS} - V_{th})/q$, where C_{ox} is the total gate capacitance considering area, V_{GS} is the gate-source voltage, and q is the elemental charge, we extracted α_H, as shown in Fig. 4(a). Even when defining threshold voltage (V_{th}) in various ways, the trends remained the same. α_H was extremely large in the subthreshold region and drastically decreased as the gate bias increased until it matched V_{th}. This result supports that the amount of active traps which cause the carrier number fluctuation decreases more significantly below V_{th} since the increased gate bias fills traps; it agrees with the change of the exponent value aforementioned. Note also that α_H gradually decreased as the gate bias increased, even after the γ exponent stabilized beyond a zero bias. Studies have shown that the Hooge parameter can depend differently on gate bias.[11,21] As suggested by the carrier number fluctuation model, we observed that α_H monotonically decreased as V_G increased, rather than remaining constant, as suggested by the mobility-fluctuation model.

Note, in Fig. 3(a) and more clearly in Fig. 4(b), the change in normalized drain-current noise PSD with gate bias (and thus with drain current). This behavior shows that the normalized PSD, an indicator of the relative strength of the drain current noise to the DC drain current signal, was fairly

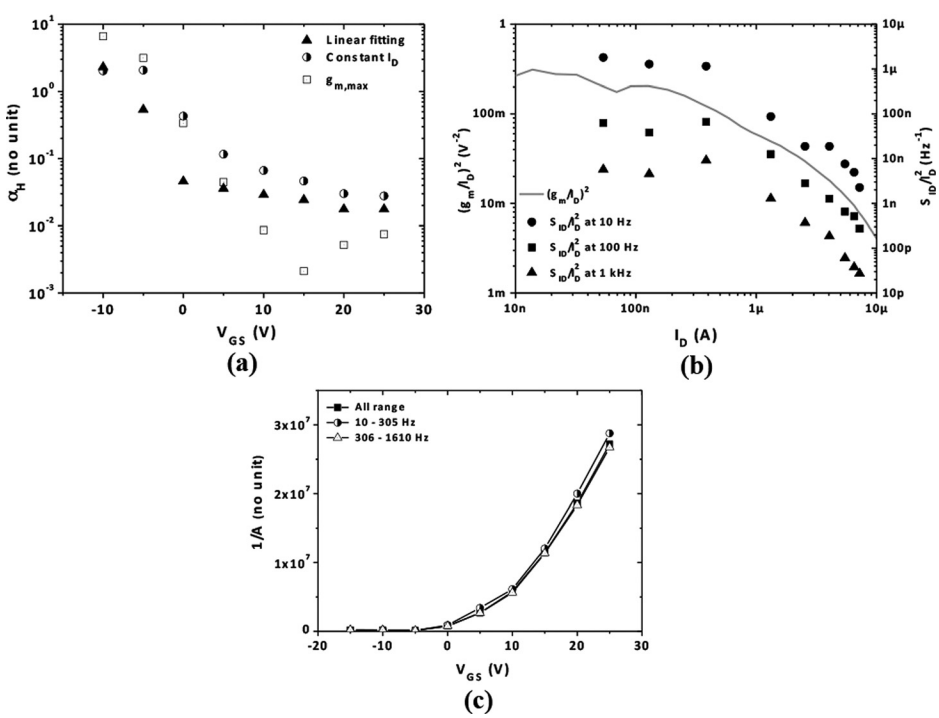

FIG. 4. (a) The Hooge parameter (α_H) as a function of gate bias. (b) $(g_m/I_D)^2$ and normalized drain-current PSD (S_{ID}/I_D^2) as functions of drain current (I_D) at various frequencies. (c) The $1/A$ parameter as a function of gate bias.[11,24]

constant at low drain current and gate bias (the subthreshold region) and began decreasing monotonically as the gate bias increased, increasing the SNR. Based on detailed analyses by Ghibaudo[22] and Ghibaudo *et al.*,[23] the drain current spectral density can be described in terms of contributions from carrier fluctuation (Δn) and mobility fluctuation ($\Delta\mu$) noise

$$S_{ID} = g_m^2 S_{Vg} + g_d^2 S_{Vd}, \text{ or } \frac{S_{ID}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{Vg} + \frac{g_d^2}{I_D^2} S_{Vd}. \quad (2)$$

The form of this equation illustrates how the carrier fluctuation is linked to the gate voltage spectral density (S_{VG}) by carrier trapping/de-trapping in the transconductance (g_m) as well as how the drain-current PSD is correlated through the output conductance (g_d). Therefore, if the Δn mechanism dominated, it would affect the first term of Eq. (2).[24] Fig. 4(b) shows similar trends for both normalized noise and g_m^2/I_D^2, supporting the dominance of the Δn model in these devices.

However, it has recently been reported that the main noise mechanism in single-layer MoS_2 transistors is the mobility fluctuation based on the analysis of extracted 1/A parameter, which also explains how the Hooge parameter is affected by gate bias.[11,13] Note that A parameter is defined from the equation $S_{ID} = A \cdot (I^n)/(f^\gamma)$, where n is the empirically obtained value from Sangwan *et al.*[13] For our multilayer MoS_2 FETs, our analysis of the $1/A$ parameter (Fig. 4(c)) over a broad operation region exhibited a superlinear or near-quadratic relationship with gate bias, an expected behavior if the $1/f$ noise is dominated by carrier number fluctuation (Δn).

In our multilayer MoS_2 FETs, the Hooge parameter in ambient conditions in the fully ON regime was on the order of 10^{-2}; this value is comparable to that measured from single-layer MoS_2 FETs under vacuum and far better than that measured from single-layer MoS_2 FETs in air.[13] The additional layers of MoS_2 on top of the first layer at the gate–dielectric interface may have prevented surface adsorbates from significantly affecting the transistor channel.

In this Letter, we studied the LFN of mechanically exfoliated multilayer MoS_2 transistors. We found that the $1/f$ noise was dominated by carrier number fluctuation. However, we were not able to determine the origin of the active traps, particularly the slow traps left unfilled at low gate biases. These traps must be further studied to optimize the fabrication of these devices in order to improve their carrier transport and SNR. The LFN characteristics of the current multilayer MoS_2 FETs in air were far better than those reported for single-layer MoS_2 FETs in air based on the much smaller Hooge parameter of our multilayer MoS_2 FETs, which provides an additional benefit of using multi-layer structures.

H.-J. Kwon and C. P. Grigoropoulos thank the U.S. Air Force Office of Scientific Research AFOSR/AOARD for Grant No. FA2386-13-4123. This research was supported by the International Research & Development Program of the National Research Foundation of Korea (NRF), funded by the Ministry of Science (Grant No. 2013K1A3A1A32035549) and the Industrial Strategic Technology Development Program (10045145).

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