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| TRƯỜNG ĐẠI HỌC BÁCH KHOA HÀ NỘI  **VIỆN ĐIỆN TỬ - VIỄN THÔNG**  logo_128  **UART**  **Universal Asynchronous Receiver Transmitter**  ***Design Specification***  ***Revision 0.1***  **Sinh viên thực hiện:**   |  |  |  | | --- | --- | --- | | Phạm Ngọc Lâm | : | 20182628 | | Phạm Minh Đức | : | 20172476 |   **GVHD:** TS. Phan Xuân Vũ  **02/12/2021** |

**Design Specification**

**UART**

**Universal Asynchronous Receiver Transmitter**

***Revision 0.1***

**Sinh viên thực hiện:**

|  |  |  |
| --- | --- | --- |
| Phạm Ngọc Lâm | : | 20182628 |
| Phạm Minh Đức | : | 20172476 |

**GVHD:** TS. Phan Xuân Vũ

**02/12/2021**

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**REVISION HISTORY**

|  |  |  |
| --- | --- | --- |
| **Revision** | **Date** | **Description of Changes** |
| 0.1 | 11-17-2021 | Create Specification |
|  |  |  |
|  |  |  |

# Top Module

## Block diagram

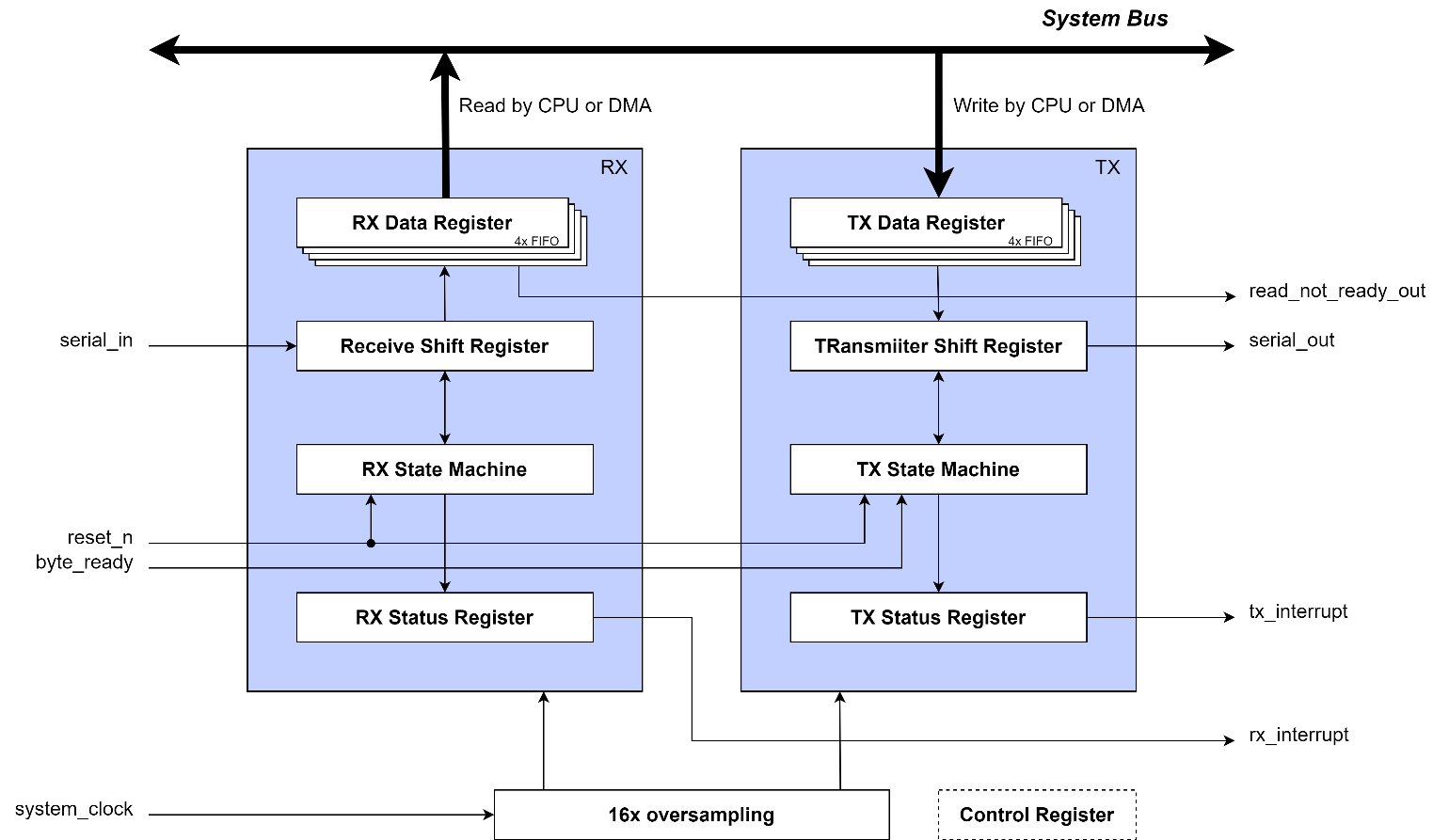


Figure 1. uart\_block\_diagram

## Interface Signals

Table 1. uart\_port\_description

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Width** | **Input/Output** | **Description** |
| Template |  |  |  |
|  |  |  |  |
|  |  |  |  |

## Function Description

**Features:**

* Baud rates 9600, 19200, 57600, 115200 bps
* Detection of Framing, Parity and Overrun errors
* Full Duplex
* 16x oversampling (8x default)
* RX and TX buffers = 4
* 8 bit data
* start- and stop-bits

**UART:**

* UART Transmiiter
* UART Receiver
* UART Clock Generator

**Extended:**

* Auto tuning baud generation
* Various error detections: Stop error, Parity error, Break error and Overflow error.

## Architecture

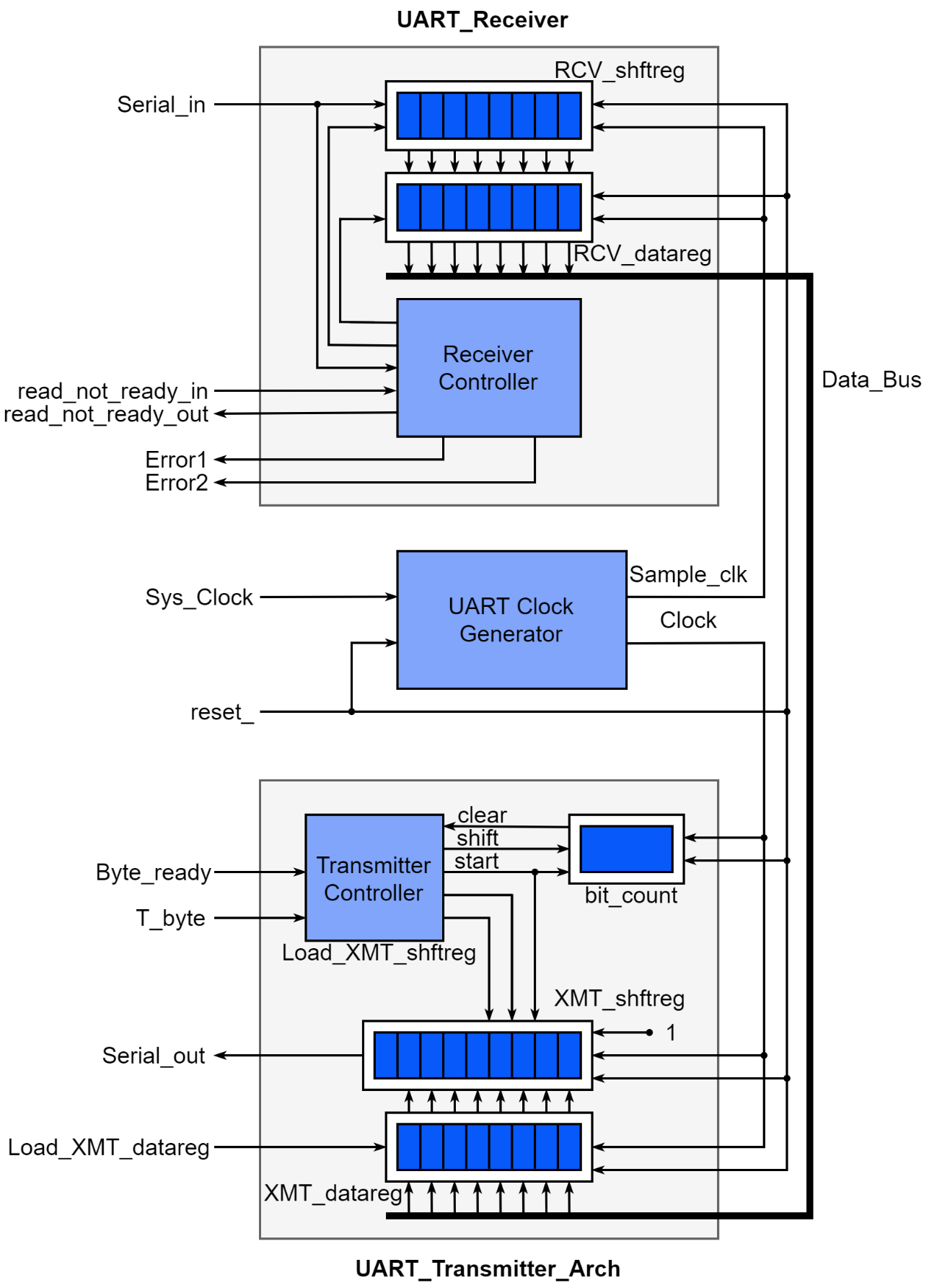


Figure 2. uart\_architecture\_demo

# Sub Module

## uart\_transmitter\_arsyn

### Block Diagram

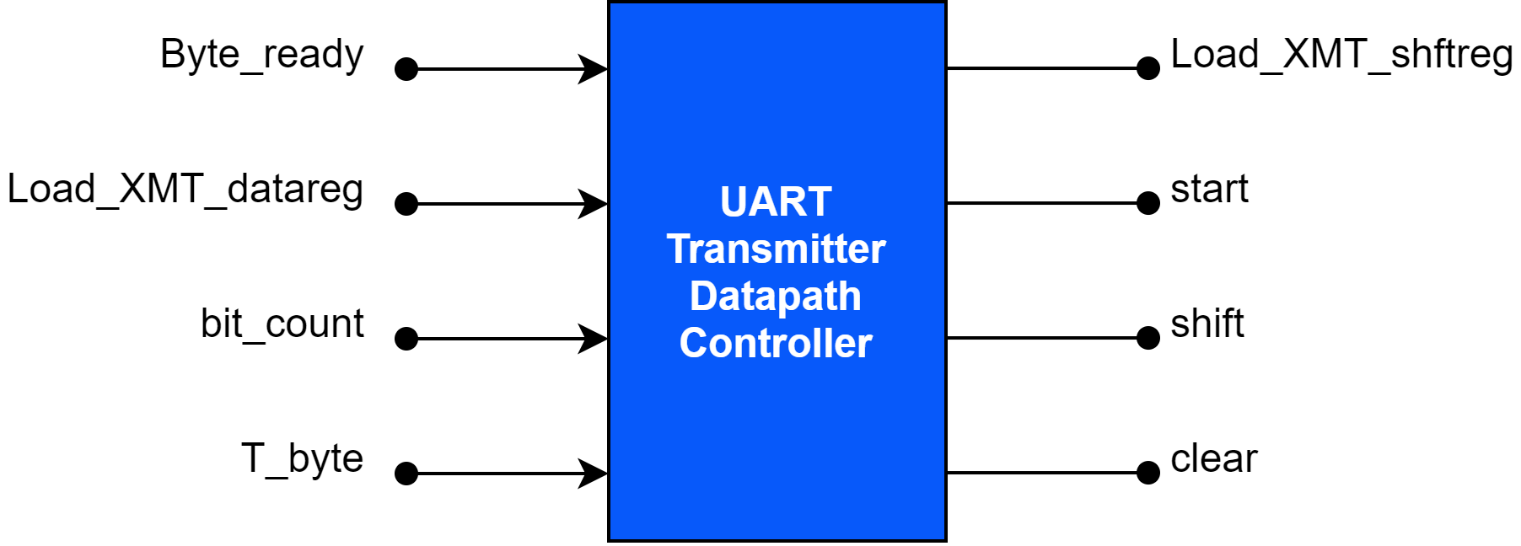


Figure 3. uart\_transmitter\_controller

### Interface Signals

Table 2. Port Description

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Width** | **Input/Output** | **Description** |
| clk | 1 | Input | Clock |
| reset\_n | 1 | Input | Asynchronous reset, active LOW |
| Byte\_ready | 1 | Input | Asserted by host machine to indicate that Data\_Bus has valid data |
| Load\_XMT\_datareg | 1 | Input | Assertion transfer Data\_Bus to the transmitter data storage register, XMT\_datareg |
| T\_byte | 1 | Input | Assertion initiates transmission of a byte of data, including the stop, start, and parity bits |
| bit\_count | bit\_count\_size | Input | Counts bits in the word during transmission |
| Data\_Bus | data\_size | Input | Bus data connect register |
| Load\_XMT\_shftreg | 1 | Output | Assertion loads the contents of XMT\_data\_reg into XMT\_shftreg |
| start | 1 | Output | Signals the start of transmission |
| shift | 1 | Output | Directs XMT\_shftreg to shift by one bit towards the LSB and to backfill with a stop bit |
| clear | 1 | Output | Clears bit\_count |
| Serial\_out | 1 | Output | TX |

### Function Description

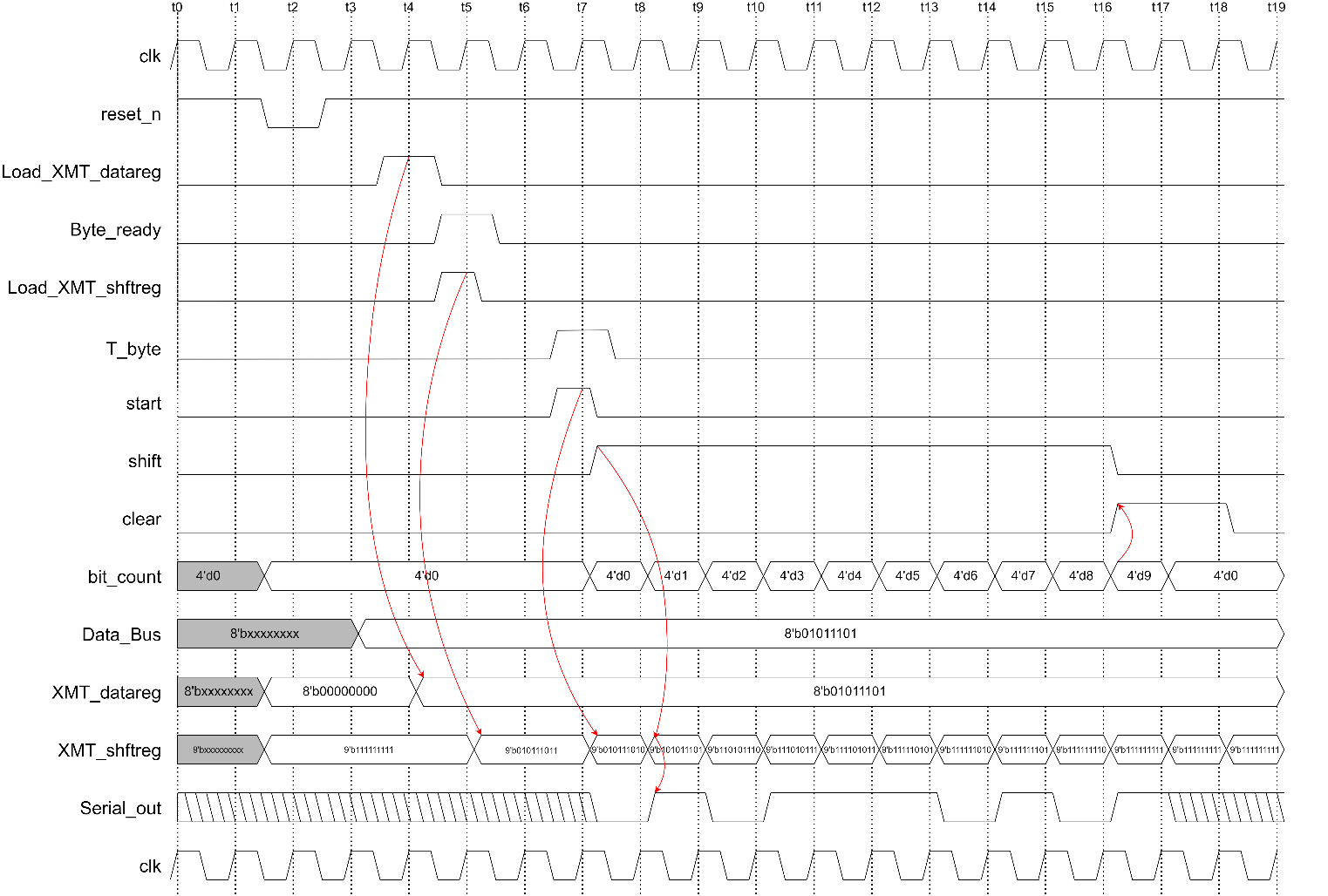


Figure 4. Timing diagram uart\_transmitter\_arsyn

### Architecture

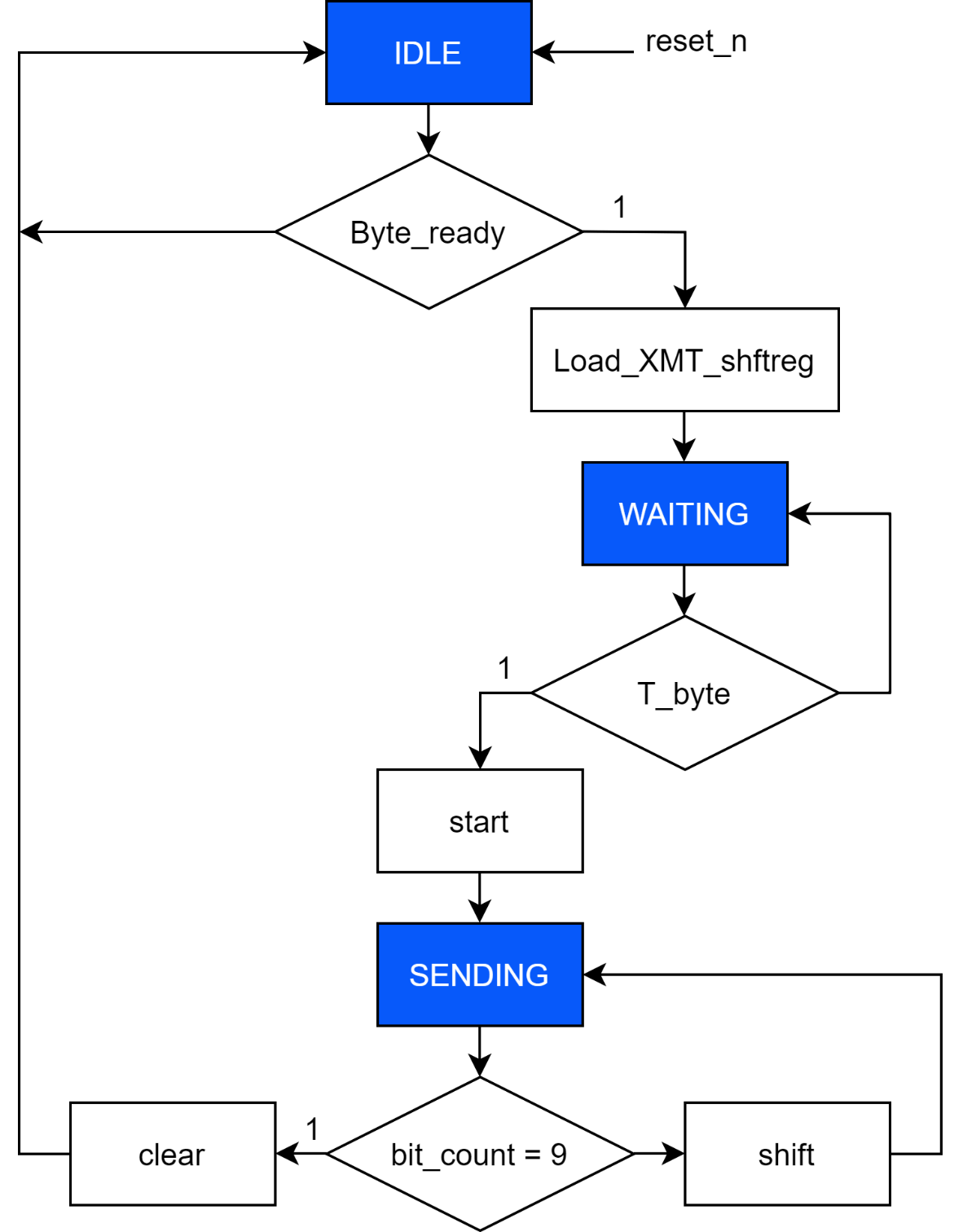


Figure 5. ASM

## uart\_receiver

### Block Diagram

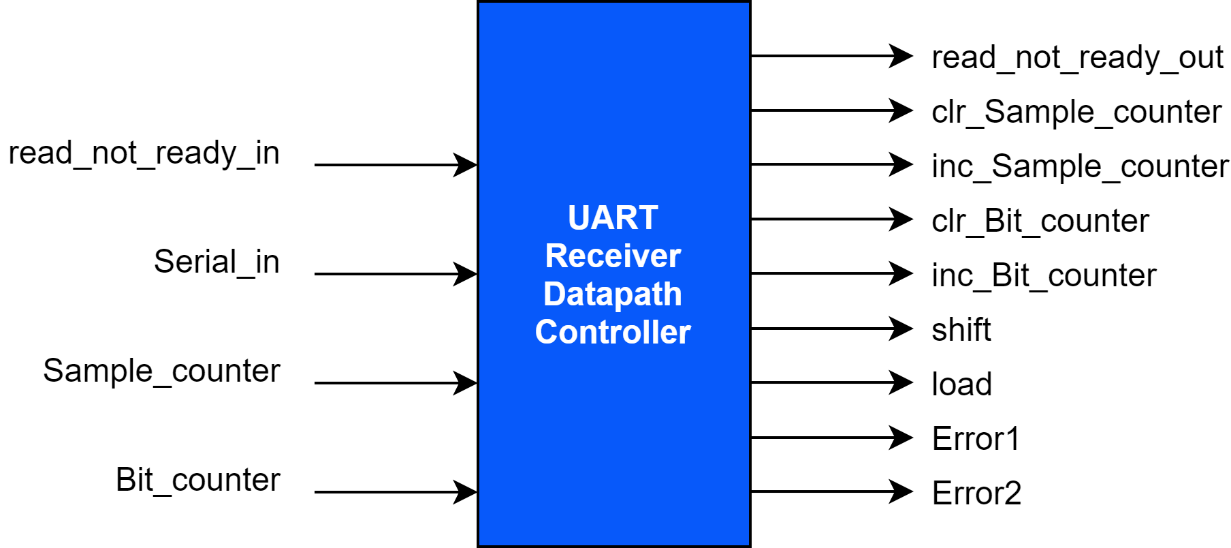


Figure 6. uart\_receiver controller block diagram

### Interface Signals

Table 3. Port Description

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Width** | **Input/Output** | **Description** |
| clk | 1 | Input | Clock |
| reset\_n | 1 | Input | Asynchronous reset, active LOW |
| read\_not\_ready\_in | 1 | Input | Signals that the host is not ready to receive data |
| Serial\_in | 1 | Input | Serial bit stream received by the unit |
| Sample\_counter | counter\_bit | Input | Counts the samples of a bit |
| Bit\_counter | counter\_bit+1 | Input | Counts the bits that have been sampled |
| read\_not\_ready\_out | 1 | Output | Signals that the receiver has received 8 bits |
| inc\_Sample\_counter | 1 | Output | Increments Sample\_counter |
| clr\_Sample\_counter | 1 | Output | Clears Sample\_counter |
| inc\_Bit\_counter | 1 | Output | Increments Bit\_counter |
| clr\_Bit\_counter | 1 | Output | Clears Bit\_counter |
| shift | 1 | Output | Causes RCV\_shftreg to shift towards the LSB |
| load | 1 | Output | Causes RCV\_shftreg to transfer data to RCV\_datareg |
| Error1 | 1 | Output | Asserts if host is not ready to receive data after last bit has been sampled |
| Error2 | 1 | Output | Asserts if the stop-bit is missing |
| RCV\_datareg | data\_size | Output | Register Data |

### Function Description

### Architecture

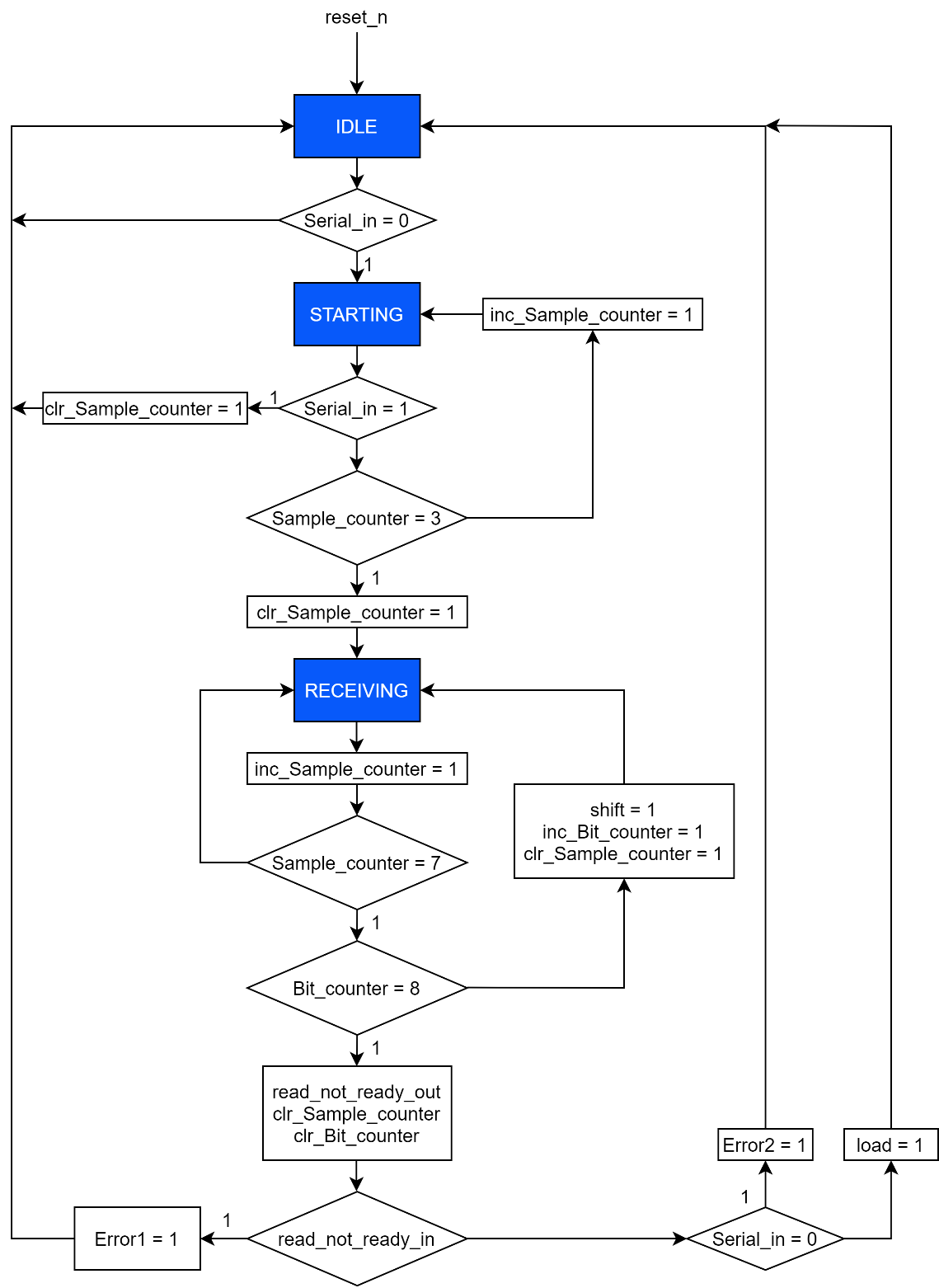


Figure 7. ASMD