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Application Note AN4137

Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)

Abstract

This paper presents practical design guidelines for off-line flyback converters employing FPS (Fairchild Power Switch). Switched mode power supply (SMPS) design is inherently a time consuming job requiring many trade-offs and iterations with a large number of design variables.

The step-by-step design procedure described in this paper helps engineers to design SMPS easily. In order to make the design process more efficient, a software design tool, **FPS design assistant** that contains all the equations described in this paper is also provided. The design procedure is verified through experimental prototype converter.

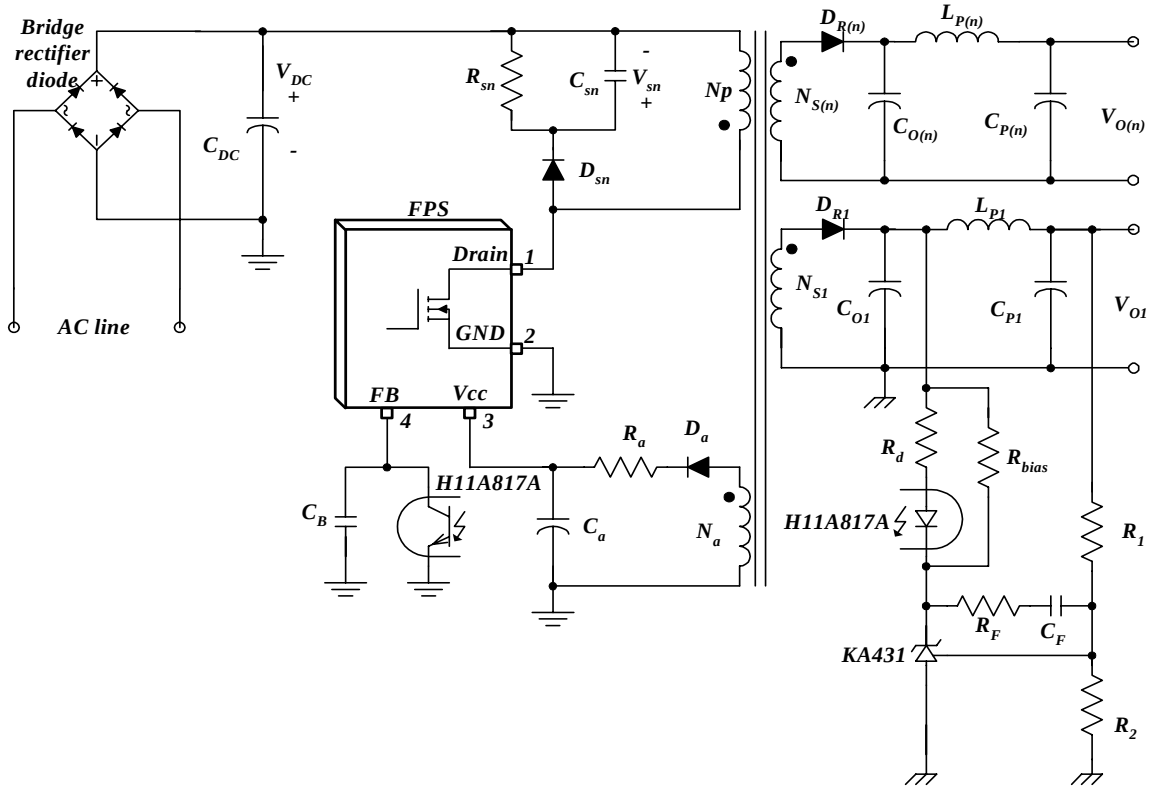


Figure 1. Basic Off-line Flyback Converter Using FPS

1. Introduction

Figure 1 shows the schematic of the basic off-line flyback converter using FPS, which also serves as the reference circuit for the design process described in this paper. Because the MOSFET and PWM controller together with various additional circuits are integrated into a single package, the design of SMPS is much easier than the discrete MOSFET and PWM controller solution. This paper provides a step-by-step design procedure for a FPS based off-line flyback converter, which includes designing the transformer and output filter, selecting the components and closing the feedback loop. The design procedure described herein is general enough to be applied to various applications. The design procedure presented in this paper is also implemented in a software design tool (FPS design assistant) to enable the engineer finish their SMPS design in a short time. In the appendix, a step-by-step design example using the software tool is provided. An experimental flyback converter from the design example has been built and tested to show the validity of the design procedure.

2. Step-by-step Design Procedure

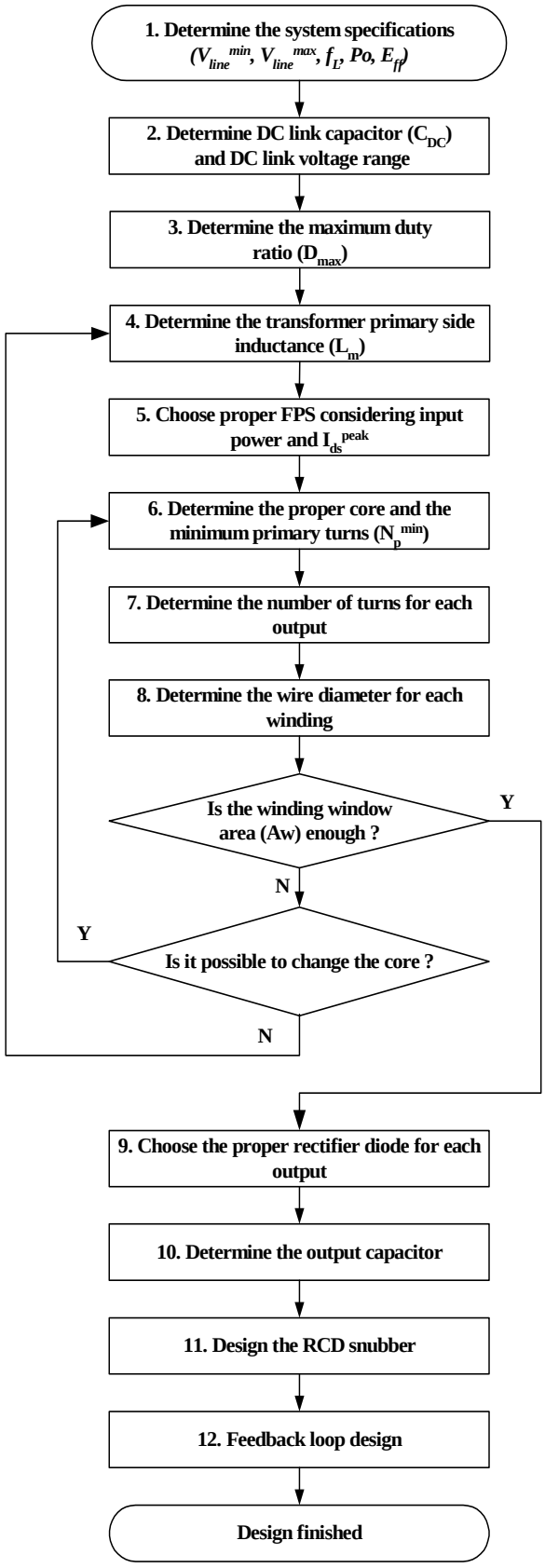


Figure 2. Flow chart of design procedure

In this section, a design procedure is presented using the schematic of figure 1 as a reference. In general, most FPS devices have the same pin configuration from pin 1 to pin 4, as shown in figure 1. Figure 2 illustrates the design flow chart. The detailed design procedures are as follows:

(1) STEP-1 : Define the system specifications

- Line voltage range (V_{line}^{min} and V_{line}^{max}).
- Line frequency (f_L).
- Maximum output power (P_o).
- Estimated efficiency (E_{ff}) : It is required to estimate the power conversion efficiency to calculate the maximum input power. If no reference data is available, set E_{ff} = 0.7~0.75 for low voltage output applications and E_{ff} = 0.8~0.85 for high voltage output applications.

With the estimated efficiency, the maximum input power is given by

$$P_{in} = \frac{P_o}{E_{ff}} \quad (1)$$

For multiple output SMPS, the load occupying factor for each output is defined as

$$K_{L(n)} = \frac{P_{o(n)}}{P_o} \quad (2)$$

where $P_{o(n)}$ is the maximum output power for the n-th output. For single output SMPS, $K_{L(1)}$=1.

(2) STEP-2 : Determine DC link capacitor (C_{DC}) and the DC link voltage range.

It is typical to select the DC link capacitor as 2-3uF per watt of input power for universal input range (85-265Vrms) and 1uF per watt of input power for European input range (195V-265Vrms). With the DC link capacitor chosen, the minimum link voltage is obtained as

$$V_{DC}^{min} = \sqrt{2 \cdot (V_{line}^{min})^2 - \frac{P_{in} \cdot (1 - D_{ch})}{C_{DC} \cdot f_L}} \quad (3)$$

where D_{ch} is the DC link capacitor charging duty ratio defined as shown in figure 3, which is typically about 0.2 and P_{in}, V_{line}^{min} and f_L are specified in step-1.

The maximum DC link voltage is given as

$$V_{DC}^{max} = \sqrt{2} V_{line}^{max} \quad (4)$$

where V_{line}^{max} is specified in step-1.

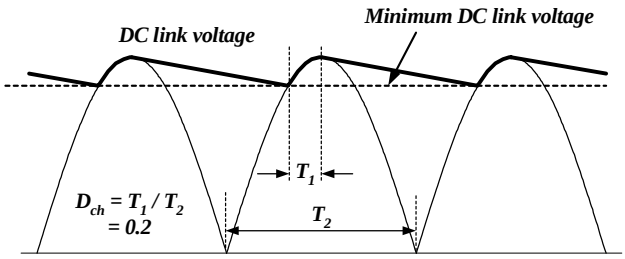


Figure 3. DC Link Voltage Waveform

(3) STEP-3 : Determine the maximum duty ratio (D_{max}).

A Flyback converter has two kinds of operation modes ; continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CCM and DCM have their own advantages and disadvantages, respectively. In general, DCM provides better switching conditions for the rectifier diodes, since the diodes are operating at zero current just before becoming reverse biased. The transformer size can be reduced using DCM because the average energy storage is low compared to CCM. However, DCM inherently causes high RMS current, which increases the conduction loss of the MOSFET and the current stress on the output capacitors. Therefore DCM is usually recommended for high voltage and low current output applications. Meanwhile, CCM is preferred for low voltage and high current output applications.

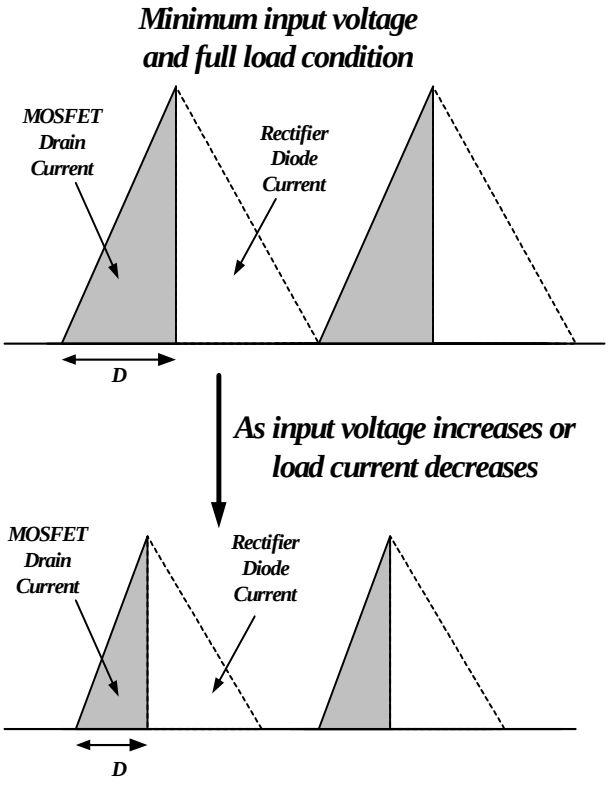


Figure 4. Current waveforms of DCM flyback converter

In the case of a CCM flyback converter, the design process is straight forward since the input-to-output voltage gain depends only on the duty cycle. Meanwhile, the input-to-output voltage gain of a DCM flyback converter depends not only on the duty cycle but also on the load condition, which causes the circuit design to be somewhat complicated. However, it is generally accepted that a DCM flyback converter is designed to operate at the boundary of DCM and CCM with minimum input voltage and maximum load as shown in Fig. 4. This minimizes MOSFET conduction losses. Therefore, under these circumstances, we can use the same voltage gain equation as the CCM flyback converter with maximum load and minimum input voltage.

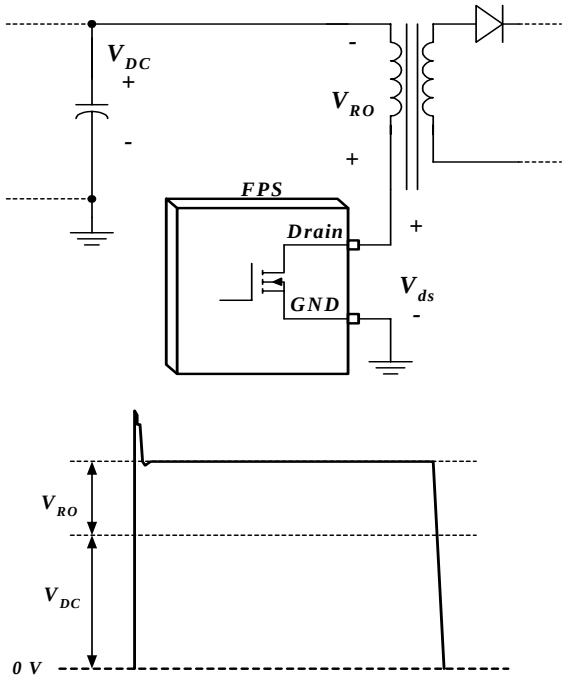


Figure 5. The output voltage reflected to the primary

When the MOSFET in the FPS is turned off, the input voltage (V_{DC}) together with the output voltage reflected to the primary (V_{RO}) are imposed on the MOSFET as shown in figure 5. After determining D_{max}, V_{RO} and the maximum nominal MOSFET voltage (V_{ds}^{nom}) are obtained as

$$V_{RO} = \frac{D_{max}}{1 - D_{max}} \cdot V_{DC}^{min} \quad (5)$$

$$V_{ds}^{nom} = V_{DC}^{max} + V_{RO} \quad (6)$$

where V_{DC}^{min} and V_{DC}^{max} are specified in equations (3) and (4) respectively. As can be seen in equation (5) and (6), the voltage stress on MOSFET can be reduced, by decreasing D_{max}. However, this increases the voltage stresses on the rectifier diodes in the secondary side. Therefore, it is desirable to set D_{max} as large as possible if there is enough margin in the MOSFET voltage rating. The maximum duty ratio

(D_{max}) should be determined so that V_{ds}^{nom} would be 65~70% of the MOSFET voltage rating considering the voltage spike caused by the leakage inductance. In the case of 650V rated MOSFET, it is typical to set D_{max} to be 0.45~0.5 for an universal input range application. Because the current mode controlled flyback converter operating in CCM causes sub-harmonic oscillation with duty ratio larger than 0.5, set D_{max} to be smaller than 0.5 for CCM.

(4) STEP-4 : Determine the transformer primary side inductance (L_m).

The operation changes between CCM and DCM as the load condition and input voltage vary. For both operation modes, the worst case in designing the inductance of the transformer primary side (L_m) is full load and minimum input voltage condition. Therefore, L_m is obtained in this condition as

$$L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2P_{in} f_s K_{RF}} \quad (7)$$

where V_{DC}^{min} is specified in equation (3), D_{max} is specified in step-3, P_{in} is specified in step-1, f_s is the switching frequency of the FPS device and K_{RF} is the ripple factor in full load and minimum input voltage condition, defined as shown in figure 6. For DCM operation, K_{RF} = 1 and for CCM operation K_{RF} < 1. The ripple factor is closely related with the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced through reducing the ripple factor, too small a ripple factor forces an increase in transformer size. When designing the flyback converter to operate in CCM, it is reasonable to set K_{RF} = 0.25-0.5 for the universal input range and K_{RF} = 0.4-0.8 for the European input range.

Once L_m is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as

$$I_{ds}^{peak} = I_{EDC} + \frac{\Delta I}{2} \quad (8)$$

$$I_{ds}^{rms} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{max}}{3}} \quad (9)$$

$$\text{where} \quad I_{EDC} = \frac{P_{in}}{V_{DC}^{min} \cdot D_{max}} \quad (10)$$

$$\text{and} \quad \Delta I = \frac{V_{DC}^{min} D_{max}}{L_m f_s} \quad (11)$$

where P_{in}, V_{DC}^{min} and L_m are specified in equations (1), (3), and (7) respectively, D_{max} is specified in step-3 and f_s is the FPS switching frequency.

The flyback converter designed for CCM at the minimum input voltage and full load condition may enter into DCM as the input voltage increases. The maximum input voltage guaranteeing CCM in the full load condition is obtained as

$$V_{DC}^{CCM} = \left(\frac{1}{\sqrt{2L_m f_s P_{in}}} - \frac{1}{V_{RO}}\right)^{-1} \quad (12)$$

where P_{in}, V_{RO} and L_m are specified in equations (1), (5) and (7), respectively, and f_s is the FPS switching frequency.
If the result of equation (12) has a negative value, the converter is always in CCM under the full load condition regardless of the input voltage variation.

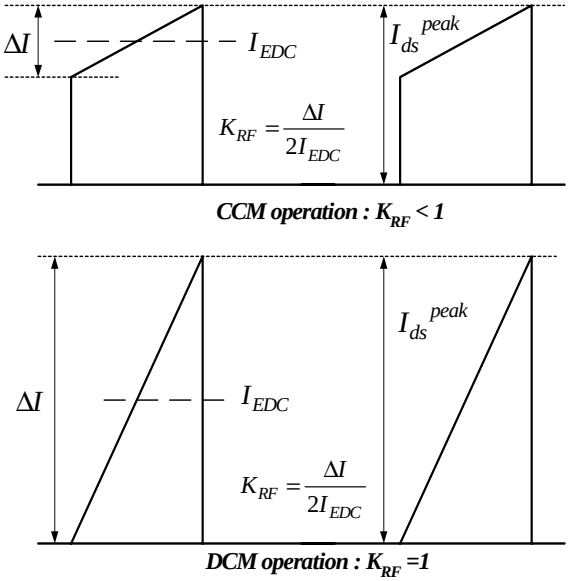


Figure 6. MOSFET Drain Current and Ripple Factor (K_{RF})

(5) STEP-5 : Choose the proper FPS considering input power and peak drain current.

With the resulting maximum peak drain current of the MOSFET (I_{ds}^{peak}) from equation (8), choose the proper FPS of which the pulse-by-pulse current limit level (I_{over}) is higher than I_{ds}^{peak}. Since FPS has ± 12% tolerance of I_{over}, there should be some margin in choosing the proper FPS device.The FPS lineup with proper power rating is also included in the software design tool.

(6) STEP-6 : Determine the proper core and the minimum primary turns.

Actually, the initial selection of the core is bound to be crude since there are too many variables. One way to select the proper core is to refer to the manufacture's core selection guide. If there is no proper reference, use the table 1 as a starting point. The core recommended in table 1 is typical for the universal input range, 67kHz switching frequency and single output application. When the input voltage range is 195-265 Vac or the switching frequency is higher than 67kHz, a smaller core can be used. For an application with multiple outputs, usually a larger core should be used than recommended in the table.

With the chosen core, the minimum number of turns for the transformer primary side to avoid the core saturation is given by

$$N_P^{min} = \frac{L_m I_{over}}{B_{sat} A_e} \times 10^6 \quad (turns) \qquad (13)$$

where L_m is specified in equation (7), I_{over} is the FPS pulse-by-pulse current limit level, A_e is the cross-sectional area of the core as shown in figure 7 and B_{sat} is the saturation flux density in tesla. Figure 8 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density (B_{sat}) decreases as the temperature goes high, the high temperature characteristics should be considered.

If there is no reference data, use B_{sat} =0.3~0.35 T. Since the MOSFET drain current exceeds I_{ds}^{peak} and reaches I_{over} in a transition or fault condition, I_{over} is used in equation (13) instead of I_{ds}^{peak} to prevent core saturation during transition.

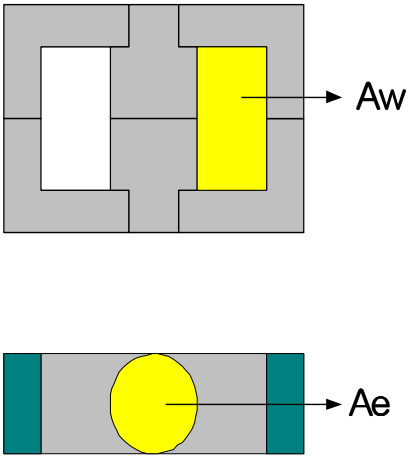


Figure 7. Window Area and Cross Sectional Area

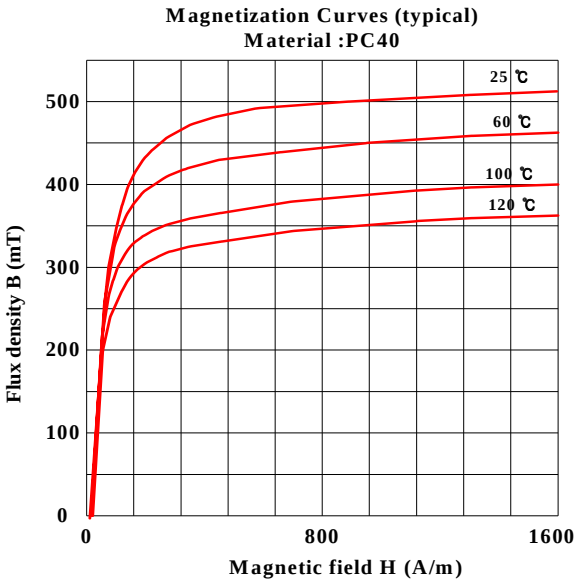


Figure 8. Typical B-H characteristics of ferrite core (TDK/PC40)

Output Power	EI core	EE core	EPC core	EER core
0-10W	EI12.5 EI16 EI19	EE8 EE10 EE13 EE16	EPC10 EPC13 EPC17	
10-20W	EI22	EE19	EPC19	
20-30W	EI25	EE22	EPC25	EER25.5
30-50W	EI28 EI30	EE25	EPC30	EER28
50-70W	EI35	EE30		EER28L
70-100W	EI40	EE35		EER35
100-150W	EI50	EE40		EER40 EER42
150-200W	EI60	EE50 EE60		EER49

Table 1. Core quick selection table (For universal input range, fs=67kHz and single output)

(7) STEP-7 : Determine the number of turns for each output

Figure 9 shows the simplified diagram of the transformer. First, determine the turns ratio (n) between the primary side and the feedback controlled secondary side as a reference.

$$n = \frac{N_P}{N_{s1}} = \frac{V_{R0}}{V_{o1} + V_{F1}} \qquad (14)$$

where N_p and N_{s1} are the number of turns for primary side and reference output, respectively, V_{o1} is the output voltage and V_{F1} is the diode (D_{R1}) forward voltage drop of the reference output.

Then, determine the proper integer for N_{s1} so that the resulting Np is larger than N_p^{min} obtained from equation (13).

The number of turns for the other output (n-th output) is determined as

$$N_{s(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \qquad (15)$$

The number of turns for Vcc winding is determined as

$$N_a = \frac{V_{cc}^* + V_{Fa}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \qquad (16)$$

where V_{cc}* is the nominal value of the supply voltage of the FPS device, and V_{Fa} is the forward voltage drop of D_a as defined in figure 9. Since V_{cc} increases as the output load increases, it is proper to set V_{cc}* as V_{cc} start voltage (refer to the data sheet) to avoid the over voltage protection condition during normal operation.

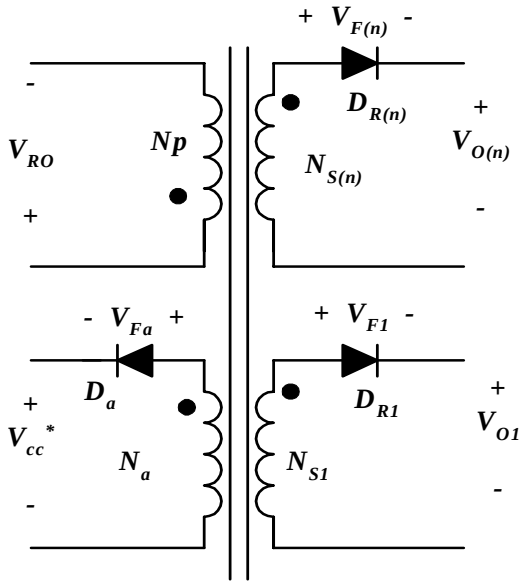


Figure 9. Simplified diagram of the transformer

With the determined turns of the primary side, the gap length of the core is obtained as

$$G = 40\pi A_e\left(\frac{N_P^{\,2}}{1000L_m} - \frac{1}{A_L}\right) \quad (mm) \qquad (17)$$

where A_L is the AL-value with no gap in nH/turns^2, *Ae* is the cross sectional area of the core as shown in figure 7, L_m is specified in equation (7) and N_p is the number of turns for the primary side of the transformer

(8) STEP-8 : Determine the wire diameter for each winding based on the rms current of each output.

The rms current of the n-th secondary winding is obtained as

$$I_{sec(n)}^{\,rms} = I_{ds}^{\,rms}\sqrt{\frac{1-D_{max}}{D_{max}}}\cdot\frac{V_{RO}\cdot K_{L(n)}}{(V_{o(n)}+V_{F(n)})} \qquad (18)$$

where V_{RO} and $I_{ds}^{\,rms}$ are specified in equations (5) and (9), $V_o(n)$ is the output voltage of the n-th output, $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage drop, D_{max} is specified in step-3 and $K_{L(n)}$ is the load occupying factor for n-th output defined in equation (2).
The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with a diameter larger than 1 mm to avoid severe eddy current losses as well as to make winding easier. For high current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect.

Check if the winding window area of the core, A_w (refer to figure 7) is enough to accommodate the wires. The required winding window area (A_{wr}) is given by

$$A_{wr} = A_c / K_F \qquad (19)$$

where A_c is the actual conductor area and K_F is the fill factor. Typically the fill factor is 0.2~0.25 for single output application and 0.15~0.2 for multiple outputs application.
If the required window (A_{wr}) is larger than the actual window area (A_w), go back to the step-6 and change the core to a bigger one. Sometimes it is impossible to change the core due to cost or size constraints. If the converter is designed for CCM and the winding window (A_w) is slightly insufficient, go back to step-4 and reduce L_m by increasing the ripple factor (K_{RF}). Then, the minimum number of turns for the primary ($N_p^{\,min}$) of the equation (13) will decrease, which results in the reduced required winding window area (A_{wr}).

(9) STEP-9 : Choose the rectifier diode in the secondary side based on the voltage and current ratings.

The maximum reverse voltage and the rms current of the rectifier diode ($D_{R(n)}$) of the n-th output are obtained as

$$V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{\,max}\cdot(V_{o(n)}+V_{F(n)})}{V_{RO}} \qquad (20)$$

$$I_{D(n)}^{\,rms} = I_{ds}^{\,rms}\sqrt{\frac{1-D_{max}}{D_{max}}}\cdot\frac{V_{RO}K_{L(n)}}{(V_{o(n)}+V_{F(n)})} \qquad (21)$$

where $K_{L(n)}$, $V_{DC}^{\,max}$, V_{RO}, $I_{ds}^{\,rms}$ are specified in equations (2), (4), (5) and (9) respectively, D_{max} is specified in step-3, $V_{o(n)}$ is the output voltage of the n-th output and $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage. The typical voltage and current margins for the rectifier diode are as follows

$$V_{RRM} > 1.3\cdot V_{D(n)} \qquad (22)$$

$$I_F > 1.5\cdot I_{D(n)}^{\,rms} \qquad (23)$$

where V_{RRM} is the maximum reverse voltage and I_F is the average forward current of the diode.

A quick selection guide for Fairchild Semiconductor rectifier diodes is given in table 2. In this table t_{rr} is the maximum reverse recovery time.

Schottky Barrier Diode				
Products	**V_{RRM}**	**I_F**	**t_{rr}**	**Package**
SB330	30 V	3 A	-	TO-210AD
SB530	30 V	5 A	-	TO-210AD
MBR1035	35 V	10 A	-	TO-220AC
MBR1635	35 V	16 A	-	TO-220AC
SB340	40 V	3 A	-	TO-210AD
SB540	40 V	5 A	-	TO-210AD
SB350	50 V	3 A	-	TO-210AD
SB550	50 V	5 A	-	TO-210AD
SB360	60 V	3 A	-	TO-210AD
SB560	60 V	5 A	-	TO-210AD
MBR1060	60 V	10 A	-	TO-220AC
MBR1660	60 V	16 A	-	TO-220AC
Ultra Fast Recovery diode				
Products	**V_{RRM}**	**I_F**	**t_{rr}**	**Package**
EGP10B	100 V	1 A	50 ns	DO-41
UF4002	100 V	1 A	50 ns	DO-41
EGP20B	100 V	2 A	50 ns	DO-15
EGP30B	100 V	3 A	50 ns	DO-210AD
FES16BT	100 V	16 A	35 ns	TO-220AC
EGP10C	150 V	1 A	50 ns	DO-41
EGP20C	150 V	2 A	50 ns	DO-15
EGP30C	150 V	3 A	50 ns	DO-210AD
FES16CT	150 V	16 A	35 ns	TO-220AC
EGP10D	200 V	1 A	50 ns	DO-41
UF4003	200 V	1 A	50 ns	DO-41
EGP20D	200 V	2 A	50 ns	DO-15
EGP30D	200 V	3 A	50 ns	DO-210AD
FES16DT	200 V	16 A	35 ns	TO-220AC
EGP10F	300 V	1 A	50 ns	DO-41
EGP20F	300 V	2 A	50 ns	DO-15
EGP30F	300 V	3 A	50 ns	DO-210AD
EGP10G	400 V	1 A	50 ns	DO-41
UF4004	400 V	1 A	50 ns	DO-41
EGP20G	400 V	2 A	50 ns	DO-15
EGP30G	400 V	3 A	50 ns	DO-210AD
UF4005	600 V	1 A	75 ns	DO-41
EGP10J	600 V	1A	50 ns	DO-41
EGP20J	600 V	2 A	50 ns	DO-15
EGP30J	600 V	3 A	50 ns	DO-210AD
UF4006	800 V	1 A	75 ns	TO-41
UF4007	1000 V	1 A	75 ns	TO-41

Table 2. Fairchild Diode quick selection table

(10) STEP-10 : Determine the output capacitor considering the voltage and current ripple.

The ripple current of the n-th output capacitor ($C_{o(n)}$) is obtained as

$$I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2} \quad (24)$$

where $I_{o(n)}$ is the load current of the n-th output and $I_{D(n)}^{rms}$ is specified in equation (21). The ripple current should be smaller than the ripple current specification of the capacitor. The voltage ripple on the n-th output is given by

$$\Delta V_{o(n)} = \frac{I_{o(n)} D_{max}}{C_{o(n)} f_s} + \frac{I_{ds}^{peak} V_{RO} R_{C(n)} K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \quad (25)$$

where $C_{o(n)}$ is the capacitance, $R_{c(n)}$ is the effective series resistance (ESR) of the n-th output capacitor, $K_{L(n)}$, V_{RO} and I_{ds}^{peak} are specified in equations (2), (5) and (8) respectively, D_{max} is specified in step-3, $I_{o(n)}$ and $V_{o(n)}$ are the load current and output voltage of the n-th output, respectively and $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter stages (post filter) can be used. When using the post filters, be careful not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency.

(11) STEP-11 : Design the RCD snubber.

When the power MOSFET is turned off, there is a high voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure of FPS. Therefore, it is necessary to use an additional network to clamp the voltage.

The RCD snubber circuit and MOSFET drain voltage waveform are shown in figure 10 and 11, respectively. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode (D_{sn}) once the MOSFET drain voltage exceeds the voltage of node X as depicted in figure 10. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle.

The first step in designing the snubber circuit is to determine the snubber capacitor voltage at the minimum input voltage and full load condition (V_{sn}). Once V_{sn} is determined, the power dissipated in the snubber network at the minimum input voltage and full load condition is obtained as

$$P_{sn} = \frac{(V_{sn})^2}{R_{sn}} = \frac{1}{2} f_s L_{lK} (I_{ds}^{peak})^2 \frac{V_{sn}}{V_{sn} - V_{RO}} \quad (26)$$

where I_{ds}^{peak} is specified in equation (8), f_s is the FPS switching frequency, L_{lk} is the leakage inductance, V_{sn} is the snubber capacitor voltage at the minimum input voltage and full load condition, V_{RO} is the reflected output voltage and R_{sn} is the snubber resistor. V_{sn} should be larger than V_{RO} and it is typical to set V_{sn} to be 2~2.5 times of V_{RO}. Too small a V_{sn} results in a severe loss in the snubber network as shown in equation (26). The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted.

Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as

$$\Delta V_{sn} = \frac{V_{sn1}}{C_{sn} R_{sn} f_s} \quad (27)$$

where f_s is the FPS switching frequency. In general, 5~10% ripple is reasonable.

The snubber capacitor voltage (V_{sn}) of equation (26) is for the minimum input voltage and full load condition. When the converter is designed to operate in CCM, the peak drain current together with the snubber capacitor voltage decrease as the input voltage increases. The snubber capacitor voltage under maximum input voltage and full load condition is obtained as

$$V_{sn2} = \frac{V_{RO} + \sqrt{(V_{RO})^2 + 2R_{sn} L_{lk} f_s (I_{ds2})^2}}{2} \quad (28)$$

where f_s is the FPS switching frequency, L_{lk} is the primary side leakage inductance, V_{RO} is the reflected output voltage, R_{sn} is the snubber resistor and I_{ds2} is the peak drain current at the maximum input voltage and full load condition. When the converter operates in CCM at the maximum input voltage and full load condition (refer to equation (12)), the I_{ds2} of equation (28) is obtained as

$$I_{ds2} = \frac{P_{in} \cdot \left(V_{DC}^{max} + V_{RO}\right)}{V_{DC}^{max} \cdot V_{RO}} + \frac{V_{DC}^{max} \cdot V_{RO}}{2 L_m f_s \cdot \left(V_{DC}^{max} + V_{RO}\right)} \quad (29)$$

When the converter operates in DCM at the maximum input voltage and full load condition (refer to equation (12)), the I_{ds2} of equation (28) is obtained as

$$I_{ds2} = \sqrt{\frac{2 \cdot P_{in}}{f_s \cdot L_m}} \quad (30)$$

where P_{in}, V_{DC}^{max}, V_{RO} and L_m are specified in equations (1), (4), (5) and (7), respectively, and f_s is the FPS switching frequency.

From equation (28), the maximum voltage stress on the internal MOSFET is given by

$$V_{ds}^{max} = V_{DC}^{max} + V_{sn2} \quad (31)$$

where V_{DC}^{max} is specified in equation (4).

Check if V_{ds}^{max} is below 90% of the rated voltage of the MOSFET (*BVdss*) as shown in figure 11. The voltage rating of the snubber diode should be higher than *BVdss*. Usually, an ultra fast diode with 1A current rating is used for the snubber network.

In the snubber design in this section, neither the lossy discharge of the inductor nor stray capacitance is considered. In the actual converter, the loss in the snubber network is less than the designed value due to this effects.

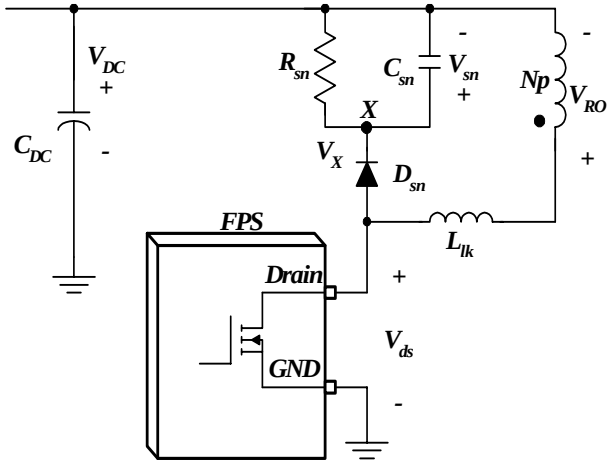


Figure 10. Circuit diagram of the snubber network

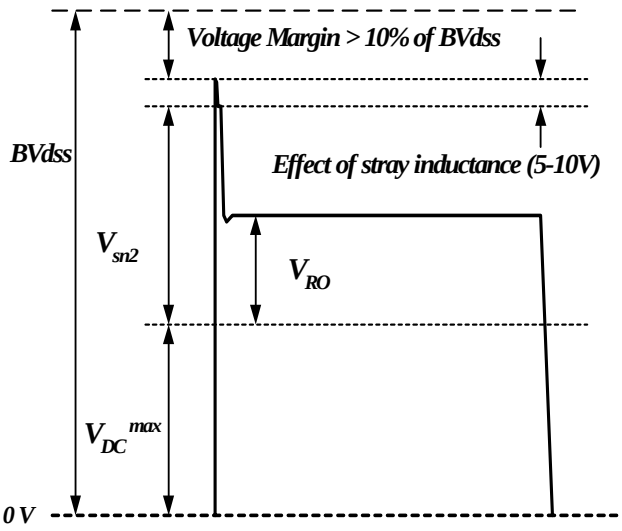


Figure 11. MOSFET drain voltage and snubber capacitor voltage

(12) STEP-12 : Design the feed back loop.

Since most FPS devices employ current mode control as shown in figure 12, the feedback loop can be simply implemented with a one-pole and one-zero compensation circuit. In the feedback circuit analysis, it is assumed that the current transfer ratio (CTR) of the opto coupler is 100%.

The current control factor of FPS, *K* is defined as

$$K = \frac{I_{pk}}{V_{FB}} = \frac{I_{over}}{V_{FBsat}} \qquad (32)$$

where I_{pk} is the peak drain current and V_{FB} is the feedback voltage, respectively for a given operating condition, I_{over} is the current limit of the FPS and V_{FBsat} is the feedback saturation voltage, which is typically 2.5V.

In order to express the small signal AC transfer functions, the small signal variations of feedback voltage (v_{FB}) and controlled output voltage (v_{o1}) are introduced as $\hat{v}_{FB}$ *and* $\hat{v}_{o1}$.

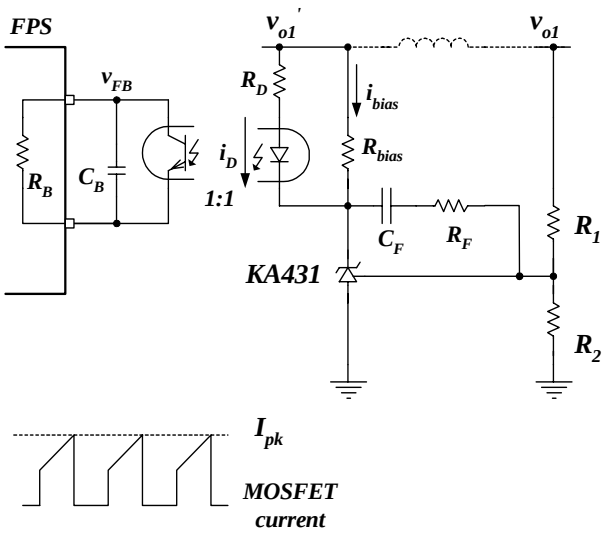


Figure 12. Control Block Diagram

For CCM operation, the control-to-output transfer function of the flyback converter using current mode control is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{\hat{v}_{FB}} = \frac{K \cdot R_L V_{DC}(N_p/N_{s1})}{2V_{RO} + v_{DC}} \cdot \frac{(1 + s/w_z)(1 - s/w_{rz})}{1 + s/w_p} \qquad (33)$$

where V_{DC} is the DC input voltage, R_L is the effective total load resistance of the controlled output, defined as V_{o1}^2/P_o, N_p and N_{s1} are specified in step-7, V_{RO} is specified in equation (5), V_{o1} is the reference output voltage, P_o is specified in step-1 and *K* is specified in equation (32). The pole and zeros of equation (33) are defined as

$$w_z = \frac{1}{R_{c1}C_{o1}},\ w_{rz} = \frac{R_L(1-D)^2}{DL_m(N_{s1}/N_p)^2} \ \text{ and } \ w_p = \frac{(1+D)}{R_L C_{o1}}$$

where L_m is specified in equation (7), *D* is the duty cycle of the FPS, C_{o1} is the reference output capacitor and R_{C1} is the ESR of C_{o1}.

When the converter has more than one output, the low frequency control-to-output transfer function is proportional to the parallel combination of all load resistance, adjusted by the square of the turns ratio. Therefore, the effective load resistance is used in equation (33) instead of the actual load resistance of V_{o1}.

Notice that there is a right half plane (RHP) zero (w_{rz}) in the control-to-output transfer function of equation (33). Because the RHP zero reduces the phase by 90 degrees, the crossover frequency should be placed below the RHP zero.

Figure 13 shows the variation of a CCM flyback converter control-to-output transfer function for different input voltages. This figure shows the system poles and zeros together with the DC gain change for different input voltages. The gain is highest at the high input voltage condition and the RHP zero is lowest at the low input voltage condition.

Figure 14 shows the variation of a CCM flyback converter control-to-output transfer function for different loads. This figure shows that the low frequency gain does not change for different loads and the RHP zero is lowest at the full load condition.

For DCM operation, the control-to-output transfer function of the flyback converter using current mode control is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{\hat{v}_{FB}} = \frac{V_{o1}}{V_{FB}} \cdot \frac{(1 + s/w_z)}{(1 + s/w_p)} \qquad (34)$$

$$\text{where} \quad w_z = \frac{1}{R_{c1}C_{o1}}\ ,\ w_p = 2/R_L C_{o1}$$

V_{o1} is the reference output voltage, V_{FB} is the feedback voltage for a given condition, R_L is the effective total resistance of the controlled output, C_{o1} is the controlled output capacitance and Rc1 is the ESR of C_{o1}.

Figure 15 shows the variation of the control-to-output transfer function of a flyback converter in DCM for different loads. Contrary to the flyback converter in CCM, there is no RHP zero and the DC gain does not change as the input voltage varies. As can be seen, the overall gain except for the DC gain is highest at the full load condition.

The feedback compensation network transfer function of figure 12 is obtained as

$$\frac{\hat{v}_{FB}}{\hat{v}_{o1}} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + 1/w_{pc}} \quad (35)$$

$$\text{where } w_i = \frac{R_B}{R_1 R_D C_F},\ w_{zc} = \frac{1}{(R_F + R_1)C_F},\ w_{pc} = \frac{1}{R_B C_B}$$

and R_B is the internal feedback bias resistor of FPS, which is typically 2.8kΩ and R_1, R_D, R_F, C_F and C_B are shown in figure 12.

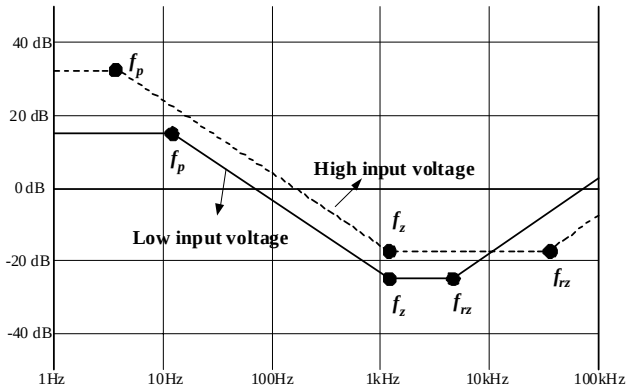


Figure 13. CCM flyback converter control-to output transfer function variation for different input voltages

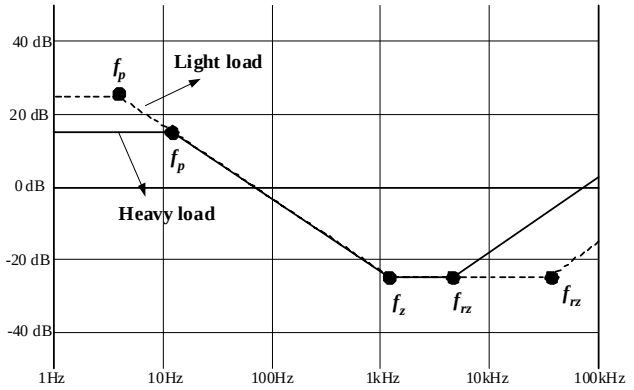


Figure 14. CCM flyback converter control-to output transfer function variation for different loads

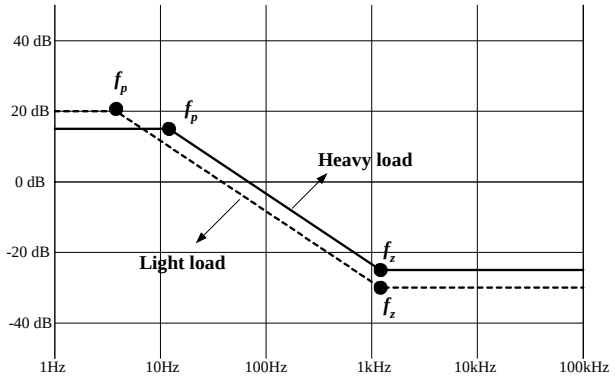


Figure 15. DCM flyback converter control-to output transfer function variation for different loads

When the input voltage and the load current vary over a wide range, it is not easy to determine the worst case for the feedback loop design. The gain together with zeros and poles vary according to the operating condition. Moreover, even though the converter is designed to operate in CCM or at the boundary of DCM and CCM in the minimum input voltage and full load condition, the converter enters into DCM changing the system transfer functions as the load current decreases and/or input voltage increases.

One simple and practical way to this problem is designing the feedback loop for low input voltage and full load condition with enough phase and gain margin. When the converter operates in CCM, the RHP zero is lowest in low input voltage and full load condition. The gain increases only about 6dB as the operating condition is changed from the lowest input voltage to the highest input voltage condition under universal input condition. When the operating mode changes from CCM to DCM, the RHP zero disappears making the system stable. Therefore, by designing the feedback loop with more than 45 degrees phase margin in low input voltage and full load condition, the stability over all the operating ranges can be guaranteed.

The procedure to design the feedback loop is as follows

(a) Determine the crossover frequency (f_c). For CCM mode flyback, set f_c below 1/3 of right half plane (RHP) zero to minimize the effect of the RHP zero. For DCM mode f_c can be placed at a higher frequency, since there is no RHP zero.

(b) When an additional LC filter is employed, the crossover frequency should be placed below 1/3 of the corner frequency of the LC filter, since it introduces a -180 degrees phase drop. Never place the crossover frequency beyond the corner frequency of the LC filter. If the crossover frequency is too close to the corner frequency, the controller should be designed to have a phase margin greater than 90 degrees when ignoring the effect of the post filter.

(c) Determine the DC gain of the compensator (w_i/w_{zc}) to cancel the control-to-output gain at f_c.

(d) Place a compensator zero (f_{zc}) around $f_c/3$.

(e) Place a compensator pole (f_{pc}) above $3f_c$.

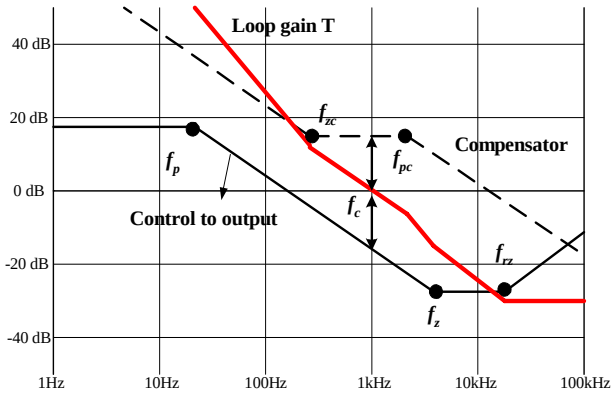


Figure 16. Compensator design

When determining the feedback circuit component, there are some restrictions as follows.

(a) The voltage divider network of R_1 and R_2 should be designed to provide 2.5V to the reference pin of the KA431. The relationship between R_1 and R_2 is given as

$$R_2 = \frac{2.5 \cdot R_1}{V_{o1} - 2.5} \quad (36)$$

where V_{o1} is the reference output voltage.

(b) The capacitor connected to feedback pin (C_B) is related to the shutdown delay time in an overload condition by

$$T_{delay} = (V_{SD} - 2.5) \cdot C_B / I_{delay} \quad (37$$

where V_{SD} is the shutdown feedback voltage and I_{delay} is the shutdown delay current. These values are given in the data sheet. In general, a 10 ~ 50 ms delay time is typical for most applications. Because C_B also determines the high frequency pole (w_{pc}) of the compensator transfer function as shown in equation (36), too large a C_B can limit the control bandwidth by placing w_{pc} at too low a frequency. Typical value for C_B is 10-50nF.

(c) The resistors R_{bias} and R_D used together with the opto-coupler H11A817A and the shunt regulator KA431 should be designed to provide proper operating current for the KA431 and to guarantee the full swing of the feedback voltage for the FPS device chosen. In general, the minimum cathode voltage and current for the KA431 are 2.5V and 1mA, respectively. Therefore, R_{bias} and R_D should be designed to satisfy the following conditions.

$$\frac{V_{o1} - V_{OP} - 2.5}{R_D} > I_{FB} \quad (38)$$

$$\frac{V_{OP}}{R_{bias}} > 1mA \quad (39)$$

where V_{o1} is the reference output voltage, V_{OP} is opto-diode forward voltage drop, which is typically 1V and I_{FB} is the feedback current of FPS, which is typically 1mA. For example, R_{bias}< 1kΩ and R_D < 1.5kΩ for V_{o1}=5V.

Miscellaneous

(a) Vcc capacitor (C_a) : The typical value for C_a is 10-50uF, which is enough for most application. A smaller capacitor than this may result in an under voltage lockout of FPS during the startup. While, too large a capacitor may increase the startup time.

(b) Vcc resistor (R_a) : The typical value for R_a is 5-20Ω. In the case of multiple outputs flyback converter, the voltage of the lightly loaded output such as Vcc varies as the load currents of other outputs change due to the imperfect coupling of the transformer. R_a reduces the sensitivity of Vcc to other outputs and improves the regulations of Vcc.

- Summary of symbols -

A_w : Winding window area of the core in mm^2
Ae : Cross sectional area of the core in mm^2
B_{sat} : Saturation flux density in tesla.
$C_{o(n)}$: Output capacitor of the n-th output
D_{max} : Maximum duty cycle ratio
E_{ff} : Estimated efficiency
f_L : Line frequency
f_s : Switching frequency of FPS
I_{ds}^{peak} : Maximum peak current of MOSFET
I_{ds}^{rms} : RMS current of MOSFET
I_{ds2} : Maximum peak drain current at the maximum input voltage condition.
I_{over} : FPS current limit level.
$I_{sec(n)}^{rms}$: RMS current of the secondary winding for the n-th output
$I_{D(n)}^{rms}$: Maximum rms current of the rectifier diode for the n-th output
$I_{cap(n)}^{rms}$: RMS Ripple current of the output capacitor for the n-th output
$I_{o(n)}$: Output load current for the n-th output
$K_{L(n)}$: Load occupying factor for the n-th output
K_{RF} : Current ripple factor
L_m : Transformer primary side inductance
L_{lk} : Transformer primary side leakage inductance
$Loss_{sn}$: Maximum power loss of the snubber network in normal operation
N_p^{min} : The minimum number of turns for the transformer primary side to avoid saturation
N_p : Number of turns for primary side
N_{s1} : Number of turns for the reference output
$N_{s(n)}$: Number of turns for the n-th output
P_o : Maximum output power
P_{in} : Maximum input power
$R_{c(n)}$: Effective series resistance (ESR) of the n-th output capacitor.
R_{sn} : Snubber resistor
R_L : Effective total output load resistor of the controlled output
V_{line}^{min} : Minimum line voltage
V_{line}^{max} : Maximum line voltage
V_{DC}^{min} : Minimum DC link voltage
V_{DC}^{max} : Maximum DC line voltage
V_{ds}^{nom} : Maximum nominal MOSFET voltage
V_{o1} : Output voltage of the reference output.
V_{F1} : Diode forward voltage drop of the reference output.
V_{cc}^{*} : Nominal voltage for Vcc
V_{Fa} : Diode forward voltage drop of Vcc winding
$V_{D(n)}$: Maximum voltage of the rectifier diode for n-th output
$\Delta V_{o(n)}$: Output voltage ripple for the n-th output
V_{RO} : Output voltage reflected to the primary
V_{sn} : Snubber capacitor voltage under minimum input voltage and full load condition
V_{sn2} : Snubber capacitor voltage under maximum input voltage and full load condition
ΔV_{sn} : Maximum Snubber capacitor voltage ripple
V_{ds}^{max} : Maximum voltage stress of the MOSFET

Appendix : Design example using FPS Design Assistant

Application	Device	Output Power	Input voltage	Output voltage (Max Current)	Ripple spec
Set-top Box	FSDM07652R	47W	85V-265VAC	3.3V (2A) 5V (2A) 12V (1.5A) 18V (0.5A) 33V (0.1A)	± 5% ± 5% ± 5% ± 5 % ± 5 %

1. Define the system specifications

Minimum Line voltage (V_{line}^{min})	85	V.rms
Maximum Line voltage (V_{line}^{max})	265	V.rms
Line frequency (f_L)	60	Hz

	$V_{o(n)}$		$I_{o(n)}$		$P_{o(n)}$		$K_{L(n)}$	
1st output for feedback	3.3	V	2.00	A	7	W	14	%
2nd output	5	V	2.00	A	10	W	21	%
3rd output	12	V	1.50	A	18	W	38	%
4th output	18	V	0.50	A	9	W	19	%
5th output	33	V	0.10	A	3	W	7	%
6th output		V		A	0	W	0	%
Maximum output power (P_o) =	46.9	W						
Estimated efficiency (E_{ff})	70	%						
Maximum input power (P_{in}) =	67.0	W						

☞ **The estimated efficiency (E_{ff}) is set to be 0.7 considering the low voltage outputs (3.3V and 5V)**

2. Determine DC link capacitor and DC link voltage range

DC link capacitor (C_{DC})	150	uF
Minimum DC link voltage (V_{DC}^{min}) =	92	V
Maximum DC link voltage (V_{DC}^{max})=	375	V

☞ **Since the input power is 67 W, the DC link capacitor is set to be 150uF by 2uF/Watt.**

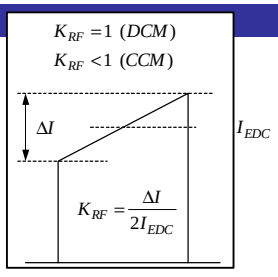
3. Determine Maximum duty ratio (Dmax)

Maximum duty ratio (D_{max})	0.48	
Max nominal MOSFET voltage (V_{ds}^{nom}) =	460	V
Output voltage reflected to primary (V_{RO})=	85	V

☞ **D_{max} is set to be 0.48 so that Vds^{nom} would be about 70% of BVdss (650V×0.7=455V)**

4. Determine transformer primary inductance (Lm)

Switching frequency of FPS (f_s)	66	kHz
Ripple factor (K_{RF})	0.33	
Primary side inductance (L_m) =	671	uH
Maximum peak drain current (I_{ds}^{peak}) =	2.01	A
RMS drain current (I_{ds}^{rms}) =	1.07	A
Maximum DC link voltage in CCM (V_{DC}^{CCM})	375	V



5. Choose the proper FPS considering the input power and current limit

Typical current limit of FPS (I_{over})	2.50	A			
Minimum I_{over} considering tolerance of 12%	2.20	A	>	2.01	A
	->O.K.				

☞ **Since the maximum peak drain current (I_{ds}^{peak}) is 2.0A, FSDM07652R is chosen, whose current limit level (I_{over}) is 2.5A. The current limit tolerance (12%) is considered.**

6. Determine the proper core and the minimum primary turns

Saturation flux density (B_{sat})	0.35	T
Cross sectional area of core (A_e)	109.4	mm^2
Minimum primary turns (N_p^{min})=	43.8	T

☞ **Ferrite core EER3530 is chosen (Ae=109.4 mm^2, Aw=210mm^2), which is a little bit larger than the core recommended in table 1 to provide enough winding window area.**

7. Determine the number of turns for each output

	$V_{o(n)}$		$V_{F(n)}$				# of turns	
Vcc (Use Vcc start voltage)	12	V	1.2	V	6.9	=>	7	T
1st output for feedback	3.3	V	0.5	V	2	=>	2	T
2nd output	5	V	0.5	V	2.9	=>	3	T
3rd output	12	V	1.2	V	6.9	=>	7	T
4th output	18	V	1.2	V	10.1	=>	10	T
5th output	33	V	1.2	V	18.0	=>	18	T
6th output	0	V	0	V	0.0	=>	0	T
VF : Forward voltage drop of rectifier diode			Primary turns (N_p)=				45	T
			--->enough turns					
Ungapped AL value (AL)	2130	nH/T^2						
Gap length (G) ; center pole gap =	0.34631	mm						

☞ **In general, the optimum turn ratio between 5V and 3.3V is 3/2, considering the diode forward voltage drop.**

8. Determine the wire diameter for each winding

	Diameter		Parallel		$I_{D(n)}^{rms}$		(A/mm^2)
Primary winding	0.5	mm	1	T	1.1	A	5.44
Vcc winding	0.3	mm	2	T	0.1	A	0.71
1st output winding	0.4	mm	4	T	3.5	A	6.97
2nd output winding	0.4	mm	4	T	3.7	A	7.30
3rd output winding	0.4	mm	3	T	2.8	A	7.30
4th output winding	0.4	mm	2	T	0.9	A	3.76
5th output winding	0.4	mm	1	T	0.2	A	1.55
6th output winding		mm		T	#####	A	#####
Copper area (A_c) =	19.70	mm^2					
Fill factor (K_F)	0.15						
Required window area (A_w)	131.33	mm^2					

☞ **Since the windings for 3.3V and 5V are short with small number of turns, relatively large current densities (> 5A/mm^2) are allowed. The fill factor is set to be 0.15 due to multiple outputs.**

9. Choose the rectifier diode in the secondary side

	$V_{D(n)}$		$I_{D(n)}^{rms}$	
Vcc diode	70	V	0.10	A
1st output diode	20	V	3.50	A
2nd output diode	29	V	3.67	A
3rd output diode	70	V	2.75	A
4th output diode	103	V	0.95	A
5th output diode	184	V	0.19	A
6th output diode	0	V	#####	A

Vcc winding	**UF4003 (200V /1A, VF=1V)**	**Ultra Fast Recovery Diode**
1st output (3.3V)	**SB540 (40V/5A, VF=0.55V) × 2**	**Schottky Barrier Diode**
2nd output (5V)	**SB560 (60V/5A, VF=0.67V) × 2**	**Schottky Barrier Diode**
3rd output (12V)	**EGP30D (200V/3A, VF=0.95V)**	**Ultra Fast Recovery Diode**
4st output (18V)	**EGP20D (200V/2A, VF=0.95V)**	**Ultra Fast Recovery Diode**
5st output (30V)	**UF4004 (400V /1A, VF=1V)**	**Ultra Fast Recovery Diode**

10. Determine the output capacitor

	$C_{o(n)}$		$R_{C(n)}$		$I_{cap(n)}$		$\Delta V_{o(n)}$	
1st output capacitor	2000	uF	100	mΩ	2.9	A	0.64	V
2nd output capacitor	2000	uF	100	mΩ	3.1	A	0.67	V
3rd output capacitor	330	uF	300	mΩ	2.3	A	1.53	V
4th output capacitor	470	uF	300	mΩ	0.8	A	0.52	V
5th output capacitor	47	uF	480	mΩ	0.2	A	0.18	V
6th output capacitor		uF		mΩ	#####	A	#####	V

Since the voltage ripples for 3.3V, 5V and 12V exceed the ripple spec of ± 5%, additional LC filter stage should be used for these three outputs. 220uF capacitor together with 2.2uH inductor are used for the post filter. To attenuate the voltage ripple caused by switching, the corner frequency of the post filter (fo) is set at about one decade below the switching frequency.

$$f_o = \frac{1}{2\pi\sqrt{L_{p1}C_{p1}}} = \frac{10^6}{2\pi\sqrt{2.2\times 220}} = 7.2kHz$$

11. Design RCD snubber

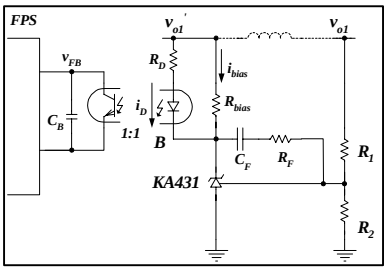
Primary side leakage inductance (L_{lk})	4.5	uH	
Maximum Voltage of snubber capacitor (V_{sn})	190	V	
Maximum snubber capacitor voltage ripple	5	%	
Snubber resistor (R_{sn})=	33.1	kΩ	
Snubber capacitor (C_{sn})=	9.2	nF	
Power loss in snubber resistor (P_{sn})=	1.1	W	(In Normal Operation)
Peak drain current at V_{DC}^{max} (I_{ds2}) =	1.75	A	
Max Voltage of Csn at V_{DC}^{max} (V_{sn2})=	172	V	
Max Voltage stress of MOSFET (V_{ds}^{max})=	547	V	

☞ **The snubber capacitor and snubber resistor are chosen as 10nF and 33kΩ, respectively. The maximum voltage stress on the MOSFET is designed to be 84% of 650V BVdss voltage of the FSDM07652R. The actual V_{ds}^{max} would be lower than this.**

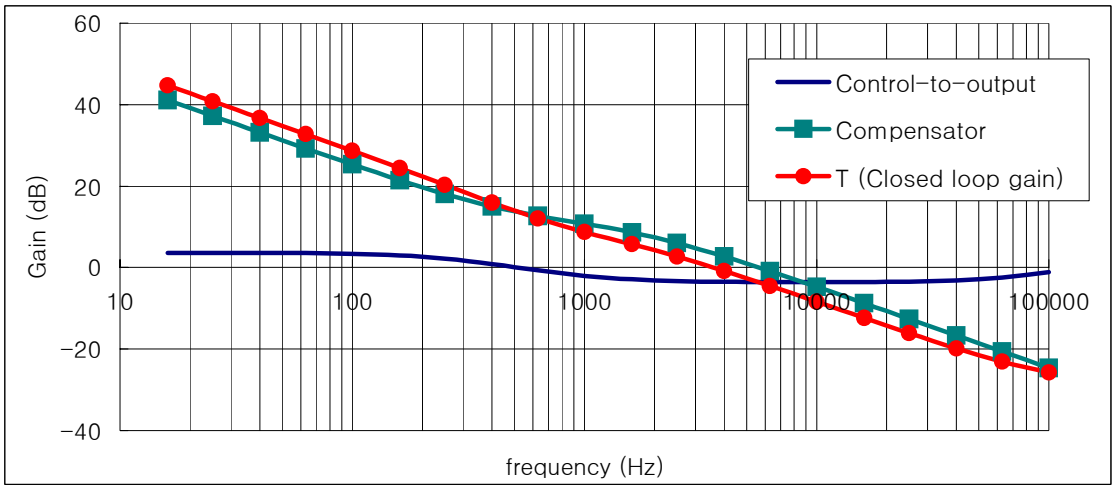
12. Design Feedback control loop

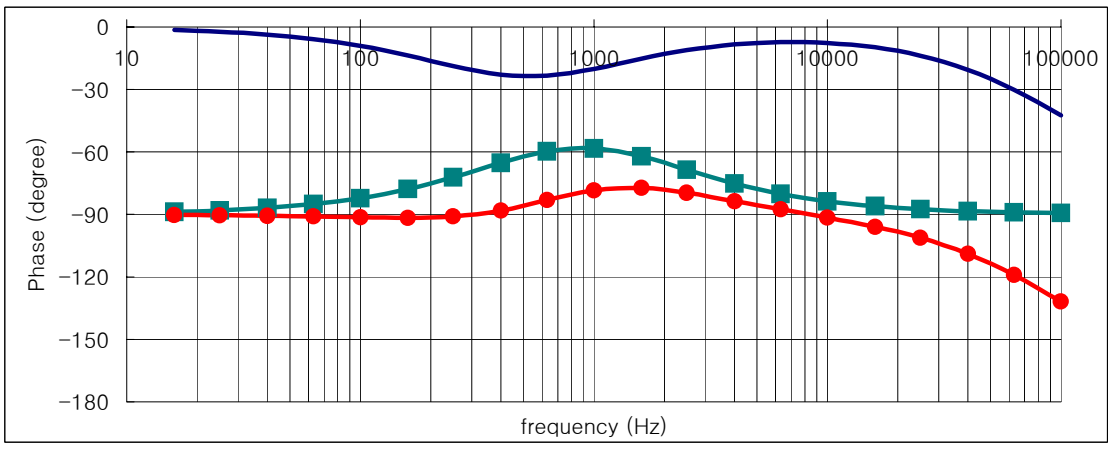
Control-to-output DC gain =	2				
Control-to-output zero (w_z) =	5000	rad/s =>	f_z=	796	Hz
Control-to-output RHP zero (w_{rz})=	694765	rad/s =>	f_{rz}=	110,631	Hz
Control-to-output pole (w_p)=	2153	rad/s =>	f_p=	343	Hz

Voltage divider resistor (R_1)	5.6	kΩ
Voltage divider resistor (R_2)=	18	kΩ
Opto coupler diode resistor (R_D)	1	kΩ
KA431 Bias resistor (R_{bias})	1.2	kΩ
Feeback pin capacitor (C_B) =	33	nF
Feedback Capacitor (C_F) =	47	nF
Feedback resistor (R_F) =	1.2	kΩ



Feedback integrator gain (w_i) =	11398	rad/s =>	f_i=	1,815	Hz
Compensator zero (w_{zc})=	3129	rad/s =>	f_{zc}=	498	Hz
Compensator pole (w_{pc})=	10101	rad/s =>	f_{pc}=	1,608	Hz





☞ **The control bandwidth is 4kHz. Since the crossover frequency is too close to the corner frequency of the post filter (fo=7.2 kHz), the controller is designed to have enough phase margin when ignoring the effect of the post filter.**

Design Summary

- For the FPS, FSDM07652R is chosen. This device has a fixed switching frequency of 66kHz. Startup and soft-start circuits are implemented inside the device.
- To limit the current, 10 ohms resistors (R_a and R_{damp}) are used in series with D_a and D_{R5}. These damping resistors improve the regulations of the very lightly loaded outputs.

Figure 17 shows the final schematic of the flyback converter designed by **FPS Design Assistant.**

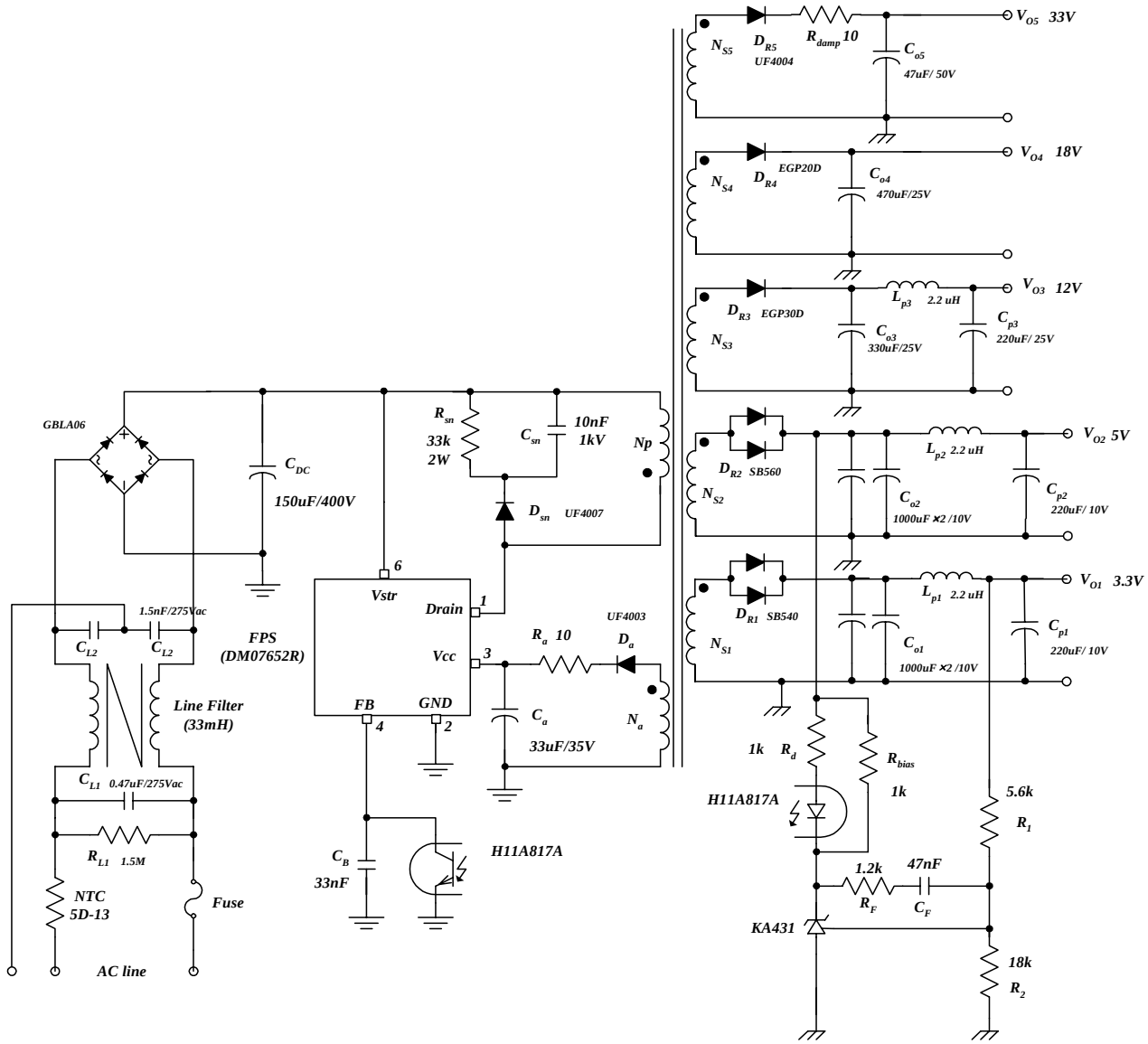


Figure 17. The final schematic of the flyback converter

Experimental Verification

In order to show the validity of the design procedure presented in this paper, the converter of the design example has been built and tested. All the circuit components are used as designed in the design example and the measured transformer characteristics are shown in table 3.

Figure 18 shows the FPS drain current and DC link voltage waveforms at the minimum input voltage and full load condition. As can be seen, the maximum peak drain current (I_{ds}^{peak}) is 2A and the minimum DC link voltage (V_{DC}^{min}) is about 90V. The designed values are 2.01A and 92V, respectively.

Figure 19 shows the FPS drain current and voltage waveforms at the minimum input voltage and full load condition. As designed, the maximum duty ratio (D_{max}) is about 0.5 and the maximum peak drain current (I_{ds}^{peak}) is 2A.

Figure 20 shows the FPS drain current and voltage waveforms at the maximum input voltage and full load condition. The maximum voltage stress on the MOSFET is about 520V, which is lower than the designed value (547V). This is because of the lossy discharge of the inductor or the stray capacitance. Another reason is that the power conversion efficiency at the maximum input voltage is higher than the estimated efficiency used in step-1.

As calculated in design step-4, the converter operates at the boundary between CCM and DCM under the maximum input voltage and full load condition (The maximum DC link voltage guaranteeing CCM at full load was obtained as 375V in design step-4).

Figure 21 shows the current and voltage waveforms of the first output (3.3V) rectifier diode. The maximum reverse voltage of this diode was calculated as 20V in step-9 and the measured value is 23V.

Table 4 shows the line regulation of each output. 3.3V and 5V output shows ±3% and ±4% regulations, respectively.

Figure 22 shows the measured efficiency at the full load condition for different input voltages. The minimum efficiency is about 73% at the minimum input voltage condition better than the 70% target efficiency specified in step-1.

Core	EER3530 (ISU ceramics)
Primary side inductance	682 uH @ 70kHz
Leakage inductance	4.5 uH @70kHz with all other windings shorted.
Resistance	0.76 Ω

Table 3. The measured transformer characteristics

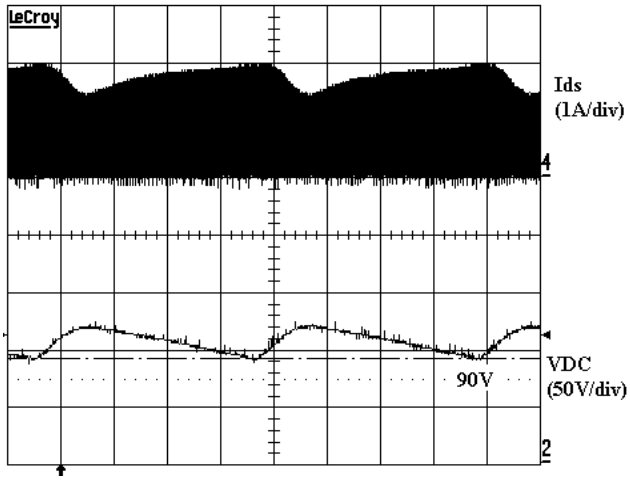


Figure 18. Waveforms of drain current and DC link voltage at 85Vac and full load condition (time:2ms/div)

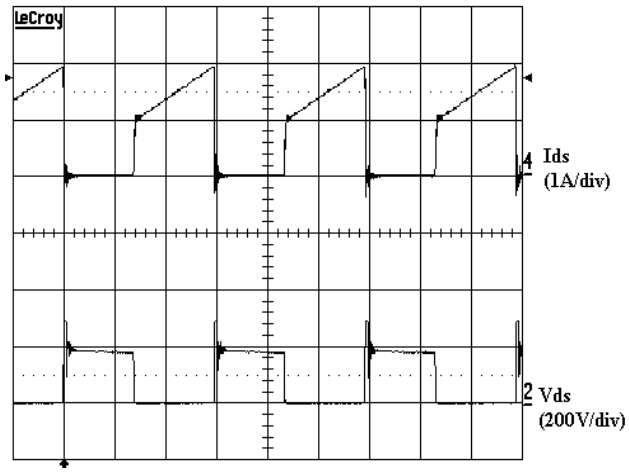


Figure 19. Waveforms of drain current and voltage at 85Vac and full load condition (time : 5us/div)

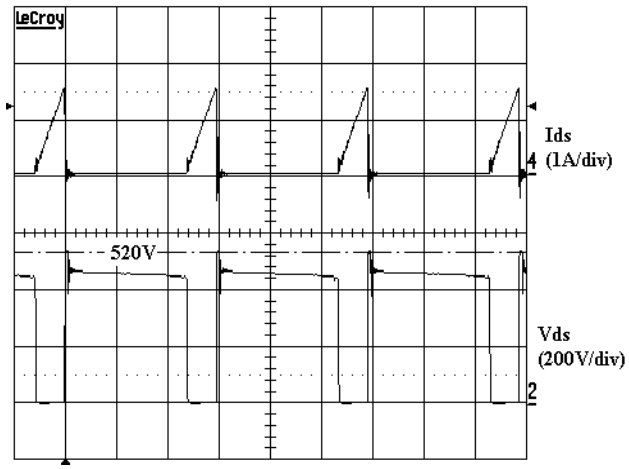


Figure 20. Waveforms of drain current and voltage at 265Vac and full load condition (time : 5us/div)

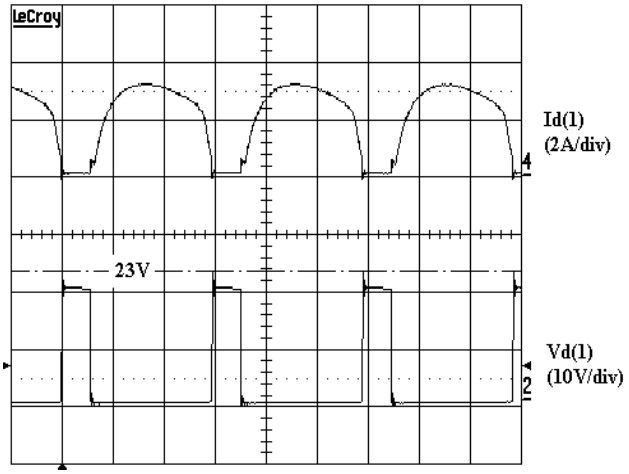


Figure 21. Current and voltage waveforms of the first output (3.3V) rectifier diode at 265Vac and full load condition (time : 5us/div)

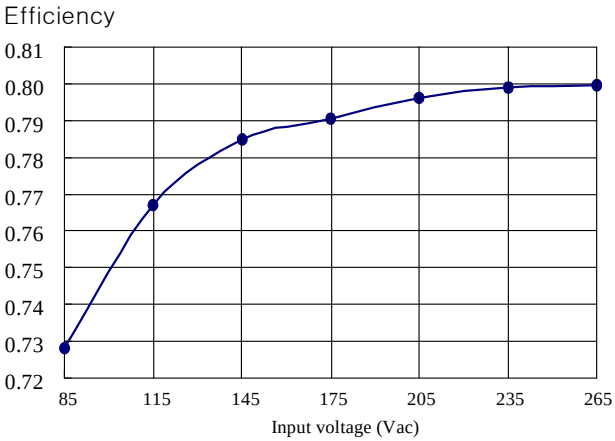


Figure 22. Measured efficiency

Input voltage	Vo1 (3.3V)	Vo2 (5V)	Vo3 (12V)	Vo4 (18V)	Vo5 (33V)
85Vac	**3.21 V**	**5.18 V**	**12.88 V**	**19.7 V**	**35.7 V**
	-2.7 %	3.6 %	7.3 %	9.4 %	8.2 %
115Vac	**3.21 V**	**5.14 V**	**12.77 V**	**19.4 V**	**34.6 V**
	-2.7 %	2.8 %	6.4 %	7.8 %	4.8 %
145Vac	**3.21 V**	**5.11 V**	**12.67 V**	**19.2 V**	**34.1 V**
	-2.7 %	2.2 %	5.6 %	6.7 %	3.2 %
175Vac	**3.21 V**	**5.09 V**	**12.57 V**	**19.1 V**	**33.8 V**
	-2.7 %	1.8 %	4.8 %	5.9 %	2.4 %
205Vac	**3.21 V**	**5.08 V**	**12.52 V**	**19.0 V**	**33.6 V**
	-2.7 %	1.6 %	4.3 %	5.4 %	1.9 %
235Vac	**3.21 V**	**5.07 V**	**12.48 V**	**18.9 V**	**33.5 V**
	-2.7 %	1.4 %	4.0 %	5.1 %	1.6 %
265Vac	**3.21 V**	**5.06 V**	**12.47 V**	**18.9 V**	**33.5 V**
	-2.7 %	1.2 %	3.9 %	5.1 %	1.4 %

Table 4. Line regulation of each output at full load condition

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