MODELING VLIW PROCESSOR

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May 11, 2017

OVERVIEW

1. Assignment Background and Description

I have modelled a basic VLIW Processor and calculated some of the Parameters like:

- Total Number Of V.L.I.W Instruction Bundles Created
- Percentage of bundles with 25% utilization
- Percentage of bundles with 50% utilization
- Percentage of bundles with 75% utilization
- Percentage of bundles with 100% utilization
- Total number of cycles taken by the VLIW Processor to run on the trace

2. Methodology

- Created a VLIW bundle and keep on adding the instructions until the all the independent instructions are added.
- When the VLIW Instruction has achieved maximum possible efficiency it is dispatched and the number of cycles and the utilization are updated accordingly.

3. Observations

- Number of instruction Bundles with 50 % utilization are the Highest followed by 75% utilization followed by 25% utilization.
- Number of instruction bundles with 100% Utilization are very less and amount to just 0.2% of the VLIW instruction Bundles created.

4. Results

Total Number of V.L.I.W Instruction Bundles Created = 988106
Percentage of bundles with 25% utilization = 11.566168
Percentage of bundles with 50% utilization = 67.19421
Percentage of bundles with 75% utilization = 21.03165
Percentage of bundles with 100% utilization = 0.20797364
Total number of cycles taken by the V.L.I.W Processor is = 1728098