MODELING THE MSI CACHE COHERENCY PROTOCOL

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April 25, 2017

OVERVIEW

1. Assignment Background and Description

I have modelled the MSI cache coherency in this lab and calculated some parameters like

- Total number of reads and writes
- Total number of read misses and write misses
- Total number of invalidations
- Total number of reads and writes misses, found in neighboring caches

2. Methodology

GIVEN:

Each Block has a size of 32 Bytes

Associativity = 4

Cache Size is 16KB

CALUCLATED:

Number Of Sets would be

16 KB/128 B = 128 Sets, So 7 Bits for the index [To be able to go through the index]

20bits Address from the trace <--> 8(Tag) + 7(Index) + 5(Offset)

Technical Description:

Created a processor class which contains a processor id and the cache class.

Created a cacheLine class which contains the states of the cacheLine and Tag .

3. Observations

- Number of reads+writes occurring in the Cache Coherency model (MSI) is more than writes demanded by the trace which is because of the some additional write backs which are required In Some Cases.
  Ex : When the cacheLine is in Modified state and when a write was snooped from the bus additional writeback is required into the main memory

4. Results

----------For 1 Processor----------

Total Number Of Reads = 133937

Total Number Of Writes = 66063

Total Number Of Write Misses = 65040

Total Number Of Read Misses = 131791

Total Number Of Read Miss Found in Neighborhood Cache = 0

Total Number Of Read Miss Found in Neighborhood Cache = 0

----------End of 1 Processor----------

----------For 2 Processors----------

Total Number Of Reads = 266978

Total Number Of Writes = 134640

Total Number Of Write Misses = 130953

Total Number Of Read Misses = 262761

Total Number Of Read Miss Found in neighborhood Cache = 4052

Total Number Of Read Miss Found in neighborhood Cache = 2042

----------End Of 2 Processors----------

----------For 4 Processors----------

Total Number Of Reads = 533400

Total Number Of Writes = 270789

Total Number Of Write Misses = 262439

Total Number Of Read Misses = 525059

Total Number Of Read Miss Found in neighborhood Cache = 24043

Total Number Of Read Miss Found in neighborhood Cache = 11979

----------End Of 4 Processors----------