

| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020
| Date : Fri Mar 29 12:18:39 2024
| Host : CEAT-ENDV350-09 running 64-bit major release (build 9200)
| Command : report_power -file top_demo_power_routed_1.rpt -pb top_demo_power_summary_routed_1.pb -rpx top_demo_power_routed_1.rpx
| Design : top_demo
| Device : xc7z020clg484-1
| Design State : routed
| Grade : commercial
| Process : typical
| Characterization : Production

Power Report

Table of Contents
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1. Summary

Total On-Chip Power (W)	17.481 (Junction temp exceeded!)
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	16.440
Device Static (W)	1.041
Effective TJA (C/W)	11.5
Max Ambient (C)	0.0
Junction Temperature (C)	125.0
Confidence Level	Low

Setting File	---
Simulation Activity File	---
Design Nets Matched	NA
+-------------------------+---------------------------------+
* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

+---------------+-----------+----------+-----------+-----------------+
| On-Chip | Power (W) | Used | Available | Utilization (%) |
+---------------+-----------+----------+-----------+-----------------+
Slice Logic	0.438	117	---	---
LUT as Logic	0.381	35	53200	0.07
Register	0.027	53	106400	0.05
CARRY4	0.024	10	13300	0.08
BUFG	0.006	1	32	3.13
Others	0.000	9	---	---
Signals	0.550	107	---	---
I/O	15.452	28	200	14.00
Static Power	1.041			
Total	17.481			
+---------------+-----------+----------+-----------+-----------------+

1.2 Power Supply Summary

+-----------+-------------+-----------+-------------+------------+-------------+-------------+------------+
| Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) | Powerup (A) | Budget (A) | Margin (A) |
+-----------+-------------+-----------+-------------+------------+-------------+-------------+------------+
Vccint	1.000	1.310	1.012	0.299	NA	Unspecified	NA
Vccaux	1.800	0.665	0.565	0.100	NA	Unspecified	NA
Vcco33	3.300	4.368	4.367	0.001	NA	Unspecified	NA
Vcco25	2.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco18	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vcco15	1.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco135	1.350	0.000	0.000	0.000	NA	Unspecified	NA
Vcco12	1.200	0.000	0.000	0.000	NA	Unspecified	NA
Vccaux_io	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vccbram	1.000	0.026	0.000	0.026	NA	Unspecified	NA

MGTAVcc	1.000	0.000	0.000	0.000	NA	Unspecified	NA
MGTAVtt	1.200	0.000	0.000	0.000	NA	Unspecified	NA
MGTVccaux	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vccpint	1.000	0.473	0.000	0.473	NA	Unspecified	NA
Vccpaux	1.800	0.010	0.000	0.010	NA	Unspecified	NA
Vccpll	1.800	0.003	0.000	0.003	NA	Unspecified	NA
Vcco_ddr	1.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco_mio0	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vcco_mio1	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vccadc	1.800	0.020	0.000	0.020	NA	Unspecified	NA

1.3 Confidence Level

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is routed	
Clock nodes activity	Low	User specified less than 75% of clocks	Provide missing clock activity with a constraint file, simulation results or by editing the "By Clock Domain" view
I/O nodes activity	Low	More than 75% of inputs are missing user specification	Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
Device models	High	Device models are Production	
Overall confidence level	Low		

2. Settings

2.1 Environment

Ambient Temp (C)	25.0
ThetaJA (C/W)	11.5
Airflow (LFM)	250
Heat Sink	none
ThetaSA (C/W)	0.0
Board Selection	medium (10"x10")
# of Board Layers	8to11 (8 to 11 Layers)
Board Temperature (C)	25.0

2.2 Clock Constraints

Clock	Domain	Constraint (ns)

3. Detailed Reports

3.1 By Hierarchy

Name	Power (W)
top_demo	16.440
div_child	0.060
driver	0.245
dut	0.268