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| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020
| Date : Fri Mar 29 12:18:39 2024
| Host : CEAT-ENDV350-09 running 64-bit major release (build 9200)
| Command : report_utilization -file route_report_utilization_0.rpt -pb route_report_utilization_0.pb
| Design : top_demo
| Device : 7z020clg484-1
| Design State : Routed

Utilization Design Information

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1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	35	0	53200	0.07
LUT as Logic	35	0	53200	0.07
LUT as Memory	0	0	17400	0.00
Slice Registers	53	0	106400	0.05
Register as Flip Flop	47	0	106400	0.04
Register as Latch	6	0	106400	<0.01
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
10	Yes	-	Reset
0	Yes	Set	-
43	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	20	0	13300	0.15
SLICEL	11	0		
SLICEM	9	0		
LUT as Logic	35	0	53200	0.07
using O5 output only	0			
using O6 output only	26			
using O5 and O6	9			
LUT as Memory	0	0	17400	0.00
LUT as Distributed RAM	0	0		
LUT as Shift Register	0	0		
Slice Registers	53	0	106400	0.05
Register driven from within the Slice	52			
Register driven from outside the Slice	1			
LUT in front of the register is unused	1			
LUT in front of the register is used	0			
Unique Control Sets	5		13300	0.04

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

3. Memory

+----------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00
+----------------+------+-------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. DSP

+-----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------+------+-------+-----------+-------+
| DSPs | 0 | 0 | 220 | 0.00 |
+-----------+------+-------+-----------+-------+

5. IO and GT Specific

+----------------------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+----------------------------+------+-------+-----------+-------+
Bonded IOB	28	28	200	14.00
IOB Master Pads	14			
IOB Slave Pads	11			
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00

IDELAYCTRL	0	0	4	0.00
IBUFDS	0	0	192	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	200	0.00
OLOGIC	0	0	200	0.00

6. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	16	0.00
MMCME2_ADV	0	0	4	0.00
PLLE2_ADV	0	0	4	0.00
BUFMRCE	0	0	8	0.00
BUFHCE	0	0	72	0.00
BUFR	0	0	16	0.00

7. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

8. Primitives

Ref Name	Used	Functional Category
FDRE	43	Flop & Latch
OBUF	18	IO
LUT6	18	LUT
CARRY4	10	CarryLogic
LUT2	8	LUT
IBUF	8	IO
LUT4	7	LUT
LDCE	6	Flop & Latch
LUT5	5	LUT
LUT3	5	LUT
FDCE	4	Flop & Latch
OBUFT	2	IO
LUT1	1	LUT
BUFG	1	Clock

9. Black Boxes

Ref Name	Used

10. Instantiated Netlists

Ref Name	Used