| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020

| Date : Fri Mar 29 12:18:39 2024

| Host : CEAT-ENDV350-09 running 64-bit major release (build 9200)

: report_timing -file route_report_timing_0.rpt -rpx route_report_timing_0.rpx | Command

: top demo | Design | Device : 7z020-clg484

| Speed File : -1 PRODUCTION 1.12 2019-11-22

Timing Report

Slack: inf Source: btn[2]

(input port)

Destination: sseg_dp

(output port)

Path Group: (none)

Path Type: Max at Slow Process Corner

Data Path Delay: 13.775ns (logic 5.286ns (38.376%) route 8.489ns (61.624%))

Logic Levels: 3 (IBUF=1 LUT5=1 OBUF=1)

Loc	cation	Delay type	Incr(ns) Path(ns)	Netlist Resource(s)
U7			0.000 0.000 f btn[2]	(IN)
		net (fo=0)	0.000 0.000 btn[2	2]
U7		IBUF (Prop_ibuf_	I_O) 1.430 1.430) f btn_IBUF[2]_inst/O
net (fo=1, routed) 6.400 7.830 driver/btn_IBUF[2]				river/btn_IBUF[2]
SLICE_X102Y76 LUT5 (Prop_lut5_I4_O) 0.150 7.980 r				
driver/segment cathodes/O				
	net (fo=1, routed) 2.089 10.068 sseg dp OBUF			seg dp OBUF
K2	0	OBUF (Prop_obu	ıf_I_O) 3.707 13.	775 r sseg_dp_OBUF_inst/O
		net (fo=0)	0.000 13.775 sse	g dp
K20	0	. ,	r sseg_dp (0	OUT)