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| Tool Version: Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020

| Date : Fri Mar 29 11:47:47 2024

| Host : CEAT-ENDV350-09 running 64-bit major release (build 9200) | Command : report_utilization -file top_demo_utilization_synth.rpt -pb

top demo utilization synth.pb

| Design : top_demo | Device : 7z020clg484-1 | Design State : Synthesized

Utilization Design Information

Table of Contents

- 1. Slice Logic
- 1.1 Summary of Registers by Type
- 2. Memory
- 3. DSP
- 4. IO and GT Specific
- 5. Clocking
- 6. Specific Feature
- 7. Primitives
- 8. Black Boxes
- 9. Instantiated Netlists
- 1. Slice Logic

+	-++
Site Type	Used Fixed Available Util%
+	-++
Slice LUTs*	36 0 53200 0.07
LUT as Logic	36 0 53200 0.07
LUT as Memory	0 0 17400 0.00
Slice Registers	53 0 106400 0.05
Register as Flip F	Flop 47 0 106400 0.04
Register as Latch	h 6 0 106400 <0.01
F7 Muxes	0 0 26600 0.00
F8 Muxes	0 0 13300 0.00
+	++

^{*} Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

+-----+ | Total | Clock Enable | Synchronous | Asynchronous | +-----+ 10 -| 0 | - [Set | |0 | - | Reset | |0 | _| Set | -| 10 | Reset | _ | - | 0 Yes | -| -| 10 Yes | - | Set | | 10 | Yes | - | Reset | 10 | Yes | Set | - | | 43 | Yes | Reset | - |

2. Memory

+-----+
| Site Type | Used | Fixed | Available | Util% |
+-----+
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00
+------+				

3. DSP

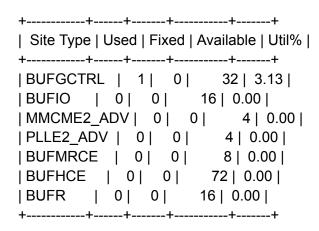
+-----+
| Site Type | Used | Fixed | Available | Util% |
+-----+
| DSPs | 0 | 0 | 220 | 0.00 |
+-----+

^{*} Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. IO and GT Specific

```
| Used | Fixed | Available | Util% |
   .----+
| Bonded IOB
                 | 28 |
                        0 |
                             200 | 14.00 |
| Bonded IPADs
                 | 0 | 0 |
                              2 | 0.00 |
| Bonded IOPADs
                  | 0| 0|
                              130 | 0.00 |
                   | 0 | 0 |
| PHY_CONTROL
                               4 | 0.00 |
                  | 0| 0|
| PHASER REF
                               4 | 0.00 |
OUT_FIFO
                 | 0| 0|
                            16 | 0.00 |
                | 0 | 0 |
IN FIFO
                            16 | 0.00 |
| IDELAYCTRL
                 | 0 | 0 |
                               4 | 0.00 |
| IBUFDS
                | 0 | 0 | 192 | 0.00 |
| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 |
                                        16 | 0.00 |
| PHASER_IN/PHASER_IN_PHY | 0 | 0 |
                                     16 | 0.00 |
| IDELAYE2/IDELAYE2 FINEDELAY | 0 | 0 |
                                      200 | 0.00 |
              | 0 | 0 | 200 | 0.00 |
ILOGIC
                | 0 | 0 | 200 | 0.00 |
OLOGIC
+-----+
```

5. Clocking



6. Specific Feature

```
+----+
| Site Type | Used | Fixed | Available | Util% |
+----+
4 | 0.00 |
|CAPTUREE2 | 0| 0|
                   1 | 0.00 |
|DNA_PORT | 0| 0|
                  1 | 0.00 |
|EFUSE_USR | 0| 0|
                   1 | 0.00 |
|FRAME_ECCE2| 0| 0|
                   1 | 0.00 |
| ICAPE2 | 0 | 0 |
                 2 | 0.00 |
|STARTUPE2 | 0| 0|
                  1 | 0.00 |
     | 0| 0|
                 1 | 0.00 |
+----+
```

7. Primitives

```
+----+
| Ref Name | Used | Functional Category |
+----+
|FDRE | 43|
                Flop & Latch |
|LUT6 | 19|
                   LUT |
| OBUF | 18 |
                    10 |
| CARRY4 | 10 |
                  CarryLogic |
LUT2
      | 8|
                   LUT |
      | 8|
| IBUF
                   10 |
                   LUT |
LUT3
      | 6|
               Flop & Latch |
LDCE
      | 6|
LUT5
      | 5|
                   LUT |
|LUT4 | 5|
                   LUT |
|FDCE | 4|
               Flop & Latch |
|OBUFT | 2|
                    10 |
|LUT1 | 2|
                   LUT |
|BUFG | 1|
                  Clock |
```

8. Black Boxes

+----+ | Ref Name | Used | +-----+

9. Instantiated Netlists
++
Ref Name Used

+----+