

| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020
| Date : Fri Mar 29 11:48:45 2024
| Host : CEAT-ENDV350-09 running 64-bit major release (build 9200)
| Command : report_timing_summary -max_paths 10 -file top_demo_timing_summary_routed.rpt -pb top_demo_timing_summary_routed.pb -rpx top_demo_timing_summary_routed.rpx -warn_on_violation
| Design : top_demo
| Device : 7z020-clg484
| Speed File : -1 PRODUCTION 1.12 2019-11-22

Timing Summary Report

| Timer Settings
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Enable Multi Corner Analysis : Yes
Enable Pessimism Removal : Yes
Pessimism Removal Resolution : Nearest Common Node
Enable Input Delay Default Clock : No
Enable Preset / Clear Arcs : No
Disable Flight Delays : No
Ignore I/O Paths : No
Timing Early Launch at Borrowing Latches : No
Borrow Time for Max Delay Exceptions : Yes
Merge Timing Exceptions : Yes

Corner Name	Analyze Max Paths	Analyze Min Paths
Slow	Yes	Yes
Fast	Yes	Yes

check_timing report

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1. checking no_clock (103)
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11. checking partial_output_delay (0)
12. checking latch_loops (0)

1. checking no_clock (103)

There are 41 register/latch pins with no clock driven by root clock pin: sysclk_125mhz (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[0]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[10]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[11]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[12]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[13]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[14]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[15]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[16]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin:
CURRENT_COUNT_reg[1]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[2]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[3]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[4]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[5]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[6]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[7]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[8]/Q (HIGH)

There are 2 register/latch pins with no clock driven by root clock pin: CURRENT_COUNT_reg[9]/Q (HIGH)

There are 4 register/latch pins with no clock driven by root clock pin: div_child/clk_count_reg[23]/Q (HIGH)

There are 6 register/latch pins with no clock driven by root clock pin: dut/FSM_sequential_state_reg[0]/Q (HIGH)

There are 6 register/latch pins with no clock driven by root clock pin: dut/FSM_sequential_state_reg[1]/Q (HIGH)

There are 6 register/latch pins with no clock driven by root clock pin: dut/FSM_sequential_state_reg[2]/Q (HIGH)

There are 6 register/latch pins with no clock driven by root clock pin: dut/FSM_sequential_state_reg[3]/Q (HIGH)

2. checking constant_clock (0)

There are 0 register/latch pins with constant_clock.

3. checking pulse_width_clock (0)

 There are 0 register/latch pins which need pulse_width check

4. checking unconstrained_internal_endpoints (98)

 There are 98 pins that are not constrained for maximum delay. (HIGH)

 There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no_input_delay (4)

 There are 4 input ports with no input delay specified. (HIGH)

 There are 0 input ports with no input delay but user has a false path constraint.

6. checking no_output_delay (11)

 There are 11 ports with no output delay specified. (HIGH)

 There are 0 ports with no output delay but user has a false path constraint

 There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple_clock (0)

 There are 0 register/latch pins with multiple clocks.

8. checking generated_clocks (0)

 There are 0 generated clocks that are not connected to a clock source.

9. checking loops (0)

 There are 0 combinational loops in the design.

10. checking partial_input_delay (0)

There are 0 input ports with partial input delay specified.

11. checking partial_output_delay (0)

There are 0 ports with partial output delay specified.

12. checking latch_loops (0)

There are 0 combinational latch loops in the design through latch input

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| Design Timing Summary
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WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints

NA NA NA NA NA NA NA NA NA NA NA NA

There are no user specified timing constraints.

| Clock Summary
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| Intra Clock Table
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Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints
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| Inter Clock Table
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From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints
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| Other Path Groups Table
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Path Group From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints
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| Timing Details
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