ECE 115C Final Project Report
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Phase	**1**	**2**	**3**
Analytical D(critical path)	39.79	N/A	55.71
Simulation D(critical path)	N/A	312.300615	559.40115
Analytical Energy	41.31	N/A	9.55
Simulation Energy	N/A	-0.99336	-0.2277408

Total Energy Reduction [%]	**Contribution from sizing**	**Contribution from Vdd**
Analytical model [%]	47.44	29.44
Simulation model [%]	19.79342836	57.28026094
Total delay increase [%]	**Contribution from sizing**	**Contribution from Vdd**
Analytical model [%]	18.4	21.6
Simulation model [%]	-8.124999049	48.124999049

Tables 1 and 2. Summary metrics.

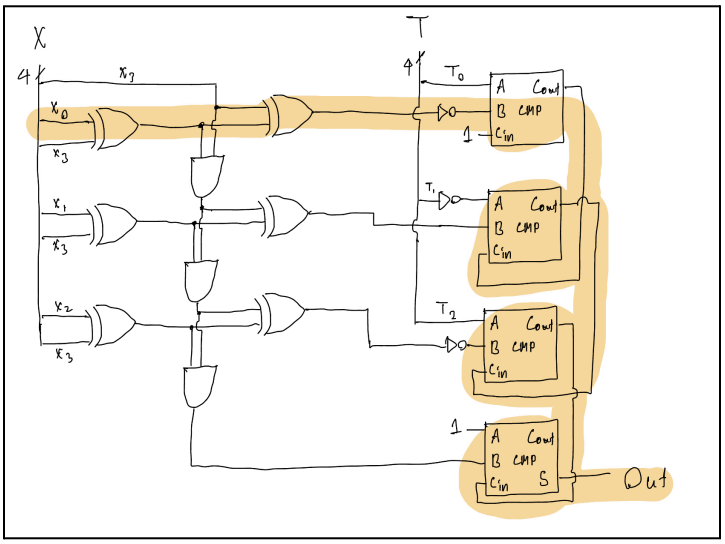


Figure 1. Top-level diagram with highlighted critical path.

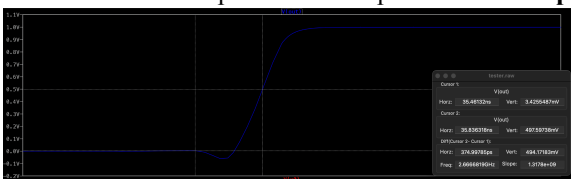
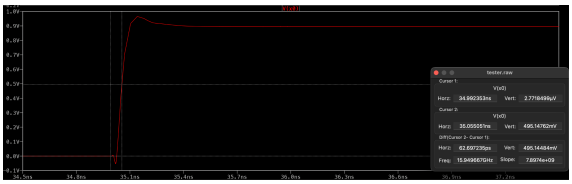
Gate	**XOR0**	**XOR3**	**INV**	**CMP0**	**CMP1**	**CMP2**	**CMP3**	**CMP Cout**
PMOS	600	778.0912035 224.9590393	1009.04729 144.8494027	2617.06821 237.6325098	3394.09048 262.9236565	4401.40598 374.3474752	5708.11672 702.0776706	7402.44158 1910.368358

NMOS	400	518.727469 149.9726929	672.6981933 96.56626848	1744.712142 158.421673	2262.726992 175.2824377	2934.270654 249.5649834	3805.41115 468.0517804	4934.961054 1273.578906
TGATE	400	518.727469 149.9726929						

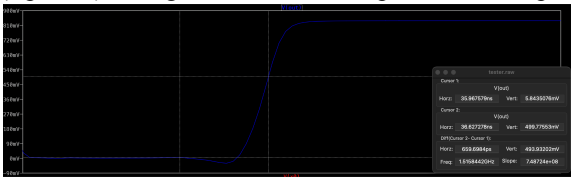
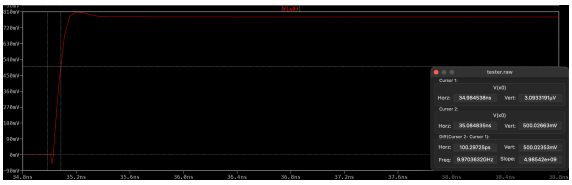
Table 3. Baseline sizing in red. Optimal sizing in blue.

Critical path practical worst case delay:

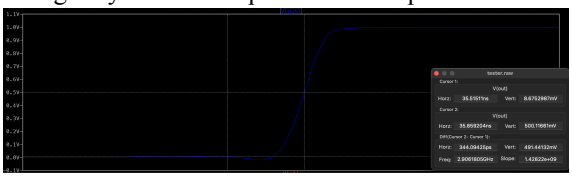
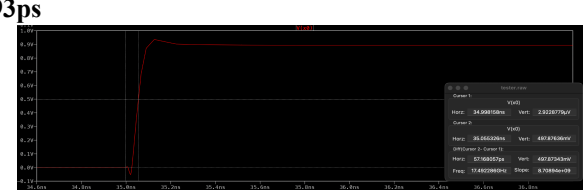
- **x=1011, t=0010 with transitions at x0: 0->1 and t2: 1->0. Switching t2 does not affect critical path but allows us to measure the output transition more clearly.**
- **Test starts at 35ns.**
  - Baseline: 374.99785ps - 62.697235ps = **312.300615ps**

  - (Optimal) Sizing + VDD: 659.6984ps - 100.29725ps = **559.40115ps**

  - Sizing only: 344.09425ps - 57.168057ps = **286.926193ps**

Design decisions and rationale:

- Initially, we minimized the number of transistors by choosing optimal logic gates. E.g., transmission gate instead of CMOS XOR, comparators instead of full adders.
- Then we used truth tables to minimize the logic. E.g. adding 0001 does not actually require full adders. Since the input is fixed, we can simplify the logic down to 1 AND and 1 XOR gate for the non-fixed inputs.
- Finally, we identified points in the critical path where we could save time. E.g., by switching the order of inputs in an XOR gate, we could have the critical path going through a shorter stage.

Trade-offs to achieve design goals:

- Size vs. VDD: increasing sizing and decreasing width to make our energy consumption a lot lower but consequently increases our delay.
- Optimizing for the critical path vs. optimizing for the rest of the circuit: we didn't want to increase the delay of the other paths by so much that they would in turn become the critical path.