



IT8733

**Environment Control – Low Pin Count Input / Output
(EC - LPC I/O)**

Preliminary Specification V0.4.1

(For D Version)

ITE TECH. INC.

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1. Features

■ Low Pin Count Interface

- Complies with Intel Low Pin Count Interface Specification Rev. 1.1
- Supports SERIRQ protocols
- Supports PCI PME# Interfaces

■ 8032 Embedded Controller

- Twin turbo version/3-stage pipelines
- 9.2 MHz for EC domain and 8032 internal timer
- Variable frequency range to gain the maximum 8032 code-fetch performance
- Instruction set compatible with standard 8051/2
- 4K SRAM for code/data space
- 2K SRAM for data space

■ ACPI & LANDesk Compliant

- ACPI V. 2.0 compliant
- Register sets compatible with "Plug and Play ISA Specification V. 1.0a"
- LANDesk 3.X compliant
- Supports 13 logical devices

■ Enhanced Hardware Monitor

- Built-in 8-bit Analog to Digital Converter
- 3 thermal inputs from either remote thermal resistor or thermal diode or diode-connected transistor, the temperature sensor of the current mode
- 8 voltage monitor inputs (3VSB and VBAT measured internally)
- 1 chassis open detection input with low power Flip-Flop dual-powered by battery or 3VSB
- Watch Dog comparison of all monitored values
- SST/PECI/AMDTSI/PCH SM-Link I/F supporting external temperature reading for fan control

■ Fan Speed Controller

- Provides fan on-off and PWM control
- Supports 4 programmable Pulse Width Modulation (PWM) outputs
- 256 steps of PWM mode
- Monitors 4 fan tachometer inputs
- Provides fan close-loop control

■ SmartGuardian Controller

- Provides programmably automatic fan speed control
- Supports mix-and-match for temperature inputs and fan speed control outputs
- Overrides fan speed controller during catastrophic situations
- Provides audible over temperature warning

■ Two 16C550 UARTs

- Supports two standard Serial Ports

■ Consumer Remote Control (TV remote) IR with Power-up Feature

- Supports two CIR Ports

■ EEE 1284 Parallel Port

- Standard mode -- Bi-directional SPP compliant
- Enhanced mode -- EPP V. 1.7 and V. 1.9 compliant
- High-speed mode -- ECP, IEEE 1284 compliant
- Back-drive current reduction
- Printer power-on damage reduction
- Supports POST (Power-On Self Test) Data Port

■ Keyboard Controller

- 8042 compatible with PS/2 keyboard and mouse
- Hardware KBC
- GateA20 and Keyboard reset output
- Supports Multiple keyboard power-on events (Any Keys, 2-5 Sequential Keys, 1-3 simultaneous Keys)
- Supports mouse double-click and/or mouse move power on events

■ 51 General Purpose I/O Pins

- Input mode supports either switch de-bounce or programmable external IRQ input routing
- Output mode supports 2 sets of programmable LED blinking periods

■ BRAM

- 192-byte battery-backed memory space mapped into host and EC side.

■ Flash Interface

- Behaves as LPC/FWH memory device (HLPC) or SPI memory slave (HSPI) to host SouthBridge
- Supports external serial flash with 32.3 MHz
- Up to 16M bytes of flash space shared by host and EC side (serial flash)
- HSPI: Supports ICH 20MHz SPI with SPI flash meeting 33MHz READ instruction

■ SMBus Controller

- SMBus spec. 2.0
- 3 SMBus masters + 2 slave
- 3 SMBus channels
- Compatible with I2C cycle

- **EC Wake Up Control**

- 30 external/internal wake up events

- **Interrupt Controller**

- 56 interrupt events to EC
 - Fixed priority

- **Watch Dog Timer**

- Time resolution 1 minute or 1 second, maximum 65535 minutes or 65535 seconds
 - Output to KRST# when expired
 - 3 internal 16-bit multi-function timers inside 8032, which is based on EC clock
 - 1 internal WDT inside 8032, which is based on EC clock
 - 1 external 16-bit timer in ETWD module, which is based on 32 k clock source
 - 1 external 16-bit WDT in ETWD module, which is based on 32 k clock source

- **KB Matrix Scan**

- Hardware keyboard scan
 - 6x2 keyboard matrix scan

- **In-System Programming**

- ISP via Parallel-Port/SMBUS interface on existing Parallel-Port/SMBUS connector
 - Flash programming with software provided by ITE

- **ITE's Innovative Automatic Power-failure Resume and Power Button De-bounce**

- **Eco-design of Energy-using Product (EuP), Extra Low Power S5 Control**

- **Intel DSW Support**

- **RTC Alarm for EUP Function**

- **Dedicated Infrared Pins**

- **Built-in 32.768 kHz Oscillator**

- **AMD CPU Power Sequence Controller**

- Built-in enhanced voltage comparator

- **Single 24/48 MHz Clock Input**

- **3VSB and VBAT Supported**

- **+3.3V Power Supply**

- **128-Pin QFP/LQFP**

- **RoHS Compliant (100% Green Available)**

2. General Description

The IT8733 is a highly integrated Super I/O using the Low Pin Count Interface. It provides the most commonly used legacy Super I/O functionality plus the latest Environment Control initiatives, including H/W Monitor and Fan Speed Controller. Besides, it not only provides external flash interface for system BIOS and EC code but also supports the external flash (or EPROM) to be shared by the host and EC side. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.1". The IT8733 is ACPI & LANDesk compliant.

The IT8733 features an enhanced hardware monitor providing three thermal inputs from remote thermal resistors, or thermal diode or diode-connected transistor (2N3904/2N3906). The device employs ITE's innovative intelligent automatic Fan ON/OFF & speed control functions (SmartGuardian) to protect the system while reducing the system noise and power consumption. The Fan Speed Controller can control up to three fan speeds through five separate 256 steps of Pulse Width Modulation (PWM) output pins and monitor up to four FANs' Tachometer inputs.

In addition, it features two 16C550 standard compatible enhanced UARTs performing asynchronous communication, one multi-mode high-performance parallel port supporting bi-directional Standard Parallel Port (SPP), Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9), and IEEE 1284 compliant Extended Capabilities Port (ECP), one integrated Keyboard Controller, nine GPIO ports controlling up to 51 GPIO pins, which can be individually enabled or disabled via software configuration registers, and IR interface supported.

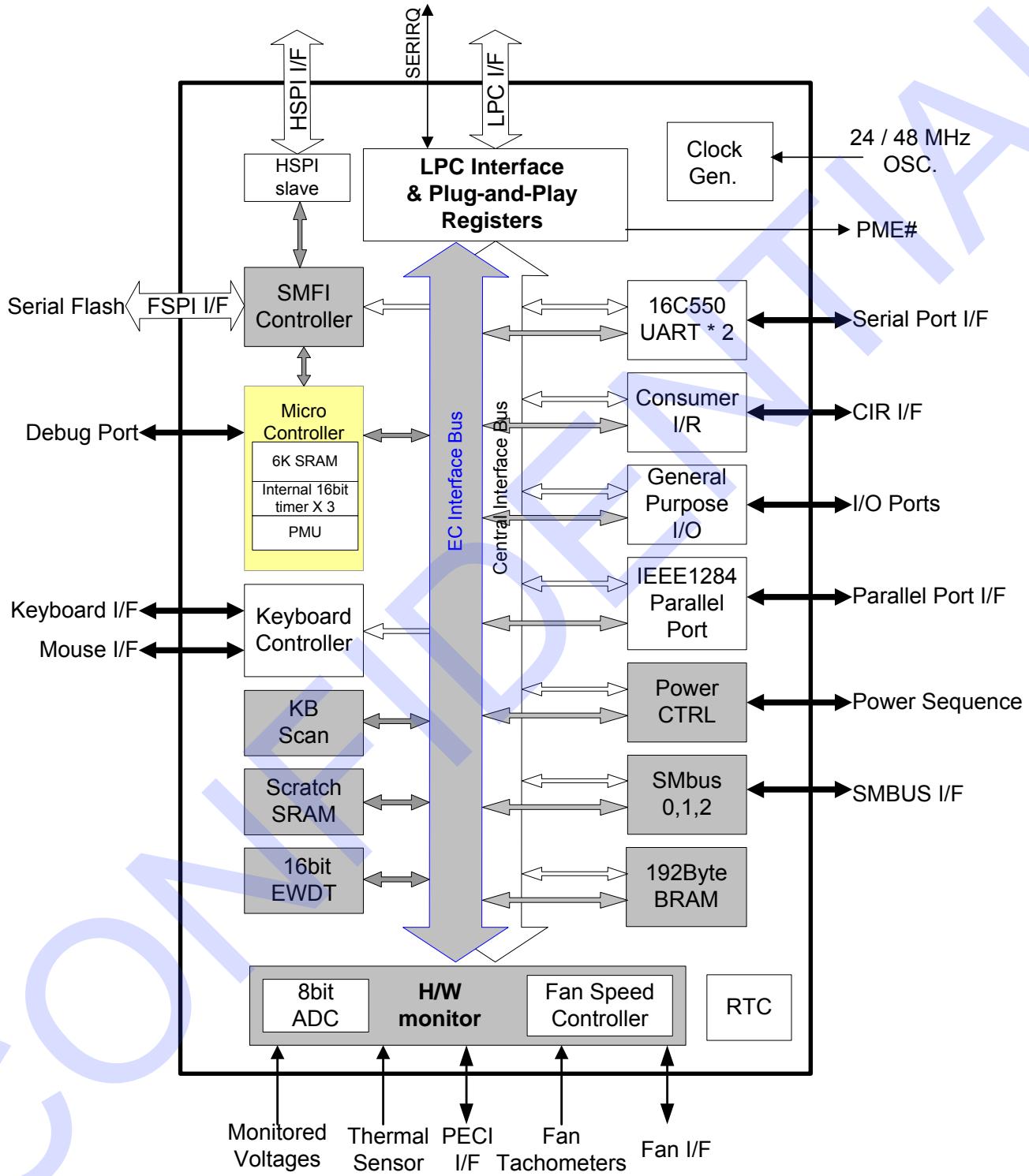
Moreover, the IT8733 provides not only a solution to reducing power consumption in S5 State but also Keyboard, Mouse, RI# and CIR wakeup events in S3/S5 State.

The IT8733 utilizes power-saving circuitry to reduce power consumption, and once a logical device is disabled, the inputs are inhibited with the clock disabled and the outputs are tri-stated. The device requires a single 24/48 MHz clock input and operates with +3.3V power supply. The IT8733 is available in 128-pin QFP/LQFP package.

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3. Block Diagram



3.1 Host/EC Mapped Memory Space

Figure 3-1. Host/Flash and EC/Flash Mapping (General)

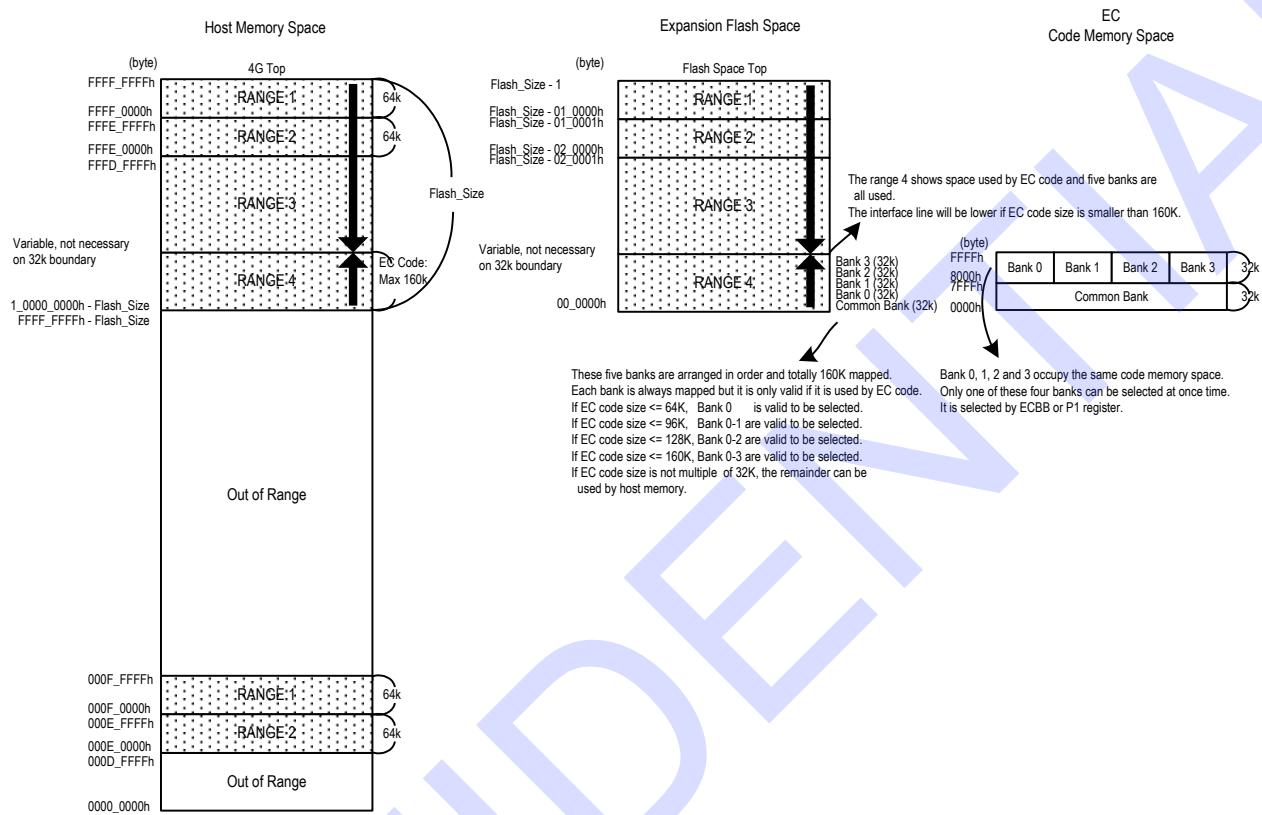
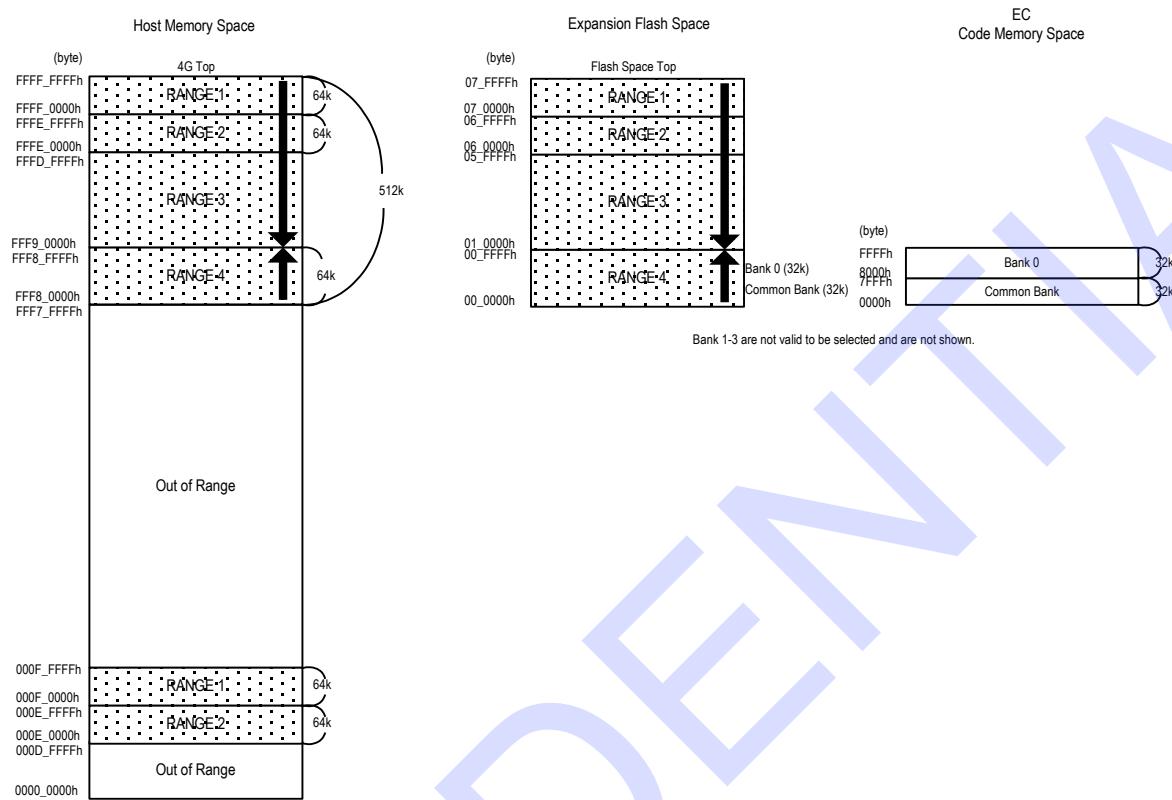


Figure 3-2. Host/Flash and EC/Flash Mapping (Flash Size = 512k, EC Code = 64k, a specific example)



The flash memory space is shared between the host side and EC side, and it is shown in Figure 3-1. An example of 512k flash size, 64k EC code size is shown in Figure 3-2.

The host memory 4G byte top is always mapped into the top of flash space and the host processor fetches the first instruction after reset at FFFF_FFF0h in the host memory, which is 16 bytes below the uppermost flash space.

The bottom of EC code is always mapped into the bottom of flash space and EC R8032TT micro-controller fetches the first instruction after reset at 00_0000h in the EC code memory, which is 1 byte in the lowermost flash space.

The interface line of host memory and EC code is variable and not necessary on 32k boundary.

Table 3-1. Host/Flash Mapping

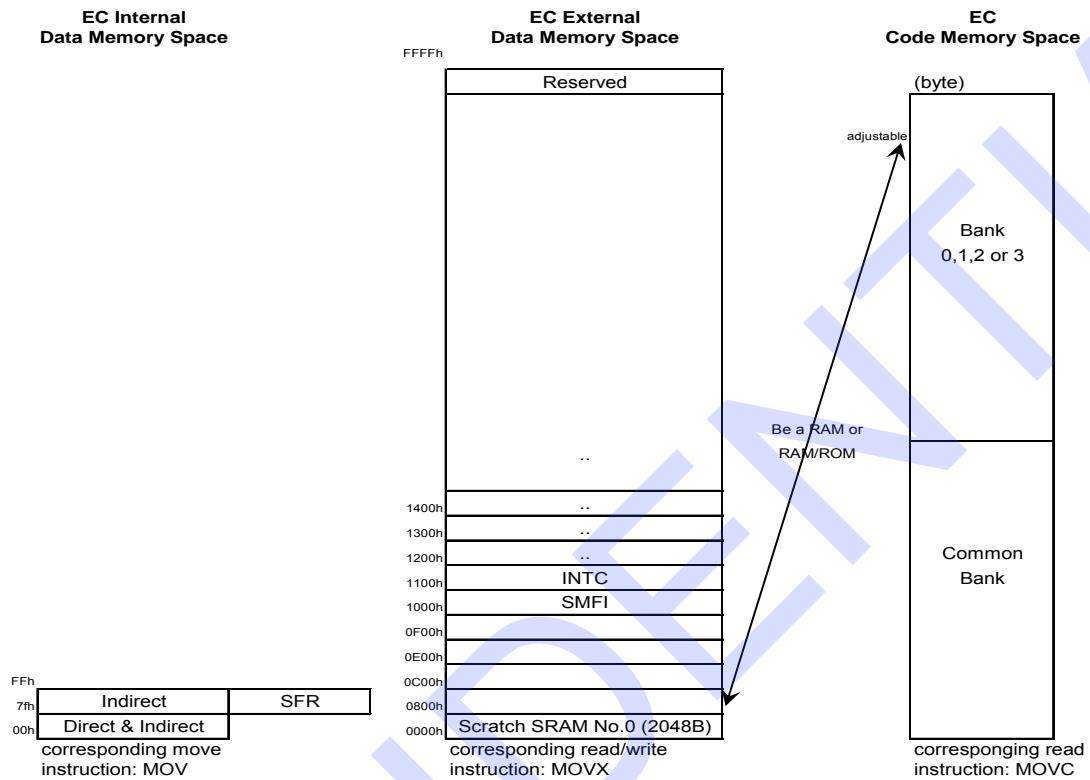
Host Memory Space on LPC Bus (byte)	Mapped Expansion Flash Space (byte)	Size (byte)	Mapping Condition
(1_0000_0000h~Flash_Size)~ FFFF_FFFFh	00_0000h~ (Flash_Size-1)	Flash_Size	Always
000F_0000h ~ 000F_FFFFh	(Flash_Size-01_0000h)~ (Flash_Size-1)	64k	Always
000E_0000h ~ 000E_FFFFh	(Flash_Size-02_0000h)~ (Flash_Size-01_0001h)	64k	BIOSEXTS=1
Note: The host side can map all flash range regardless of EC code space. Note: All host mappings are controlled by HBREN bit in HCTRL2R register. Note: Flash Size is defined in FMSSR register.			

Table 3-2. EC/Flash Mapping

EC Code Memory Space (byte)	Mapped Flash Address Range (byte)	Size (byte)	Mapping Condition	Bank Selected Condition
Bank 3: 8000h ~ FFFFh	02_0000h ~ 02_7FFFh	32k	Always	ECBB=11
Bank 2: 8000h ~ FFFFh	01_8000h ~ 01_FFFFh	32k	Always	ECBB=10
Bank 1: 8000h ~ FFFFh	01_0000h ~ 01_7FFFh	32k	Always	ECBB=01
Bank 0: 8000h ~ FFFFh	00_8000h ~ 00_FFFFh	32k	Always	ECBB=00
Common Bank: 0000h ~ 7FFFh	00_0000h ~ 00_7FFFh	32k	Always	Always
Note: EC code can use the maximum 160k by banking. Note: All EC code memory space is mapped to both EC and host side at the same time. The EC size is not necessary on 32k boundary. Note: If BSO=1, ECBB is replaced with P1 register of 8032. ECBB means ECBB field in FECBSR register. BSO means BSO bit in FPCFG register.				

3.2 EC Mapped Memory Space

Figure 3-3. EC 8032 Data/Code Memory Map



See also Figure 9-14. Scratch SRAM in Data Space on page 172.

There is one internal Scratch SRAMs No 0, which are always mapped into data space and may be mapped into code space if their corresponding code space mapping registers are enabled. It means that Scratch SRAM may be mapped into data and code space at the same time and the firmware on Scratch ROM can access the same Scratch RAM. It is called Scratch RAM when being located at data space (default after reset) and called Scratch ROM when being located at code space.

The EC code space is 64k bytes and physically occupies the maximum 160 k bytes at the bottom of the flash space. Refer to Figure 3-1 on page 6 for the details.

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4. Pin Configuration

Figure 4-1. IT8733F 128-QFP

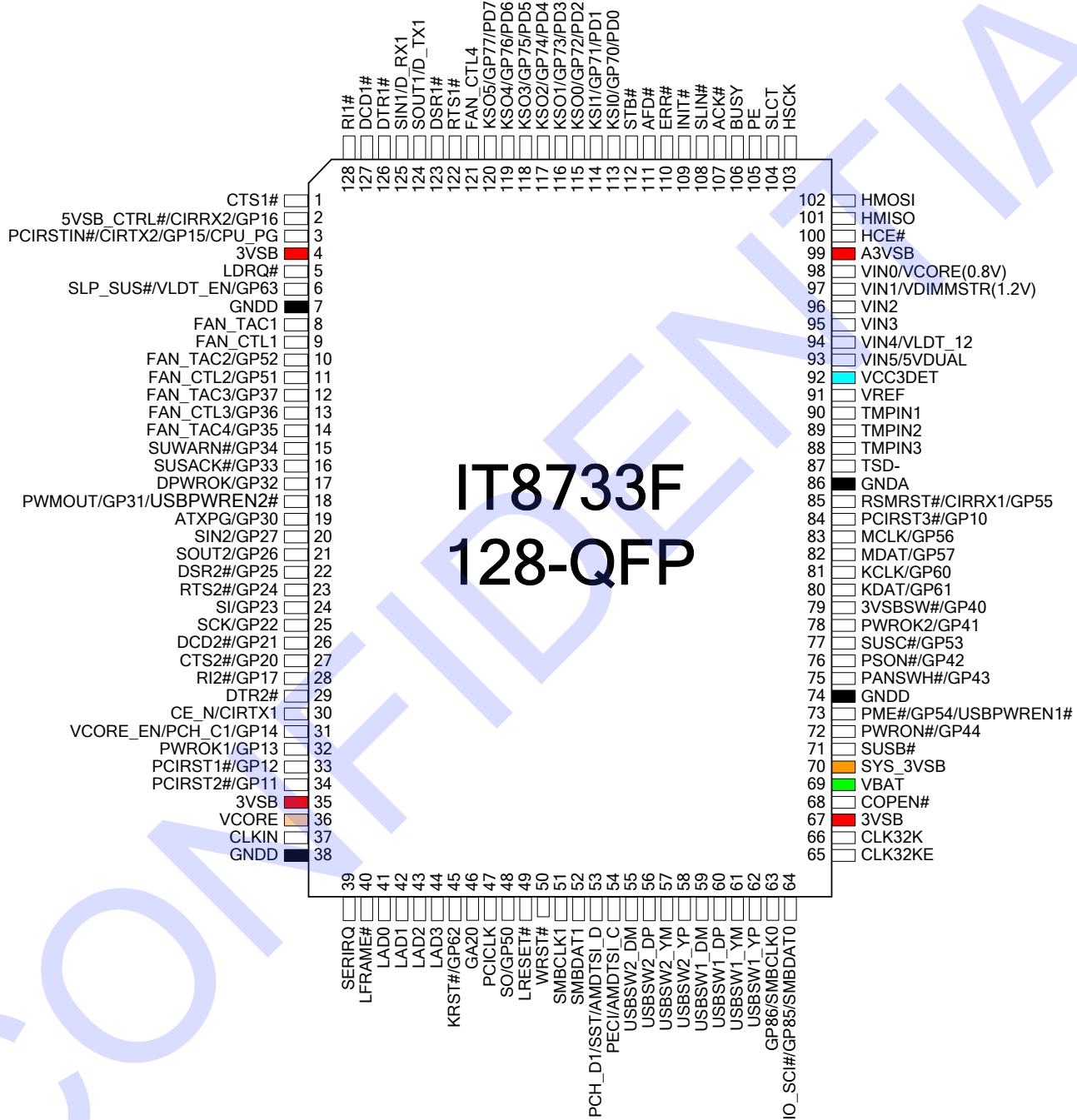


Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CTS1#	33	PCIRST1#/GP12	65	CLK32KE	97	VIN1
2	5VSB_CTRL#/CIRRX2/GP16	34	PCIRST2#/GP11	66	CLK32K	98	VIN0/VCORE(0.8V)
3	PCIRSTIN#/CIRTX2/GP15/CPU_PG	35	3VSB	67	3VSB	99	A3VSB
4	3VSB	36	VCORE	68	COPEN#	100	HCE#
5	LDRQ#	37	CLKIN	69	VBAT	101	HMISO
6	SLP_SUS#/VLDT_EN/GP63	38	GNDD	70	SYS_3VSB	102	HMOSI
7	GNDD	39	SERIRQ	71	SUSB#	103	HSCK
8	FAN_TAC1	40	LFRAME#	72	PWRON#/GP44	104	SLCT
9	FAN_CTL1	41	LAD0	73	PME#/GP54/USBPWREN1#	105	PE
10	FAN_TAC2/GP52	42	LAD1	74	GNDD	106	BUSY
11	FAN_CTL2/GP51	43	LAD2	75	PANSWH#/GP43	107	ACK#
12	FAN_TAC3/GP37	44	LAD3	76	PSON#/GP42	108	SLIN#
13	FAN_CTL3/GP36	45	KRST#/GP62	77	SUSC#/GP53	109	INIT#
14	FAN_TAC4/GP35	46	GA20	78	PWROK2/GP41	110	ERR#
15	SUSWARN#/GP34	47	PCICLK	79	3VSBSW#/GP40	111	AFD#
16	SUSACK#/GP33	48	SO/GP50	80	KDAT/GP61	112	STB#
17	DPWROK/GP32	49	LRESET#	81	KCLK/GP60	113	KSI0/GP70/PD0
18	PWMOUT/GP31/USBPWREN2#	50	WRST#	82	MDAT/GP57	114	KSI1/GP71/PD1
19	ATXPG/GP30	51	SMCLK1	83	MCLK/GP56	115	KSO0/GP72/PD2
20	SIN2/GP27	52	SMDAT1	84	PCIRST3#/GP10	116	KSO1/GP73/PD3
21	SOUT2/GP26	53	PCH_D1/SST/AMDTSI_D	85	RSMRST#/CIRRX1/GP55	117	KSO2/GP74/PD4
22	DSR2#/GP25	54	PECI/AMDTSI_C	86	GNDA	118	KSO3/GP75/PD5
23	RTS2#/GP24	55	USBSW2_DM	87	TSD-	119	KSO4/GP76/PD6
24	SI/GP23	56	USBSW2_DP	88	TMPIN3	120	KSO5/GP77/PD7
25	SCK/GP22	57	USBSW2_YM	89	TMPIN2	121	FAN_CTL4
26	DCD2#/GP21	58	USBSW2_YP	90	TMPIN1	122	RTS1#
27	CTS2#/GP20	59	USBSW1_DM	91	VREF	123	DSR1#
28	RI2#/GP17	60	USBSW1_DP	92	VCC3DET	124	SOUT1/D_TX1
29	DTR2#	61	USBSW1_YM	93	VIN5/5VDUAL	125	SIN1/D_RX1
30	CE_N_CIRTX1	62	USBSW1_YP	94	VIN4/VLDT_12	126	DTR1#
31	VCORE_EN/PCH_C1/GP14	63	GP86/SMCLK0	95	VIN3	127	DCD1#
32	PWROK1/GP13	64	IO_SCI#/GP85/SMDAT0	96	VIN2	128	RI1#

Figure 4-2. IT8733E 128-LQFP

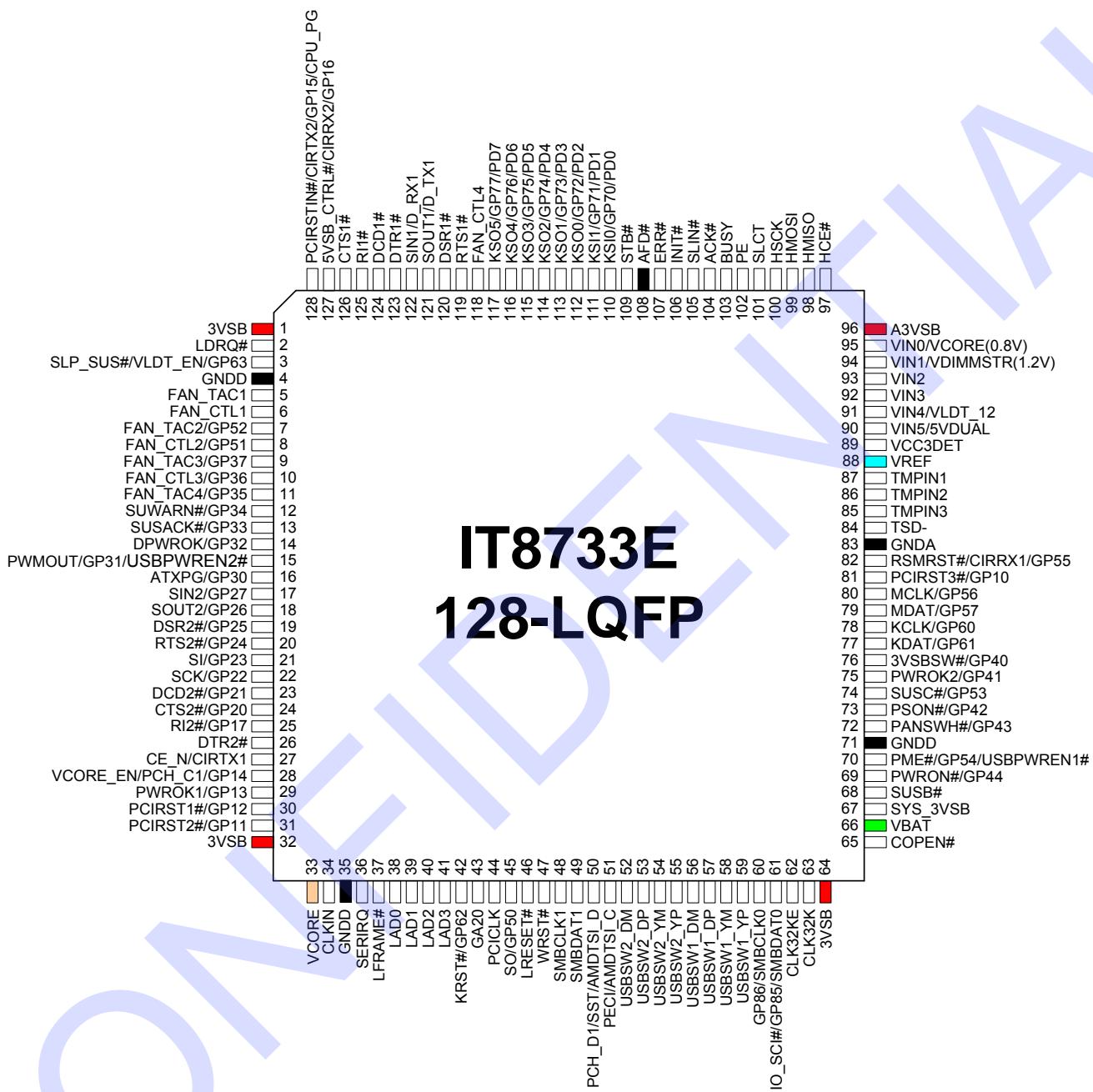


Table 4-2. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	3VSB	33	VCORE	65	COPEN#	97	HCE#
2	LDRQ#	34	CLKIN	66	VBAT	98	HMISO
3	SLP_SUS#/VLDT_EN/GP63	35	GNDD	67	SYS_3VSB	99	HMOSI
4	GNDD	36	SERIRQ	68	SUSB#	100	HSCK
5	FAN_TAC1	37	LFRAME#	69	PWRON#/GP44	101	SLCT
6	FAN_CTL1	38	LAD0	70	PME#/GP54/USBPWREN1#	102	PE
7	FAN_TAC2/GP52	39	LAD1	71	GNDD	103	BUSY
8	FAN_CTL2/GP51	40	LAD2	72	PANSWH#/GP43	104	ACK#
9	FAN_TAC3/GP37	41	LAD3	73	PSON#/GP42	105	SLIN#
10	FAN_CTL3/GP36	42	KRST#/GP62	74	SUSC#/GP53	106	INIT#
11	FAN_TAC4/GP35	43	GA20	75	PWROK2/GP41	107	ERR#
12	SUSWARN#/GP34	44	PCICLK	76	3VSBSW#/GP40	108	AFD#
13	SUSACK#/GP33	45	SO/GP50	77	KDAT/GP61	109	STB#
14	DPWROK/GP32	46	LRESET#	78	KCLK/GP60	110	KSI0/GP70/PD0
15	PWMOUT/GP31/USBPWREN2#	47	WRST#	79	MDAT/GP57	111	KSI1/GP71/PD1
16	ATXPG/GP30	48	SMCLK1	80	MCLK/GP56	112	KSO0/GP72/PD2
17	SIN2/GP27	49	SMDAT1	81	PCIRST3#/GP10	113	KSO1/GP73/PD3
18	SOUT2/GP26	50	PCH_D1/SST/AMDTSI_D	82	RSMRST#/CIRRX1/GP55	114	KSO2/GP74/PD4
19	DSR2#/GP25	51	PECI/AMDTSI_C	83	GNDA	115	KSO3/GP75/PD5
20	RTS2#/GP24	52	USBSW2_DM	84	TSD-	116	KSO4/GP76/PD6
21	SI/GP23	53	USBSW2_DP	85	TMPPIN3	117	KSO5/GP77/PD7
22	SCK/GP22	54	USBSW2_YM	86	TMPPIN2	118	FAN_CTL4
23	DDC2#/GP21	55	USBSW2_YP	87	TMPPIN1	119	RTS1#
24	CTS2#/GP20	56	USBSW1_DM	88	VREF	120	DSR1#
25	RI2#/GP17	57	USBSW1_DP	89	VCC3DET	121	SOUT1/D_TX1
26	DTR2#	58	USBSW1_YM	90	VIN5/5VDUAL	122	SIN1/D_RX1
27	CE_N/ CIRTX1	59	USBSW1_YP	91	VIN4/VLDT_12	123	DTR1#
28	VCORE_EN/PCH_C1/GP14	60	GP86/SMCLK0	92	VIN3	124	DCD1#
29	PWROK1/GP13	61	IO_SCI#/GP85/SMDAT0	93	VIN2	125	RI1#
30	PCIRST1#/GP12	62	CLK32KE	94	VIN1	126	CTS1#
31	PCIRST2#/GP11	63	CLK32K	95	VIN0/VCORE(0.8V)	127	5VSB_CTRL#/CIRRX2/GP16
32	3VSB	64	3VSB	96	A3VSB	128	PCIRSTIN#/CIRTX2/GP15/CPU_PG

5. Pin Description

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
4, 35, 67	1, 32, 64	3VSB	PWR	-	+3.3V Standby Power Supply
99	96	A3VSB	PWR	-	+3.3V Analog Power Supply
69	66	VBAT	PWR	-	+3V Battery Supply
36	33	VCORE	AO	-	Internal Power supply(1.8V) It is required to connect this pin with the external capacitance.
7, 38, 74	4, 35, 71	GNDD	GND	-	Digital Ground
86	83	GNDA	GND	-	Analog Ground

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
49	46	LRESET#	DI	VCC3	LPC RESET # EC block will not be reset by LRESET#, which is controlled by VCC3 PWROK.
50	47	WRST#	DI	3VSB	Warm Reset# For EC domain function, reset after power up.
39	36	SERIRQ	DIO16	VCC3	Serial IRQ
40	37	LFRA ME#	DI	VCC3	LPC Frame # This signal indicates the start of the LPC cycle.
41-44	38-41	LAD[0:3]	DIO16	VCC3	LPC Address / Data 0-3 4-bit LPC address/bi-directional data lines. LAD0 is LSB and LAD3 is MSB.
5	2	LDRQ#	DO8	VCC3	LPC DMA REQUEST# This is an encoded signal for DMA channel select.
47	44	PCICLK	DI	VCC3	PCI Clock 33 MHz PCI clock input for LPC I/F and SERIRQ.
73	70	PME#	DOD8	3VSB	Power Management Event # The function of this symbol is Power Management Event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state.
		GP54	DIOD8	3VSB	General Purpose I/O 54 The function of this symbol is General Purpose I/O Port 5 Bit 4.
		USBPW REN1#	DOD8	3VSB	USB Set 1 Power Control

Table 5-3. Pin Description of GPIO Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
48	45	SO	DI	3VSB	Serial Flash Data Output The function of this symbol is Serial Data Output from Serial Flash.
		GP50	DIOD8	3VSB	General Purpose I/O 50 The function of this symbol is General Purpose I/O Port 5 Bit 0.
28	25	RI2#	DI	3VSB	Ring Indicator 2 # The function of this symbol is Ring Indicator 2 #. When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP17	DIOD8	3VSB	General Purpose I/O 17 The function of this symbol is General Purpose I/O Port 1 Bit 7.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
29	26	DTR2#	DO8	VCC3	Data Terminal Ready 2 # The function of this symbol is Data Terminal Ready 2 #. DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.
27	24	CTS2#	DI	VCC3	Clear to Send 2 # The function of this symbol is Clear to Send 2 #. When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP20	DIOD8	3VSB	General Purpose I/O 20 The function of this symbol is General Purpose I/O Port 2 Bit 0.
26	23	DCD2#	DI	VCC3	Data Carrier Detect 2 # The function of this symbol is Data Carrier Detect 2 #. When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP21	DIOD8	3VSB	General Purpose I/O 21 The function of this symbol is General Purpose I/O Port 2 Bit 1.
25	22	SCK	DO8	3VSB	Serial Flash Clock The function of this symbol is Serial Clock for Serial Flash. Note: Place the SPI device as close to IT8733 as possible.
		GP22	DIOD8	3VSB	General Purpose I/O 22 The function of this symbol is General Purpose I/O Port 2 Bit 2.
24	21	SI	DO8	3VSB	Serial Flash in Data The function of this symbol is Serial in Data for Serial Flash.
		GP23	DIOD8	3VSB	General Purpose I/O 23 The function of this symbol is General Purpose I/O Port 2 Bit 3.
23	20	RTS2#	DO8	VCC3	Request to Send 2 # The function of this symbol is When this signal is low, the output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state.
		GP24	DIOD8	3VSB	General Purpose I/O 24 The function of this symbol is General Purpose I/O Port 2 Bit 4.
22	19	DSR2#	DI	VCC3	Data Set Ready 2 # The function of this symbol is Data Set Ready 2 #. When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP25	DIOD8	3VSB	General Purpose I/O 25 The function of this symbol is General Purpose I/O Port 2 Bit 5.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
21	18	SOUT2	DO8	VCC3	Serial Data Output 2 The function of this symbol is Serial Data Output 2. This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
		GP26	DIOD8	3VSB	General Purpose I/O 26 The function of this symbol is General Purpose I/O Port 2 Bit 6.
20	17	SIN2	DI	VCC3	Serial Data Input 2 The function of this symbol is SIN2. This input receives serial data from the communications link.
		GP27	DIOD8	3VSB	General Purpose I/O 27 The function of this symbol is General Purpose I/O Port 2 Bit 7.

Table 5-4. Pin Description of Hardware Monitor Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
98	95	VINO	AI	A3VSB	Voltage Analog Input 0 The function of this symbol is 0 to 2.8V FSR Analog Input.
		VCORE (0.8V)	AI	A3VSB	VCORE (0.8V) Analog Inputs The function of this symbol is VCORE (0.8V) Analog Input.
97	94	VIN1	AI	A3VSB	Voltage Analog Input 1 The function of this symbol is 0 to 2.8V FSR Analog Input.
		VDIMM_STR	AI	A3VSB	VDIMM DUAL STR (1.5V) Analog Input The function of this symbol is VDIMM DUAL STR (1.5V) Analog Input.
96	93	VIN2	AI	A3VSB	Voltage Analog Input 2 The function of this symbol is 0 to 2.8V FSR Analog Input.
95	92	VIN3	AI	A3VSB	Voltage Analog Input 3 The function of this symbol is 0 to 2.8V FSR Analog Inputs.
94	91	VIN4	AI	A3VSB	Voltage Analog Input 4 The function of this pin is 0 to 2.8V FSR Analog Input.
		VLDT_12	AI	A3VSB	VLDT (1.2V) Analog Inputs The function of this symbol is VLDT (1.2V) Analog Input.
93	90	VIN5	AI	A3VSB	Voltage Analog Input 5 The function of this symbol is 0 to 2.8V FSR Analog Input.
		5VDUAL	AI	A3VSB	System 5VDUAL Monitor The function of this symbol is analog input for system 5VDUAL Monitor. When the voltage drops below 0.7V, the 5VDUAL monitor circuit will assert SUSACK#. The function configuration of the pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 2> = 1b)
92	89	VCC3DET	AI	A3VSB	VCC3 Detect Pin The function of this symbol is VCC3 input
91	88	VREF	AO	A3VSB	Reference Voltage Output (2.8V) Regulated and referred voltage for external temperature sensors and negative voltage monitors.
88-90	85-87	TMPIN[1:3]	AI	A3VSB	External Thermal Inputs [1:3] These pins are connected to thermistors [1:3] or thermal temperature sensors.
87	84	TS_D-	AI	A3VSB	Thermal Diode Negative Input
8	5	FAN_TA_C1	DI	3VSB	Fan Tachometer Input 1 The function of this symbol is Fan Tachometer Input 1, 0 to +5V amplitude fan tachometer input.

IT8733 (For D Version)

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
10	7	FAN_TA_C2	DI	3VSB	Fan Tachometer Input 2 The function of this symbol is Fan Tachometer Input 2, 0 to +5V amplitude fan tachometer input.
		GP52	DIOD8	3VSB	General Purpose I/O 52 The function of this symbol is General Purpose I/O Port 5 Bit 2.
12	9	FAN_TA_C3	DI	3VSB	Fan Tachometer Input 3 The function of this symbol is Fan Tachometer Input 3, 0 to +5V amplitude fan tachometer input.
		GP37	DIOD8	3VSB	General Purpose I/O 37 The function of this symbol is General Purpose I/O Port 3 Bit 7.
19	16	ATXPG	DI	VCC3	ATX Power Good The function of this symbol is ATX Power Good. <u>PWROK1/2</u> will be (<u>VCC3 power-level-detect AND SUSB#</u> AND ATXPG) if bit 0 of Index 2Ch is 1, or (<u>VCC3 power-level-detect AND SUSB#</u>) if the bit is 0.
		GP30	DIOD8	3VSB	General Purpose I/O 30 The function of this symbol is General Purpose I/O Port 3 Bit 0.
18	15	PWMOUT	DOD8	3VSB	PWM Output The first function of the pin is PWMOUT. It is the PWM output and the frequency is 35.9K ~ 140Hz or 128 ~ 0.5 Hz.
		GP31	DIOD8	3VSB	General Purpose I/O 31 The function of this symbol is General Purpose I/O Port 3 Bit 1.
		USBPWR_EN2#	DOD8	3VSB	USB Set 2 Power Control
17	14	DPWROK	DOD8	3VSB	3VSB Power OK Output The function of this symbol is 3VSB Power OK Output. The function configuration of this pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 3> = 0b).
		GP32	DIOD8	3VSB	General Purpose I/O 32 The function of this symbol is General Purpose I/O Port 3 Bit 2.
16	13	SUSACK#	DOD8	3VSB	SUSACK# The function of this symbol is SUSACK# output. When 5VDUAL pin drops below 0.7V. SIO will issue SUSACK# to PCH. The function configuration of this pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 2> = 1b).
		GP33	DIOD8	3VSB	General Purpose I/O 33 The function of this symbol is General Purpose I/O Port 3 Bit 3.
15	12	SUSWARN#	DI	3VSB	SUSWARN# The function of this symbol is a signal from CPT PCH, When this signal is low, it indicates PCH is in the deep sleep state. The function configuration of this pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 2> = 1b).
		GP34	DIOD8	3VSB	General Purpose I/O 34 The function of this symbol is General Purpose I/O Port 3 Bit 4.
14	11	FAN_TA_C4	DI	3VSB	Fan Tachometer Input 4 The function of this symbol is Fan Tachometer Input 3, 0 to +5V amplitude fan tachometer input.
		GP35	DIOD8	3VSB	General Purpose I/O 35 The function of this symbol is General Purpose I/O Port 3 Bit 5.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
6	3	SLP_SU_S#	DI	3VSB	Deep Sleep Indication From CPT PCH, when asserted low, this signal indicates PCH is in the deep sleep state. The function configuration of this pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 2> = 1b).
		VLDT_E_N	DOD8	3VSB	VLDT Enable The function of this symbol is to enable VLDT voltage. The external pull high resistor is required.
		GP63	DIOD8	3VSB	General Purpose I/O 63 The function of this symbol is General Purpose I/O Port 6 Bit 3.
68	65	COPEN#	DIOD8	3VSB or VBAT	Case Open Detection # The Case Open Detection is connected to a specially designed low power CMOS flip-flop dual-powered by battery or 3VSB for case open state preservation during power loss.
2	127	5VSB_CTRL#_RL#	DOD8	3VSB	5VSB_CTRL# Power Control Signal Please refer to section 錯誤!找不到參照來源。錯誤!找不到參照來源。on page 錯誤!尚未定義書籤。for the detail.
		CIRRX2	DI	VCC3	Consumer Infrared Receive Input 2 The function of this symbol is Consumer Infrared Receive Input 2.
		GP16	DIOD8	3VSB	General Purpose I/O 16 The function of this symbol is General Purpose I/O Port 1 Bit 6.

Table 5-5. Pin Description of Fan Controller Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
9	6	FAN_CT_L1	DOD8	3VSB	Fan Control Output 1 The function of this symbol is Fan Control Output 1. (PWM output signal to Fan's FET.)
		FAN_CT_L2	DOD8	3VSB	Fan Control Output 2 The function of this symbol is Fan Control Output 2. (PWM output signal to Fan's FET.)
11	8	GP51	DIOD8	3VSB	General Purpose I/O 51 The function of this symbol is General Purpose I/O Port 5 Bit 1.
		FAN_CT_L3	DOD8	3VSB	Fan Control Output 3 The function of this symbol is Fan Control Output 3. (PWM output signal to Fan's FET.)
13	10	GP36	DIOD8	3VSB	General Purpose I/O 36 The function of this symbol is General Purpose I/O Port 3 Bit 6.
		FAN_CT_L4	DOD8	3VSB	Fan Control Output 4 The function of this symbol is Fan Control Output 4. (PWM output signal to Fan's FET.)
121	118				

Table 5-6. Pin Description of Infrared Port Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
30	27	CE_N	DO8	3VSB	Serial Flash Chip Enable The function of this symbol is Serial Flash Chip Enable.
		CIRTX1	DOD8	3VSB	Consumer Infrared Transmit Output 1 The function of this symbol is Consumer Infrared Transmit Output 1.
85	82	RSMRST #	DOD8	3VSB	Resume Reset # The function of this symbol is Resume Reset #. It is a power good signal of 3VSB.
		CIRRX1	DI	3VSB	Consumer Infrared Receive Input 1 The function of this symbol is Consumer Infrared Transmit Input 1.
		GP55	DIOD8	3VSB	General Purpose I/O 55 The function of this symbol is General Purpose I/O Port 5 Bit 5.
3	128	PCIRSTI N#	DI	3VSB	PCI Reset Input # The function of this symbol is PCI Reset Input #. (for PCIRST2# only)
		CIRTX2	DOD8	3VSB	Consumer Infrared Transmit Output 2 The function of this symbol is Consumer Infrared Transmit Output 2.
		GP15	DIOD8	3VSB	General Purpose I/O 15 The function of this symbol is General Purpose I/O Port 1 Bit 5.
		CPU_PG	DOD8	3VSB	CPU Power-good The function of this symbol is to indicate that CPU power-good is ready. The external pull-high resistor is required.
2	127	5VSB_CTRL# RL#	DOD8	3VSB	5VSB_CTRL# Power Control Signal Please refer to section 錯誤!找不到參照來源。錯誤!找不到參照來源。on page 錯誤!尚未定義書籤。for the detail.
		CIRRX2	DI	VCC3	Consumer Infrared Receive Input 2 The function of this symbol is Consumer Infrared Receive Input 2.
		GP16	DIOD8	3VSB	General Purpose I/O 16 The function of this symbol is General Purpose I/O Port 1 Bit 6.
70	67	SYS_3VS_B	AI	3VSB	System 3.3V Standby Power Detector The function of this symbol is System Standby Power Detector for RSMRST# output and EuP signal Control. Please refer to Figure 7-1. IT8733 EUP Applications Circuitry for Intel ICH on page43, section 錯誤!找不到參照來源。錯誤!找不到參照來源。on page 錯誤!尚未定義書籤。and section 12.15 DSW Timings for the detail.

Table 5-7. Pin Description of Serial Port 1 and 2 Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
128	125	RI1#	DI	3VSB	Ring Indicator 1 # When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
127	124	DCD1#	DI	VCC3	Data Carrier Detect 1 # When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
126	123	DTR1#	DO8	VCC3	Data Terminal Ready 1 # DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.
125	122	SIN1	DI	VCC3	Serial Data Input 1 The function of this symbol is SIN1. This input receives serial data from the communications link.
		D_RX1	DI	3VSB	Debug_RX1 The function of this symbol is D_RX1.
124	121	SOUT1	DO8	VCC3	Serial Data Output 1 This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
		D_TX1	DO8	3VSB	Debug_TX1 The function of this symbol is Debug_TX1.
123	120	DSR1#	DI	VCC3	Data Set Ready 1 # When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
122	119	RTS1#	DO8	VCC3	Request to Send 1 # When this signal is low, the output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state.
1	126	CTS1#	DI	VCC3	Clear to Send 1 # When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
28	25	RI2#	DI	3VSB	Ring Indicator 2 # When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP17	DIOD8	3VSB	General Purpose I/O 17 The function of this symbol is General Purpose I/O Port 1 Bit 7.
29	26	DTR2#	DO8	VCC3	Data Terminal Ready 2 # DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
27	24	CTS2#	DI	VCC3	Clear to Send 2 # When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP20	DIOD8	3VSB	General Purpose I/O 20 The function of this symbol is General Purpose I/O Port 2 Bit 0.
26	23	DCD2#	DI	VCC3	Data Carrier Detect 2 # When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP21	DIOD8	3VSB	General Purpose I/O 21 The function of this symbol is General Purpose I/O Port 2 Bit 1.
23	20	RTS2#	DO8	VCC3	Request to Send 2 # When this signal is low, the output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state.
		GP24	DIOD8	3VSB	General Purpose I/O 24 The function of this symbol is General Purpose I/O Port 2 Bit 4.
22	19	DSR2#	DI	VCC3	Data Set Ready 2 # When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
		GP25	DIOD8	3VSB	General Purpose I/O 25 The function of this symbol is General Purpose I/O Port 2 Bit 5.
21	18	SOUT2	DO8	VCC3	Serial Data Output 2 This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
		GP26	DIOD8	3VSB	General Purpose I/O 26 The function of this symbol is General Purpose I/O Port 2 Bit 6.
20	17	SIN2	DI	VCC3	Serial Data Input 2 The function of this symbol is SIN2. This input receives serial data from the communications link.
		GP27	DIOD8	3VSB	General Purpose I/O 27 The function of this symbol is General Purpose I/O Port 2 Bit 7.

Table 5-8. Pin Description of SPI Memory Slave Interface (HSPI)

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
SPI Memory Slave Interface (3.3V CMOS I/F)					
100	97	HCE#	DI	3VSB	HSPI Chip Enable Connected to the Southbridge.
101	98	HMISO	DO	3VSB	HSPI Master In/Slave Out Connected to the Southbridge.
102	99	HMOSI	DI	3VSB	HSPI Master Out/Slave In Connected to the Southbridge.
103	100	HSCK	DI	3VSB	HSPI Clock Clock from the Southbridge.

Table 5-9. Pin Description of Parallel Port Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
Printer Select					
104	101	SLCT	DI	VCC3	The function of this symbol is Printer Select. This signal goes high when the line printer has been selected.
105	102	PE	DI	VCC3	Printer Paper End The function of this symbol is Printer Paper End. This signal is set high by the printer when it runs out of paper.
106	103	BUSY	DI	VCC3	Printer Busy The function of this symbol is Printer Busy. This signal goes high when the line printer has a local operation in progress and cannot accept any data.
107	104	ACK#	DI	VCC3	Printer Acknowledge # The function of this symbol is Printer Acknowledge #. This signal goes low to indicate that the printer has already received a character and is ready to accept another one.
108	105	SLIN#	DIO24	VCC3	Printer Select Input # The function of this symbol is Printer Select Input #. When this signal is low, the printer is selected and it is derived from the complement of bit 3 of Control Port Register (Base Address 1 + 02h) (refer to page 138).
109	106	INIT#	DIO24	VCC3	Printer Initialize # The function of this symbol is Printer Initialize #. When this signal is low, the printer is selected and it is derived from the complement of bit 2 of Control Port Register (Base Address 1 + 02h) (refer to page 138).
110	107	ERR#	DI	VCC3	Printer Error # The function of this symbol is Printer Error #, which will be configured by programming the software configuration registers (LDN3 (parallel port) enabled). When this signal is low, it indicates that the printer has encountered an error and the error message can be read from bit 3 of Status Port Register (Base Address 1 + 01h) (refer to page 138).
111	108	AFD#	DIO24	VCC3	Printer Auto Line Feed # The function of this symbol is Printer Auto Line Feed #. When this signal is low, it is derived from the complement of bit 1 of Control Port Register (Base Address 1 + 02h) (refer to page 138) and is used to advance one line after each line is printed.
112	109	STB#	DI	VCC3	Printer Strobe # The function of this symbol is Printer Strobe. When this signal is low, it is the complement of bit 0 of Control Port Register (Base Address 1 + 02h) (refer to page 138) and is used to strobe the printing data into the printer.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
113	110	KSI0	DI	3VSB	Keyboard Scan Input 0 Keyboard matrix scan input 0 for switch-based keyboard.
		GP70	DIOD24	3VSB	General Purpose I/O 70 The function of this symbol is General Purpose I/O Port 7 Bit 0.
		PD0	DIO24	VCC3	Parallel Port Data 0 The function of these pins is Parallel Port Data 0. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
114	111	KSI1	DI	3VSB	Keyboard Scan Input 1 Keyboard matrix scan input 1 for switch-based keyboard.
		GP71	DIOD24	3VSB	General Purpose I/O 71 The function of this symbol is General Purpose I/O Port 7 Bit 1.
		PD1	DIO24	VCC3	Parallel Port Data 1 The function of these pins is Parallel Port Data 1. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
115	112	KSO0	DO24	3VSB	Keyboard Scan Output 0 Keyboard matrix scan output 0.
		GP72	DIOD24	3VSB	General Purpose I/O 72 The function of this symbol is General Purpose I/O Port 7 Bit 2.
		PD2	DIO24	VCC3	Parallel Port Data 2 The function of these pins is Parallel Port Data 2 This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
116	113	KSO1	DO24	3VSB	Keyboard Scan Output 1 Keyboard matrix scan output 1.
		GP73	DIOD24	3VSB	General Purpose I/O 73 The function of this symbol is General Purpose I/O Port 7 Bit 3.
		PD3	DIO24	VCC3	Parallel Port Data 3 The function of these pins is Parallel Port Data 3 This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
117	114	KSO2	DO24	3VSB	Keyboard Scan Output 2 Keyboard matrix scan output 2.
		GP74	DIOD24	3VSB	General Purpose I/O 74 The function of this symbol is General Purpose I/O Port 7 Bit 4.
		PD4	DIO24	VCC3	Parallel Port Data 4 The function of these pins is Parallel Port Data 4 This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
118	115	KSO3	DO24	3VSB	Keyboard Scan Output 3 Keyboard matrix scan output 3.
		GP75	DIOD24	3VSB	General Purpose I/O 75 The function of this symbol is General Purpose I/O Port 7 Bit 5.
		PD5	DIO24	VCC3	Parallel Port Data 5 The function of these pins is Parallel Port Data 5 This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
119	116	KSO4	DO24	3VSB	Keyboard Scan Output 4 Keyboard matrix scan output 4.
		GP76	DIOD24	3VSB	General Purpose I/O 76 The function of this symbol is General Purpose I/O Port 7 Bit 6.
		PD6	DIO24	VCC3	Parallel Port Data 6 The function of these pins is Parallel Port Data 6 This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
120	117	KSO5	DO24	3VSB	Keyboard Scan Output 5 Keyboard matrix scan output 5.
		GP77	DIOD24	3VSB	General Purpose I/O 77 The function of this symbol is General Purpose I/O Port 7 Bit 7
		PD7	DIO24	VCC3	Parallel Port Data 7 The function of these pins is Parallel Port Data 7 This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.

Table 5-10. Pin Description of SMBus/PECI Controller Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
51	48	SMCLK1	DIO24	3VSB	SMBUS 1 Clock The function of this symbol is SMCLK1.
52	49	SMDAT1	DIO24	3VSB	SMBUS 1 Data The function of this symbol is SMDAT1.
53	50	SST	SST	VCC3	SST The function of this symbol is SST. Specifically when External Thermal Sensor Host (SST、PECI、AMDTSI、PCH SM-Link) is enabled (bit 6-4 of EC Index 0Ah), The function of this symbol is selected as SST or ETS DAT.
		AMDTSI_D	DIOD24	VCC3	AMDTSI I/F Data Pin The secondnd function of this pin is AMDTSI I/F Data.
		PCH_D	DIOD24	VCC3	PCH SM-Link Data Pin The function of this symbol is PCH SM-Link Data.
54	51	PECI	PECI	VCC3	PECI The function of this symbol is PECl. Specifically when External Thermal Sensor Host (SST、PECI、AMDTSI、PCH SM-Link) is enabled (bit 6-4 of EC Index 0Ah), this pin is selected as PECl or ETS_CLK.
		AMDTSI_C	DIOD24	VCC3	AMDTSI I/F Clock Pin The secondnd function of this pin is AMDTSI I/F Clock.
63	60	GP86	DIOD24	3VSB	General Purpose I/O 86 The function of this symbol is General Purpose I/O Port 8 Bit 6.
		SMCLK0	DIO24	3VSB	SMBUS 0 Clock The function of this symbol is SMCLK0.
64	61	IO_SCI#	DO24	3VSB	IO_SCI# The first function of the pin is SCI# Output.
		GP85	DIOD24	3VSB	General Purpose I/O 85 The function of this symbol is General Purpose I/O Port 8 Bit 5.
		SMDAT0	DIO24	3VSB	SMBUS 0 Data The function of this symbol is SMDAT0.

Table 5-11. Pin Description of GPIO Function

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
31	28	PCH_C1	DIOD8	VCC3	PCH SM-Link Set 1 Clock Pin The function of this symbol is PCH SM-Link Clock.
		VCORE_EN	DOD8	VCC3	VCORE Enable The function of this symbol is VCORE Enable, which is to enable the PWM controller for CPU core voltage. The external pull-high resistor is required. The function configuration of this pin is determined by the power-on strapping option (JP4).
		GP14	DIOD8	3VSB	General Purpose I/O 14 The function of this symbol is General Purpose I/O Port 1 Bit 4.
32	29	PWROK_1	DOD8	VCC3	Power OK 1 of VCC3 The function of this symbol is Power OK 1 of VCC3.
		GP13	DIOD8	3VSB	General Purpose I/O 13 The function of this symbol is General Purpose I/O Port 1 Bit 3.
33	30	PCIRST1 #	DO8	VCC3	PCI Reset 1 # The function of this symbol is PCI Reset 1 #, which is a buffer of LRESET#.
		GP12	DIOD8	3VSB	General Purpose I/O 12 The function of this symbol is General Purpose I/O Port 1 Bit 2.
34	31	PCIRST2 #	DO8	VCC3	PCI Reset 2 # The function of this symbol is PCI Reset 2 #, which is a buffer of LRESET# / PCIRSTIN#.
		GP11	DIOD8	3VSB	General Purpose I/O 11 The function of this symbol is General Purpose I/O Port 1 Bit 1.
84	81	PCIRST3 #	DO8	VCC3	PCI Reset 3 # The function of this symbol is PCI Reset 3 #, which is a buffer of LRESET#.
		GP10	DIOD8	3VSB	General Purpose I/O 10 The function of this symbol is General Purpose I/O Port 1 Bit 0.
63	60	GP86	DIOD24	3VSB	General Purpose I/O 86 The fist function of this pin is General Purpose I/O Port 8 Bit 6.
		SMCLK0	DIO24	3VSB	SMBUS 0 Clock The function of this symbol is SMCLK0.
64	61	IO_SCI#	DO24	3VSB	IO_SCI# The first function of the pin is SCI# output.
		GP85	DIOD24	3VSB	General Purpose I/O 85 The function of this symbol is General Purpose I/O Port 8 Bit 5.
		SMDAT0	DIO24	3VSB	SMBUS 0 Data The function of this symbol is SMDAT0..

Table 5-12. Pin Description of Keyboard Controller Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
80	77	KDAT	DIOD24	3VSB	Keyboard Data The function of this symbol is Keyboard Data.
		GP61	DIOD24	3VSB	General Purpose I/O 61 The function of this symbol is General Purpose I/O Port 6 Bit 1. This set only supports Simple I/O function. This pin doesn't support internal pull-up.
81	78	KCLK	DIOD24	3VSB	Keyboard Clock The function of this symbol is Keyboard Clock.
		GP60	DIOD24	3VSB	General Purpose I/O 60 The function of this symbol is General Purpose I/O Port 6 Bit 0. This set only supports Simple I/O function. This pin doesn't support internal pull-up.
82	79	MDAT	DIOD24	3VSB	PS/2 Mouse Data The function of this symbol is PS/2 Mouse Data.
		GP57	DIOD24	3VSB	General Purpose I/O 57 The function of this symbol is General Purpose I/O Port 5 Bit 7. This pin doesn't support internal pull-up.
83	80	MCLK	DIOD24	3VSB	PS/2 Mouse Clock The function of this symbol is PS/2 Mouse Clock.
		GP56	DIOD24	3VSB	General Purpose I/O 56 The function of this symbol is General Purpose I/O Port 5 Bit 6. This pin doesn't support internal pull-up.
45	42	KRST#	DO8	VCC3	Keyboard Reset # The function of this symbol is Keyboard Reset #.
		GP62	DIOD8	3VSB	General Purpose I/O 62 The function of this symbol is General Purpose I/O Port 6 Bit 2. This set only supports Simple I/O function.
46	43	GA20	DO8	VCC3	Gate Address 20 GA20 Signal

Table 5-13. Pin Description of Miscellaneous Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
37	34	CLKIN	DI	VCC3	24 or 48 MHz Clock Input
72	69	PWRON #	DOD8	3VSB	Power On Request Output # The function of this symbol is Power On Request Output #. When the Internal 3VSB-OK is ready, the Hi/Lo status of PWRON# will be detected. RSMRST# output is detected by 3VSB
		GP44	DIOD8	3VSB	General Purpose I/O44 The function of this symbol is General Purpose I/O Port 4 Bit 4.
75	72	PANSW H#	DI	3VSB	Main Power Switch Button Input # The function of this symbol is Main Power Switch Button Input #.
		GP43	DIOD8	3VSB	General Purpose I/O 43 The function of this symbol is General Purpose I/O Port 4 Bit 3.
76	73	PSON#	DOD8	3VSB	Power Supply On-Off Output # The function of this symbol is Power Supply On-Off Control Output #.
		GP42	DIOD8	3VSB	General Purpose I/O 42 The function of this symbol is General Purpose I/O Port 4 Bit 2.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
71	68	SUSB#	DI	3VSB	SUSB # Input The function of this symbol is SUSB# Input.
77	74	SUSC#	DI	3VSB	SUSC# Input The function of this symbol is SUSC# Input.
		GP53	DIOD8	3VSB	General Purpose I/O 53 The function of this symbol is General Purpose I/O Port 5 Bit 3.
78	75	PWROK 2	DOD8	VCC3	Power OK 2 of VCC3 The function of this symbol is Power OK 2 of VCC3.
		GP41	DIOD8	3VSB	General Purpose I/O 41 The function of this symbol is General Purpose I/O Port 4 Bit 1.
79	76	3VSBSW #	DO8	3VSB	3VSBSW# The function of this symbol is 3VSBSW#.
		GP40	DIOD8	3VSB	General Purpose I/O 40 The function of this symbol is General Purpose I/O Port 4 Bit 0.
65	62	CLK32K E	OSCIO	3VSB	32.768 kHz Crystal X2 It is connected to the internal crystal oscillator.
66	63	CLK32K	OSCI	3VSB	32.768 kHz Crystal X1 It is connected to the internal crystal oscillator.

Table 5-14. DSW (Deep Sleep Well) Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
6	3	SLP_SU S#	DI	3VSB	Deep Sleep Indication From CPT PCH, when asserted low, this signal indicates PCH is in the deep sleep state. The function configuration of this pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 2> = 1b).
		VLDT_E N	DOD8	3VSB	VLDT Enable The function of this symbol is to enable VLDT Voltage. The external pull high resistor is required.
		GP63	DIOD8	3VSB	General Purpose I/O 63 The function of this symbol is General Purpose I/O Port 6 Bit 3.
17	14	DPWRO K	DOD8	3VSB	3VSB Power OK Output The function of this symbol is 3VSB Power OK Output. The function configuration of this pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 3> = 0b).
		GP32	DIOD8	3VSB	General Purpose I/O 32 The function of this symbol is General Purpose I/O Port 3 bit 2.
16	13	SUSACK #	DOD8	3VSB	SUSACK# The function of this symbol is SUSACK# output. When 5VDUAL pin drops below 0.7V. SIO will issue SUSACK# to PCH. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
		GP33	DIOD8	3VSB	General Purpose I/O 33 The function of this symbol is General Purpose I/O Port 3 bit 3.

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
15	12	SUS_WA_RN#	DI	3VSB	SUSWARN# The function of this symbol is a signal from CPT PCH. When this signal is low, it indicates PCH is in the deep sleep state. The function configuration of this pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 2> = 1b).
		GP34	DIOD8	3VSB	General Purpose I/O 34 The function of this symbol is General Purpose I/O Port 3 Bit 4.
93	90	VIN5	AI	A3VSB	Voltage Analog Input 5 The function of this symbol is 0 to 2.8V FSR Analog Input.
		5VDUAL	AI	A3VSB	System 5VDUAL Monitor The function of this symbol is Analog Input for System 5VDUAL Monitor. When the voltage drops below 0.7V, the 5VDUAL monitor circuit will assert SUSACK#. The function configuration of the pin is determined by the power-on strapping option (LDN7/Index 2Dh<bit 2> = 1b)

Table 5-15. USB Signals

Pin(s) No.		Symbol	Attribute	Power	Description
QFP	LQFP				
55	52	USBSW2_DM	DIO16	VCC3	Connect to PCH USB HOST Set2 D+ Please refer to Section 10.10 USB Host Controller for the detail.
56	53	USBSW2_DP	DIO16	VCC3	Connect to PCH USB HOST Set2 D- Please refer to Section 10.10 USB Host Controller for the detail.
57	54	USBSW2_YM	DIO16	3VSB	Connect to USB Device Set2 D+ Please refer to Section 10.10 USB Host Controller for the detail.
58	55	USBSW2_YP	DIO16	3VSB	Connect to USB Device Set2 D- Please refer to Section 10.10 USB Host Controller for the detail.
59	56	USBSW1_DM	DIO16	VCC3	Connect to PCH USB HOST Set1 D+ Please refer to Section 10.10 USB Host Controller for the detail.
60	57	USBSW1_DP	DIO16	VCC3	Connect to PCH USB HOST Set1 D- Please refer to Section 10.10 USB Host Controller for the detail.
61	58	USBSW1_YM	DIO16	3VSB	Connect to USB Device Set1 D+ Please refer to Section 10.10 USB Host Controller for the detail.
62	59	USBSW1_YP	DIO16	3VSB	Connect to USB Device Set1 D- Please refer to Section 10.10 USB Host Controller for the detail.
73	70	PME#	DOD8	3VSB	Power Management Event # The function of this symbol is Power Management Event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state.
		GP54	DIOD8	3VSB	General Purpose I/O 54 The function of this symbol is General Purpose I/O Port 5 Bit 4.
		USBPW_REN1#	DOD8	3VSB	USB Set 1 Power Control

Table 5-16. Pad Power Of GPIO

GP I/O Group 1	GPIO10	GPIO11	GPIO12	GPIO13	GPIO14	GPIO15	GPIO16	GPIO17
Pad power	✓	-	-	-	-	-	-	-
GP I/O Group 2	GPIO20	GPIO21	GPIO22	GPIO23	GPIO24	GPIO25	GPIO26	GPIO27
Pad power	✓	✓	✓	✓	✓	✓	✓	✓
GP I/O Group 3	GPIO30	GPIO31	GPIO32	GPIO33	GPIO34	GPIO35	GPIO36	GPIO37
Pad power	-	-	-	-	-	-	-	-
GP I/O Group 4	GPIO40	GPIO41	GPIO42	GPIO43	GPIO44	GPIO45	GPIO46	GPIO47
Pad power	✓	✓	✓	✓	✓	✗	✗	✗
GP I/O Group 5	GPIO50	GPIO51	GPIO52	GPIO53	GPIO54	GPIO55	GPIO56	GPIO57
Pad power	-	-	-	✓	✓	✓	-	-
GP I/O Group 6	GPIO60	GPIO61	GPIO62	GPIO63	GPIO64	GPIO65	GPIO66	GPIO67
Pad power	-	-	-	-	✗	✗	✗	✗
GP I/O Group 7	GPIO70	GPIO71	GPIO72	GPIO73	GPIO74	GPIO75	GPIO76	GPIO77
Pad power	✓	✓	✓	✓	✓	✓	✓	✓
GP I/O Group 8	GPIO80	GPIO81	GPIO82	GPIO83	GPIO84	GPIO85	GPIO86	GPIO87
Pad power	✗	✗	✗	✗	✗	✓	✓	✗

✓ : Powered by 3VSB

- : Power determined by the register 2012h[bit 5]. 2012h[bit 5] = 1 is powered by 3VSB while 2012h[bit 5] = 0 is powered by VCC3.

✗ : Not supported

Note 1: SPI pins (**SCK, SI, SO, CE_N**) should be pulled high if these pins are not connected to the flash device.

Note 2: These GPIO pins are kept by VCC in default but can be changed to be kept by 3VSB if EC side writes 1 to 2012h[bit 5].

Note 3: KSO2, KSO3 should be pulled high to 3VSB to avoid accessing to the DBGR mode.

IO Cell:

DO8: 8mA Digital Output buffer

DOD8: 8mA Digital Open-Drain Output buffer

DO16: 16mA Digital Output buffer

DO24: 24mA Digital Output buffer

DO24L: 24mA sink/8mA drive Digital Output buffer

DIO8: 8mA Digital Input/Output buffer

DIOD8: 8mA Digital Open-Drain Input/Output buffer

DIO16: 16mA Digital Input/Output buffer

DIOD16: 16mA Digital Open-Drain Input/Output buffer

DIO24: 24mA Digital Input/Output buffer

DIOD24: 24mA Digital Open-Drain Input/Output buffer

DI: Digital Input

AI: Analog Input

AO: Analog Output

SST: Special design for SST interface

PECI: Special design for PECL interface

IO_SW: Special type of Input/Output; pins of this type connected in pairs through a switch

5.1 Chip Power Planes and Power States

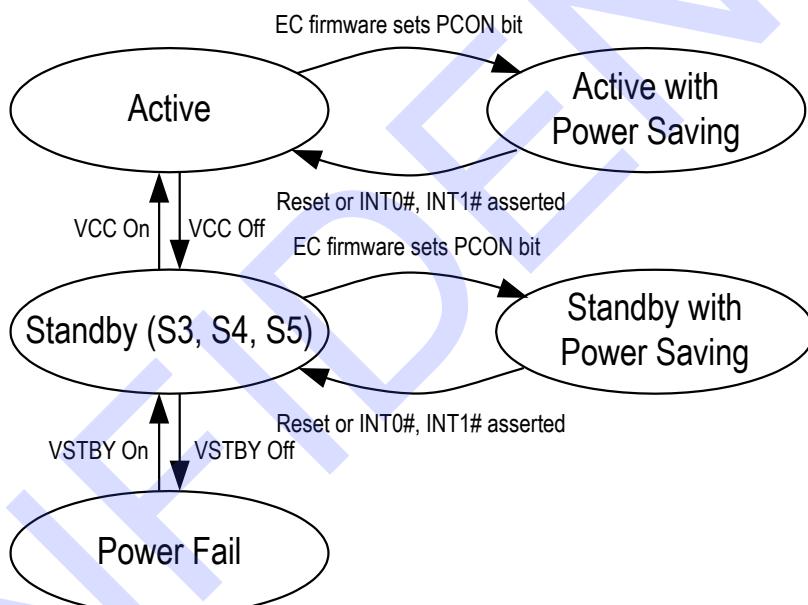
Table 5-17. Power States

Power State	VCC pin	VSTBY/AVSTBY pin
Active	Supplied	Supplied
Active with Power Saving	Supplied	Supplied EC is in Idle, Doze or Sleep Mode
Standby	Not Supplied	Supplied
Standby with Power Saving	Not Supplied	Supplied EC is in Idle, Doze or Sleep Mode
Power Fail	Not Supplied	Not Supplied

Note:

- (1) The AVSTBY should be derived from VSTBY.
- (2) All other combinations of VCC / VSTBY are invalid.
- (3) In Power Saving mode, 8032 program counter is stopped and no instruction will be executed no matter whether EC Clock is running or not.

Figure 5-1. Power State Transitions



5.2 Reset Sources and Types

Table 5-18. Reset Sources

Reset Sources	Description
VSTBY Power-Up Reset	Activated after VSTBY is power up and DPLL is stable It takes t_{PLLS} for PLL stablizing, and the external flash has to be ready before VSTBY Power-Up Reset finish
VCC Power-Up Reset	Activated after VCC is power up
Warm Reset	Activated if WRST# is asserted
LPC Hardware Reset	Activated if LPCRST# is asserted
Watch Dog Reset	Activated if 8032 WDT or External WDT time-out

Table 5-19. Reset Types and Applied Module

Reset Types	Sources	Applied Module
Host Domain Hardware Reset	Warm Reset, VCC Power-Up Reset or LPC Hardware Reset	LPC, PNPCFG, and Logical Devices.
EC Domain Reset	Warm Reset, VSTBY Power-Up Reset or Watch Dog Reset	EC Domain

The WRST# should be driven low for at least t_{WRSTW} before going high (Refer to section 12.3 WARMRESET Timings on page 357).

If the firmware wants to assert an EC Domain Reset, start an internal or external watchdog without clearing its counter or write invalid data to EWDKEYR register (refer to EWDKEYEN and EWDKEYR registers).

If the firmware wants to determine the source of the last EC Domain Reset, use LRS field in RSTS register.

5.3 Chip Power Mode

The 8032 can enter Idle/Doze/Sleep mode to reduce some power consumption. After entering the Idle mode, timers and the Watch Dog timer of 8032 still work. After entering Doze/Sleep mode, clock of 8032 is stopped and internal timers are stopped but the external timer still works. After entering Doze mode, EC domain clock is stopped and all internal timers are stopped. Also see Table 5-21 on page 34 for the details.

The way to wake up 8032 from the Idle mode is to enable internal or external interrupts, or hardware reset. The way to wake up 8032 from Doze/Sleep mode is to enable external interrupts or hardware reset. Firmware may set PLLCTRL bit before setting PD bit to enter the Sleep mode, since stopping PLL can reduce more power consumption, but it takes more time to wake up from Sleep mode due to waiting for PLL being stable. The steps to enter and exit Idle/Doze/Sleep are listed below:

- (a) Set related bits of IE register if they are cleared.
- (b) Set channels of WUC which wants to wake up 8032 and disable unwanted channels.
- (c) Set channels of INTC which wants to wake up 8032 and disable unwanted channels.
- (d) Set PLLCTRL bit for Sleep mode, or clear it for Doze mode.
- (e) Set IDL bit in PCON to enter the Idle mode, or set PD bit in PCON to enter the Doze/Sleep mode.
- (f) 8032 waits for an interrupt to wake up.
- (g) After an interrupt is asserted, 8032 executes the corresponding interrupt routine and return the next instruction after setting PCON.

Table 5-20. Power Saving by EC Clock Operation Mode

Mode	Item	Description
Normal	Enter	VSTBY is supplied and hardware reset done
	Exit	Enter other modes
	DPLL	On
	EC Domain Clock	Driven by PLL
	8032 Clock	The same as EC Domain Clock
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Idle	Enter	Set IDL bit in PCON of 8032
	Exit	Interrupt from INTC, interrupt from 8032 timer, watchdog reset or hardware reset
	DPLL	On
	EC Domain Clock	Driven by PLL
	8032 Clock	Core: Off Internal timer/WDT: On
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Doze	Enter	Set PD bit in PCON of 8032
	Exit	Interrupt from INTC or hardware reset
	DPLL	On, clearing PLLCTRL of ECPM module is required
	EC Domain Clock	Driven by PLL
	8032 Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Sleep	Enter	Set PD bit in PCON of 8032
	Exit	Interrupt from INTC or hardware reset
	DPLL	D2EC disabled: Off, setting PLLCTRL of ECPM module is required D2EC enabled: On
	EC Domain Clock	Driven by PLL
	8032 Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)

Note: The PD bit in PCON register may trigger the Doze or Sleep mode of EC Domain.

Table 5-21. Module Status in Each Power State/Clock Operation

Power State and/or Clock Operation	Running Module	Stopped Module	Off Module	Note
Active Active with Power Saving	LPC, PNPCFG, and all host parts			List host related modules only
Standby Standby with Power Saving			LPC, PNPCFG, and host parts	List host related modules only
Active with Idle Mode Standby with Idle Mode	All other EC modules 8032 internal timer/WDT	8032 core logic except its internal timer/WDT		List EC modules only
Active with Doze Mode Standby with Doze Mode	All other EC modules	8032		List EC modules only
Active with Sleep Mode Standby with Sleep Mode	GPIO, WUC and its sources, INTC and its sources from running modules, ETWD, BRAM	All other EC modules		List all

Note: Running module means this module works well.

Stopped module means this module is frozen because its clock is stopped.

Off module means this module is turned off due to power lost.

6. List of GPIO Pins

Table 6-1. GPIO Alternate Function

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
GPIO 1x	0	PCIRST3# (D08)		GP10 (DIOD8)	25h<0>=1					8mA	Internal Pull Up Default: Disable
	1	PCIRST2# (D08)		GP11 (DIOD8)	25h<1>=1					8mA	Internal Pull Up Default: Disable
	2	PCIRST1# (D08)		GP12 (DIOD8)	25h<2>=1					8mA	Internal Pull Up Default: Disable
	3	PWROK1 (DOD8)		GP13 (DIOD8)	25h<3>=1					8mA	Internal Pull Up Default: Disable
	4	VCORE_EN (DOD8)		GP14 (DIOD8)	25h<4>=1	PCH_C1 (DIOD8)	2Ah<2>=1			8mA	Internal Pull Up Default: Disable
	5	PCIRSTIN# (DI)	2Ch<2>=1	CIRTX2 (DOD8)	CIR IER<7>=1	GP15 (DIOD8)	25h<5>=1	CPU_PG (DOD8)		8mA	Internal Pull Up Default: Enable

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
GPIO 2x	6	5VSB_CTRL# (DOD8)		CIRRX2 (DI)	CIR IER<6>=1	GP16 (DIOD8)	25h<6>=1			8mA	Internal Pull Up Default: Disable
	7	RI2# (DI)		GP17 (DIOD8)	25h<7>=1					8mA	Internal Pull Up Default: Disable
	0	GP20 (DIOD8)	26h<0>=1	CTS2# (DI)	26h<0>=0					8mA	Internal Pull Up Default: Disable
	1	GP21 (DIOD8)	26h<1>=1	DCD2# (DI)	26h<1>=0					8mA	Internal Pull Up Default: Disable
	2	SCK (DO8)	2Ch<3> = 1	GP22 (DIOD8)	26h<2>=1					8mA	Internal Pull Up Default: Disable
	3	SI (DO8)	2Ch<3> = 1	GP23 (DIOD8)	26h<3>=1					8mA	Internal Pull Up Default: Disable
	4	GP24 (DIOD8)	26h<4>=1	RTS2# (DO8)	26h<4>=0					8mA	Internal Pull Up Default: Disable

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
GPIO 3x	5	GP25 (DIOD8)	26h<5>=1	DSR2# (DI)	26h<5>=0					8mA	Internal Pull Up Default: Disable
	6	GP26 (DIOD8)	26h<6>=1	SOUT2# (DO8)	26h<6>=0					8mA	Internal Pull Up Default: Disable
	7	GP27 (DIOD8)	26h<7>=1	SIN2# (DI)	26h<7>=0					8mA	Internal Pull Up Default: Disable
GPIO 3x	0	ATXPG (DI)	27h<0>=0 2Bh<6>=0	GP30 (DIOD8)	27h<0>=1					8mA	Internal Pull Up Default: Disable
	1	PWM_OUT (DOD8)		GP31 (DIOD8)	27h<1>=1	USBPWREN 2# (DOD8)				8mA	Internal Pull Up Default: Disable
	2	DPWROK (DOD8)		GP32 (DIOD8)	27h<2>=1					8mA	Internal Pull Up Default: Disable
	3	SUSACK# (DOD8)		GP33 (DIOD8)	27h<3>=1					8mA	Internal Pull Up Default: Disable

IT8733 (For D Version)

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
GPIO 4x	4	SUSWARN# (DOD8)		GP34 (DIOD8)	27h<4>=1					8mA	Internal Pull Up Default: Disable
	5	FAN_TAC4 (DI)		GP35 (DIOD8)	27h<5>=1					8mA	Internal Pull Up Default: Disable
	6	FAN_CTL3 (DOD8)		GP36 (DIOD8)	27h<6>=1					8mA	Internal Pull Up Default: Disable
	7	FAN_TAC3 (DI)		GP37 (DIOD8)	27h<7>=1					8mA	Internal Pull Up Default: Disable
GPIO 4x	0	3VSBSW# (D08)	2Ah<7>=1	GP40 (DIOD8)	28h<0>=1					8mA	Internal Pull Up Default: Disable
	1	PWROK2 (DOD8)		GP41 (DIOD8)	28h<1>=1						Internal Pull Up Default: Disable
	2	PSON# (DOD8)		GP42 (DIOD8)	28h<2>=1					8mA	Internal Pull Up Default: Disable

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
GPIO 5x	3	PANSH# (DI)		GP43 (DIOD8)	28h<3>=1					8mA	Internal Pull Up Default: Disable
	4	PWRON# (DOD8)		GP44 (DIOD8)	28h<4>=1					8mA	Internal Pull Up Default: Disable
	0	SO (DI)	2Ch<3>=1	GP50 (DIOD8)	29h<0>=1					8mA	Internal Pull Up Default: Disable
	1	FAN_CTL2 (DOD8)		GP51 (DIOD8)	29h<1>=1					8mA	Internal Pull Up Default: Disable
	2	FAN_TAC2 (DI)		GP52 (DIOD8)	29h<2>=1					8mA	Internal Pull Up Default: Disable
	3	SUSC# (DI)		GP53 (DIOD8)	29h<3>=1					8mA	Internal Pull Up Default: Disable

IT8733 (For D Version)

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
GPIO 6x	4	PME# (DOD8)		GP54 (DIOD8)	29h<4>=1	USBPWREN 1# (DOD8)				8mA	Internal Pull Up Default: Disable
	5	RSMRST# (DOD8)		CIRRX1 (DI)	29h<5>=0	GP55 (DIOD8)	29h<5>=1			8mA	Internal Pull Up Default: Disable
	6	MCLK (DIOD24)		GP56 (DIOD24)	29h<6>=1					24mA	Internal Pull Up Default: Disable
	7	MDAT (DIOD24)		GP57 (DIOD24)	29h<6>=1					24mA	Internal Pull Up Default: Disable
GPIO 6x	0	KCLK (DIOD24)		GP60 (DIOD24)	29h<6>=1					24mA	Internal Pull Up Default: Disable
	1	KDAT (DIOD24)		GP61 (DIOD24)	29h<6>=1					24mA	Internal Pull Up Default: Disable
	2	KRST# (DO8)		GP62 (DIOD16)	29h<6>=1					16mA	Internal Pull Up Default: Disable

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
GPIO 7x	3	SLP_SUS# (DI)		VLDT_EN (DOD8)		GP63 (DIOD8)	29h<7>=1			8mA	Internal Pull Up Default: Disable
	0	GP70 (DIOD24)		KSI0 (DI)		PD0 (DIO24)				8mA	No Internal Pull Up Simple I/O Only
	1	GP71 (DIOD24)		KSI1 (DI)		PD1 (DIO24)				8mA	No Internal Pull Up Simple I/O Only
	2	GP72 (DIOD24)		KSO0 (DO8)		PD2 (DIO24)				8mA	No Internal Pull Up Simple I/O Only
	3	GP73 (DIOD24)		KSO1 (DO8)		PD3 (DIO24)				8mA	No Internal Pull Up Simple I/O Only
	4	GP74 (DIOD24)		KSO2 (DO8)		PD4 (DIO24)				8mA	No Internal Pull Up Simple I/O Only
	5	GP75 (DIOD24)		KSO3 (DO8)		PD5 (DIO24)				8mA	No Internal Pull Up Simple I/O Only
	6	GP76 (DIOD24)		KSO4 (DO8)		PD6 (DIO24)				8mA	No Internal Pull Up Simple I/O Only

Group	Bit	1 st Func	Condition	2 nd Func	Condition	3 rd Func	Condition	4 th Func	Condition	Output Driving (mA)	Note
	7	GP77 (DIOD24)		KSO5 (DO8)		PD7 (DIO24)				8mA	No Internal Pull Up Simple I/O Only
GP IO8x	5	IO SCI (DO24)	13h<1>=1	GP85 (DIOD24)		SMDAT0 (DIOD24)				24mA	No Internal Pull Up Simple I/O Only
	6	GP86 (DIOD24)		SMCLK0 (DIOD24)						24mA	No Internal Pull Up Simple I/O Only

7. Special Pin Routings

Figure 7-1. IT8733 EUP Applications Circuitry for Intel ICH

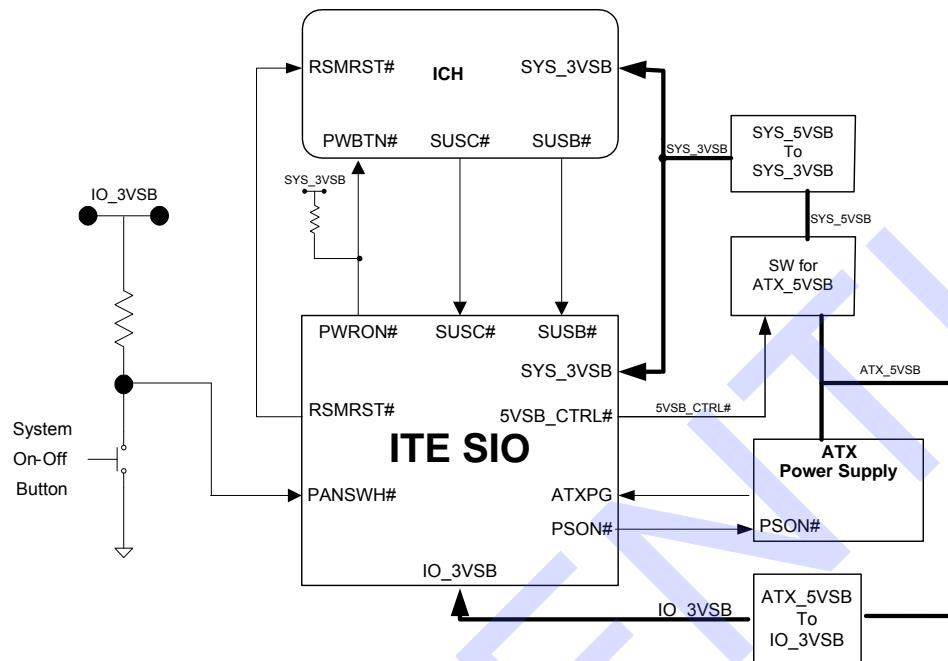
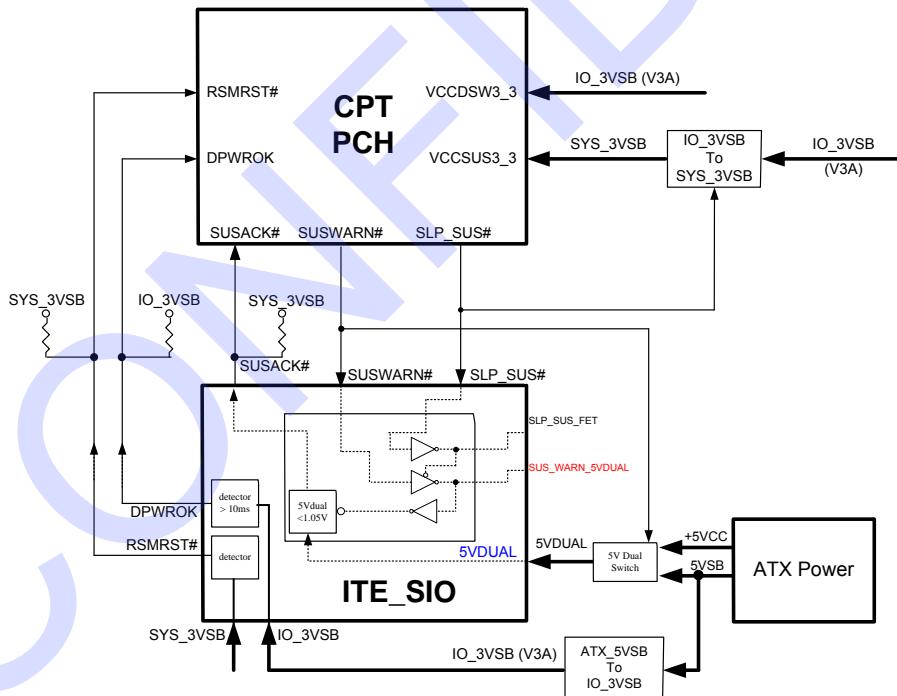


Figure 7-2. IT8733 DSW Applications Circuitry for Intel CPT/PCH



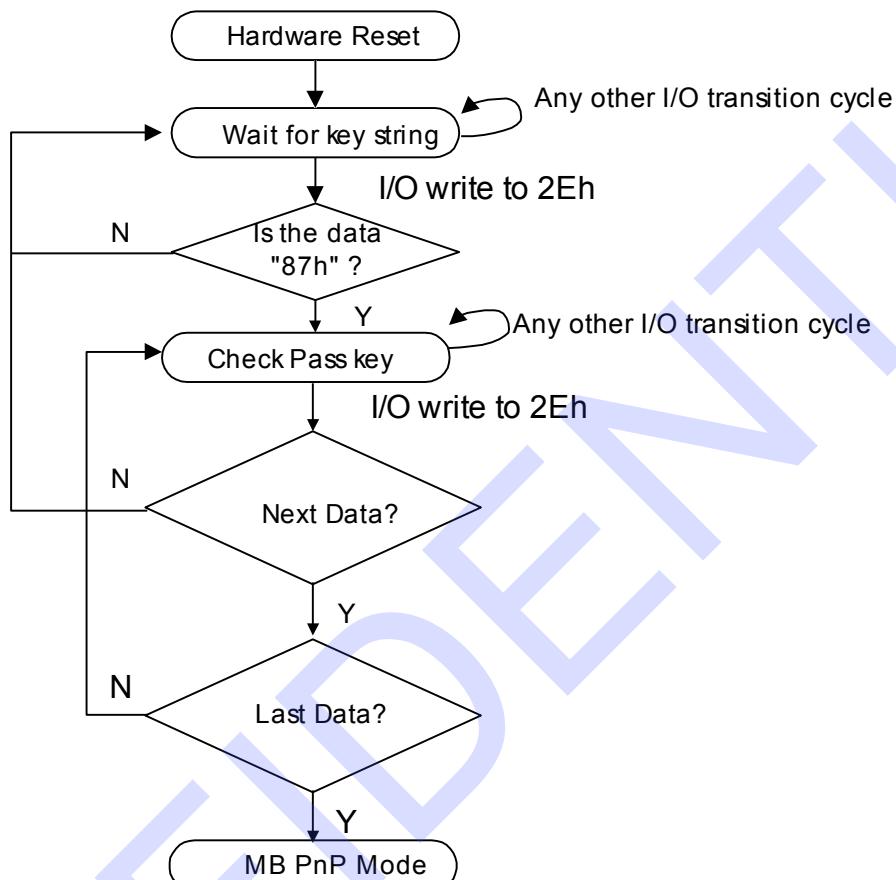
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CONFIDENTIAL

8. Configuration

8.1 Configuring Sequence

After hardware reset or power-on reset, the IT8733 enters the normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is "1".



There are three steps below to completing the configuration setup:

- (1) Enter MB PnP Mode
- (2) Modify data of configuration registers
- (3) Exit MB PnP Mode

The undesired result may occur if the MB PnP Mode is not exited properly.

(1) Enter MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are required to be performed during the Wait for Key state and in order to ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) of the next step.

	Address Port	Data Port
87h, 01h, 55h, 55h;	2Eh	2Fh
or 87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modify Data of Configuration Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

The Configuration can be accessed by uC, and the base address is 2900h.

(3) Exit MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to "1" to exit the MB PnP Mode.

8.2 Configuration Registers

All registers except APC/PME registers will be reset to the default state when RESET is activated.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number (LDN)
All	13h	R/W	01h	Super I/O Control (SIOCTRL)
All	15h	R/W	00h	Super I/O IRQ Configuration (SIOIRQ)
All	20h	R	87h	Chip ID Byte 1
All	21h	R	33h	Chip ID Byte 2
All	22h	W-R	03h	Chip Version
All	23h	R/W	00h	Clock Selection Register
07h Note1	25h	R/W	00h	GPIO Set 1 Multi-Function Pin Selection Register Bit 0 powered by 3VSB.
07h Note1	26h	R/W	FFh	GPIO Set 2 Multi-Function Pin Selection Register Bit 7-0 Powered by 3VSB
07h Note1	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
07h Note1	28h	R/W	C0h	GPIO Set 4 Multi-Function Pin Selection Register Bit 7-0 Powered by 3VSB
07h Note1	29h	R/W	00h	GPIO Set 5 Multi-Function Pin Selection Register Bit 5-3 powered by 3VSB.
07h Note1	2Ah	R/W	00h	Extended 1 Multi-Function Pin Selection Register Bit 7-0 Powered by 3VSB
All	2Bh	R/W	00h	PANSWH# Mask Time Register
07h Note1	2Ch	R/W	8Bh	Extended 2 Multi-Function Pin Selection Register Bit 7-0 Powered by 3VSB
07h Note1	2Dh	R/W	00h	Special Function Control Register Bit 7-0 Powered by 3VSB
F4h Note1	2Eh	R/W	00h	Test 1 Register
F4h Note1	2Fh	R/W	00h	Test 2 Register

Note 1: These registers can be read from all LDNs.

Table 8-2. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register 1

Table 8-3. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 2 Activate
01h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
01h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1

Table 8-4. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select ^{Note2}
03h	F0h	R/W	0Bh ^{Note2}	Parallel Port Special Configuration Register

Note 2: When the bit 2 of the Primary Base Address LSB Register of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

Table 8-5. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	Environment Controller Activate
04h	60h	R/W	02h	Environment Controller Base Address MSB Register
04h	61h	R/W	90h	Environment Controller Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	Environment Controller Interrupt Level Select
04h	F0h	R/W	00h	APC/PME Event Enable Register
04h	F1h	R/W	00h	APC/PME Status Register
04h	F2h	R/W	00h	APC/PME Control Register 1
04h	F3h	R/W	00h	Environment Controller Special Configuration Register
04h	F4h	R-R/W	00h	APC/PME Control Register 2
04h	F5h	R/W	-	APC/PME Special Code Index Register
04h	F6h	R/W	-	APC/PME Special Code Data Register
04h	FAh	R/W	-	Special Configuration Register 1
04h	FBh	R/W	-	Special Configuration Register 2

Table 8-6. KBC(Keyboard) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
05h	30h	R/W	01h	KBC(Keyboard) Activate
05h	60h	R/W	00h	KBC(Keyboard) Data Base Address MSB Register
05h	61h	R/W	60h	KBC(Keyboard) Data Base Address LSB Register
05h	62h	R/W	00h	KBC(Keyboard) Command Base Address MSB Register
05h	63h	R/W	64h	KBC(Keyboard) Command Base Address LSB Register
05h	70h	R/W	01h	KBC(Keyboard) Interrupt Level Select
05h	71h	R-R/W	02h	KBC(Keyboard) Interrupt Type ^{Note3}
05h	F0h	R/W	48h	KBC(Keyboard) Special Configuration Register

Table 8-7. KBC(Mouse) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
06h	30h	R/W	00h	KBC(Mouse) Activate
06h	70h	R/W	0Ch	KBC(Mouse) Interrupt Level Select
06h	71h	R-R/W	02h	KBC(Mouse) Interrupt Type ^{Note3}
06h	F0h	R/W	00h	KBC(Mouse) Special Configuration Register

Note 3: These registers are **read only** unless the write enable bit (Index=F0h) is asserted.

Table 8-8. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	60h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
07h	61h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
07h	62h	R/W	00h	Simple I/O Base Address MSB Register
07h	63h	R/W	00h	Simple I/O Base Address LSB Register
07h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
07h	71h	R/W	00h	Watch Dog Timer Control Register
07h	72h	R/W	20h	Watch Dog Timer Configuration Register
07h	73h	R/W	38h	Watch Dog Timer Time-out Value (LSB) Register
07h	74h	R/W	00h	Watch Dog Timer Time-out Value (MSB) Register
07h	A0h	R/W	00h	Simple Input SET 9 Enable Register
07h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
07h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
07h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
07h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
07h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
07h	B8h	R/W	00h	GPIO Set 1 Pin Internal Pull-up Enable Register
07h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
07h	Bah	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
07h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
07h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register

LDN	Index	R/W	Reset	Configuration Register or Action
07h	BDh	R/W	00h	GPIO Set 6 Pin Internal Pull-up Enable Register
07h	C0h	R/W	01h	Simple I/O Set 1 Enable Register Bit 0 powered by 3VSB.
07h	C1h	R/W	00h	Simple I/O Set 2 Enable Register Bit 7-0 Powered by 3VSB
07h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
07h	C3h	R/W	40h	Simple I/O Set 4 Enable Register Bit 7-0 Powered by 3VSB
07h	C4h	R/W	00h	Simple I/O Set 5 Enable Register Bit 7-0 Powered by 3VSB
07h	C8h	R/W	00h	Simple I/O Set 1 Output Enable Register
07h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
07h	CaH	R/W	00h	Simple I/O Set 3 Output Enable Register
07h	CBh	R/W	00h	Simple I/O Set 4 Output Enable Register Bit 7-0 Powered by 3VSB
07h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register Bit 7-0 Powered by 3VSB
07h	CDh	R/W	00h	Simple I/O Set 6 Output Enable Register Bit 7-0 Powered by 3VSB
07h	Ceh	R/W	00h	Simple I/O Set 7 Output Enable Register Bit 7-0 Powered by 3VSB
07h	CFh	R/W	00h	Simple I/O Set 8 Output Enable Register Bit 7-0 Powered by 3VSB
07h	E0h	R/W	00h	Panel Button De-bounce 0 Input Pin Mapping Register
07h	E1h	R/W	00h	Panel Button De-bounce 1 Input Pin Mapping Register
07h	E2h	R/W	00h	IRQ External Routing 0 Input Pin Mapping Register
07h	E3h	R/W	00h	IRQ External Routing 1 Input Pin Mapping Register
07h	E4h	R/W	00h	IRQ External Routing 1-0 Interrupt Level Selection Registers
07h	F0h	R/W	00h	SMI# Control Register 1
07h	F1h	R/W	00h	SMI# Control Register 2
07h	F2h	R/W	00h	SMI# Status Register 1
07h	F3h	R/W	00h	SMI# Status Register 2
07h	F4h	R/W	00h	SMI# Pin Mapping Register
07h	F5h	R/W	00h	Hardware Monitor Thermal Output Pin Mapping Register Bit 7-0 powered by 3VSB
07h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
07h	F7h	R/W	00h	Keyboard Lock Pin Mapping Register
07h	F8h	R/W	00h	GP LED Blinking 1 Pin Mapping Register Bit 7-0 Powered by 3VSB

LDN	Index	R/W	Reset	Configuration Register or Action
07h	F9h	R/W	00h	GP LED Blinking 1 Control Register Bit 7-0 Powered by 3VSB.
07h	Fah	R/W	00h	GP LED Blinking 2 Pin Mapping Register Bit 7-0 Powered by 3VSB
07h	FBh	R/W	00h	GP LED Blinking 2 Control Register Bit 7-0 Powered by 3VSB

Table 8-9. RTC Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
08h	30h	R/W	00h	RTC Activate
08h	60h	R/W	02h	RTC Base Address MSB Register
08h	61h	R/W	70h	RTC Base Address LSB Register
08h	70h	R/W	00h	RTC Interrupt Level Select
08h	F0h	R/W	00h	RTC Special Configuration Register

Table 8-10. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Ah	30h	R/W	00h	Consumer IR Activate
0Ah	60h	R/W	03h	Consumer IR Base Address MSB Register
0Ah	61h	R/W	10h	Consumer IR Base Address LSB Register
0Ah	70h	R/W	0Bh	Consumer IR Interrupt Level Select
0Ah	F0h	R/W	06h	Consumer IR Special Configuration Register

Table 8-11. Shared Memory/Flash Interface (SMFI) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Fh	30h	R/W	00h	SMFI Activate
0Fh	60h	R/W	00h	SMFI Base Address MSB Register
0Fh	61h	R/W	00h	SMFI Base Address LSB Register
0Fh	F0h	R/W	00h	LPC Memory Window Base Address [31:24]
0Fh	F1h	R/W	00h	LPC Memory Window Base Address [23:16]
0Fh	F2h	R/W	00h	LPC Memory Window Mapping Region Select
0Fh	F3h	R/W	00h	LPC Memory Window Control Register
0Fh	F4h	R/W	F0h	Shared Memory Configuration Register
0Fh	F5h	R/W	00h	H2RAM-HLPC Base Address [15:12]
0Fh	F6h	R/W	00h	H2RAM-HLPC Base Address [23:16]

Table 8-12. BRAM Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
10h	30h	R/W	00h	BRAM Activate
10h	60h	R/W	00h	BRAM BANK0 Base Address MSB Register
10h	61h	R/W	70h	BRAM BANK0 Base Address LSB Register
10h	62h	R/W	00h	BRAM BANK1 Base Address MSB Register
10h	63h	R/W	72h	BRAM BANK1 Base Address LSB Register
10h	F3h	R/W	NA	P80L Begin Index
10h	F4h	R/W	NA	P80L End Index
10h	F5h	R/W	NA	P80L Current Index

Table 8-13. Power Management I/F Channel 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
11h	30h	R/W	00h	PMC1 Activate
11h	60h	R/W	00h	PMC1 Data Base Address MSB Register
11h	61h	R/W	62h	PMC1 Data Base Address LSB Register
11h	62h	R/W	00h	PMC1 Command Base Address MSB Register.
11h	63h	R/W	66h	PMC1 Command Base Address LSB Register.
11h	70h	R/W	01h	PMC1 Interrupt Level Select

Table 8-14. Power Management I/F Channel 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
12h	30h	R/W	00h	PMC2 Activate
12h	60h	R/W	00h	PMC2 Data Base Address MSB Register
12h	61h	R/W	68h	PMC2 Data Base Address LSB Register
12h	62h	R/W	00h	PMC2 Command Base Address MSB Register
12h	63h	R/W	6Ch	PMC2 Command Base Address LSB Register
12h	64h	R/W	00h	PMC2 Mailbox Base Address MSB Register
12h	65h	R/W	00h	PMC2 Mailbox Base Address LSB Register
12h	70h	R/W	01h	PMC2 Interrupt Level Select
12h	F0h	W	NA	General Purpose Interrupt

Table 8-15. SMBus Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
19h	30h	R/W	00h	SMBus Activate
19h	60h	R/W	02h	SMBus ADDR Base Address MSB Register
19h	61h	R/W	15h	SMBus ADDR Base Address LSB Register
19h	62h	R/W	02h	SMBus DATA Base Address MSB Register
19h	63h	R/W	16h	SMBus DATA Base Address LSB Register
19h	70h	R/W	01h	SMBus Interrupt Level Select
19h	76h	R/W	00h	SMBus Special Configuration Register

8.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-16. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=1 SERIAL PORT 1	Base + (0 -7)	
LDN=2 SERIAL PORT 2	Base + (0 -7)	
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST data port
LDN=4 Environment Controller	Base1 + (0 -7) Base2 + (0 -3)	Environment Controller PME#
LDN=5 KBC	Base1 + Base2	KBC
LDN=8 RTC	Base1 + (0 - 7) Base2 + (0 - 3)	
LDN=A Consumer IR	Base + (0 - 7)	
LDN=11 PMC1	Base1 + Base2	PMC1
LDN=12 PMC2	Base1 + Base2 + Base3	PMC2
LDN=19 SMBus	Base1 + Base2	SMBus

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is write only. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and the software is not required to clear them.

Bit	Description
7-2	Reserved
1	Returns to the “Wait for Key” state. This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This register is, read/write, which is to select the current logical devices. By reading data from or writing data to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices.

8.3.3 Super I/O Control Register (SIOCTRL) (Index=13h, Default=01h)

This register contains general Super I/O configurations.

Bit	Description
7-2	Reserved
1	SCI_Enable Register(SCI_EN) The bit controls the SCI_ function of QFP:Pin-64 (LQFP:Pin-61). 0: SCI_ output disabled 1: SCI_ output enabled
0	Reserved

8.3.4 Super I/O IRQ Configuration Register (SIOIRQ) (Index=15h, Default=00h)

This register contains general Super I/O configurations.

Bit	Description
7-5	Reserved
4	PMC1&2 SMI# to IRQ2 Enable (SMI2IRQ2) This bit enables using IRQ number 2 in the SERIRQ protocol as a SMI# interrupt. (For PMC1&2 only) This bit is similar to LDACT bit in LDA register. 0: Disable 1: Enable
3-0	Reserved

8.3.5 Chip ID Byte 1 (Index=20h, Default=87h)

This register is Chip ID Byte 1 and **read only**. Bits [7:0]=87h when read.

8.3.6 Chip ID Byte 2 (Index=21h, Default=33h)

This register is Chip ID Byte 2 and **read only**. Bits [7:0]=33h when read.

8.3.7 Chip Version (Index=22h, Default=03h)

Bit	Description
7-4	Reserved
3-0	Version 0000b for AX Version 0001b for BX Version 0010b for CX Version - 0011b for DX Version The part no. is IT8733F/DX(QFP package) or IT8733E/DX(LQFP package).

8.3.8 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-5	Reserved
4	Clock Source Select of Watch Dog Timer 0: Internal oscillating clock (Default) 1: External CLKIN
3-2	Reserved
1	KB/MS Software Swap Enable 0: Disable (Default) 1: Enable LDN4 IndexF4h<bit7> must be set to "1b" for "disable".
0	CLKIN Frequency 0: 48 MHz (Default) 1: 24 MHz

8.3.9 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of QFP:Pin-28 (LQFP:Pin-25) 0: Reserved (Default) 1: GP17
6	Function Selection of QFP:Pin-2 (LQFP:Pin-127) 0: 5VSB_CTRL# or CIRRX2 if bit6 of CIR IER = 1. (Default) 1: GP16
5	Function Selection of QFP:Pin-3 (LQFP:Pin-128) 0: PCIRSTIN# if bit2 of index 2C is 1 CIRTX2 if bit7 of CIR IER = 1 (Default) 1: GP15
4	Function Selection of QFP:Pin-31 (LQFP:Pin-28) This pin is VCORE_EN if K8 Power-sequence is selected. 0: PCH_C1 1: GP14
3	Function Selection of QFP:Pin-32 (LQFP:Pin-29) 0: PWROK1 1: GP13
2	Function Selection of QFP:Pin-33 (LQFP:Pin-30) 0: PCIRST1# (Default) 1: GP12

Bit	Description
1	Function Selection of QFP:Pin-34 (LQFP:Pin-31) 0: PCIRST2# (Default) 1: GP11
0	Function Selection of QFP:Pin-84 (LQFP:Pin-81) 0: PCIRST3# (Default) 1: GP10

8.3.10 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=FFh)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of QFP:Pin-20 (LQFP:Pin-17) 0: SIN2 1: GP27 (Default)
6	Function Selection of QFP:Pin-21 (LQFP:Pin-18) 0: SOUT2 1: GP26 (Default)
5	Function Selection of QFP:Pin-22 (LQFP:Pin-19) 0: DSR2# 1: GP25 (Default)
4	Function Selection of QFP:Pin-23 (LQFP:Pin-20) 0: RTS2# 1: GP24 (Default)
3	Function Selection of QFP:Pin-24 (LQFP:Pin-21) The function of QFP:Pin-24 (LQFP:Pin-21) is SI if bit3 of index 2C is 1. If bit3 of index 2C is 0, the function is 0: Reserved 1: GP23
2	Function Selection of QFP:Pin-25 (LQFP:Pin-22) The function of QFP:Pin-25 (LQFP:Pin-22) is SCK if bit3 of index 2C is 1. If bit3 of index 2C is 0, the function is 0: Reserved 1: GP22
1	Function Selection of QFP:Pin-26 (LQFP:Pin-23) 0: DCD2# 1: GP21 (Default)
0	Function Selection of QFP:Pin-27 (LQFP:Pin-24) 0: SIN2 1: GP20 (Default)

8.3.11 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of QFP:Pin-12 (LQFP:Pin-9) 0: FAN_TAC3 (Default) 1: GP37
6	Function Selection of QFP:Pin-13 (LQFP:Pin-10) 0: FAN_CTL3 (Default) 1: GP36
5	Function Selection of QFP:Pin-14 (LQFP:Pin-11) 0: FAN_TAC4 (Default) 1: GP35
4	Function Selection of QFP:Pin-15 (LQFP:Pin-12) 0: SUSWARN# (Default) 1: GP34
3	Function Selection of QFP:Pin-16 (LQFP:Pin-13) 0: SUSACK# (Default) 1: GP33
2	Function Selection of QFP:Pin-17 (LQFP:Pin-14) 0: DPWROK (Default) 1: GP32
1	Function Selection of QFP:Pin-18 (LQFP:Pin-15) 0: PWMOUT or USBPWREN2# (Default) 1: GP31
0	Function Selection of QFP:Pin-19 (LQFP:Pin-16) 0: ATXPG 1: GP30

8.3.12 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=C0h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Reserved
6	Reserved
5	Function Selection of QFP:Pin-71 (LQFP:Pin-68) 0: SUSB# (Default) 1: Reserved
4	Function Selection of QFP:Pin-72 (LQFP:Pin-69) 0: PWRON# (Default) 1: GP44
3	Function Selection of QFP:Pin-75 (LQFP:Pin-72) 0: PANSWH# (Default) 1: GP43
2	Function Selection of QFP:Pin-76 (LQFP:Pin-73) 0: PSION# (Default) 1: GP42

Bit	Description
1	Function Selection of QFP:Pin-78 (LQFP:Pin-75) 0: PWROK2 1: GP41
0	Function Selection of QFP:Pin-79 (LQFP:Pin-76) 0: 3VSB# (Default) 1: GP40

8.3.13 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of QFP:Pin-83, 82 (LQFP:Pin-80, 79) 0: MCLK, MDAT 1: GP56, GP57
6	Function Selection of QFP:Pin-81, 80, 45 (LQFP:Pin-78, 77, 42) 0: KCLK, KDAT, KRST# (Default) 1: GP60, GP61, GP62
5	Function Selection of QFP:Pin-85 (LQFP:Pin-82) 0: CIRRX1 or RSMRST# (Default) RSMRST# is an open-drain output function, which is active low about 60ms when 3VSB is powered on. 1: GP55
4	Function Selection of QFP:Pin-73 (LQFP:Pin-70) 0: PME# or USBPWREN1# (Default) 1: GP54
3	Function Selection of QFP:Pin-77 (LQFP:Pin-74) 0: SUSC# (Default) 1: GP53
2	Function Selection of QFP:Pin-10 (LQFP:Pin-7) 0: FAN_TAC2 (Default) 1: GP52
1	Function Selection of QFP:Pin-11 (LQFP:Pin-8) 0: FAN_CTL2 (Default) 1: GP51
0	Function Selection of QFP:Pin-48 (LQFP:Pin-45) The function of QFP:Pin-48 (LQFP:Pin-45) is SO if bit3 of index 2C is 1. If bit3 of index 2C is 0, the function is 0: Reserved 1: GP50

8.3.14 Extended 1 Multi-Function Pin Selection Register (Index=2Ah, Default=00h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Enable 3VSBSW# (For System Suspend-to-RAM) 0: 3VSBSW# is always inactive. (Default) 1: 3VSBSW# is enabled. It will be (NOT SUSB#) NAND SUSC#.
6	Multi-Function Selection of QFP:Pin-53 (LQFP:Pin-50) 0: Reserved 1: External Thermal Sensor Data Specifically when External Thermal Sensor Host is enabled (bit 6-4 of EC Index 0Ah). The function of this pin is selected as SST or ETS_DAT.
5	Extended Multi-Function Selection of QFP:Pin-30 (LQFP:Pin-27) The function of Pin 30 is CE_N if bit3 of index 2C is 1. If bit3 of index 2C is 0, the function is 0: Reserved 1: CIRTX1
4	Reserved
3	Reserved
2	Reserved
1	Extended Multi-Function Selection of QFP:Pin-31 (LQFP:Pin-28) If bit 4 of index 25 is 0, the function of QFP:Pin-31 (LQFP:Pin-29) is 0: Reserved 1: PCH_C If bit 4 of index 25 is 1, this bit must be set to 0.
0	Delay Time Selection of 3VSBSW# Rising Edge to PWROK1/2 Rising Edge 0: 1us (Default) 1: 135ms

8.3.15 PANSWH# Mask timer Register (Index=2Bh, Default=00h)

Bit	Description
7	Reserved
6	ATXPG Enable (QFP:Pin-19, LQFP:Pin-16) 0: Enable (Default) 1: Disable
5-3	Reserved
2-0	PANSWH# Mask Time 000: Default 001: 1 second 010: 2 seconds 011: 3 seconds 100: 4 seconds

8.3.16 Extended 2 Multi-Function Pin Selection Register (Index=2Ch, Default=8Bh)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	PS2 Mouse Double Click Wake-up Mode Selection 0: 3-Byte mode (Default) 1: 4-Byte mode
3	FSPI Enable 0: Disable 1: Enable (Default)
2	Enable PCIRSTIN# of QFP:Pin-3 (LQFP:Pin-128) 0: Disable(Default) 1: Enable
1	Reserved
0	VIN3 Function Selection 0: External VIN3 voltage sensor 1: Internal Voltage Divider for ACC3. (Default)

8.3.17 Special Function Control Register (Index=2Dh, Default=00h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7-5	Reserved
4	Enable DPWROK of QFP:Pin-17 (LQFP:Pin-14) 0: Enable (Default) 1: Disable
3	Intel DSW Power-Sequence 0: Disable (Default) 1: Enable
2	USB 48Mhz Clock Enable 0: Disable(Default) 1: Enable
0	AMD K8 Power Sequence 0: Disable (Default) 1: Enable

8.3.18 Test 1 Register (Index=2Eh, Default=00h)

This register is reserved for ITE and should not be set.

8.3.19 Test 2 Register (Index=2Fh, Default=00h)

This register is reserved for ITE and should not be set.

8.4 Serial Port 1 Configuration Registers (LDN=01h)

8.4.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port 1 Enable 1: Enable 0: Disable

8.4.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only as “0h” for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.4.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3]
2-0	Read only as “000b”

8.4.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	Reserved with default “0h”
3-0	Interrupt Select Level for Serial Port 1 Please refer to Table 8-17. Interrupt Level Mapping Table.

8.4.5 Serial Port 1 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6-4	Serial Port 1 Mode 000: Standard (default) Else : Reserved Except the standard mode, COM1 and COM2 cannot be selected in the same mode.
3	Serial Port 1 Pin Gating 0: Gated by VCC 1: No Gating
2-1	Clock Source 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: Reserved 11: Reserved
0	IRQ Type 1: IRQ sharing 0: Normal

8.5 Serial Port 2 Configuration Registers (LDN=02h)

8.5.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port 2 Enable 1: Enable 0: Disable

8.5.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only with “0h” for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.5.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	Read/write , mapped as Base Address [7:3]
2-0	Read only as “000b”

8.5.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	Reserved with default “0h”
3-0	Interrupt Level Select for Serial Port 2 Please refer to Table 8-17. Interrupt Level Mapping Table.

8.5.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6-4	Serial Port 2 Mode 000: Standard (Default) Else: Reserved Except the standard mode, COM1 and COM2 cannot be selected in the same mode.
3	Serial Port 2 Gating 0: Gated by VCC 1: No Gating
2-1	Clock Source 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: Reserved 11: Reserved
0	IRQ Type 1: IRQ sharing 0: Normal

8.6 Parallel Port Configuration Registers (LDN=03h)

8.6.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Parallel Port Enable 1: Enable 0: Disable

8.6.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only as “0h” for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.6.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	Read/write , mapped as Base Address[7:2]
1-0	Read only as “00b”

8.6.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	Read only as “0h” for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.6.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	Read/write , mapped as Base Address[7:2]
1-0	Read only as “00b”

8.6.6 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	Reserved with default “0h”
3-0	Interrupt Level Select for Parallel Port Please refer to Table 8-17. Interrupt Level Mapping Table.

8.6.7 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	Reserved with default “00h”
2-0	DMA Channel Select for Parallel Port Please refer to Table 8-19. DMA Channel Mapping Table on page 90.

8.6.8 Parallel Port Special Configuration Register (Index=F0h, Default=0Bh)

Bit	Description
7-3	Reserved
2	IRQ Type 1: IRQ sharing 0: Normal
1-0	Parallel Port Modes 00 : Standard Parallel Port mode (SPP) 01 : EPP mode 10 : ECP mode 11 : EPP mode & ECP mode These bits are independent. If bit 1 is set, ECP mode is enabled. If bit 0 is set, EPP mode is enabled except when bit 2 of Parallel Port Primary Base Address LSB Register is set to 1 in accordance with the EPP specification.

8.7 Environment Controller Configuration Registers (LDN=04h)

8.7.1 Environment Controller Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Environment Controller Enable 1: Enable 0: Disable This is a read/write register.

8.7.2 Environment Controller Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write, mapped as Base Address[11:8]

8.7.3 Environment Controller Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	Read/write, mapped as Base Address[7:3]
2-0	Read only as "000b"

8.7.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write, mapped as Base Address[11:8]

8.7.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	Read/write, mapped as Base Address[7:3]
2-0	Read only as "000b."

8.7.6 Environment Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	Reserved with default "0h"
3-0	Interrupt Level Select for Environment Controller Please refer to Table 8-17. Interrupt Level Mapping Table on page 89.

8.7.7 APC/PME Event Enable Register (PER) (Index=F0h, Default=00h)

Bit	Description
7	This bit is set to 1 when 3VSB is off and becomes ineffective if 0 is written to it. This bit is write clear..
6	RTC Event 0: Disable 1: Enable
5	Reserved with default “0b”
4	PS/2 Mouse Event 0: Disable 1: Enable
3	Keyboard Event 0: Disable 1: Enable
2	Reserved
1	USB Host Password Wake Up Event (Enabled with EC 2FE2<0>) 0: Disable 1: Enable
0	CIR Event 0: Disable 1: Enable

8.7.8 APC/PME Status Register (PSR) (Index=F1h, Default=00h)

Bit	Description
7	This bit is set to 1 when VCC3 is on at the previous AC power failure whereas 0 when VCC3 is off. This bit is write 1 to clear.
6	0: No RTC event detected 1: RTC event detected
5	Reserved
4	0: No PS/2 mouse event detected 1: PS/2 mouse event detected
3	0: No keyboard event detected 1: Keyboard event detected
2	Reserved
1	USB Host Password Wake Up Event Status (Enabled with EC 2FE2<0>) 0: No USB event detected 1: USB event detected.
0	0: No CIR event detected 1: CIR event detected

8.7.9 APC/PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	PER and PSR Normal Run Access Enable
6	PME# Output Control 0: Enable 1: Disable
5	This bit is restored automatically to the previous VCC3 state before the power failure occurs. Note: AC failure resume can be made by either IO or South Bridge. For the use of IO, the BIOS needs to be set as the following: LDN4 F4<5> and LDN4 F2<5> setting: 1 X :Always ON 0 1 :Memory 0 0 :Always OFF For the use of South Bridge, F4 bit 5 and F4 bit 6 need to be set to 1.
4	Reserved
3	Keyboard Event Mode Selection 1: Determined by PCR 2 0: Pulse falling edge on KCLK
2	Mouse Event at VCC3 off 1: Click key twice sequentially 0: Pulse falling edge on MCLK
1	Mouse Event at VCC3 on 1: Click key twice sequentially 0: Pulse falling edge on MCLK
0	CIRRX1 Pin Selection 1: Pin 84(QFP) / Pin 81(LQFP) 0: Pin 85(QFP) / Pin 82(LQFP)

8.7.10 Environment Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-6	Reserved
0	IRQ Type 1: IRQ sharing 0: Normal

8.7.11 APC/PME Control Register 2 (PCR 2) (Index=F4h, Default=00h)

Bit	Description
7	Auto-swap of KCLK/KDAT and MCLK/MDAT 0: Enable (Default) 1: Disable
6	Gate Extra PWRON# Pulse at First 3VSB Power-on 0: None gating (Default) 1: Gating Note: AC failure resume can be made by either IO or South Bridge. For the use of IO, the BIOS needs to be set as the following: LDN4 F4<5> and LDN4 F2<5> setting: 1 X :Always ON 0 1 :Memory 0 0 :Always OFF For the use of South Bridge, F4 bit 5 and F4 bit 6 need to be set to 1.
5	PSON# state when 3VSB is switched from off to on 0: High-Z (power OFF in default) 1: Inverting of PSIN
4	Reserved
3-2	Key Number of Keyboard Power-up Event 00: 5 Key string mode, 3 keys simultaneous mode 01: 4 Key string mode, 2 keys simultaneous mode 10: 3 Key string mode, 1 key simultaneous mode 11: 2 Key string mode, Reserved (Not valid for simultaneous mode)
1-0	Mode Selection of Keyboard Power-up Event 00: KCLK falling edge 01: Key string mode 10: Simultaneous key stroke mode 11: Reserved

8.7.12 APC/PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	Reserved (should be "00")
5-0	Indicate which Identification Key Code or CIR code register to be read/written via 0xF6 00h~04h: Key code 20h~32h: CIR code 34h~37h: VBAT registers 38h~3Eh: VBAT registers

8.7.13 APC/PME Special Code Data Register (Index=F6h)

There are 5 bytes for the Key String mode, 3 bytes for Stroke Keys at the same time mode and CIR event codes.

8.7.14 Special Configuration Register 1 (Index=FAh)

Bit	Description
7-5	Reserved
4	EuP Wake-up Event 0: Disable 1: Enable
3	RI2# Wake-up Event 0: Disable 1: Enable
2	RI1# Wake-up Event 0: Disable 1: Enable
1	5VSB_CTL# Enable 0: Disable (Default) 1: Enable
0	Reserved

8.7.15 Special Configuration Register 2 (Index=FBh)

Bit	Description
7-4	Reserved
3	RI2# Wake-up Event Status 0: No RI2# event detected 1: RI2# event detected
2	RI1# Wake-up Event Status 0: No RI1# event detected 1: RI1# event detected
1-0	Reserved

8.8 KBC(Keyboard) Configuration Registers (LDN=05h)

8.8.1 KBC(Keyboard) Activate (Index=30h, Default=01h)

Bit	Description
7-1	Reserved
0	KBC(Keyboard) Enable 1: Enable 0: Disable

8.8.2 KBC(Keyboard) Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.8.3 KBC(Keyboard) Data Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.8.4 KBC(Keyboard) Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.8.5 KBC(Keyboard) Command Base Address LSB Register (Index=63h, Default=64h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.8.6 KBC(Keyboard) Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-4	Reserved with default "0h"
3-0	Interrupt Level Select for KBC(Keyboard) Please refer to Table 8-17. Interrupt Level Mapping Table on page 89.

8.8.7 KBC(Keyboard) Interrupt Type (Index=71h, Default=02h)

This register indicates the interrupt type set for KBC(Keyboard) and is **read only** as "02h" when bit 0 of the KBC(Keyboard) Special Configuration Register is cleared. When bit 0 is set, the interrupt type can be selected as level or edge trigger.

Bit	Description
7-2	Reserved
1	1: High level 0: Low level
0	1: Level type 0: Edge type

8.8.8 KBC(Keyboard) Special Configuration Register (Index=F0h, Default=08h)

Bit	Description
7-5	Reserved Must be "000b"
4	IRQ Type 1: IRQ sharing 0: Normal
3	KBC Clock 1: 8 MHz 0: 12 MHz
2	KBC Lock 1: Enable 0: Disable
1	Interrupt Type Change Enable 1: The interrupt type for KBC(Keyboard) can be changed. 0: The interrupt type for KBC(Keyboard) is fixed.
0	Reserved

8.9 KBC(Mouse) Configuration Registers (LDN=06h)

8.9.1 KBC(Mouse) Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	KBC(Mouse) Enable 1: Enable 0: Disable

8.9.2 KBC(Mouse) Interrupt Level Select (Index=70h, Default=0Ch)

Bit	Description
7-4	Reserved with default “0h”
3-0	Interrupt Level Select for KBC(Mouse) Please refer to Table 8-17. Interrupt Level Mapping Table on page 89.

8.9.3 KBC(Mouse) Interrupt Type (Index=71h, Default=02h)

This register indicates the interrupt type set for KBC(Mouse) and is read only as “02h” when bit 0 of the KBC(Mouse) Special Configuration Register is cleared. When bit 0 is set, the interrupt type can be selected as level or edge trigger.

Bit	Description
7-2	Reserved
1	1: High level 0: Low level
0	1: Level type 0: Edge type

8.9.4 KBC(Mouse) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	Reserved with default “00h”
1	IRQ Type 1: IRQ sharing 0: Normal
0	Interrupt Type Change Enable 1: The interrupt type for KBC(Mouse) can be changed. 0: The interrupt type for KBC(Mouse) is fixed.

8.10 GPIO Configuration Registers (LDN=07h)

8.10.1 SMI# Normal Run Access Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.10.2 SMI# Normal Run Access Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-2	Read/write , mapped as Base Address [7:2]
1-0	Read only as "00b"

8.10.3 Simple I/O Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.10.4 Simple I/O Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:0]
2-0	Read only as "00b"

The Simple I/O can be accessed by uC, and the base address is 2C00h.

8.10.5 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	Reserved
3-0	Interrupt Level Select for Panel Button De-bounce Please refer to Table 8-17. Interrupt Level Mapping Table on page 89.

8.10.6 Watch Dog Timer Control Register (Index=71h, Default=00h)

Bit	Description
7	WDT is reset upon a CIR interrupt.
6	WDT is reset upon a KBC(Mouse) interrupt.
5	WDT is reset upon a KBC(Keyboard) interrupt.
4	Reserved
3-2	Reserved
1	Force Time-out This bit is self-cleared.
0	WDT Status 1: WDT value is equal to 0. 0: WDT value is not is equal to 0.

8.10.7 Watch Dog Timer Configuration Register (Index=72h, Default=20h)

Bit	Description
7	WDT Time-out Value Select 1 1: Second 0: Minute
6	WDT Output through KRST (pulse) Enable 1: Enable 0: Disable
5	WDT Time-out Value Extra Select 1: 64ms x WDT Timer-out value (default = 4s) 0: Determined by WDT Time-out value select 1 (bit 7 of this register)
4	Reserved
3-0	Interrupt Level Select for WDT Please refer to Table 8-17. Interrupt Level Mapping Table on page 89.

8.10.8 Watch Dog Timer Time-out Value (LSB) Register (Index=73h, Default=38h)

Bit	Description
7-0	WDT Time-out Value 7-0

8.10.9 Watch Dog Timer Time-out Value (MSB) Register (Index=74h, Default=00h)

Bit	Description
7-0	WDT Time-out Value 15-8

8.10.10 Simple Input Set 9 Enable Reigster (Index=A0h, Default=00h)

This register is to select the function as the Simple Input function or the Alterante function.

Bit	Description
7-6	Reserved
5-0	1: Simple Input function 0: Alternate function

8.10.11 GPIO Pin Set 1, 2, 3, 4, and 5 Polarity Registers (Index=B0h, B1h, B2h, B3h and B4h, Default=00h)

These registers are to program the GPIO pin type for polarity inverting or non-inverting.

Bit	Description
7-0	GPIO Polarity Select 1: Inverting 0: Non-inverting

8.10.12 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, BC_h, BD_h, Default=00h, 00h, 00h, 00h, 00h, and 00h)

These registers are to enable the GPIO pin internal pull-up.

Bit	Description
7-0	GPIO Pin Internal Pull-up 1: Enable 0: Disable

8.10.13 Simple I/O Set 1, 2, 3, 4 and 5 Enable Registers (Index=C0h, C1h, C2h, C3h and C4h, Default=01h, 00h, 00h, 40h, and 00h)

These registers are to select the function as the Simple I/O function or the Alternate function.

Bit	Description
7-0	1: Simple I/O function 0: Alternate function

8.10.14 Simple I/O Set 1, 2, 3, 4, 5, 6, and 7 Output Enable Registers (Index=C8h, C9h, CAh, CBh, CCh, CDh, and CEh, Default=00h, 00h, 00h, 00h, 00h, 00h, and 00h)

These registers are to determine the direction of the Simple I/O.

Bit	Description
7-0	0: Input mode 1: Output mode

8.10.15 Simple I/O Set 8 Output Enable Register (Index=CFh, Default=00h)

The register is to determine the direction of the Simple I/O.

Bit	Description
7	Reserved
6-5	0: Input mode 1: Output mode
4-0	Reserved

8.10.16 Panel Button De-bounce 0 Input Pin Mapping Register (Index=E0h, Default=00h)

Bit	Description
7	Reserved
6	IRQ Enable
5-0	Input Pin Location Please refer to Table 8-17. Location Mapping on page 89. Table 8-18. Location Mapping

8.10.17 Panel Button De-bounce 1 Input Pin Mapping Register (Index=E1h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Input Pin Location Please refer to Table 8-17. Location Mapping on page 89. Table 8-18. Location Mapping

8.10.18 IRQ External Routing 1-0 Input Pin Mapping Registers (Index=E3h-E2h, Default=00h)

Bit	Description
7	Reserved
6	IRQ Enable
5-0	Input Pin Location Please refer to Table 8-17. Location Mapping on page 89. Table 8-18. Location Mapping

8.10.19 IRQ External Routing 1-0 Interrupt Level Selection Registers (Index=E4h, Default=00h)

Bit	Description
7-4	Interrupt Level Select for IRQ External Routing 1 Please refer to Table 8-17. Interrupt Level Mapping Table on page 89.
3-0	Interrupt Level Select for IRQ External Routing 0 Please refer to Table 8-17. Interrupt Level Mapping Table on page 89.

8.10.20 SMI# Control Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6	This bit is to enable the generation of an SMI# due to KBC(Mouse)'s IRQ (EN_MIRQ).
5	This bit is to enable the generation of an SMI# due to KBC(Keyboard)'s IRQ (EN_KIRQ).
4	This bit is to enable the generation of an SMI# due to Environment Controller's IRQ (EN_ECIRQ).
3	This bit is to enable the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ).
2	This bit is to enable the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ).
1	This bit is to enable the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ).
0	Reserved

8.10.21 SMI# Control Register 2 (Index=F1h, Default=00h)

Bit	Description
7	Reserved
6	0: Edge trigger 1: Level trigger
5-3	Reserved
2	This bit is to enable the generation of an SMI# due to WDT's IRQ (EN_WDT).
1	This bit is to enable the generation of an SMI# due to CIR's IRQ (EN_CIR).
0	Enable Generation of an SMI# due to PBD's IRQ (EN_PBD)

8.10.22 SMI# Status Register 1 (Index=F2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	Reserved
6	KBC (PS/2 Mouse)'s IRQ
5	KBC(Keyboard)'s IRQ
4	Environment Controller's IRQ
3	Parallel Port's IRQ
2	Serial Port 2's IRQ
1	Serial Port 1's IRQ
0	Reserved

8.10.23 SMI# Status Register 2 (Index=F3h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7-6	Panel Button De-bounce Status 1-0 Writing 1 will reset the status. 0: None detected 1: Detected
5-4	Reserved
3	Reserved
2	WDT's IRQ
1	CIR's IRQ
0	PBD's IRQ

8.10.24 SMI# Pin Mapping Register (Index=F4h, Default=00h)

Bit	Description
7-6	Reserved
5-0	SMI# Pin Location Please refer to Table 8-18. Location Mapping on page 89.

8.10.25 Hardware Monitor Thermal Output Pin Mapping Register (Index=F5h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Thermal Output Pin Location Please refer to Table 8-18. Location Mapping on page 89.

8.10.26 Hardware Monitor Alert Beep Pin Mapping Register (Index=F6h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Alert Beep Pin Location Please refer to Table 8-18. Location Mapping on page 89.

8.10.27 Keyboard Lock Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Keyboard Lock Pin Location Please refer to Table 8-18. Location Mapping on page 89.

8.10.28 GP LED Blinking 1 Pin Mapping Register (Index=F8h, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED Blinking 1 Location Please refer to Table 8-18. Location Mapping on page 89.

8.10.29 GP LED Blinking 1 Control Register (Index=F9h, Default=00h)

Bit	Description
7-4	Reserved
3	GP LED Blinking 1 Short Low Pulse Enable
2-1	GP LED 1 Frequency Control 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	GP LED Blinking 1 Output Low Enable

8.10.30 GP LED Blinking 2 Pin Mapping Register (Index=FAh, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED Blinking 2 Location Please refer to Table 8-18. Location Mapping on page 89.

8.10.31 GP LED Blinking 2 Control Register (Index=FBh, Default=00h)

Bit	Description
7-4	Reserved
3	GP LED Blinking 2 Short Low Pulse Enable
2-1	GP LED 2 Frequency Control 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	GP LED Blinking 2 Output Low Enable

8.11 RTC Configuration Registers (LDN=08h)

8.11.1 RTC Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	RTC Enable 1: Enable 0: Disable

8.11.2 RTC Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only with “0h” for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.11.3 RTC Base Address LSB Register (Index=61h, Default=70h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3]
2-0	Read only as “000b”

8.11.4 RTC Interrupt Level Select (Index=70h, Default=00h)

Bit	Description
7-4	Reserved with default “0h”
3-0	Interrupt Level Select for RTC Please refer to Table 8-17. Interrupt Level Mapping Table.

8.11.5 RTC Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-1	Reserved with default “00h”
0	IRQ Type 1: IRQ sharing 0: Normal

8.12 Consumer IR Configuration Registers (LDN=0Ah)

8.12.1 Consumer IR Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Consumer IR Enable 1: Enable 0: Disable

8.12.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only with “0h” for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.12.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3]
2-0	Read only as “000b”

8.12.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	Reserved with default “0h”
3-0	Interrupt Level Select for Consumer IR Please refer to Table 8-17. Interrupt Level Mapping Table.

8.12.5 Consumer IR Special Configuration Register (Index=F0h, Default=06h)

Bit	Description
7-1	Reserved with default “00h”
0	IRQ Type 1: IRQ sharing 0: Normal

8.13 Shared Memory/Flash Interface (SMFI) Configuration Registers (LDN=0Fh)

This section lists the default value for each register respectively and more detailed information for this logical device.

8.13.1 SMFI Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	SMFI Enable 1: Enable 0: Disable

8.13.2 SMFI Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-0	Read/write , mapped as Base Address[15:8]

8.13.3 SMFI Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-4	Read/write , mapped as Base Address[7:4]
3-0	Read only as “0000b”

8.13.4 LPC Memory Window Base Address [31:24] (Index=F0h, Default=00h)

The base address of LPC memory window should not overlap with legacy BIOS range, extended legacy BIOS range and HLPGRAMBA.

Bit	Description
7-0	LPC Memory Window Base Address [31:24] (LPCMWB[31:24]) Specify the base address of the user-defined 64K window on LPC memory space for PCH LGMR application.

8.13.5 LPC Memory Window Base Address [23:16] (Index=F1h, Default=00h)

Bit	Description
7-0	LPC Memory Window Base Address [23:16] (LPCMWB[23:16]) Specify the base address of the user-defined 64K window on LPC memory space for PCH LGMR application.

8.13.6 LPC Memory Window Mapping Region Select (Index=F2h, Default=00h)

Bit	Description
7-0	LPC Memory Window Mapping Region Select (LPCMWMRS) The LPC memory window is mapped into the region that ranges from (10000_0000h – flash size + 64K*LPCMWRS) to (FFFF_FFFFh – fihash size + 64K*(LPCMWRS + 1)) on LPC memory space. The flash size is specified by FMSS.

8.13.7 LPC Memory Window Control Register (Index=F3h, Default=00h)

Bit	Description
7-6	Reversed
0	LPC Memory Window Enable (LPCMWE) 0b: Disable. 1b: The LPC memory cycle of which address is located in the user-defined LPC memory window will be decoded and mapped into the region that is specified by LPCMW/MRS.

8.13.8 Shared Memory Configuration Register (Index=F4h, Default=F0h)

Bit	Description
7-4	BIOS FWH ID (FWHID) These bits correspond to the 4-bit ID which is part of a FWH transaction.
3-2	Reserved
1	BIOS Extended Space Enable (BIOSEXTS) This bit expands the BIOS address space to make this chip respond the Extended BIOS address range.
0	Reserved

8.13.9 H2RAM-HLPC Base Address [15:12] (Index=F5h, Default=00h)

The H2RAM-HLPC base address is only within the range of FFXX_X000h. (X denotes it's programmable by registers).

The H2RAM-HLPC function will be disabled if SPI follow mode is enabled.

Bit	Description
7-4	H2RAM-HLPC Base Address Bits [15:12] (HLPCRAMBA[15:12]) Define EC internal RAM base address on LPC memory space.
3-0	Reserved

8.13.10 H2RAM-HLPC Base Address [23:16] (Index=F6h, Default=00h)

Bit	Description
7-0	H2RAM-HLPC Base Address Bits [23:16] (HLPCRAMBA[23:16]) Define EC internal RAM base address on LPC memory space.

8.14 BRAM Configuration Registers (LDN=10h)

8.14.1 BRAM Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	BRAM Enable 1: Enable 0: Disable

8.14.2 BRAM BANK0 Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-0	Read/write, mapped as Base Address[15:8]

8.14.3 BRAM BANK0 Base Address LSB Register (Index=61h, Default=70h)

Bit	Description
7-1	Read/write, mapped as Base Address[7:1]
0	Read only as “0b”

8.14.4 BRAM BANK1 Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-0	Read/write, mapped as Base Address[15:8]

8.14.5 BRAM BANK1 Base Address LSB Register (Index=63h, Default=72h)

Bit	Description
7-1	Read/write, mapped as Base Address[7:1]
0	Read only as “0b”

8.14.6 P80L Begin Index (P80LB) (Index=F3h, Default=-h)

Bit	Description
7-6	Reserved
5-0	P80L Begin Index (P80LBI) It indicates the P80L queue begins in BRAM Bank 1. Refer to section 10.7.3.1 P80L on page 317.

8.14.7 P80L End Index (P80LE) (Index=F4h, Default=-h)

Bit	Description
7-6	Reserved
5-0	P80L End Index (P80LEI) It indicates the P80L queue ends in BRAM Bank 1. Refer to section 10.7.3.1 P80L on page 317.

8.14.8 P80L Current Index (P80LC) (Index=F5h, Default=-h)

Bit	Description
7-6	Reserved
5-0	P80L Current Index (P80LC) It indicates the P80L queue current in BRAM Bank 1. Refer to section 10.7.3.1 P80L on page 317.

8.15 Power Management I/F Channel 1 Configuration Registers (LDN=11h)

8.15.1 PMC1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	PMC1 Enable 1: Enable 0: Disable

8.15.2 PMC1 Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-3	Read only as "00000b"
2-0	Read/write , mapped as Base Address[10:8]

8.15.3 PMC1 Data Base Address LSB Register (Index=61h, Default=62h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.15.4 PMC1 Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-3	Read only as "00000b"
2-0	Read/write , mapped as Base Address[10:8]

8.15.5 PMC1 Command Base Address LSB Register (Index=63h, Default=66h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.15.6 PMC1 Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-0	Interrupt Level Select for PMC1 Please refer to Table 8-17. Interrupt Level Mapping Table.

8.16 Power Management I/F Channel 2 Configuration Registers (LDN=12h)

8.16.1 PMC2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	PMC2 Enable 1: Enable 0: Disable

8.16.2 PMC2 Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-3	Read only as "00000b"
2-0	Read/write , mapped as Base Address[10:8]

8.16.3 PMC2 Data Base Address LSB Register (Index=61h, Default=68h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.16.4 PMC2 Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-3	Read only as "00000b"
2-0	Read/write , mapped as Base Address[10:8]

8.16.5 PMC2 Command Base Address LSB Register (Index=63h, Default=6Ch)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.16.6 PMC2 Mailbox Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.16.7 PMC2 Mailbox Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-4	Read/write , mapped as Base Address[7:4]
3-0	Read only as "0000b"

8.16.8 PMC2 Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-0	Interrupt Level Select for PMC2 Please refer to Table 8-17. Interrupt Level Mapping Table.

8.16.9 General Purpose Interrupt (Index=F0h, Default=--h)

Bit	Description
7-4	Reserved
3	General Purpose Interrupt 3 (GPINT3) Writing 1 to this bit will issue an interrupt to INT35.
2	General Purpose Interrupt 2 (GPINT2) Writing 1 to this bit will issue an interrupt to INT34.
1	General Purpose Interrupt 1 (GPINT1) Writing 1 to this bit will issue an interrupt to INT33.
0	General Purpose Interrupt 0 (GPINT0) Writing 1 to this bit will issue an interrupt to INT32.

8.17 SMBus Configuration Registers (LDN=19h)

8.17.1 SMBus Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	SMBus Enable 1: Enable 0: Disable

8.17.2 SMBus ADDR Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-3	Read only as "00000b"
2-0	Read/write , mapped as Base Address[10:8]

8.17.3 SMBus ADDR Base Address LSB Register (Index=61h, Default=15h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.17.4 SMBus DATA Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-3	Read only as "00000b"
2-0	Read/write , mapped as Base Address[10:8]

8.17.5 SMBus DATA Base Address LSB Register (Index=63h, Default=16h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.17.6 SMBus Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-0	Interrupt Level Select for SMBus Please refer to Table 8-17. Interrupt Level Mapping Table.

8.17.7 SMBus Special Configuration Register (Index=76h, Default=00h)

Bit	Description
7-2	Reserved
1	Function Select of QFP:Pin-63, 64 (LQFP:Pin-60, 61) for SMBus Channel 0 0: Disable SMBUS0 1: Enable SMBUS0
0	Function Select of QFP:Pin-65, 66 (LQFP:Pin-62, 63) for SMBus Channel 2 0: Disable SMBUS2 1: Enable SMBUS2

Table 8-17. Interrupt Level Mapping Table

Value	Description
Fh-Dh	Not Valid
Ch	IRQ12
2h	Not Valid
1h	IRQ1
0h	No Interrupt Selected
Else	Not Valid

Table 8-18. Location Mapping Table

Location	Description
001 000	GP10
001 001	GP11
001 010	GP12
001 011	GP13
001 100	GP14
001 101	GP15
001 110	GP16
001 111	GP17
010 000	GP20
010 001	GP21
010 010	GP22
010 011	GP23
010 100	GP24
010 101	GP25
010 110	GP26
010 111	GP27
011 000	GP30
011 001	GP31
011 010	GP32
011 011	GP33
011 100	GP34
011 101	GP35
011 110	GP36
011 111	GP37
100 000	GP40
100 001	GP41
100 010	GP42
100 011	GP43
100 100	GP44
100 110	GP46
100 111	GP47
101 000	GP50
101 001	GP51
101 010	GP52
101 011	GP53
101 100	GP54
101 101	GP55
101 110	GP56
101 111	GP57
Else	Reserved

Table 8-19. DMA Channel Mapping Table

Value	Description
7h-5h	Invalid
4h	No DMA Channel Selected
3h	DMA3
2h	DMA2
1h	DMA1
0h	DMA0

9. Functional Description

9.1 LPC Interface

The IT8733 supports the peripheral side of the LPC I/F as described in the LPC Interface Specification Rev.1.1. In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK (the same as PCICLK.)), the IT8733 also supports LDRQ#, SERIRQ and PME#.

9.1.1 LPC Transactions

The IT8733 supports the required transfer cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will react according to the DMA requests from the DMA devices in the Super I/O modules, and decide whether to ignore the current transaction or not.

The ECP are 8-bit DMA devices, so if the LPC Host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and respond with an SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA device: the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to trace DMA requests quickly. Nevertheless, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there are at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and send those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8733 follows the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature, and is able to interface most PC chipsets. The IT8733 encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the Continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the turn-around state of the current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enters the Continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when the situation that one SIRQ Slave detects its input IRQn/events have been changed happens, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity = low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

Figure 9-1. Start Frame Timing

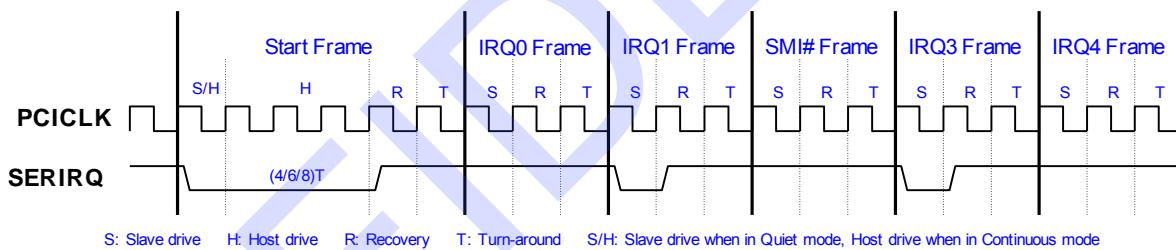
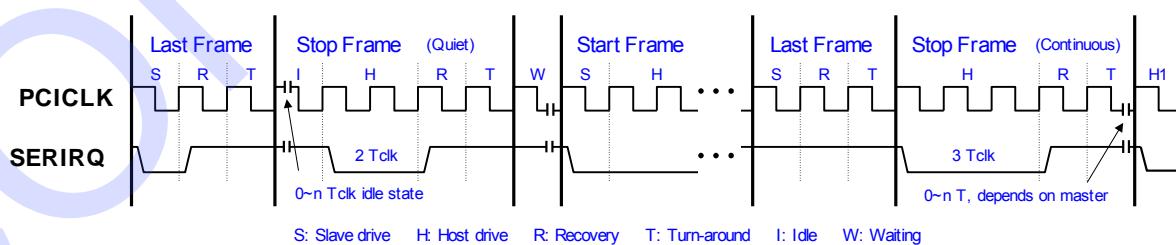


Figure 9-2. Stop Frame Timing



9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn/Events	#of Clocks Past Start	IT8733
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8733 provides nine sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index 25h, 26h, 27h, 28h and 29h of the Global Configuration Registers) are set. The GPIO functions include the simple I/O function and alternate function, and the function selection is determined by the Simple I/O Enable Registers (LDN=07h, Index=C0h, C1h, C2h, C3h and C4h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into eight registers. The accessed I/O ports are programmable and are eight consecutive I/O ports (Base Address+0, Base Address+1, Base Address+2, Base Address+3, Base Address+4, Base Address+5, Base Address+6, Base Address+7). Base Address is programmed on the registers of GPIO Simple I/O Base Address LSB and MSB registers (LDN=07h, Index=62h and 63h).

The Alternate function provides several special functions for users, including Watch Dog Timer, SMI# output routing, External Interrupt routing, Panel Button De-bounce, Keyboard Lock input routing, LED Blinking, Thermal output routing, and Beep output routing. The last two are sub-functions of the Hardware Monitor. (GPIO set 6, 7, 8 support the simple I/O function only.)

The Panel Button De-bounce is an input function. After it is enabled, a related status bit will be set when an active low pulse is detected on the GPIO pin. The status bits will be cleared by writing 1's to them. Panel Button De-bounce Interrupt will be issued if any of the status bit is set. However, the newly set status will not issue another interrupt unless the previous status bit is cleared before being set.

The Key Lock function locks the keyboard to inhibit the keyboard interface. The way of programming is to set bit 2 on the register Index F0h of KBC(Keyboard) (LDN=5). The pin location mapping, Index F7h also must be programmed correctly.

The Blinking function provides a low frequency blink output. By connecting to some external components, it can be used to control a power LED. There are several frequencies for selection.

The Watch Dog Timer (WDT) function is constituted by a time counter, a time-out status register, and the timer reset control logic. The time-out status bit may be mapped to an interrupt or KRST# through the WDT configuration register. The WDT has a programmable time-out ranging from 1 to 65535 minutes or 1 to 65535 seconds. The unit, either a minute or a second, is also programmable via bit 7 of the WDT configuration register. When the WDT Time-out Value register is set to a non-zero value, the WDT loads the value and begin counting down from the value. When the value reaches to 0, the WDT status register will be set. There are several system events including a CIR interrupt, a Keyboard Interrupt, a Mouse Interrupt that can reload the non-zero value into the WDT. The effect on the WDT for each of the events may be enabled or disabled through bits in the WDT control register. No matter what the value in the time counter is, the host may force a time-out to occur by writing a "1" to bit 1 of the WDT configuration register.

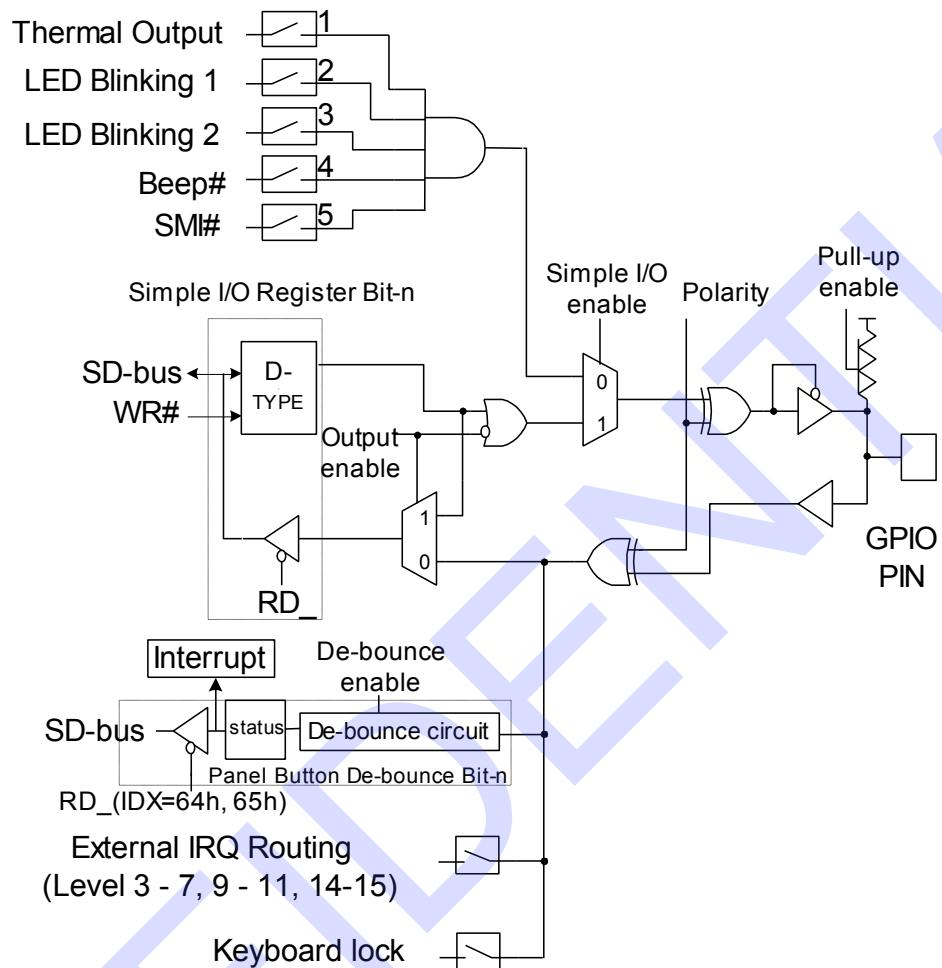
The External Interrupt routing function provides a useful feature for motherboard designers. Through this function, the parallel interrupts of other on-board devices can be easily re-routed into the Serial IRQ.

The SMI# is a non-maskable interrupt dedicated to the transparent power management. It consists of different enabled interrupts generated from each of the functional blocks in the IT8733. The interrupts are redirected as the SMI# output via the SMI# Control Register 1 and SMI# Control Register 2. The SMI# Status Register 1 and 2 are used to read the status of the SMI input event. All the SMI# Status Register bits can be cleared when the corresponding source events become invalidated. These bits can also be cleared by writing 1 to bit 7 of SMI# Control Register 2 no matter whether the events of the corresponding sources are invalidated or not. The SMI# events can be programmed as the pulse mode or level mode whenever an SMI# event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_EC and EC_SMI) or (EN_PBDIRQ or PBDIRQ) or (EN_KIRQ and KIRQ) or (EN_MIRQ and

MIRQ) or (EN_CIR and CIR_IRQ) or (EN_WDT and WDT_IRQ)

Figure 9-3. General Logic of GPIO Function



9.4 Advanced Power Supply Control and Power Management Event (PME#)

The circuit for advanced power supply control (APC) provides power-up events including Keyboard, Mouse, CIR and RI#. When any of these events is activated, PWRON# will perform a low state until VCC3 is switched to the ON state.

Here are the details of these events:

1. Detection of KCLK edge or special pattern of KCLK and KDAT. The special pattern of KCLK means pressing pre-set key string sequentially, and KDAT means pressing pre-set keys simultaneously.
2. Detection of MCLK edge or special pattern of MCLK and MDAT. The special pattern of MCLK and MDAT means clicking on any mouse button twice sequentially.
3. Receiving CIR pattern matches the previous one stored at the APC/PME Special Code Index and Data Register.
4. Detection of RI1# falling edge.

The PANSWH# and PSON# are especially designed for the system. PANSWH# serves as a main power switch input, which is wire-AND to the APC output PWRON#. PSON# is the ATX Power control output, which is a power-failure gating circuit. The power-failure gating circuit is responsible for gating the PSIN input until PANSWH# becomes active when the 3VSB is switched from OFF to ON.

The power-failure gating circuit can be disabled by setting the APC/PME Control Register 2 (LDN=04h, index F4h, bit 5). The gating circuit also provides an auto-restore function. After bit 5 of PCR1 is set, the previous PSON# state will be restored when the 3VSB is switched from OFF to ON.

The Mask PWRON# Activation bit (bit 4 of PCR 1) is used to mask all power-up events except switch-on event when the 3VSB state is just switched from FAIL to OFF. In other words, when this bit is set and the power state is switched from FAIL to OFF, the only validated function is PANSWH#.

The PCR2 register is responsible for determining the keyboard power-up event and APC conditions. Bit 4 is used to mask the PANSWH# power-on event on the PWRON# pin. To enable this bit, the keyboard power-up event should be enabled and set by (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously. The APC/PME# special code index and data registers are used to specify the special key codes in the special power-up events of (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously.

A CIR event is generated if the input CIR RX pattern is the same as that previously stored at PME Special Code Index and Data Registers (LDN=04h, Index=F5h and F6h). The total maximum physical codes are nineteen bytes (from Index 20h to 32h). The first byte (Index 20h) is used to specify the pattern length (in bytes). Bit 7-4 are used when VCC3 is on and Bit 3-0 when VCC3 goes OFF. The length represented in each 4-bit will be incremented by 3 internally as the actual length is to be compared. For most of the CIR protocols, the first several bytes are always the same for each key (or pattern). The differences are always in the last several bytes. Thus, the system designer can program the IT8733 to generate a CIR PME# event as any keys when VCC3 is ON and a special key (i.e. POWER-ON) when VCC3 is OFF.

All APC registers (Index=F0h, F2h, F4h, F5h, F6h, FAh and FBh) are powered by back-up power (VBAT) when 3VSB is OFF.

PME# is used to wake up the system from low-power states (S1-S5). There will be five events of APC to generate PME#. A falling edge on these pins issues PME# events if the enable bits are set.

9.5 Environment Controller

The Environment Controller (EC), built in the IT8733, includes seven voltage inputs, three temperature sensor inputs, four FAN Tachometer inputs, and four sets of advanced FAN Controllers. The EC monitors the hardware environment and implements the environmental control for personal computers.

The IT8733 contains an 8-bit ADC (Analog-to-Digital Converter), which is responsible for monitoring the voltages and temperatures. The ADC converts the analog inputs ranging from 0V to 2.8V (VREF) to 8-bit digital byte. With additional external components, the analog inputs can be made to monitor different voltage ranges, in addition to monitoring the fixed input range of 0V to 2.8V. Through external thermistors or thermal diodes, the temperature sensor inputs can be converted into 8-bit digital byte, enabling the sensor inputs to monitor the temperature of various components. A built-in ROM is also provided to adjust the non-linear characteristics of thermistors.

FAN Tachometer inputs are digital inputs with an acceptable range from 0V to 5V, and are responsible for measuring the FAN's Tachometer pulse periods.

The EC of the IT8733 provides multiple internal registers and an interrupt generator for programmers to monitor the environment and control the FANS. Both of the LPC Bus and Serial Bus interfaces are supported to accommodate the needs for various applications.

9.5.1 Interface

LPC Bus: The Environment Controller of the IT8733 decodes two addresses.

Table 9-1. Address Map on LPC Bus

Register or Port	Address
Address register of EC	Base+05h
Data register of EC	Base+06h

Note 1: The Base Address is determined by the Logical Device configuration registers of the Environment Controller (LDN=04h, registers index=60h, 61h).

To access an EC register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

uC Bus: The Environment Controller of the IT8733 can be accessed by uC. The base address is 2A00h. For example, to access SMI# Mask Register (Index = 04h), read or write data from or to the register via 2A04h.

9.5.2 Registers

9.5.2.1 Address Port (Base+05h, Default=00h)

Bit	Description
7	Outstanding; read only This bit is set when a data write is performed to Address Port via the LPC Bus.
6-0	Index Internal Address of RAM and Registers.

Table 9-2. Environment Controller Registers

Index	R/W	Default	Registers or Action
00h	R/W	18h	Configuration Register
01h	R	00h	Interrupt Status Register 1
02h	R	00h	Interrupt Status Register 2
03h	R	00h	Interrupt Status Register 3
04h	R/W	00h	SMI# Mask Register 1
05h	R/W	00h	SMI# Mask Register 2
06h	R/W	00h	SMI# Mask Register 3
07h	R/W	00h	Interrupt Mask Interrupt Mask 1
08h	R/W	00h	Interrupt Mask Interrupt Mask 2
09h	R/W	80h	Interrupt Mask Interrupt Mask 3
0Ah	R/W	44h	Interface Selection Register
0Bh	R/W	0Fh	Fan PWM Smoothing Step Frequency Selection Register
0Ch	R/W	00h	Fan Tachometer 16-bit Counter Enable Register
0Dh	R	-	Fan Tachometer 1 Reading Register
0Eh	R	-	Fan Tachometer 2 Reading Register
0Fh	R	-	Fan Tachometer 3 Reading Register
10h	R/W	-	Fan Tachometer 1 Limit Register
11h	R/W	-	Fan Tachometer 2 Limit Register
12h	R/W	-	Fan Tachometer 3 Limit Register
13h	R/W	07h	Fan Controller Main Control Register
14h	R/W	40h	FAN_CTL Control Register
15h	R/W	00h	FAN_CTL1 PWM Control Register
16h	R/W	00h	FAN_CTL2 PWM Control Register
17h	R/W	00h	FAN_CTL3 PWM Control Register
18h	R	-	Fan Tachometer 1 Extended Reading Register
19h	R	-	Fan Tachometer 2 Extended Reading Register
1Ah	R	-	Fan Tachometer 3 Extended Reading Register
1Bh	R/W	-	Fan Tachometer 1 Extended Limit Register
1Ch	R/W	-	Fan Tachometer 2 Extended Limit Register
1Dh	R/W	-	Fan Tachometer 3 Extended Limit Register
20h	R	-	VIN0 Voltage Reading Register
21h	R	-	VIN1 Voltage Reading Register
22h	R	-	VIN2 Voltage Reading Register
23h	R	-	VIN3 Voltage Reading Register
24h	R	-	VIN4 Voltage Reading Register
25h	R	-	VIN5 Voltage Reading Register
26h	R	-	VIN6 Voltage Reading Register
28h	R	-	VBAT Voltage Reading Register

Index	R/W	Default	Registers or Action
29h	R	-	TMPIN1 Temperature Reading Register
2Ah	R	-	TMPIN2 Temperature Reading Register
2Bh	R	-	TMPIN3 Temperature Reading Register
30h	R/W	-	VIN0 High Limit Register
31h	R/W	-	VIN0 Low Limit Register
32h	R/W	-	VIN1 High Limit Register
33h	R/W	-	VIN1 Low Limit Register
34h	R/W	-	VIN2 High Limit Register
35h	R/W	-	VIN2 Low Limit Register
36h	R/W	-	VIN3 High Limit Register
37h	R/W	-	VIN3 Low Limit Register
38h	R/W	-	VIN4 High Limit Register
39h	R/W	-	VIN4 Low Limit Register
3Ah	R/W	-	VIN5 High Limit Register
3Bh	R/W	-	VIN5 Low Limit Register
3Ch	R/W	-	VIN6 High Limit Register
3Dh	R/W	-	VIN6 Low Limit Register
3Eh	R/W	-	VIN7 High Limit Register
3Fh	R/W	-	VIN7 Low Limit Register
40h	R/W	-	TMPIN1 High Limit Register
41h	R/W	-	TMPIN1 Low Limit Register
42h	R/W	-	TMPIN2 High Limit Register
43h	R/W	-	TMPIN2 Low Limit Register
44h	R/W	-	TMPIN3 High Limit Register
45h	R/W	-	TMPIN3 Low Limit Register
50h	R/W	00h	ADC Voltage Channel Enable Register
51h	R/W	00h	ADC Temperature Channel Enable Register
52h	R/W	7Fh	TMPIN1 Thermal Output Limit Register
53h	R/W	7Fh	TMPIN2 Thermal Output Limit Register
54h	R/W	7Fh	TMPIN3 Thermal Output Limit Register
55h	R/W	40h	ADC Temperature Extra Channel Enable Register
56h	R/W	00h	Thermal Diode 1 Zero Degree Adjust Register
57h	R/W	00h	Thermal Diode 2 Zero Degree Adjust Register
58h	R	90h	ITE Vendor ID Register
59h	R/W	00h	Thermal Diode 3 Zero Degree Adjust Register
5Bh	R	12h	Core ID Register
5Ch	R/W	60h	Beep Event Enable Register
5Dh	R/W	00h	Beep Frequency Divisor of Fan Event Register
5Eh	R/W	00h	Beep Frequency Divisor of Voltage Event Register

Index	R/W	Default	Registers or Action
5Fh	R/W	00h	Beep Frequency Divisor of Temperature Event Register
60h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of OFF Register
61h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
62h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Register
63h	R/W	80h	FAN_CTL1 SmartGuardian Automatic Mode Start PWM Register
64h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Control Register
65h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Δ -Temperature Register
66h	R/W	0Fh	FAN_CTL1 Target Zone Register
68h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of OFF Register
69h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
6Ah	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Full Speed Register
6Bh	R/W	80h	FAN_CTL2 SmartGuardian Automatic Mode Start PWM Register
6Ch	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Control Register
6Dh	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Δ -Temperature Register
6Eh	R/W	0Fh	FAN_CTL2 Target Zone Register
70h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of OFF Register
71h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
72h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Full Speed Register
73h	R/W	80h	FAN_CTL3 SmartGuardian Automatic Mode Start PWM Register
74h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Control Register
75h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Δ -Temperature Register
76h	R/W	0Fh	FAN_CTL3 Target Zone Register
7Bh	R/W	80h	FAN_CTL4 Start PWM Register
80h	R	-	Fan Tachometer 4 Reading LSB Register
81h	R	-	Fan Tachometer 4 Reading MSB Register
84h	R/W	-	Fan Tachometer 4 Limit LSB Register
85h	R/W	-	Fan Tachometer 4 Limit MSB Register
88h	R/W	-00h	External Temperature Sensor Host Status Register
89h	R/W	00h	External Temperature Sensor Host Target Address Register
8Ah	R/W	00h	External Temperature Sensor Host Write Length Register
8Bh	R/W	00h	External Temperature Sensor Host Read Length Register
8Ch	R/W	00h	External Temperature Sensor Host Command (Write Data 1) Register

Index	R/W	Default	Registers or Action
8Dh	R/W	00h	External Temperature Sensor Write Data (2-8) Register
8Eh	R/W	02h	External Temperature Sensor Host Control Register
8Fh	R	--h	External Temperature Sensor Read Data (1-16) Register
90h	R/W	FFh	Special FAN Control Mode Extra Vector A Temperature Limit of Fan Start Register
91h	R/W	00h	Special FAN Control Mode Extra Vector A Slope Register
92h	R/W	00h	Special FAN Control Mode Extra Vector A Δ -Temperature Register
94h	R/W	FFh	Special FAN Control Mode Extra Vector B Temperature Limit of Fan Start Register
95h	R/W	00h	Special FAN Control Mode Extra Vector B Slope Register
96h	R/W	00h	Special FAN Control Mode Extra Vector B Δ -Temperature Register
98h	R/W	---00000b	PCH/AMDTSI Host Status Register
99h	R/W	00h	PCH/AMDTSI Host Target Address Register
9Ch	R/W	00h	PCH/AMDTSI Host Command Register
9Dh	R/W	--h	PCH/AMDTSI Write Data Register
9Eh	R/W	02h	PCH/AMDTSI Host Control Register
9Fh	R/W	--h	PCH/AMDTSI Read Data (1-16) Register

9.5.2.2 Register Description

9.5.2.2.1 Configuration Register (Index=00h, Default=58h)

Bit	R/W	Description
7	R/W	Initialization A “1” restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is “0”.
6	R/W	Update VBAT Voltage Reading 1: Not updated yet 0: Updated After writing 1 to Start (bit 0 of Configuration Register), this bit will be cleared to 0.
5	R/W	COPEN# Cleared Write “1” to clear COPEN#. Note: The COPEN# status register (Index 01h<bit4>) will be cleared when first writing this register and then reading Index 01h<bit4>.
4	R	Read only; always “1”
3	R/W	INT_Clear A “1” disables the SMI# and IRQ outputs while the contents of interrupt status bits remain unchanged.
2	R/W	IRQ Enable This bit is to enable the IRQ Interrupt output.
1	R/W	SMI# Enable A “1” enables the SMI# Interrupt output.
0	R/W	Start A “1” enables the startup of monitoring operations and a “0” sets the monitoring operation in the STANDBY mode.

9.5.2.2.2 Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-5	R	Reserved
4	R	COPEN# Status A “1” indicates a Case Open event has occurred. Note: The COPEN# status register (Index 01h<bit4>) will be cleared when first writing Index 00h<bit5> and then reading this register.
3-0	R	A “1” indicates the FAN_TAC4-1 Count limit has been reached.

9.5.2.2.3 Interrupt Status Register 2 (Index=02h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-0	R	A “1” indicates a High or Low limit of VIN7-0 has been reached.

9.5.2.2.4 Interrupt Status Register 3 (Index=03h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	R	Reserved
2-0	R	A “1” indicates a High or Low limit of Temperature 3-1 has been reached.

9.5.2.2.5 SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7	R/W	Reserved
6	R/W	Reserved
5	R/W	Reserved
4	R/W	A “1” disables the Case Open Intrusion interrupt status bit for SMI#.
3-0	R/W	A “1” disables the FAN_TAC4-1 interrupt status bit for SMI#.

9.5.2.2.6 SMI# Mask Register 2 (Index=05h, Default=00h)

Bit	R/W	Description
7-0	R/W	A “1” disables the VIN7-0 interrupt status bit for SMI#.

9.5.2.2.7 SMI# Mask Register 3 (Index=06h, Default=00h)

Bit	R/W	Description
7-3	R/W	Reserved
2-0	R/W	A “1” disables the Temperature 3-1 interrupt status bit for SMI#.

9.5.2.2.8 Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7	R/W	Reserved
6	R/W	Reserved
5	R/W	Reserved
4	R/W	A “1” disables the Case Open Intrusion interrupt status bit for IRQ.
3-0	R/W	A “1” disables the FAN_TAC4-1 interrupt status bit for IRQ.

9.5.2.2.9 Interrupt Mask Register 2 (Index=08h, Default=00h)

Bit	R/W	Description
7-0	R/W	A “1” disables the VIN7-0 interrupt status bit for IRQ.

9.5.2.2.10 Interrupt Mask Register 3 (Index=09h, Default=80h)

Bit	R/W	Description
7	R/W	A “1” disables the External Thermal Sensor interrupt.
6-3	R/W	Reserved
2-0	R/W	A “1” disables the Temperature 3-1 interrupt status bit for IRQ.

9.5.2.2.11 Interface Selection Register (Index=0Ah, Default=44h)

Bit	R/W	Description
7	R/W	Pseudo-EOC (End of Conversion of ADC) A Pseudo-EOC bit can speed up the setup time of FAN speed in the SmartGuardian automatic mode. (Write 1 to the bit then write 0.)
6	R/W	External Thermal Sensor SMB Host Enable 0: SMB Disable 1: SMB Enable
5-4	R/W	SST/PECI Selection 00: Disable 01: SST Slave Device 10: PECL 11: SST Host
3	R/W	SST/PECI Host Controller Clock Selection 0: 32MHz generated internally 1: 24MHz
2	R/W	SST/PECI Host Controller (Auto Speed No-change Tolerance) t-bit 1 Setting 0: (2 host clocks) no less than 1 host clock 1: (1 host clock) less than 1 host clock
1	R/W	SST/PECI Host Controller Transition Speed Mode Selection 0: Auto 1: Fixed at 666kHz
0	R/W	PECL2.0 Host Controller Hardware AWFCs Enable 0: Disable 1: Enable

9.5.2.2.12 Fan PWM Smoothing Step Frequency Selection Register (Index=0Bh, Default=0Fh)

Bit	R/W	Description
7-6	R/W	FAN PWM Smoothing Step Frequency Selection 00: 32Hz 01: 16Hz 10: 8Hz 11: 4Hz
5-4	R/W	Reserved Must be "00b"
3-2	R/W	Reserved
1-0	R/W	FAN_CTL4 Selection 00: The same as FAN_CTL1 01: The same as FAN_CTL2 10: The same as FAN_CTL3 11: None

9.5.2.2.13 Fan Tachometer 16-bit Counter Enable Register (Index=0Ch, Default=00h)

Bit	R/W	Description
7	R/W	TMPIN3 Enhanced Interrupt Mode Enable 0: Original mode 1: The interrupt will be generated when TMPIN3 is higher than the high limit or lower than the low limit.
6	R/W	TMPIN2 Enhanced Interrupt Mode Enable 0: Original mode 1: The interrupt will be generated when TMPIN2 is higher than the high limit or lower than the low limit.
5	R/W	Reserved
4	R/W	FAN_TAC4 Enable 0: Disable 1: Enable
3	R/W	TMPIN1 Enhanced Interrupt Mode Enable 0: Original mode 1: The interrupt will be generated when TMPIN1 is higher than the high limit or lower than the low limit.
2	R/W	FAN_TAC3 16-bit Counter Divisor Enable Always enabled
1	R/W	FAN_TAC2 16-bit Counter Divisor Enable Always enabled
0	R/W	FAN_TAC1 16-bit Counter Divisor Enable Always enabled

9.5.2.2.14 Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	R	Count Number of Internal Clock per Revolution

9.5.2.2.15 Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R/W	Limit Value

9.5.2.2.16 Fan Controller Main Control Register (Index=13h, Default=07h)

Bit	R/W	Description
7	R	Reserved
6-4	R/W	FAN_TAC3-1 Enable 0: Disable 1: Enable
3	R/W	Full Speed Control of FAN_CTL Automatic Mode 0: The full speeds of FAN_CTL1-3 automatic mode are independent. 1: All FAN_CTL1-3 will enter their respective full speeds when the temperature exceeds the full Speed Temperature Limit.
2-0	R/W	FAN_CTL3-1 Output Mode Selection 0: ON/OFF mode 1: SmartGuardian mode

9.5.2.2.17 FAN_CTL Control Register (Index=14h, Default=40h)

Bit	R/W	Description
7	R/W	FAN_CTL Polarity (for all FANs) 0: Active low 1: Active high
6-4	R/W	PWM Base Clock Select (for FAN1, 3) 000: 48MHz (PWM Frequency=187.5kHz) 001: 24MHz (PWM Frequency=93.75kHz) 010: 12MHz (PWM Frequency=46.87kHz) 011: 8MHz (PWM Frequency=31.25kHz) 100: 6MHz (PWM Frequency=23.43kHz) (Default) 101: 3MHz (PWM Frequency=11.7kHz) 110: 1.5MHz (PWM Frequency=5.86kHz) 111: 51kHz (PWM Frequency=200Hz)
3	R/W	PWM Minimum Duty Select (for FAN1, 3) 0: 0 % For a given PWM value, the actual duty is PWM/256 X 100%. 1: 20 % For a given PWM value (except 00h), the actual duty is (PWM+64)/320 X 100%. If the given PWM value is 00h, the actual duty will be 0%.
2-0	R/W	FAN_CTL ON/OFF Mode Control These bits are only available when the relative output modes are selected in the ON/OFF mode. 0: OFF 1: ON

9.5.2.2.18 FAN_CTL 1-3 PWM Control Register (Index=15h,16h,17h, Default=00h)

Bit	R/W	Description
7	R/W	FAN_CTL1-3 PWM Mode Automatic/Software Operation Selection 0: Software operation 1: Automatic operation
6-0	R/W	When bit 7 =0: Bit 7-0 of Index 63h, 6Bh, 73h: 256 Steps of PWM Control When in Software Operation When bit 7 =1: Bit 2: Tachometer Closed-loop Mode Enable Bit 0: Disable 1: Enable Bit 1-0: Temperature Input Selection 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved Bit 6-3: Reserved

9.5.2.2.19 Fan Tachometer 1-3 Extended Reading Registers (Index=18h-1Ah)

Bit	R/W	Description
7-0	R	Count Number of Internal Clock per Revolution [15:8]

9.5.2.2.20 Fan Tachometer 1-3 Extended Limit Registers (Index=1Bh-1Dh)

Bit	R/W	Description
7-0	R	Limit Value [15:8]

9.5.2.2.21 VIN6-0 Voltage Reading Registers (Index=26h-20h)

Bit	R/W	Description
7-0	R	Voltage Reading Value Note: For monitoring Internal A3VSB If LDN7, Index 2Ch<bit 0>=1, A3VSB voltage = VIN3 reading value * 2 * 12mV

9.5.2.2.22 3VSB Voltage Reading Registers (Index=27h)

Bit	R/W	Description
7-0	R	Internal 3VSB Voltage Reading Value The 3VSB voltage = reading value * 2 * 12mV

9.5.2.2.23 VBAT Voltage Reading Register (Index=28h)

Bit	R/W	Description
7-0	R	VBAT Voltage Reading Value Note: 1. Dynamic loading on VBAT will be enabled when both EC Index5Ch<Bit 7=1> and EC Index pointer is set to this register (28h). 2. The VBAT voltage = reading value * 2 * 12mV

9.5.2.2.24 TMPIN3-1 Temperature Reading Registers (Index=2Bh-29h)

Bit	R/W	Description
7-0	R	Temperature Reading Value

9.5.2.2.25 VIN7-0 High Limit Registers (Index=3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h)

Bit	R/W	Description
7-0	R/W	High Limit Value

9.5.2.2.26 VIN7-0 Low Limit Registers (Index=3Fh, 3Dh, 3Bh, 39h, 37h, 35h, 33h, 31h)

Bit	R/W	Description
7-0	R/W	Low Limit Value

9.5.2.2.27 TMPIN3-1 High Limit Registers (Index=44h, 42h, 40h)

Bit	R/W	Description
7-0	R/W	High Limit Value

9.5.2.2.28 TMPIN3-1 Low Limit Registers (Index=45h, 43h, 41h)

Bit	R/W	Description
7-0	R/W	Low Limit Value

9.5.2.2.29 ADC Voltage Channel Enable Register (Index=50h, Default=00h)

Bit	R/W	Description
7-0	R/W	ADC VIN7-0 Scan Enable

9.5.2.2.30 ADC Temperature Channel Enable Register (Index=51h, Default=00h)

TMPIN3-1 cannot be enabled in both Thermal Resistor mode and Thermal Diode (Diode connected Transistor) mode.

Bit	R/W	Description
7-6	R/W	SST/PECI Host Temperature Reading Report Register Selection 00: None 01: TMPIN1 Temperature Reading Register.(Index 29h) 10: TMPIN2 Temperature Reading Register.(Index 2Ah) 11: TMPIN3 Temperature Reading Register.(Index 2Bh)
5-3	R/W	TMPIN3-1 is enabled in the Thermal Resistor mode.
2-0	R/W	TMPIN3-1 is enabled in the Thermal Diode (or Diode-connected Transistor) mode.

9.5.2.2.31 TMPIN3-1 Thermal Output Limit Registers (Index=54h-52h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Thermal Output Limit Value

9.5.2.2.32 ADC Temperature Extra Channel Enable Register (Index=55h, Default=40h)

Bit	R/W	Description
7	R/W	PCH Temperature Mapping Enable Enable PCH temperature mapping to 2Ah for SMI-Link Function.
6-4	R/W	FAN_CTRL2 PWM Base Clock Select 000: 48MHz (PWM Frequency=187.5kHz) 001: 24MHz (PWM Frequency=93.75kHz) 010: 12MHz (PWM Frequency=46.87kHz) 011: 8MHz (PWM Frequency=31.25kHz) 100: 6MHz (PWM Frequency=23.43kHz) (Default) 101: 3MHz (PWM Frequency=11.7kHz) 110: 1.5MHz (PWM Frequency=5.86kHz) 111: 0.75MHz (PWM Frequency=2.93kHz)
3	R/W	FAN_CTRL2 PWM Minimum Duty Select 0: 0 % For a given PWM value, the actual duty is PWM/256 X 100%. 1: 20 % For a given PWM value (except 00h), the actual duty is (PWM+64)/320 X 100%. If the given PWM value is 00h, the actual duty will be 0%.
2	R/W	Reserved
1-0	R/W	VIN5-4 is enabled in the Thermal Resistor mode.

9.5.2.2.33 Thermal Diode Zero Degree Adjust 3-1 Registers (Index=59h, 57h, 56h, Default=00h)

These registers are read only unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	Thermal Diode Zero Degree Voltage Value

9.5.2.2.34 Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	R	ITE Vendor ID; read Only

9.5.2.2.35 Code ID Register (Index=5Bh, Default=12h)

Bit	R/W	Description
7-0	R	ITE Vendor ID; read Only

9.5.2.2.36 Beep Event Enable Register (Index=5Ch, Default=60h)

Bit	R/W	Description
7	R/W	Thermal Diode Zero Degree Adjust Register Write Enable
6-4	R/W	ADC Clock Selection 000: 500kHz 001: 250kHz 010: 125K 011: 62.5kHz 100: 31.25kHz 101: 24MHz 110: 1MHz(Default) 111: 2MHz
3	R/W	Reserved
2	R/W	This bit can enable the beep action when TMPINs exceed the limit
1	R/W	This bit can enable the beep action when VINs exceed the limit.
0	R/W	This bit can enable the beep action when FAN_TACs exceed the limit.

9.5.2.2.37 Beep FrequencyDivisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone Divisor Tone=500/(bits[7:4]+1)
3-0	R/W	Frequency Divisor Frequency=10K/(bits[3:0]+1)

9.5.2.2.38 Beep FrequencyDivisor of Voltage Event Register (Index=5Eh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone Divisor Tone=500/(bits[7:4]+1).
3-0	R/W	Frequency Divisor Frequency=10K/(bits[3:0]+1)

9.5.2.2.39 Beep FrequencyDivisor of Temperature Event Register (Index=5Fh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone Divisor Tone=500/(bits[7:4]+1)
3-0	R/W	Frequency Divisor Frequency=10K/(bits[3:0]+1)

9.5.2.2.40 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of OFF Registers (Index=70h, 68h, 60h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan OFF

9.5.2.2.41 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers (Index=71h, 69h, 61h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan Start

9.5.2.2.42 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers (Index=72h, 6Ah, 62h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan Full Speed

9.5.2.2.43 FAN_CTL3-1 SmartGuardian Automatic Mode Start PWM Registers (Index=73h, 6Bh, 63h, Default=80h)

For Original Fan Control Mode:

Bit	R/W	Description
7-0	R/W	When bit 7 of index 15h, 16h, 17h =0: 256 Steps of PWM Control When in Software Operation When bit 7 of index 15h, 16h, 17h =1: PWM Value

For Tachometer Closed-loop Mode:

Bit	R/W	Description
7-0	R/W	Initial Value of Target RPM RPM = 16 * Bit[7:0]

9.5.2.2.44 FAN_CTL3-1 SmartGuardian Automatic Mode Control Registers (Index=74h, 6Ch, 64h, Default=00h)

For Original Fan Control Mode:

Bit	R/W	Description
7	R/W	FAN Smoothing This bit enables the FAN PWM smoothing change. 0: Disable 1: Enable
6-0	R/W	Slope PWM Bit[6:0] Slope = (Slope PWM bit[6:3] + Slope PWM bit[2:0] / 8) PWM value/°C

For Tachometer Closed-loop Mode:

Bit	R/W	Description
5-0	R/W	Slope of Target RPM Slope = 8 * Bit[5:0] (RPM/°C)

9.5.2.2.45 FAN_CTL3-1 SmartGuardian Automatic Mode △-Temperature Registers (Index=75h, 6Dh, 65h, Default=00h)

Bit	R/W	Description
7	R/W	Direct-Down Control This bit is to determine the PWM linear changing decreasing mode. 0: Slow decreasing mode 1: Direct decreasing mode
6	R/W	FAN Full Limit Control as Thermal out Reached When the relevant enable bit is set and the FAN output mode is selected as Automatic mode by bit7 of EC index 15h, 16h, 17h, the corresponding FAN output will be forced to full PWM if any thermal output limit is reached. 0: Disable 1: Enable
5	-	Reserved
4-0	R/W	△-Temperature Interval [4:0]

9.5.2.2.46 FAN_CTL3-1 Target Zone Registers (Index=76h, 6Eh, 66h, Default=0Fh)

For Tachometer Closed-loop Mode:

Bit	R/W	Description
3-0	R/W	Target Zone Boundary Target Zone = Target RPM +/- (8 * bit[3:0]) (RPM/°C)

9.5.2.2.47 FAN_CTL4 Start PWM Register (Index=7Bh Default=80h)

For Original Fan Control Mode:

Bit	R/W	Description
7-0	R/W	256 Steps of PWM Control

9.5.2.2.48 Fan Tachometer 4 Reading LSB Registers (Index=80h)

Bit	R/W	Description
7-0	R	Count Number of Internal Clock per Revolution

9.5.2.2.49 Fan Tachometer 4 Reading MSB Registers (Index=81h)

Bit	R/W	Description
7-0	R	Count Number of Internal Clock per Revolution

9.5.2.2.50 Fan Tachometer 4 Limit LSB Registers (Index=84h)

Bit	R/W	Description
7-0	R/W	Limit Value

9.5.2.2.51 Fan Tachometer 4 Limit MSB Registers (Index=85h)

Bit	R/W	Description
7-0	R/W	Limit Value

9.5.2.2.52 External Temperature Sensor Host Status Register (Index=88h, Default= -00h)

Bit	R/W	Description
7	R/W	Data FIFO Pointer Clear Writing 1 clears the Read/Write Data FIFO pointers. 0: No action It always reports 0 when reading it. 1: Both Read and Write Data FIFO pointers cleared Read Data register will point to Read Data 1, and Write Data register will point to Write Data 2.
6	R/WC	SST Bus Abnormal/Contention Error This bit reports the SST/PECI line status. 0: No error 1: Abnormal/Contention error
5	R/WC	SST Slave Message Phase t-bit Extend over Error/SST or PECL Received Error Code This bit reports the SST/PECI line status and received error code (8000h-81FFh). 0: No error 1: Error found
4	R/WC	SST/PECI Line High-Z Status/Failed This bit reports the SST/PECI line High-Z status. 0: SST/PECI line does not drive High-Z. 1: SST/PECI line drives High-Z.
3	R/WC	Write_FCS_ERR Writing 1 clears this bit. In the SST/PECI mode, it reports Write FCS error and it cannot work in the AMDTSI mode. 0: No Error 1: Write FCS error
2	R/WC	NotValid/Read_FCS_ERR Writing 1 clears this bit. In the AMDTSI mode, it reports the valid bit of Data phase. If this bit is 0(valid data =0), the data is valid. In the SST/PECI mode, it reports Read FCS error. 0: No Error 1: Read FCS error
1	R/WC	Finish (FNSH) Writing 1 clears this bit. 0: None 1: This bit is set when the stop condition is detected.
0	R	Host Busy (BUSY) 0: The current transaction is completed. 1: This bit is set while the command is in operation.

9.5.2.2.53 External Temperature Sensor Host Target Address Register (Index=89h, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Target Address Register (HAddr [7:0]) This register is the Target Address field of the SST/PECI protocol.

9.5.2.2.54 External Temperature Sensor Host Write Length Register (Index=8Ah, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Write Length Register (HW_length [7:0]) This register is the Write Length field of the SST/PECI protocol.

9.5.2.2.55 External Temperature Sensor Host Read Length Register (Index=8Bh, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Read Length Register (HR_length [7:0]) This register is the Read Length field of the SST/PECI protocol.

9.5.2.2.56 External Temperature Sensor Host Command (Write Data 1) Register (Index=8Ch, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Command Register (HCMD [7:0]) This register is the command field of the protocol. In the PECI/SST mode, it is the command (W/rte Data 1) byte. In the AMDTSI mode, it is the Command field. If the host controller is busy, the value of this register cannot be changed or the host will send the wrong command. If the value is out of definition (for example, 03h to FFh for AMDTSI protocol), the host will transfer it into the normal value and no error will be detected by the host controller.

9.5.2.2.57 External Temperature Sensor Write Data (2-8) Register (Index=8Dh, Default=--h)

Bit	R/W	Description
7-0	R/W	Write Data (2-8) [7:0] (in SST/PECI mode) This is a 16-byte FIFO register, which is only valid in the PECI/SST mode.

9.5.2.2.58 External Temperature Sensor Host Control Register (Index=8Eh, Default=02h)

Bit	R/W	Description
7-6	R/W	Auto-Start Control (Auto-START) The host will start the transaction in a regular rate automatically. 00: 32 Hz 01: 16 Hz 10: 8 Hz 11: 4 Hz
5	R/W	Auto-Start (Auto-START) 0: Disable 1: Enable The host will start the transaction in a regular rate, which is determined by bit [6:5] automatically.
4	R/W	SST/PECI Host Auto-abort at FCS Error This bit enables the SST/PECI host to abort the transaction when an error occurs to FCS. 0: Disable 1: Enable
3	R/W	Auto-Start Two-Domain Enable 0: One-Domain 1: Two-Domain
2	R/W	SST Contention Control/AMDTSI Clock Selection This bit enables the SST bus contention control. 0: Disable (100 kbits/s) 1: Enable (400 kbits/s) When the SST bus is contentious, the host will abort the transaction.

Bit	R/W	Description
1	R/W	SST_Idle_High/AMDTSI_Byt Sel This bit sets the SST bus idle-high in the SST host mode, or selects 8/16 bit data in the AMDTSI mode. 0: SST Idle Low/AMDTSI 8-bit data 1: SST Idle High/AMDTSI 16-bit data
0	R/W	Start (START) This bit is write-only. Writing 0 to it during transaction will issue a "kill process" and bit 4 of 8Bh register will be set. Writing 1 to it during the "NOT BUSY" state (bit 0 of 88h = 0) will start a transaction. Writing 1 to it during the "BUSY" state (bit 0 of 88h = 1) will not issue any transaction. So, the programmer should check the "BUSY" status before issuing a transaction. 0: This bit always returns 0 at read. 1: When this bit is set, the host controller will perform the transaction.

9.5.2.2.59 External Temperature Sensor Read Data (1-16) Register (Index=8Fh, Default=--h)

Bit	R/W	Description
7-0	R/W	Read Data (1-16) [7:0] This is a 32-byte FIFO register.

9.5.2.2.60 Special FAN Control Mode Extra Vector A, B Temperature Limit of Fan Start Registers (Index=90h, 94h, Default=FFh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan Start

9.5.2.2.61 Special FAN Control Mode Extra Vector A, B Slope Registers (Index=91h, 95h, Default=00h)

For Original Fan Control Mode:

Bit	R/W	Description
7	R/W	Temperature Input Select 0 Please refer to the description of Special FAN Control Mode Extra Vector A, B △-Temperature Registers for the detail.
6-0	R/W	Slope PWM Bit[6:0] Slope = (Slope PWM bit[6:3] + Slope PWM bit[2:0] / 8) PWM value/°C

For Tachometer Closed-Loop Mode:

Bit	R/W	Description
7	R/W	Reserved
6-0	R/W	Slope of Extra A and B RPM Slope = 8 * Bit[6:0] (RPM/°C)

9.5.2.2.62 Special FAN Control Mode Extra Vector A, B \triangle -Temperature Registers (Index=92h, 96h, Default=00h)

Bit	R/W	Description
7	R/W	Temperature Input Select 1 For Temperature Input Select 0, please refer to bit 7 of Special FAN Control Mode Extra Vector A, B Slope Registers. 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved
6-5	R/W	Target FAN Select These bits are to determine the target FAN to be added for extra vector. 00: None 01: FAN1 10: FAN2 11: FAN3
4-0	R/W	\triangle -Temperature Interval [4:0]

9.5.2.2.63 PCH/AMDTSI Host Status Register (Index=98h, Default=---00000b)

Bit	R/W	Description
7	R/W	Data FIFO Pointer Clear Writing 1 clears the Read/Write Data FIFO pointers. 0: No action It always reports 0 when reading it. 1: Both Read and Write Data FIFO pointers cleared Read Data register will point to Read Data 1, and Write Data register will point to Write Data 2.
6	R/W	Bus Selection This bit selects the SMB host protocol. 0: PCH 1: AMDTSI
5	R/WC	Reserved
4	R/WC	Transmission Killed
3	R/WC	Bus Error 0: No Error 1: Error
2	R/WC	Data Valid Writing 1 clears this bit. In the AMDTSI mode, it reports the valid bit of Data phase. If this bit is set to 0 (valid data =0), the data is valid. In the SST/PECI mode, it reports Read FCS error. 0: Data valid 1: Data invalid
1	R/WC	Finish (FNSH) Writing 1 clears this bit. 0: None 1: This bit is set when the stop condition is detected.
0	R	HOST Busy (BUSY) 0: The current transaction is completed. 1: This bit is set while the command is in operation.

9.5.2.2.64 PCH/AMDTSI Host Target Address Register (Index=99h, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Target Address Register (HAddr [7:0]) This register is the Target Address field of the PCH/AMDTSI protocol.

9.5.2.2.65 PCH/AMDTSI Host Command Register (Index=9Ch, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Command Register (HCMD [7:0]) This register is the command field of the protocol. In the AMDTSI mode, it is the Command field. If the host controller is busy, the value of this register cannot be changed or the host will send the wrong command. If the value is out of definition (for example, 03h to FFh for AMDTSI protocol), the host will transfer it into the normal value and no error will be detected by the host controller.

9.5.2.2.66 PCH/AMDTSI Write Data Register (Index=9Dh, Default=--h)

Bit	R/W	Description
7-0	R/W	Write Data This is a 16-byte FIFO register.

9.5.2.2.67 PCH/AMDTSI Host Control Register (Index=9Eh, Default=02h)

Bit	R/W	Description
7-6	R/W	Auto-Start Control (Auto-START) The host will start the transaction in a regular rate automatically. 00: Disable auto-start 01: 16 Hz 10: 8 Hz 11: 4 Hz
5-4	R/W	For AMDTSI Temperature Reading Report Register Selection 00: None 01: Index 29h (TMPIN1) 10: Index 2Ah (TMPIN2) 11: Index 2Bh (TMPIN3) For SM-Link Max. Temperature of CPU or MCH Reading Report Register Selection 01: Index 29h 11: Index 2Bh For SM-Link PCH Temperature Reading Report Register Selection 00: Index 2Ah, if 9Eh<1>=1.
3	R/W	Reserved
2	R/W	AMDTSI Clock Selection 0: 100 kbits/s 1: 400 kbits/s
1	R/W	AMDTSI_byte_sel/PCH EC IBX Temp Report to 2Ah This bit selects 8/16-bit data in the AMDTSI mode. 0: AMDTSI 8-bit data/disabled 1: AMDTSI 16-bit data/enabled

Bit	R/W	Description
0	R/W	<p>Start (START)</p> <p>This bit is write-only. Writing 0 to it during transaction will issue a “kill process” and bit 4 of 88h register will be set. Writing 1 to it during the “NOT BUSY” state (bit 0 of 88h = 0) will start a transaction. Writing 1 to it during the “BUSY” state (bit 0 of 88h = 1) will not issue any transaction. So, the programmer should check the “BUSY” status before issuing a transaction.</p> <p>0: This bit always returns 0 at read. 1: When this bit is set, the host controller will perform the transaction.</p>

9.5.2.2.68 PCH/AMDTSI Read Data (1-16) Register (Index=9Fh, Default=--h)

Bit	R/W	Description
7-0	R/W	<p>Read Data (1-16) [7:0]</p> <p>This is a 21-byte FIFO register.</p>

9.5.3 Operation

9.5.3.1 Power on Reset and Software Reset

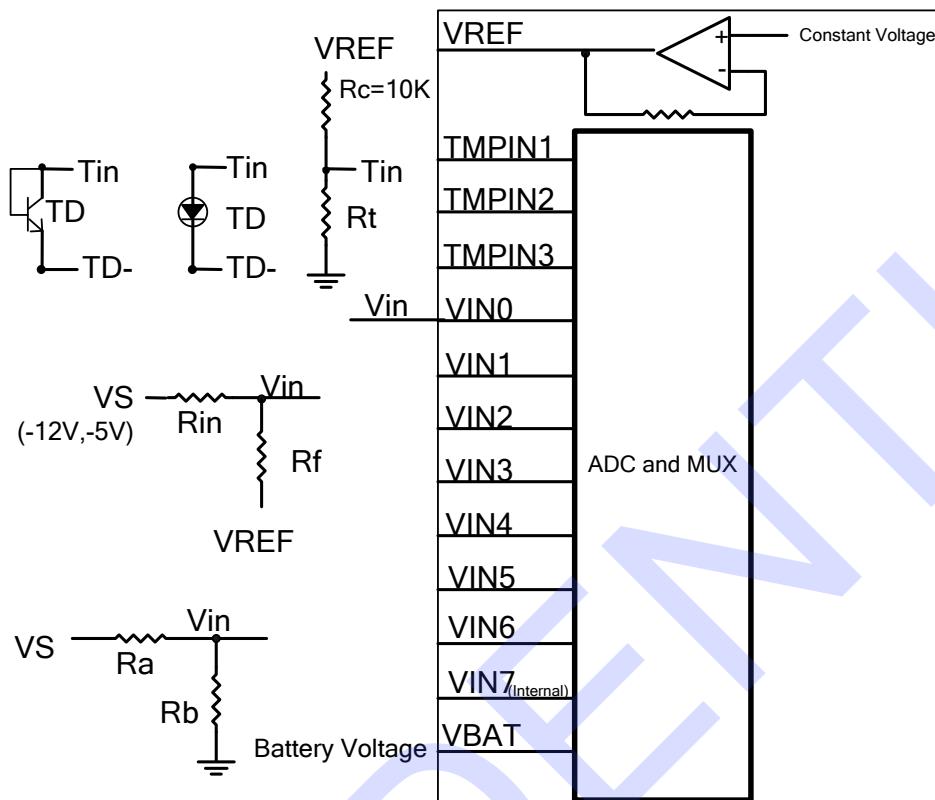
When the system power is first applied, the Environment Controller performs “power on reset” on the registers, making them return to their individual default values during a system hardware reset, and the EC will acquire a monitored value before it goes inactive. The ADC is activated to monitor the VBAT pin and then goes inactive. A software reset through bit 7 of Configuration Register (Index=00h, Default=58h) (refer to page 101) performs the same functions as the hardware reset except the function of the Serial Bus Interface Address register.

9.5.3.2 Starting Conversion

The monitoring function in the EC is activated when bit 3 of Configuration Register is cleared (low) and bit 0 of Configuration Register is set (high). Otherwise, this function will be enabled by setting several enabled bits, which are categorized into three groups, positive voltages, temperatures and FAN Tachometer inputs. Before the EC monitoring function is able to be executed then the monitoring process can then be started.

1. Set the limits.
2. Set the interrupt masks.
3. Set the enable bits.

Figure 9-4. Application Example



Note: The resistor should provide approximately 2V at the Analog Inputs.

9.5.3.3 Voltage and Temperature Inputs

The 8-bit ADC has a 10.9mV LSB with an input range from 0V to 2.8V. The 2.5V supplies of PC applications can be directly connected to the inputs. When the input voltage is great than 2.8V. It is necessary to divide the input voltage into an acceptable range. When the divided circuit is used to measure the positive voltage, the recommended range for Ra and Rb is from 10K Ω to 100K Ω . The negative voltage can be measured by the same divider, which is connected to VREF (constant voltage, 2.8V), and do not attempt to measure it with the divider connected to the ground. The EC temperature measurement system converts the voltage of the TMPINs to 8-bit two's-complement. The system also includes an OP amp providing a constant voltage, an external thermistor, a constant resistance, the ADC and a conversion table ROM.

Temperature	Digital Output Format	
	Binary	Hex
+ 125°C	01111101	7Dh
+ 25°C	00011001	19h
+ 1°C	00000001	01h
+ 0°C	00000000	00h
- 1°C	11111111	FFh
- 25°C	11100111	E7h
- 55°C	11001001	C9h

With the addition of the external application circuit, the actual voltages are calculated below:

Positive Voltage: $V_s = V_{in} \times (R_a + R_b) / R_b$

Negative Voltage: $V_s = (1 + R_{in}/R_f) \times V_{in} - (R_{in}/R_f) \times V_{REF}$

All the analog inputs are equipped with the internal diodes that clamp the input voltage exceeding the power supply and ground; nevertheless, the current limiting input resistor is recommended since no dividing circuit is available.

9.5.3.4 Layout and Grounding

A separate and low-impedance ground plane for analog ground is essential to achieve accurate measurement. The analog ground also provides a ground point for the voltage dividers including the temperature loops and analog components. Analog components such as voltage dividers, feedback resistors and the constant resistors of the temperature loops should be located as closely as possible to the IT8733. However, the thermistors of the temperature loops should be positioned within the measuring area. In addition, the power supply bypass and the parallel combination of $10\mu F$ and $0.1\mu F$ bypass capacitors connected between A3VSB and analog ground also needs to be located as closely as possible to the IT8733.

Due to the small differential voltage of thermal diode (diode-connected transistor), it is necessary to adhere to the steps below for PCB layout.

- Position the sensor as closely as possible to the EC.
- The sensor ground should be directly shorted to GNDA with excellent noise immunity.
- Keep traces away from any noise sources. (High voltage, fast data bus, fast clock, CRTs ...)
- Use trace width of 10 mil minimum and provide guard ground (flanking and under).
- Position $0.1\mu F$ bypass capacitors as closely as possible to IT8733.

9.5.3.5 Fan Tachometer

The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit or 16-bit counter (maximum count=255 or 65535) for one period of the input signals. Counts are based on two pulses per revolution for tachometer output.

$$RPM = 1.35 \times 10^6 / (\text{Count} \times \text{Divisor}) ; (\text{Default Divisor} = 2)$$

The maximum input signal range is from 0 to VCC. An additional external circuit is needed to clamp the input voltage and current.

9.5.3.6 Interrupt of the EC

The EC generates interrupts as a result of each of its Limit registers on the analog voltage, temperature, and FAN monitor. All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled by Configuration Register (Index=00h, Default=58h) (refer to page 101). The Interrupt Status Registers will be reset after a read operation. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. It takes EC 1.5 seconds to allow all the EC Registers to be safely updated between completed read operations. When bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume after this bit is cleared.

All analog voltage inputs have both high and low Limit Registers to generate interrupts whereas FAN monitoring inputs only have low Limit Register to warn the host. The IT8733 provides three modes dedicated to temperature interrupts in the EC: "Interrupt" mode, "Enhanced Interrupt" mode and "Comparator" mode.

Interrupt Mode

An interrupt will be generated whenever the temperature exceeds Th limit, and the corresponding interrupt status bits will be set to high until being reset by reading Interrupt Status Register 3 (Index=03h, Default=00h)

(refer to page 102). Once an interrupt event occurs by exceeding Th limit, an interrupt will only occur again when the temperature goes below TL limit after being reset. Again, it will set the corresponding status bit to high until being reset by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 102).

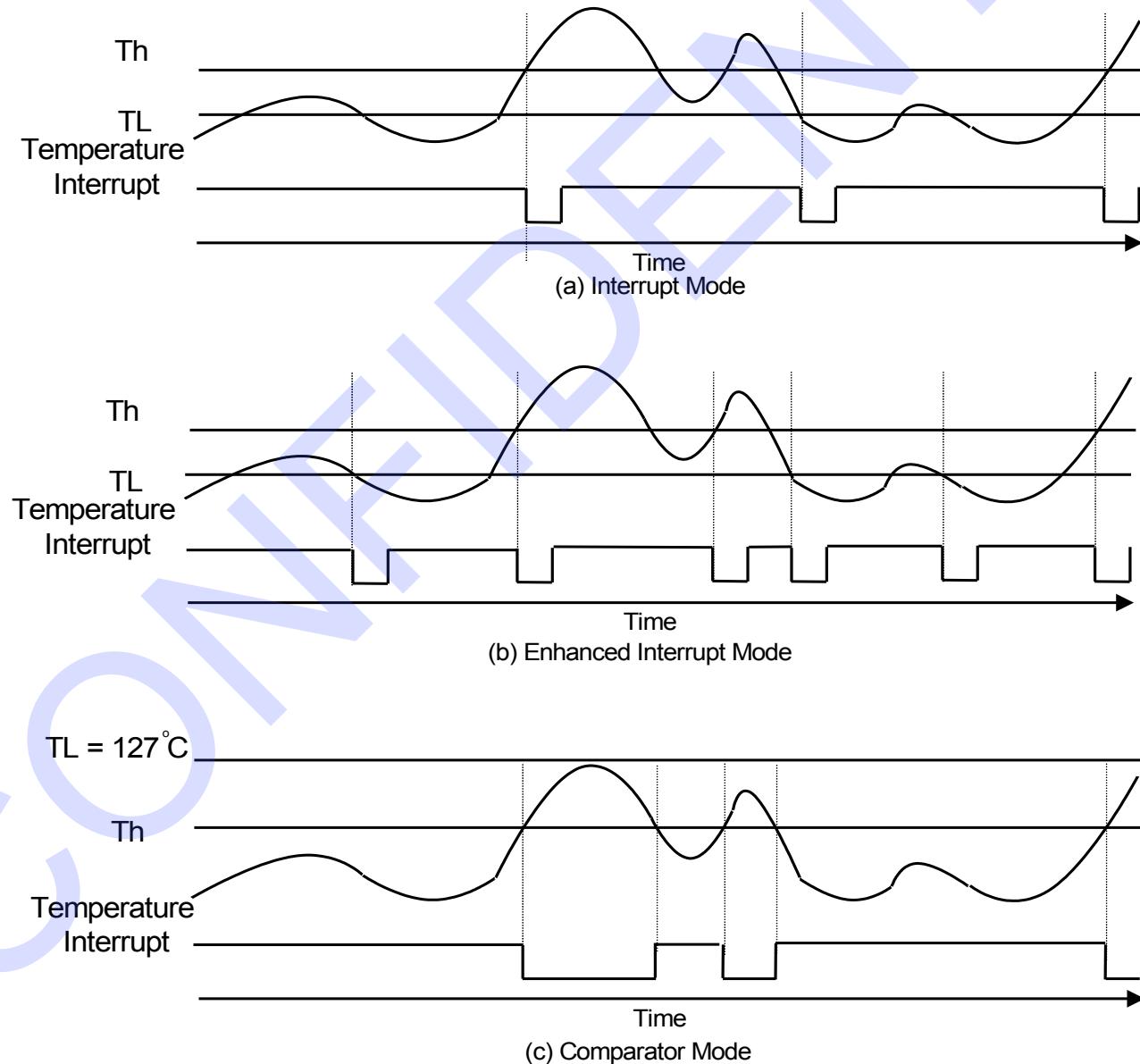
Enhanced Interrupt Mode

When the enhanced interrupt mode is enabled (bit 3, 6 and 7 of Fan Tachometer 16-bit Counter Enable Register (Index=0Ch, Default=00h) for TMPIN1, 2, and 3 respectively) (refer to page 104), an interrupt will be generated when the temperature is higher than the high limit or lower than the low limit.

Comparator Mode

This mode is entered when the TL limit register is set to 127°C. In this mode, an interrupt will be generated whenever the temperature exceeds the Th limit. The interrupt will also be cleared by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 102), but the interrupt will be set again following the completion of another measurement cycle. It will remain set until the temperature goes below the Th limit.

Figure 9-5. Temperature Interrupt Response Diagram



9.5.3.7 FAN Controller FAN_CTL's ON-OFF and SmartGuardian Modes

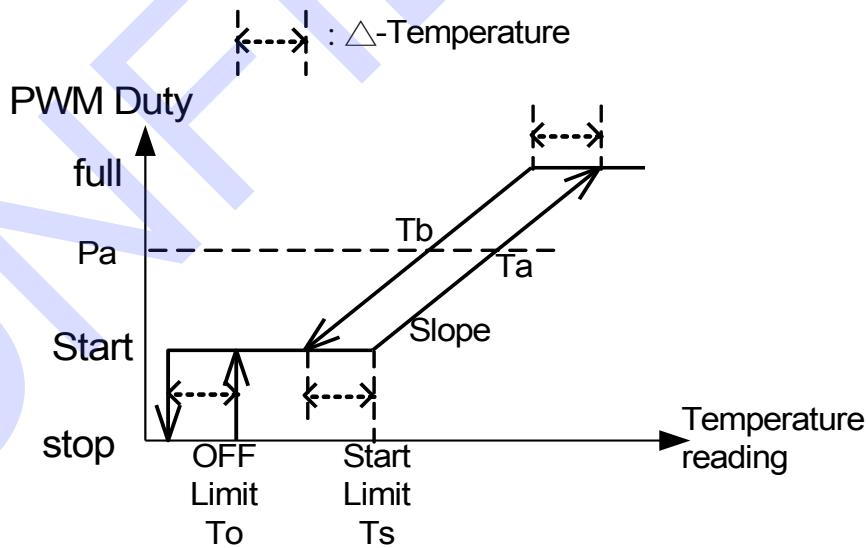
The IT8733 provides an advanced FAN Controller. Two modes, ON/OFF and SmartGuardian, are provided for each controller. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application circuits, the FAN's voltage values can be varied easily.

In the SmartGuardian Mode, there are two operational choices, software control or automatic control.

While under software control, the PWM value is subject to the changes in the values of bit 6-0 of FAN_CTL 1-3 PWM Control Registers (Index=15h, 16h, 17h). With the application circuits, FAN_CTL can generate 128 steps of voltage. So, the FAN_CTL 1-3 PWM Control Registers can vary the voltage by changing the PWM value. Fan speeds or other voltage control cooling device can be varied in 128 steps.

While under automatic mode, the PWM value is subject to the temperature inputs by linear changes. When the temperature exceeds a start limit, FAN_CTL spins in a start PWM value (Index 73h, 6Bh, 63h). When the temperature reading is between the Start limit and the full limit ($=Ts + (128 - \text{Start PWM})/\text{Slope}$), the PWM value changes depending on the temperature reading if the reading exceeds the right boundary. If the temperature increases $X^{\circ}\text{C}$, the PWM value will increase $X * K$. K (Slope) is a constant value with 4 bits for the integer and 3 bits for the decimal, and is determined by bit 7 of FAN_CTL 3-1 SmartGuardian Automatic mode Start PWM register and bit 5-0 of FAN_CTL 3-1 SmartGuardian Automatic mode control registers. However, if the reading doesn't exceed the right boundary, the PWM value will keep the original value. For example, if PWM is currently at a value of Pa , it will not change if $Tb < \text{temperature reading} < Ta$. If the new reading (T_{new}) $> Ta$, the new PWM value will be Start PWM + $K * (T_{\text{new}} - Ts)$. If the new reading $< Tb$, there are two decreasing modes. If bit 7 of FAN_CTL 3-1 SmartGuardian Automatic mode \triangle -Temperature is 0, the new PWM value will be Start PWM + $K * ((T_{\text{new}} + Ta)/2 - Ts)$. If the bit is 1, the new PWM value will be Start PWM + $K * (T_{\text{new}} - Ts)$. When the temperature is lower than the start limit but larger than the OFF limit (Index 70h, 68h, 60h), FAN_CTL will not stop, but keep in the start PWM value until the temperature is lower than the OFF limit.

Figure 9-6. SmartGuardian Automatic Mode



9.5.3.8 External Thermal Sensor Programming Procedure

Figure 9-7. PCH SMLink Programming Procedure

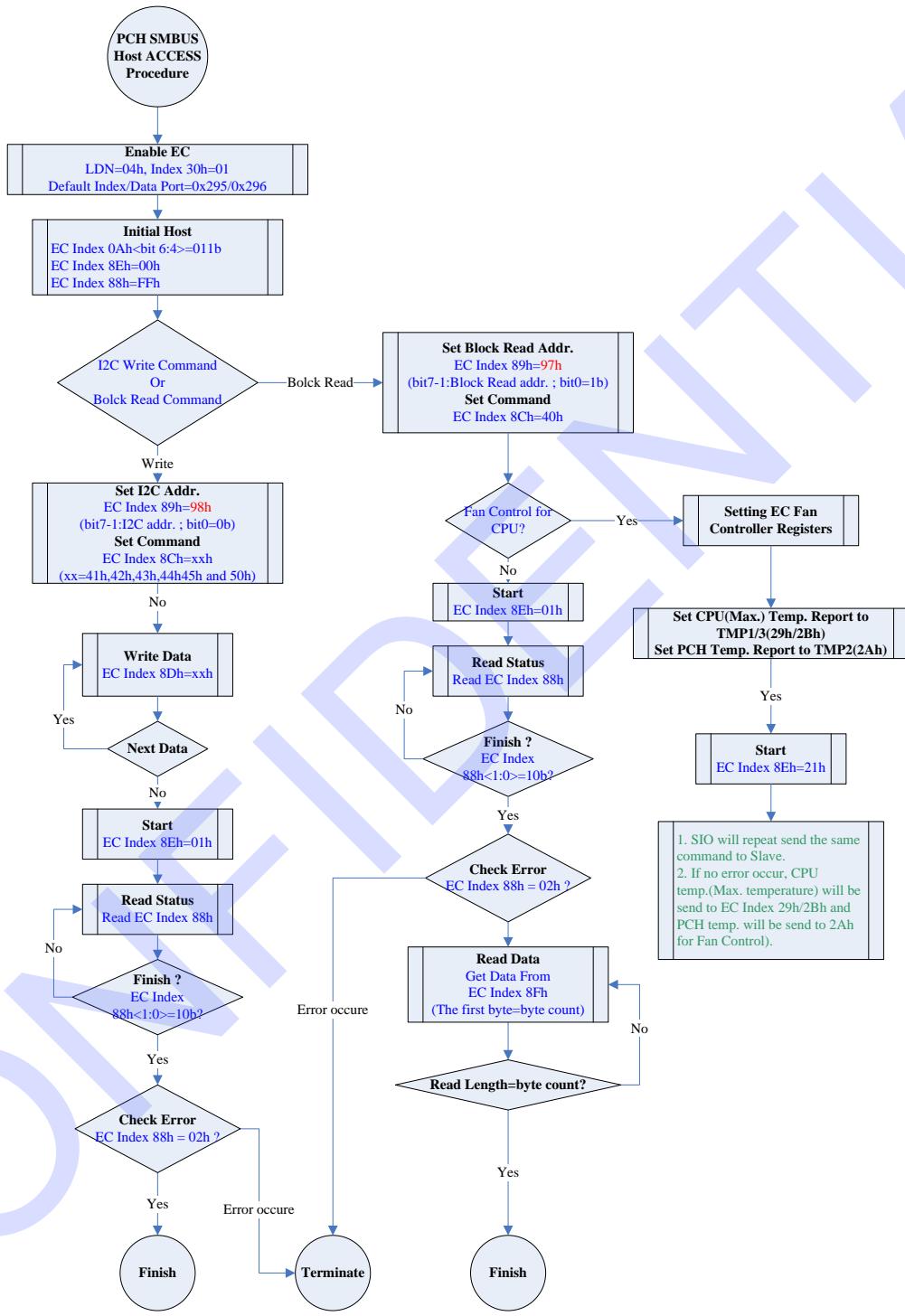


Figure 9-8. SST Host Programming Procedure

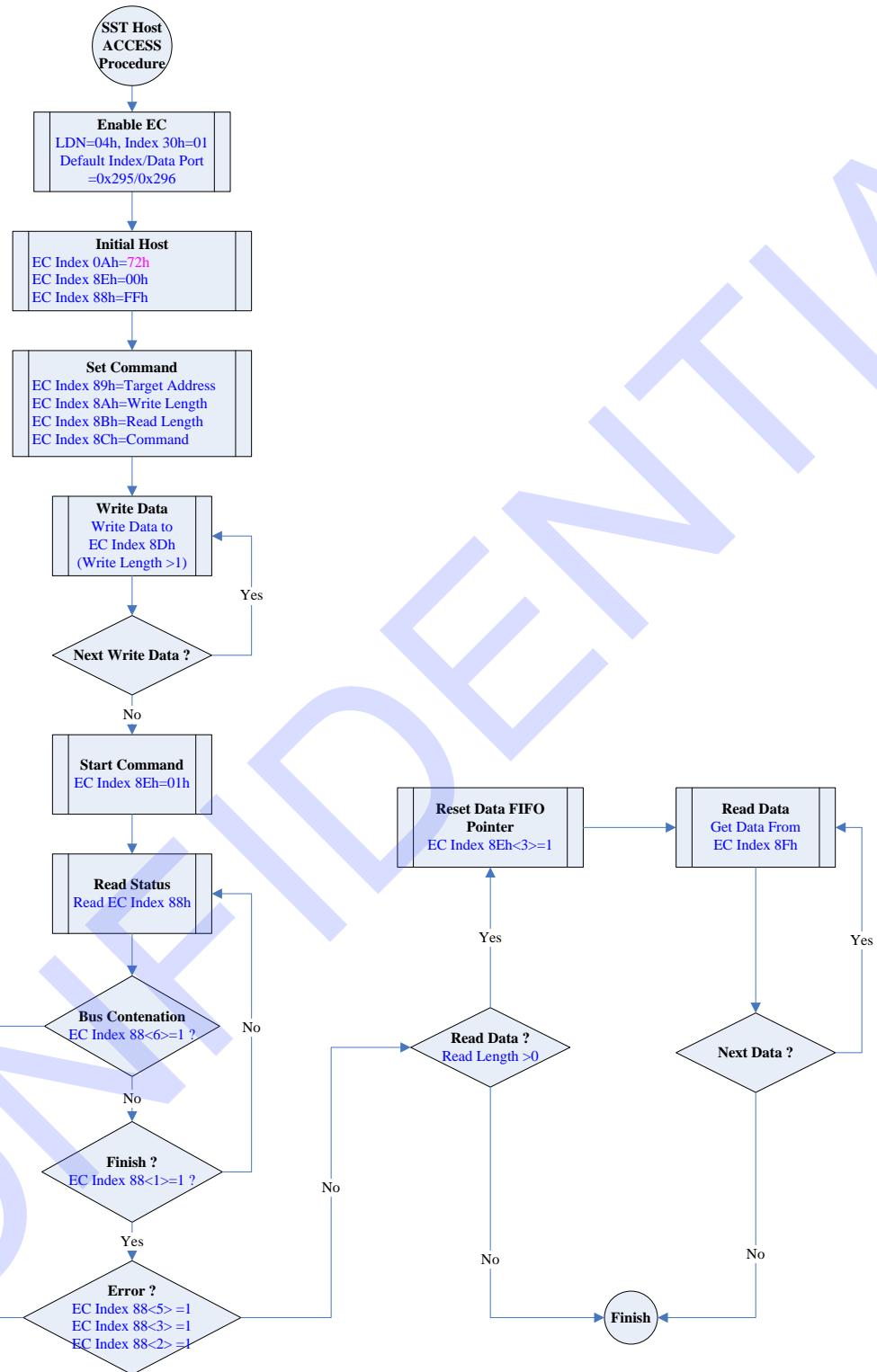


Figure 9-9. PECI Host Programming Procedure

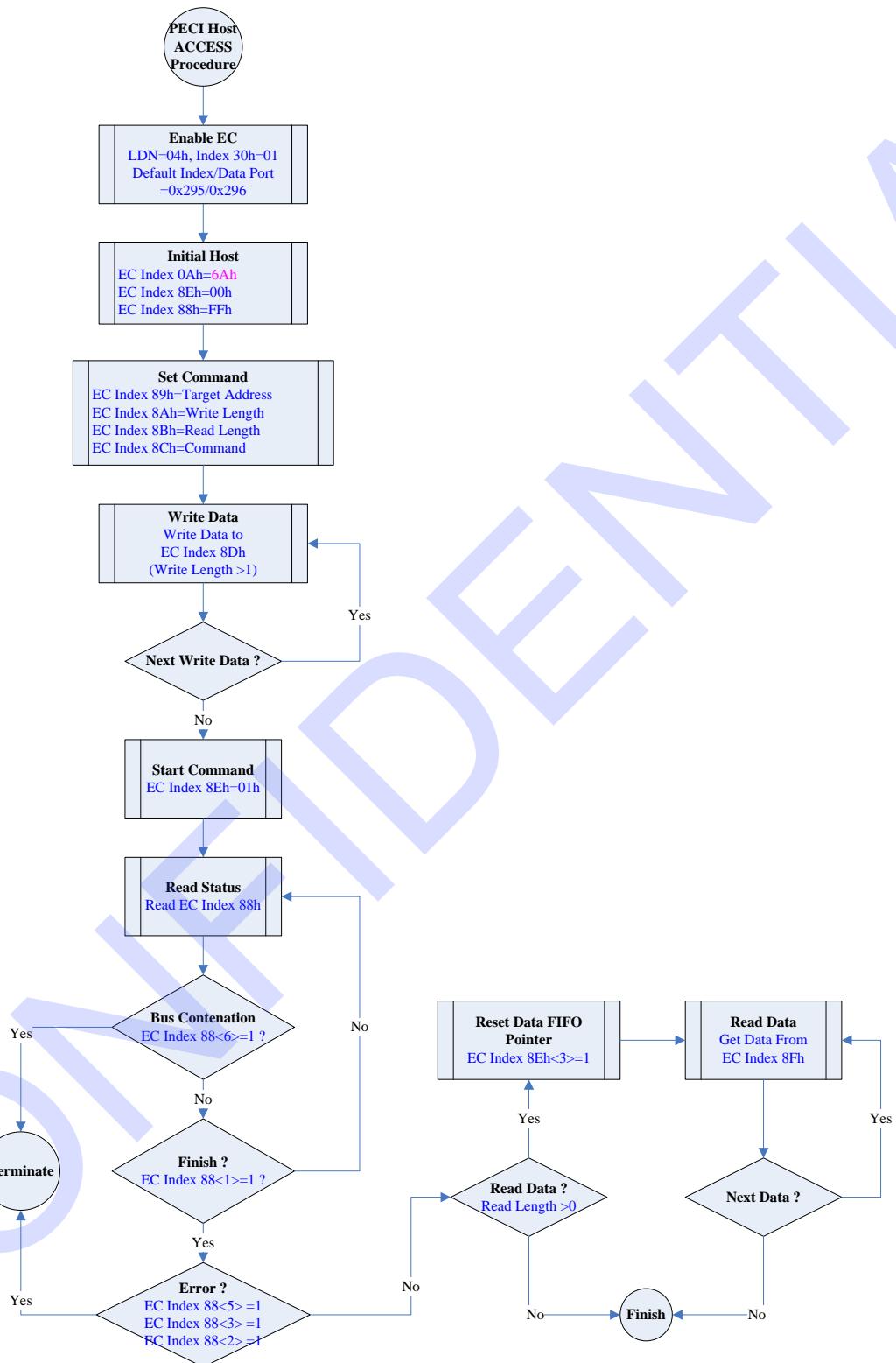


Figure 9-10. SST Slave Programming Procedure

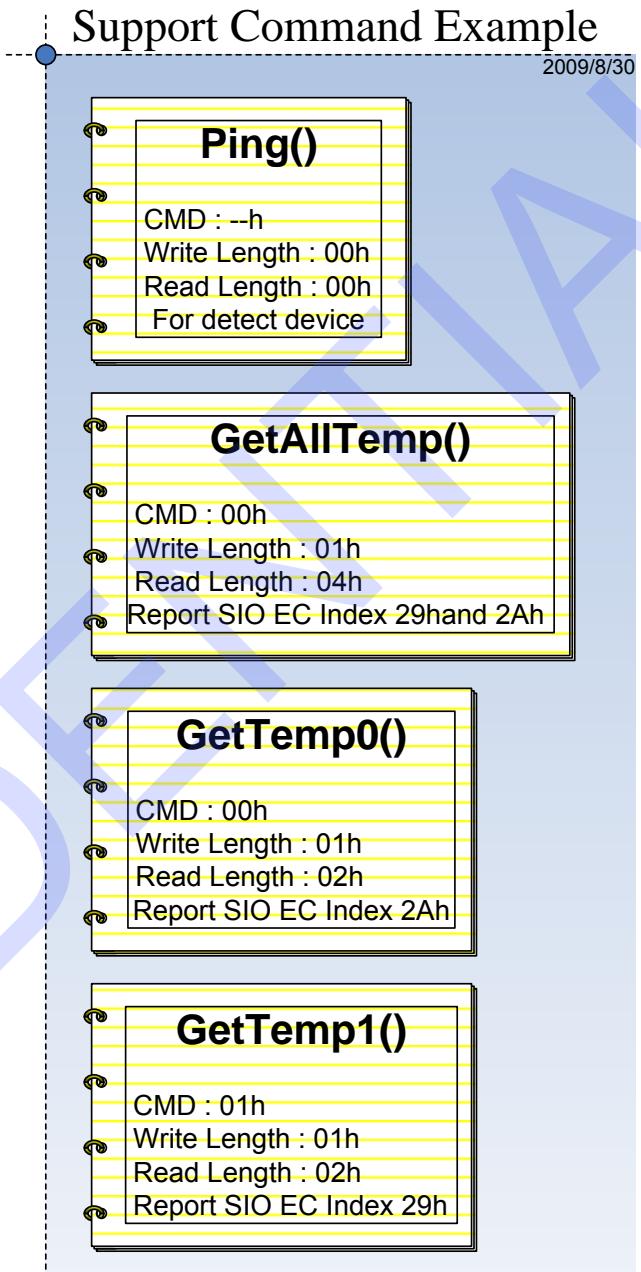
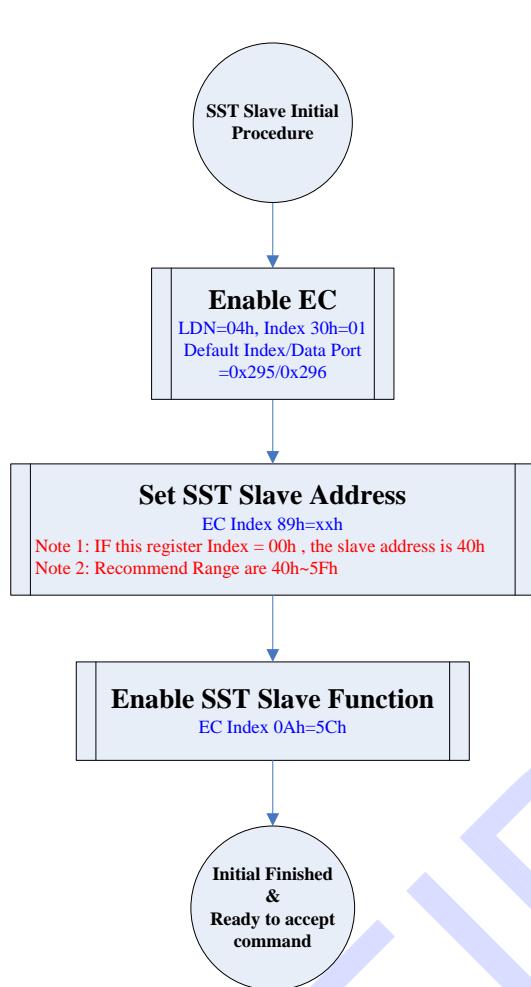
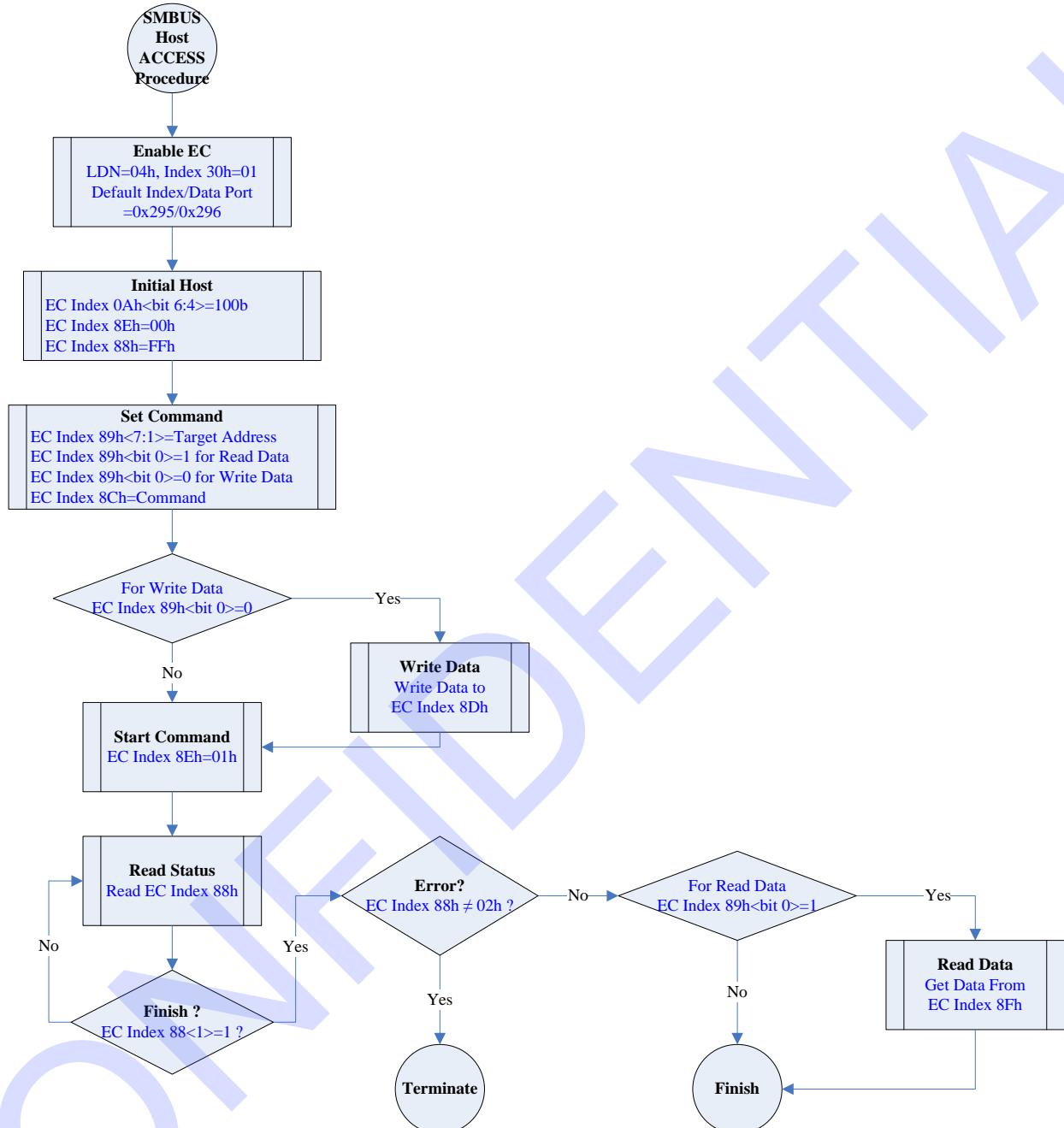


Figure 9-11. SMBus Host Slave Programming Procedure



9.6 Serial Port (UART)

The IT8733 incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can be programmed from 115.2K baud down to 50 baud as well. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

The Seiral Port 1 can be accessed by uC. The base address Is 2700h

The Seiral Port 2 can be accessed by uC. The base address Is 2800h

Table 9-3. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

9.6.1 Data Register

The TBR and RBR individually hold five to eight data bits. If the transmitted data are less than eight bits, it aligns to the LSB. Either received or transmitted data are buffered by a shift register, and are latched first by a holding register. Bit 0 of any word is first received and transmitted.

9.6.1.1 Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

9.6.1.2 Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before data transmission.

9.6.2 Control Register

9.6.2.1 Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0)

The IER is to enable or disable four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Bit	Default	Description
7-4	-	Reserved
3	0	Enable Modem Status Interrupt Set this bit high to enable the modem status interrupt when one of the modem status registers changes its bit status.
2	0	Enable Receiver Line Status Interrupt Set this bit high to enable the receiver line status interrupt, which happens when overrun, parity, framing or break occurs.
1	0	Enable Transmitter Holding Register Empty Interrupt Set this bit high to enable the transmitter holding register empty interrupt.
0	0	Enable Received Data Available Interrupt Set this bit high to enable the received data available interrupt and time-out interrupt in the FIFO mode.

9.6.2.2 Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine the interrupt priority and its source. The four existing interrupts are listed below in priority order.

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the interrupt type is stored in the IIR which is accessed by the host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the host. Any new interrupts will not be acknowledged until the host access is completed. Please refer to the following table for the detail.

Table 9-4. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register				Interrupt Set and Reset Function			
	Bit 3	Bit 2	Bit 1	Bit 0	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	X	X	1	-	None	None	-	
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR	
0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level	
1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last four character times and there is at least one character in it during this period.	Read RBR	
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR	
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR	

Note: X = Not Defined

IIR(7), IIR(6): Set when FCR(0) = 1.

IIR(5), IIR(4): Always logic 0.

IIR(3): In the non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out interrupt is pending.

IIR(2), IIR(1): Used to identify the highest priority interrupt pending.

IIR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled environment with a logic 0 state. In such a case, IIR contents may be used as a pointer that points to the appropriate interrupt service routine.

9.6.2.3 FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to not only enable and clear the FIFO but also set the RCVR FIFO trigger level.

Bit	Default	Description
7-6	-	Receiver Trigger Level Selection These bits are to set the trigger level for the RCVR FIFO interrupt.
5-4	0	Reserved
3	0	This bit does not affect Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.
2	0	Transmitter FIFO Reset This self-cleared bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1".
1	0	Receiver FIFO Reset Setting this self-cleared bit to a logic "1" will clear all contents of the RCVR FIFO and resets its related counter to "0" (except the shift register).
0	0	FIFO Enable XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT whereas disabled and cleared respectively when this bit is cleared to low. This bit must be a logic "1" if data are written to the other bits of the FCR, or they will not be properly programmed. When this register is switched to the non-FIFO mode, all of its contents will be cleared.

Table 9-5. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

9.6.2.4 Divisor Latches (DLL, DLM) (Read/Write, Address offset=0,1 DLAB=0)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in a 16-bit binary format. They are loaded during initialization to generate a desired baud rate.

9.6.2.5 Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG, which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The number of DLL or DLM is in 16-bit format, providing the divisor ranging from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 9-6. Baud Rate Using (24 MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

9.6.2.6 Scratch Pad Register (Read/Write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

9.6.2.7 Line Control Register (LCR) (Read/Write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line.

Bit	Default	Description
7	0	Divisor Latch Access Bit (DLAB) This bit must be set high to access the Divisor Latches of the baud rate generator during READ or WRITE operation whereas set low to access Data Register (refer to page 127) or Interrupt Identification Register (IIR) (Read only, Address offset=2) (refer to page 128).
6	0	Set Break This bit forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, which will be preserved until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.
5	0	Stick Parity When this bit and LCR(3) are high at the same time, the parity bit is transmitted and then detected by a receiver in an opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	Even Parity Selection When the parity is enabled (LCR(3) = 1), 0: Odd parity 1: Even parity
3	0	Parity Enable A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.

Bit	Default	Description
2	0	Number of Stop Bit This bit specifies the number of stop bits in each serial character, as summarized in Table 9-7. Stop Bit Number Encoding.
1-0	00	Word Length Select [1:0] 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 9-7. Stop Bit Number Encoding

LCR (2)	Word Length	No. of Stop Bit
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

9.6.2.8 Modem Control Register (MCR) (Read/Write, Address offset=4)

This register controls the interface by the modem or data set (or device emulating a modem).

Bit	Default	Description
7-5	-	Reserved
4	0	Internal Loopback This bit provides a loopback feature for diagnostic test of the serial channel when set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs and forced to inactive high then the transmitted data are immediately received, allowing the processor to verify the transmitted and received data path of the serial channel.
3	0	OUT2 The Output 2 bit enables the serial port interrupt output by a logic 1.
2	0	OUT1 This bit does not have an output pin and can only be read or written by CPU.
1	0	Request to Send (RTS) This bit controls the Request to Send (RTS#), which is in an inverse logic state with that of MCR(1).
0	0	Data Terminal Ready (DTR) This bit controls the Data Terminal Ready (DTR#), which is in an inverse logic state with that of the MCR(0).

9.6.3 Status Registers

9.6.3.1 Line Status Register (LSR) (Read/Write, Address offset=5)

This register provides the status indication and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

Bit	Default	Description
7	0	Error in Receiver FIFO In the 16450 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.
6	1	Transmitter Empty This read only bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty. Otherwise, this bit is "0" and has the same function as that in the FIFO mode.
5	1	Transmitter Holding Register Empty (THRE) This read only bit indicates that the TBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to the XMIT FIFO.
4	0	Line Break The Line Break (LB) Interrupt status bit indicates that the last character received is a break character, which is invalid but complete. It includes parity and stop bits. This situation occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in IIR, with bit 2 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) previously enabled(refer to page 128).
3	0	Framing Error (FE) A logic 1 indicates that the stop bit in the received character is not valid. It will be reset low when CPU reads the contents of the LSR.
2	0	Parity Error (PE) A logic 1 indicates that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever LSR is read by CPU.
1	0	Overrun Error (OE) A logic 1 indicates that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, OE occurs when FIFO is full and the next character has been completely received by the Shift Register. It will be reset when LSR is read by the CPU.
0	0	Data Ready A logic 1 indicates a character has been received by RBR. A logic 0 indicates all the data in RBR or RCVR FIFO have been read.

9.6.3.2 Modem Status Register (MSR) (Read/Write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or the peripheral devices in addition to this current state information. Four of these eight bits, MSR(4) - MSR(7), can provide the state change information when the modem control input changes the state. It is reset low when the host reads the MSR.

Bit	Default	Description
7	0	Data Carrier Detect(DCD) This bit indicates the complement status of Data Carrier Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.
6	0	Ring Indicator(RI) This bit indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.
5	0	Data Set Ready(DSR) This bit indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# of MCR.
4	0	Clear to Send(CTS) This bit indicates the complement of CTS# input. When the serial channel is in the Loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# of MCR.
3	0	Delta Data Carrier Detect(DDCD) This bit indicates that the DCD# input state has been changed since being read by the host last time.
2	0	Trailing Edge Ring Indicator(TERI) This bit indicates that the RI input state to the serial channel has been changed from low to high since being read by the host last time. The change in a logic "1" does not activate the TERI.
1	0	Delta Data Set Ready(DDSR) A logic "1" indicates that the DSR# input state to the serial channel has been changed since being read by the host last time.
0	0	Delta Clear to Send(DCTS) This bit indicates the CTS# input to the chip has changed the state since MSR was read last time.

9.6.4 Reset

The reset of the IT8733 should be held to an idle mode reset high for 500 ns until initialization, which causes the initialization of the internal clock counters of transmitter and receiver.

Table 9-8. Reset Control of Register and Pinout Signal

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high, others are low
Modem Status Register	Reset	High
SOUT1, SOUT2	Reset	Bits 0-3 low, bits 4-7 input signals
RTS1#, RTS2#, DTR1#, DTR2#	Reset	High
IRQ of Serial Port	Reset	High Impedance

9.6.5 Programming

Each serial channel of the IT8733 is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though these control registers can be written in any given order, IER should be the last register written because it controls whether the interrupt is enabled or not. After the port is programmed, these registers still can be updated whenever the port does not transfer data.

9.6.6 Software Reset

This approach allows the serial port to return to a completely known state without a system reset. It is achieved by writing the required data to LCR, DLL, DLM and MCR. LSR and RBR must be read before interrupts are enabled to clear out any residual data or status bits that may be invalid for subsequent operations.

9.6.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, not exactly 1.8432 MHz.

9.6.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

By setting bit 0 of FIFO Control Register (FCR) (Write Only, Address offset=2) (refer to page 130) and bit 0 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) (refer to page 128) high, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

The receive data available interrupt will be issued only when the FIFO has reached its programmed trigger level and cleared as soon as the FIFO drops below its trigger level.

The receiver line status interrupt has higher priority over the received data available interrupt.

The time-out timer will be reset after receiving a new character or after the host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the host reads one character from RCVR FIFO.

For the RCVR FIFO time-out interrupt, it will occur under the following conditions by enabling the RCVR FIFO

and receiver interrupts:

The RCVR FIFO time-out interrupt will occur only if there is at least one character in FIFO whenever the interval between the most recently received serial character and the most recent Host READ from the FIFO is longer than four consecutive character times.

The time-out timer will be reset after receiving a new character or after the host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the host reads one character from RCVR FIFO.

(2) XMIT Interrupt

By setting bit 0 of FIFO Control Register (FCR) (Write Only, Address offset=2) (refer to page 130) and bit 1 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) (refer to page 128) high, the XMIT FIFO and transmitter interrupts are enabled. The XMIT interrupt occurs under the following conditions:

- a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.
- b. The transmitter FIFO empty indications will be delayed for one character time minus the last stop bit time whenever the following condition occurs:

THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication will be delayed for one character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts have the same priority as the received data available interrupt. The XMIT FIFO empty has the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are 0].

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via LSR described below:

LSR(7): RCVR FIFO error indication

LSR(6): XMIT FIFO and Shift register empty

LSR(5): The XMIT FIFO empty indication

LSR(4) - LSR(1): Specify that errors have occurred. The character error status is handled in the same way as that in the interrupt mode. The IIR is not affected since IER(2)=0.

LSR(0): High whenever RCVR FIFO contains at least one byte.

No trigger level is reached or time-out condition indicated in FIFO Polled Mode.

9.7 Parallel Port

The IT8733 incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). For enabling/disabling, changing the base address of the parallel port, and operation mode selection, please refer to section 8.6 configuration registers on page 63 for the detail.

Table 9-9. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	11	STB#	WRITE#	NStrobe
2-9	12-19	PD0 - 7	PD0 - 7	PD0 - 7
10	6	ACK#	INTR	nAck
11	5	BUSY	WAIT#	Busy PeriphAck(2)
12	4	PE	(NU) (1)	PError nAckReverse(2)
13	3	SLCT	(NU) (1)	Select
14	10	AFD#	DSTB#	nAutoFd HostAck(2)
15	9	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	8	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	7	SLIN#	ASTB#	nSelectIn

Note 1: NU: Not used

Note 2: Fast mode

Note 3: For more information, please refer to the IEEE 1284 standard.

9.7.1 SPP and EPP Mode

Table 9-10. Address Map and Bit Map for SPP and EPP Mode

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1h	R	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 0	Base 1+4h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 1	Base 1+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 2	Base 1+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 3	Base 1+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

9.7.1.1 Data Port Register (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by bit 5 of the logic state of Control Port Register (Base Address 1 + 02h), which forwards the direction when the bit is low (0) whereas reverses the direction when the bit is high (1).

9.7.1.2 Status Port Register (Base Address 1 + 01h)

This is a **read only** register. Writing data to this register has no effects. The contents of this register are latched during an IOR cycle.

Bit 7: BUSY#

Inverse of printer BUSY signal; a logic "0" means that the printer is busy and cannot accept another character whereas a logic "1" means that it is ready to accept the next character.

Bit 6: ACK#

Printer acknowledge; a logic "0" means that the printer has received a character and is ready to accept another whereas a logic "1" means that it is still processing the last character.

Bit 5: PE

Paper end; a logic "1" indicates the paper end.

Bit 4: SLCT

Printer selected; a logic "1" means that the printer is on line.

Bit 3: ERR#

Printer error signal; a logic "0" means an error has been detected.

Bits 2-1: Reserved

These bits are always "1" at read.

Bit 0: TMOUT

This bit is valid only in the EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurs whereas a logic "1" means that a time-out error has been detected. This bit is cleared by an LRESET# or by writing a logic "1" to it. When the chip is selected as the non-EPP mode (SPP or ECP), this bit is always a logic "1" at read.

9.7.1.3 Control Port Register (Base Address 1 + 02h)

This is a **read/write** register and the port provides all output signals to control the printer.

Bit 7-6: Reserved

These two bits are always "1" at read.

Bit 5: PDDIR

Data port direction control. This bit determines the direction of the data port register. Set this bit "0" to output the data port to PD bus whereas "1" to input from PD bus.

Bit 4: IRQE

Interrupt request enable. Setting this bit "1" enables the interrupt request from the parallel port to the host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.

Bit 3: SLIN

Inverse of SLIN# pin; setting this bit to "1" selects the printer.

Bit 2: INIT

Initiate printer; setting this bit to "0" initializes the printer.

Bit 1: AFD

Inverse of the AFD# pin; setting this bit to "1" causes the printer to automatically advance one line after each line is printed.

Bit 0: STB

Inverse of the STB# pin; this pin controls the data strobe signal to the printer.

9.7.1.4 EPP Address Port Register (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the host writes data to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is at this address) causes an EPP ADDRESS WRITE cycle. When the host reads data from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is at this address) causes an EPP ADDRESS READ cycle.

9.7.1.5 EPP Data Port 0-3 Register (Base Address 1 + 04-07h)

The EPP Data Ports are only available in the EPP mode. When the host writes data to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is at this address) causes an EPP DATA WRITE cycle. When the host reads data from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is at this address) causes an EPP DATA READ cycle.

9.7.2 EPP Mode Operation

When the parallel port of the IT8733 is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by Control Port Register (Base Address 1 + 02h) (refer to page 138). The direction of the data port is controlled by bit 5 of Control Port Register (Base Address 1 + 02h). There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active, the IT8733 will issue Long Wait in SYNC field) high (EPP READ/WRITE cycle) to WAIT# being de-asserted. If a time-out occurs, the current EPP READ/WRITE cycle will be aborted and a logic "1" will be read from bit 0 of Status Port Register (Base Address 1 + 01h) (refer to page 138). The host must write 0 to bit 0, 1, 3 of Control Port Register (Base Address 1 + 02h) before any EPP READ/WRITE cycle (EPP spec.). Pin STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

9.7.2.1 EPP ADDRESS WRITE

1. The host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus, allowing the host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

9.7.2.2 EPP ADDRESS READ

1. The host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts ASTB# after IOR becomes active.
3. The peripheral drives the PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7, allowing the host to complete the I/O READ cycle.
4. The peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.7.2.3 EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04h - 07h). The chip drives D0- D7 onto PD0 -PD7.
2. The chip asserts WRITE# (STB#) and DSTB# (AFD#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus, allowing the host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

9.7.2.4 EPP DATA READ

1. The host reads a byte from the EPP DATA Port (Base address +04h - 07h). The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts DSTB# after IOR becomes active.
3. The peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7, allowing the host to complete the I/O READ cycle.
4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.7.3 ECP Mode Operation

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. It provides an automatic high-burst-bandwidth channel that supports the DMA or ECP mode in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and enhance the maximum bandwidth requirement allowed. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports hardware run-length encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8733 does not support hardware RLE compression. For the detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 9-11. Bit Map of ECP Register

Register	D7	D6	D5	D4	D3	D2	D1	D0	
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							
dsr	nBusy	nAck	PError	Select	nFault	1	1	1	
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe	
cFifo	Parallel Port Data FIFO								
ecpDFifo	ECP Data FIFO								
tFifo	Test FIFO								
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	0	intrValue	0	0	0	0	0	0	
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty	

9.7.3.1 ECP Register Definition

Name	Address	I/O	ECP Mode	Function
data	Base 1 +000h	R/W	000-001	Data Register
ecpAFifo	Base 1 +000h	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001h	R/W	All	Status Register
dcr	Base 1 +002h	R/W	All	Control Register
cFifo	Base 2 +000h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000h	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000h	R/W	110	Test FIFO
cnfgA	Base 2 +000h	R	111	Configuration Register A
cnfgB	Base 2 +001h	R	111	Configuration Register B
ecr	Base 2 +002h	R/W	All	Extended Control Register

Note 1: Base address 1 depends on Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h) and Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h) (refer to page 63 and 63).

Note 2: Base address 2 depends on the Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h) and Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h) (refer to page 63 and 63).

9.7.3.2 ECP Mode Description

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: For the mode selection, please refer to ECP Register Definition on page 141 for the detail.

9.7.3.3 ECP Pin Description

Name	Attribute	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device
PD0-PD7	I/O	Address or data or RLE data
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the host
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (handshaking with nStrobe) whereas for determining whether a command or data information is present on PD0-PD7 in the reverse direction.
Perror (nAckReverse)	I	Used to acknowledge nlinit from the peripheral which drives this signal low, allowing the host to drive the PD bus
Select	I	Printer On-Line Indication
nAutoFd (HostAck)	O	This signal is used for handshaking between the nAck and the host in the reverse direction. A peripheral data byte is requested when it is asserted. This signal is to determine whether a command or data information is present on PD0-PD7 in the forward direction.
nFault (nPeriphRequest)	I	For the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while entering the ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to the host, which has the ultimate control over the transfer direction.
nlinit (nReverseRequest)	O	The host may drive this signal low to make the PD bus in the reverse direction. The peripheral is permitted to drive the PD bus when nlinit is low and nSelectIn high in the ECP mode.
NSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

9.7.3.4 Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a reset. The contents of the LPC data fields are latched by the Data Register then sent without being inverted to PD0-PD7 in **write** operation whereas the contents of data ports are read and sent to the host in **read** operation.

9.7.3.5 ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data bytes written to this port are placed in FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends these data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

9.7.3.6 Device Status Register (dsr) (Base 1 +01h, Mode All)

Bit 2-0 of this register are not implemented. The states of these bits remain high in **read** operation of the Printer Status Register.

- dsr(7): This bit is the inverted level of the Busy input.
- dsr(6): This bit is the state of the nAck input.
- dsr(5): This bit is the state of the PError input.
- dsr(4): This bit is the state of the Select input.
- dsr(3): This bit is the state of the nFault input.
- dsr(2)-dsr(0): These bits are always 1.

9.7.3.7 Device Control Register (dcr) (Base 1+02h, Mode All)

There is no function provided by bit 7-6 of this register, which are **read only** and set high in **read** operation. Contents of bit 5-0 are initialized to 0 when the RESET pin is active.

dcr(7)-dcr(6): These two bits are always high.

dcr(5): Except in mode 000 and 010, setting this bit low means that the PD bus is in output operation whereas setting it high means that it is in input operation. This bit will be forced to low in mode 000.

dcr(4): Setting this bit high enables the interrupt request from peripheral to the host due to a rising edge of the nAck input.

dcr(3): This bit is inverted and output to SelectIn.

dcr(2): This bit is output to nInit without inversion.

dcr(1): This bit is inverted and output to nAutoFd.

dcr(0): This bit is inverted and output to nStrobe.

9.7.3.8 Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the host to this FIFO are sent by a hardware handshaking to the peripheral according to the Standard Parallel Port protocol. This operation is only defined for the forward direction.

9.7.3.9 ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The host can receive these bytes by performing **read** operations or DMA transfer from this FIFO.

9.7.3.10 Test FIFO (tFifo) (Base 2+00h, Mode 110)

The host may operate READ/WRITE or DMA transfer to this FIFO in any directions. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Operating READ from an empty tFifo causes the last data byte to return.

9.7.3.11 Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

9.7.3.12 Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is **read only**.

cnfgB(7): A logic “0” read indicates that the chip does not support hardware RLE compression.

cnfgB(6): Reserved.

cnfgB(5)-cnfgB(3): A value 000 read indicates that the interrupt must be selected with jumpers.

cnfgB(2)-cnfgB(0): A value 000 read indicates that the DMA channel is set to 8-bit DMA.

9.7.3.13 Extended Control Register (ecr) (Base 2+02h, Mode All)

This is an ECP function control register.

ecr(7)-ecr(5): These bits are used for READ/WRITE and mode selection.

Table 9-12. Mode and Description of Extended Control Register (ECR)

ECR	Mode and Description
000	Standard Parallel Port Mode The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	PS/2 Parallel Port Mode It is similar to the SPP mode, except that the dcr(5) is read/write . When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	Parallel Port Data FIFO Mode This mode is similar to the 000 mode, except that the host writes or DMA transfers the data bytes to FIFO. The FIFO data are then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	ECP Parallel Port Mode In the forward direction, bytes in the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	Reserved; undefined
110	Test Mode In this mode, FIFO may be read from or written to, but it cannot be sent to the peripheral.
111	Configuration Mode In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode

- 1: Disable the interrupt generated on the asserting edge of the nFault input.
- 0: Enable the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted or if this bit is written from 1 to 0 in the low-level nFault.

ecr(3): dmaEn, READ/WRITE

- 1: Enable DMA. DMA is started when servicelntr (ecr(2)) is 0.
- 0: Disable DMA unconditionally.

ecr(2): Servicelntr, READ/WRITE

- 1: Disable DMA and all service interrupts.
- 0: Enable the service interrupts. This bit will be set to "1" by hardware when one of the three service interrupts occurs.

Writing "1" to this bit will not generate an interrupt.

Case 1: dmaEn=1

During DMA, this bit will be set to 1 (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0

This bit is set to 1 (a service interrupt generated) whenever there is writeIntrThreshold or more bytes space free in FIFO.

Case 3: dmaEn=0, dcr(5)=1

This bit is set to 1 (a service interrupt generated) whenever there is readIntrThreshold or more valid bytes to be read from FIFO.

ecr(1): full, **read only**

- 1: FIFO is full and cannot accept another byte.
- 0: FIFO has at least one free data byte space.

ecr(0): empty, **read only**

- 1: FIFO is empty.
- 0: FIFO contains at least one data byte.

9.7.3.14 Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data transmission are software-controlled. Setting the mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

For mode 000 and 001, they may be immediately switched. To change the direction, the mode must be set to 001 first.

In the extended forward mode, FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In the ECP reverse mode, all data must be read from FIFO before returning to mode 000 or 001. Usually, unneeded data are accumulated during ECP reverse handshaking when the mode is changed during a data transfer. In such a condition, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

9.7.3.15 Software Operation (ECP)

Before the ECP operation can be started, it is necessary for the host to switch the mode to 000 first in order to negotiate with the parallel port. During this process, the host determines whether the peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfer is PWord-wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. The ECP Address/RLE bytes may be automatically sent by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change the direction, the host has to switch the mode to 001. It then negotiates either the forward or reverse channel, sets the direction to 1 or 0, and finally switches the mode to 001. If the direction is set to 1, the hardware performs the handshaking for each ECP data byte read, and then tries to fill FIFO. At this time, PWords may be read from the ecpDFifo while retaining data. It is also possible to perform the ECP transfer by handshaking with individual bytes under programmed control in mode 001 or 000 even though this is a comparatively time-consuming approach.

9.7.3.16 Hardware Operation (DMA)

The Standard PC DMA protocol (through LDRQ#) is followed. As in the programmed I/O case, software sets the direction and state. Next, the desired count and memory addresses are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents of FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr, DMA is disabled when the DMA controller reaches the terminal count. By not asserting LDRQ# for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing transfer, the host DMA controller is disabled, serviceIntr is then set to 1, and dmaEn is next set to 0. If the contents in FIFO are empty or full, DMA will start again. This is first done by enabling the host DMA controller, and then setting dmaEn to 1. Finally, serviceIntr is set to 0. Upon completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low, ensuring that all data successfully reach the peripheral device.

9.7.3.17 Interrupt

It is necessary to generate an interrupt when any of the following states is reached.

1. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold.
2. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of PWords in the FIFO is greater than or equal to readIntrThreshold.
3. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count.
4. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
5. ackIntEn = 1. In current implementation of using existing parallel ports, the generated interrupt may be either edge or level trigger type.

9.7.3.18 Interrupt-driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is 0 and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the Test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

For any PC LPC bus implementation adjusted to expedite DMA or I/O transfer, it is necessary to ensure that the bandwidth on ISA is maintained on the interface. Although the LPC (even PCI) bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at the optimum speed.

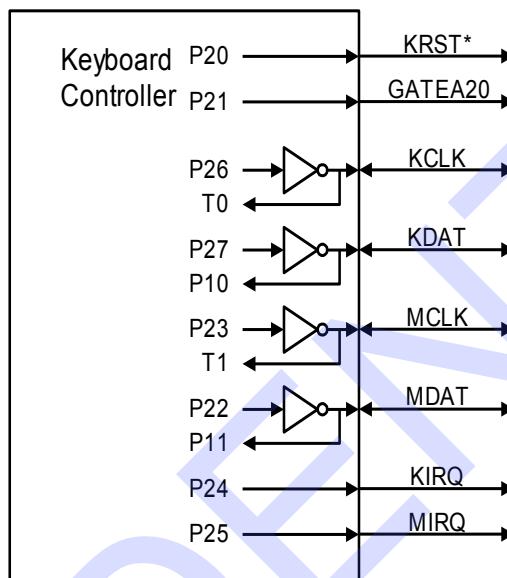
9.7.3.19 Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 KB/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

9.8 Keyboard Controller (KBC)

The keyboard controller is implemented using an 8-bit microcontroller that is capable of executing the 8042 instruction set. For general information, please refer to the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter the power-down mode by executing two types of power-down instructions.

Figure 9-12. Keyboard and Mouse Interface



9.8.1 Host Interface

The keyboard controller interfaces with the system through the 8042 style host interface. The following table shows how the interface decodes the control signals.

Table 9-13. Data Register READ/WRITE Controls

Host Address ^{Note}	R/W*	Function
60h	R	READ DATA
60h	W	WRITE DATA, (Clear F1)
64h	R	READ Status
64h	W	WRITE Command, (Set F1)

Note: These are the default values of LDN5, 60h and 61h (DATA); LDN5, 62h and 63h (Command). All these registers are programmable.

READ DATA: This is an 8-bit read only register. When read, the KIRQ output is cleared and OBF flag in the status register is cleared.

WRITE DATA: This is an 8-bit write only register. When written, the F1 flag of the Status register is cleared and the IBF bit is set.

READ Status: This is an 8-bit read only register. Refer to the description of the Status register for more information.

WRITE Command: This is an 8-bit write only register. When written, both F1 and IBF flags of the Status register are set.

9.8.2 Data Registers and Status Register

The keyboard controller provides two data registers, one is DBIN for data input, and the other is DBOUT for data output. Both are 8-bit wide. A write (microcontroller) to the DBOUT will load Keyboard Data Read Buffer, set OBF flag and set the KIRQ output. A read (microcontroller) of DBIN will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag.

The status register holds information concerning the status of the data registers, the internal flags, and some user-defined status bits. Please refer to Table 9-14. Status Register below. The bit 0 OBF is set to "1" when the microcontroller writes data into DBOUT, and is cleared when the system initiates DATA READ operation. The bit 1 IBF is set to "1" when the system initiates WRITE operation, and is cleared when the microcontroller executes an "IN A, DBB" instruction. The F0 and F1 flags can be set or reset when the microcontroller executes clear and complement flag instructions. F1 also holds the system WRITE information when the system performs WRITE operation.

Table 9-14. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF

9.8.3 Keyboard and Mouse Interface

KCLK is a keyboard clock pin. Its output is the inversion of pin P26 of the microcontroller, and the input of KCLK is connected to the T0 pin of the microcontroller. KDAT is the keyboard data pin; its output is the inversion of pin P27 of the microcontroller, and the input of KDAT is connected to the P10 of the microcontroller. MCLK is the mouse clock pin. Its output is the inversion of pin P23 of the microcontroller, and the input of MCLK is connected to the T1 pin of the microcontroller. MDAT is the Mouse data pin. Its output is the inversion of pin P22 of the microcontroller, and the input of MDAT is connected to the P11 of the microcontroller. KRST# is pin P20 of the microcontroller. GATEA20 is the pin P21 of the microcontroller. These two pins are used as software-controlled or user defined outputs. External pull-ups may be required for these pins.

9.8.4 KIRQ and MIRQ

KIRQ is the interrupt request for the keyboard (Default IRQ1), and MIRQ is the interrupt request for the mouse (Default IRQ12). KIRQ is internally connected to P24 pin of the microcontroller, and MIRQ is internally connected to pin P25 of the microcontroller.

9.9 Real Time Clock (RTC)

9.9.1 General Description

The RTC device incorporates a timer module that includes a time of day clock and a multi-century calendar, alarm facilities, and three programmable timer interrupts, 242-byte RAM contents which can be backed up by the external battery during the power loss, and the power management circuitry which can reduce the standby current when the power is supplied by the VBAT.

The RTC's alarm and calendar registers support not only BCD and binary modes but also 24- and 12-hour formats. There is only an interrupt line requested to handle three interrupt conditions, the alarm interrupt, periodic interrupt, and update-ended interrupt. The RTC also incorporates a power switching circuitry which can detect the absence of VSB power and switch the power core of the whole block (including RAM block) to VBAT, and a power-saving circuitry which can reduce the power consumption when the power is switched to VBAT.

The RAM contents are divided into two parts: lower bank (114 bytes) and upper bank (128 bytes). Access to the RAM may be selectively locked. See Section 8.11.5 "RTC Special Configuration Register" for details.

9.9.2 Register Description

For 10 time registers and 4 control registers, please refer to Table 9-15, the Register Address Map of RTC Bank 0 for the detail. To initialize the time, calendar and alarm A registers properly, the SET bit of CRB must be set to "1" to avoid the generation of the update cycle, after which the SET bit must be set to 0 to enable the update cycle. When the time corresponds to the alarm time, the alarm will occur once per day. If the data in the hour-alarm register is between C0 to FF, the alarm will be generated once per hour if the data in the minutes and seconds register corresponds to the data in the minute-alarm and second-alarm registers. If both data of hour-alarm and minute-alarm registers are located between C0 to FF, the alarm will occur once per minute if the data in the second register corresponds to the one in the second-alarm register. If all data of the hour-alarm, minute-alarm and second-alarm registers are located between C0 to FF, the alarm will be generated once per second.

Table 9-15. RTC Register List, Bank 0 (Primary Address, default = 70h/71h)

Index	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours 12-hr mode	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours 24-hr mode	0-23	00-17	00-23
5	Hours Alarm 12-hr	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours Alarm 24-hr	0-23	00-17	00-23
6	Day of the week (Sunday=1)	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99
A	Control register A (CRA)	R/W * Bit 7 is read only		
B	Control register B (CRB)	R/W * Bit 0 is read only		
C	Control register C (CRC)	Read only		
D	Control register D (CRD)	Read only		
80h	Century	0-99	00-63	00-99
81h	Seconds Wake-up	0-59	00-3B	00-59
82h	Minutes Wake-up	0-59	00-3B	00-59
83h	Hours Wake-up (12-hr mode)	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours Wake-up (24-hr mode)	0-23	00-17	00-23
84h	Day of the Week Wake-up	1-7	01-07	01-07
85h	Date of the Month Wake-up	1-31	01-1F	01-31
86h	Month Wake-up	1-12	01-0C	01-12
87h	Year Wake-up	0-99	00-63	00-99
88h	Century Wake-up	0-99	00-63	00-99
89h	RTC Wake-up status	--	--	--

9.9.2.1.1 RTC Control Register A (CRA)

Bit	R/W	Description
7	R/W	UIP (Update In Progress) UIP can be cleared by SET=1, but cannot be modified by LRESET#. 1: The update cycle is in progress or will occur soon. 0: The update cycle is not in progress and will not occur within at least 244μs.
6-4	R/W	DV2-0 (Divider Chain Control) Select the conditions of the divider chain and these three bits are not affected by RESET. DV2-0 Mode 000b Oscillator disabled 001b Oscillator disabled 010b Normal operation, Oscillator on and divider chain enabled 10Xb Test 11Xb Oscillator on and divider chain disabled
3-0	R/W	RS3-0 (Periodic Interrupt Rates Select) Select one of fifteen states on the divider or disable the divider output, and these four bits are not affected by LRESET#. RS3-0 Periodic Rate of Interrupt 0000b None 0001b 3.90625 ms 0010b 7.8125 ms 0011b 122.070 μs 0100b 244.141 μs 0101b 488.281 μs 0110b 976.562 μs 0111b 1.953125 ms 1000b 3.90635 ms 1001b 7.8125 ms 1010b 15.625 ms 1011b 31.25 ms 1100b 62.5 ms 1101b 125 ms 1110b 250 ms 1111b 500 ms

9.9.2.1.2 RTC Control Register B (CRB)

Bit	R/W	Description
7	R/W	SET SET cannot be modified by Master Reset or any internal functions. 0: Execute the update cycle once per second. 1: The update cycle is disabled and the initial time and calendar bytes can be written.
6	R/W	PIE (Periodic Interrupt Enable) PIE can be cleared by Master Reset and cannot be modified by any internal functions. The generation rate of the Periodic Interrupt is determined by DS3-0 in CRA. 0: Disable the generation of the Periodic Interrupt. 1: Enable the generation of the Periodic Interrupt.
5	R/W	AIE (Alarm Interrupt Enable) AIE can be cleared by Master Reset and cannot be modified by any internal functions. The Alarm Interrupt is generated immediately after a time update that the Seconds, Minutes, Hours, and Day-of-month time is equal to their respective alarm counterparts. 0: Disable the generation of the Alarm Interrupt. 1: Enable the generation of the Alarm Interrupt.
4	R/W	UIE (Update-ended Interrupt Enable) This bit will be cleared by Master Reset. This interrupt is generated at the time when an update occurs. 0: Disable the generation of the Update-ended Interrupt. 1: Enable the generation of the Update-ended Interrupt.
3	R/W	Unused The original definition of 146818 is “Square Wave Enable” but is not supported by the RTC of this chip. Writing data to this bit has no effects.
2	R/W	DM (Data Mode) This bit selects the data mode and is not affected by Master Reset. 0: Data in the time and calendar registers are in BCD format. 1: Data in the time and calendar registers are in binary format.
1	R/W	24/12 (24- or 12-hour) This bit selects the hour format and it is not affected by Master Reset. 0: 12-hour format. 1: 24-hour format.
0	R/W	DSE (Daylight Saving Enable) This bit selects the hour format, and it is not affected by Master Reset. In spring, time advances from 1:59:59 to 3:00:00 on the first Sunday in April. In fall, time returns from 1:59:59 to 1:00:00 on the last Sunday in October. 0: Disable daylight saving mode. 1: Enable daylight saving mode.

9.9.2.1.3 RTC Control Register C (CRC)

The RTC supports three interrupt events, Periodic Interrupt, Alarm Interrupt, and Update-ended Interrupt. When an interrupt occurs, the related flag bit is set to "1" in CRC. These flag bits are set despite the statuses of the corresponding enable bits in CRB. Only when the interrupt enable bit is set and the corresponding interrupt flag bit is set, the IRQF bit in CRC will be activated and IRQ of RTC is pulled low. The states of the interrupt flag bits and RTC IRQ will not be cleared until the read cycle of CRC is completed.

Bit	R/W	Description
7	RO	IRQF (Interrupt Request Flag) This bit is the inverse of the value on the IRQ output signal of the RTC module. 0: RTC IRQ is inactive. 1: RTC IRQ is active when both PF and PIE are 1; or both AF and AIE are 1; or both UF and UIE are 1.
6	RO	PF (Periodic Interrupt Flag) PF can be cleared by Master Reset and reading this register. 0: No transition occurs to the selected tap since last read. 1: At least a transition occurs to the selected tap since last read.
5	RO	AF (Alarm Interrupt Flag) AF can be cleared by Master Reset and reading this register. 0: No alarm was detected since last read. 1: An alarm condition was detected.
4	RO	UF (Update-ended Interrupt Flag) This bit will be cleared by Master Reset and reading this register. 0: Disable the generation of the Update-ended Interrupt. 1: Enable the generation of the Update-ended Interrupt.
3-0	-	Reserved

9.9.2.1.4 RTC Control Register D (CRD), Bank 0

Bit	R/W	Description
7	RO	VRT (Valid RAM and Time) This bit is affected by Master Reset, and can only be set if the VBAT voltage is not too low when CRD is read. 0: The voltage of VBAT is too low. 1: The contents of RTC and RAM are valid.
6	-	Reserved
5-0	R/W	DATE_ALARM (Date Alarm Bits) These six bits, not affected by Master Reset, store the date of month alarm value. If set to 000000b, the Date Alarm is "Don't care". The legal values for these six bits are 01 to 31 in BCD format and 01 to 1F in binary format.

9.9.2.1.5 The Function of Wake-up Alarm

Wake-up Alarm registers are used to set the wake up alarm time. When the wake up alarm time specified is up, the hardware will set RTC_EVT_STS of GPE1_STS_2. If the related enabled bits are set, the Wake-up Alarm event may cause activation of PSON#, PWUREQ#, SIOSM#, and SWC IRQ.

When all of the eight Wake-up Alarm registers (with addresses from C1h to C8h) are set in an appropriate time, the alarm signal will occur at the specified time. The Wake-up Alarm registers can also serve to set bits[7:6] of one or more Wake-up Alarm registers to “11” to create a “Don’t Care” situation. Take the Hour Wake-up Alarm register for example, the alarm will be generated once per hour if the first two bits of Hour Wake-up Alarm register are set to “11”.

An “OR” function is provided for Day of Week Wake-up Alarm (C4h) and Date of Month Wake-up Alarm (C5h) registers. The alarm will be generated once every day if bits[7:6] of the above two registers are set to “11”, which will result in “Don’t Care” situation. The alarm is generated on the day of month when the Date of Month Wake-up Alarm (C5h) is written with appropriate data and the Day of Week Wake-up Alarm (C4h) is “Don’t Care”. (Bits[7:6] are set to “11”.) The alarm is generated on the day of week if the Date of Month Wake-up Alarm (C5h) is “Don’t Care”. (Bits[7:6] are set to “11”), and the Day of Week Wake-up Alarm (C4h) is written with appropriate data. When both of the two registers are written with appropriate data except “Don’t Care”, the alarm will be generated on either the day of week or the day of month.

9.10 Consumer Remote Control (TV Remote) IR (CIR)

9.10.1 Overview

CIR is used in the consumer remote control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisors and sensitivity ranges, the CIR registers are able to support the popular protocols such as RC-5, NEC, and RECS-80. Software driver programming can support new protocols. The CIR can be accessed by uC, and the base address is 2300h.

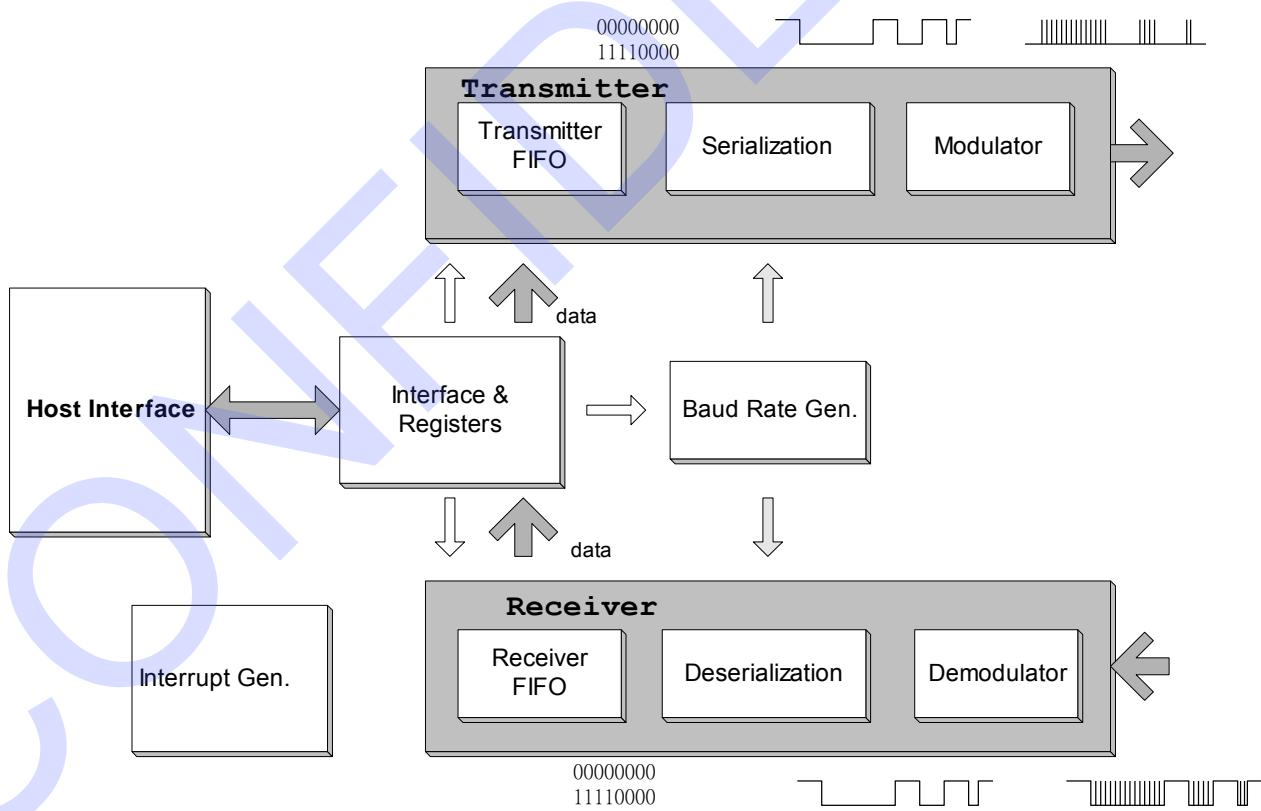
9.10.2 Features

- Supports 30 kHz - 57 kHz (low frequency) or 400 kHz - 500 kHz (high frequency) carrier transmission
- Baud rate up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral function
- 32-byte FIFO for data transmission or data reception

9.10.3 Block Diagram

CIR consists of two parts, transmitter and receiver. Regarding the transmitter part, it is responsible for transmitting data to FIFO, processing FIFO data by serialization and modulation and sending out data through the LED device. As for the receiver part, it is responsible for receiving data, processing data by demodulation and deserialization and storing data in the Receiver FIFO.

Figure 9-13. CIR Block Diagram



9.10.4 Transmit Operation

The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with the carrier frequency and sent to the CIRTX output. The data are either in bit-string format or run-length decode.

Before the data transmission can be started, code byte write operation must be performed to the Transmitter FIFO DR. Bit TXRLE of TCR1 needs to be set to “1” before the data in run-length decode can be written into the Transmitter FIFO. Setting TXENDF of TCR1 will enable the data transmission deferral, and avoid the Transmitter FIFO underrun. The bit width of the serialized bit string is determined by the value programmed in the baud rate divisor registers, BDLR and BDHR. When the two bits, HCFS and CFQ[4:0], are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bit TXMPM[1:0] and TXMPW[2:0] specify the pulse number in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic “0” can activate the Transmitter LED in the format of a series of modulating pulses.

9.10.5 Receive Operation

The Receiver function will be enabled if bit RXEN of RCR is set to “1”. Either demodulated or modulated RX# signal is loaded into Receiver FIFO, and bit RXEND of RCR determines whether the demodulation logic should be used or not. It determines the baud rate by programming the baud rate divisor registers BDLR and BDHR, and the carrier frequency by programming bit HCFS and CFQ[4:0]. Set RDWOS to “0” to synchronize. Bit RXACT of RCR is set to “1” when the serial data or the selected carrier is incoming, and the sampled data will then be kept in Receiver FIFO. Write “1” to bit RXACT to stop the Receiver operation whereas “0” to bit RXEN to disable it.

9.10.6 Register Description and Address

Table 9-16. CIR Register

Register Name	R/W	Address	Default
CIR Data Register (DR)	R/W	Base + 0h	FFh
CIR Interrupt Enable Register (IER)	R/W	Base + 1h	00h
CIR Receiver Control Register (RCR)	R/W	Base + 2h	01h
CIR Transmitter Control Register 1 (TCR1)	R/W	Base + 3h	00h
CIR Transmitter Control Register 2 (TCR2)	R/W	Base + 4h	5Ch
CIR Transmitter Status Register (TSR)	R	Base + 5h	00h
CIR Receiver Status Register (RSR)	R	Base + 6h	00h
CIR Baud Rate Divisor Low Byte Register (BDLR)	R/W	Base + 5h	00h
CIR Baud Rate Divisor High Byte Register (BDHR)	R/W	Base + 6h	00h
CIR Interrupt Identification Register (IIR)	R/W	Base + 7h	01h

9.10.6.1 CIR Data Register (DR)

The DR, an 8-bit read/write register, is the data port for CIR. Data are transmitted and received through it.

Address: Base Address + 0h

Bit	R/W	Default	Description
7-0	R/W	FFh	CIR Data Register (DR[7:0]) Writing data to this register causes data to be written to Transmitter FIFO. Reading data from this register causes data to be received from Receiver FIFO.

9.10.6.2 CIR Interrupt Enable Register (IER)

The IER, an 8-bit **read/write** register, is to enable the CIR interrupt request.

Address: Base Address + 1h

Bit	R/W	Default	Description
7	R/W	0b	Transmitter Data Output Select (TX_sel) This bit is to select transmitter data output. 0: CIRTX1 (Default) 1: CIRTX2
6	R/W	0b	Receiver Data Input Select (RX_sel) This bit is to select receiver data input. 0: CIRRX1 (Default) 1: CIRRX2
5	R/W	0b	Reset The function of this bit is software reset. Writing "1" to this bit resets register DR, IER, TCR1, BDLR, BDHR and IIR and then it will be self-cleared to the initial value.
4	R/W	0b	Baud Rate Register Enable (BR) This bit is to control whether the baud rate register can enable read/write function or not. 1: Enable 0: Disable
3	R/W	0b	Interrupt Enable Control (IEC) This bit is to control whether the interrupt function can be enabled or not. 1: Enable 0: Disable
2	R/W	0b	Receiver FIFO Overrun Interrupt Enable (RFOIE) This bit is to control Receiver FIFO Overrun Interrupt request. 1: Enable 0: Disable
1	R/W	0b	Receiver Data Available Interrupt Enable (RDAIE) This bit is to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in FIFO exceed the FIFO threshold level. 1: Enable 0: Disable
0	R/W	0b	Transmitter Low Data Level Interrupt Enable (TLDLIE) This bit is to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in FIFO are less than the FIFO threshold Level. 1: Enable 0: Disable

9.10.6.3 CIR Receiver Control Register (RCR)

The RCR, an 8-bit read/write register, is to control the CIR Receiver.

Address: Base Address + 2h

Bit	R/W	Default	Description
7	R/W	0b	Receiver Data without Sync. (RDWOS) This bit is to control the sync. logic for received data. Set this bit to "1" to obtain the received data without sync. logic. Set this bit to "0" to obtain the received data with sync. logic.
6	R/W	0b	High-Speed Carrier Frequency Select (HCFS) This bit is to select the carrier frequency between the high-speed and low-speed. 0: 30-58 kHz (Default) 1: 400-500 kHz
5	R/W	0b	Receiver Enable (RXEN) This bit is to enable the Receiver function. Receiver Enable and RXACT will be activated if the selected carrier frequency is received. 1: Enable 0: Disable
4	R/W	0b	Receiver Demodulation Enable (RXEND) This bit is to control the Receiver Demodulation logic. If the Receiver device can not demodulate the correct carrier, set this bit to "1" to enable it. 1: Enable 0: Disable
3	R/W	0b	Receiver Active (RXACT) This bit is to control the Receiver operation. This bit is set to "0" when the Receiver is inactive. This bit will be set to "1" when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with the correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Write a "1" to this bit to clear the Receiver Active condition and make the Receiver enter the inactive mode.
2-0	R/W	001b	Receiver Demodulation Carrier Range (RXDCR[2:0]) These three bits are to set the tolerance of the Receiver. For the detailed demodulation carrier frequency, please refer to Table 9-18. Receiver Demodulation Low Frequency (HCFS = 0) and Table 9-19. Receiver Demodulation High Frequency (HCFS = 1) on page 161 and 161.

9.10.6.4 CIR Transmitter Control Register 1 (TCR1)

The TCR1, an 8-bit **read/write** register, is used to control the Transmitter.

Address: Base Address + 3h

Bit	R/W	Default	Description																		
7	R/W	0b	FIFO Clear (FIFOCLR) Writing a “1” to this bit clears FIFO. This bit is then self-cleared to “0”.																		
6	R/W	0b	Internal Loopback Enable (ILE) This bit is to execute internal loopback for test and must be “0” in normal operation. 1: Enable 0: Disable																		
5-4	R/W	0b	FIFO Threshold Level (FIFOTL) These two bits are used to set the FIFO threshold level. The FIFO length is 32 bytes for TX or RX function (ILE = 0) in normal operation and 16 bytes for both TX and RX in the internal loopback mode (ILE = 1). <table style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">16-Byte Mode</td> <td style="text-align: center;">32-Byte Mode</td> </tr> <tr> <td style="text-align: center;">00</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">01</td> <td style="text-align: center;">3</td> </tr> <tr> <td style="text-align: center;">10</td> <td style="text-align: center;">7</td> </tr> <tr> <td style="text-align: center;">11</td> <td style="text-align: center;">13</td> </tr> <tr> <td></td> <td style="text-align: center;">1 (Default)</td> </tr> <tr> <td></td> <td style="text-align: center;">7</td> </tr> <tr> <td></td> <td style="text-align: center;">17</td> </tr> <tr> <td></td> <td style="text-align: center;">25</td> </tr> </table>	16-Byte Mode	32-Byte Mode	00	1	01	3	10	7	11	13		1 (Default)		7		17		25
16-Byte Mode	32-Byte Mode																				
00	1																				
01	3																				
10	7																				
11	13																				
	1 (Default)																				
	7																				
	17																				
	25																				
3	R/W	0b	Transmitter Run Length Enable (TXRLE) This bit controls the Transmitter Run Length encoding/decoding mode, which condenses a series of “1” or “0” into one byte with the bit value stored in bit 7 and number of bits minus 1 in bit 6-0. 1: Enable 0: Disable																		
2	R/W	0b	Transmitter Deferral (TXENDF) This bit is to avoid Transmitter underrun condition. When this bit is set to “1”, the Transmitter FIFO data will be kept until the transmitter time-out condition occurs, or FIFO reaches full.																		
1-0	R/W	0b	Transmitter Modulation Pulse Mode (TXMPM[1:0]) These two bits are to define the Transmitter modulation pulse mode. TXMPM[1:0] Modulation Pulse Mode C_pls mode (Default): Pulses are generated continuously for the entire logic 0 bit period. 8_pls mode: 8 pulses are generated for each logic 0 bit. 6 pls mode: 6 pulses are generated for each logic 0 bit. 11: Reserved.																		

9.10.6.5 CIR Transmitter Control Register (TCR2)

The TCR2, an 8-bit **read/write** register, is to determine the carrier frequency.

Address: Base Address + 4h

Bit	R/W	Default	Description																											
7-3	R/W	01011b	Carrier Frequency (CFQ[4:0]) These five bits are to determine the modulation carrier frequency. Please refer to the following table.																											
2-0	R/W	100b	Transmitter Modulation Pulse Width (TXMPW[2:0]) These three bits are to set the Transmitter Modulation pulse width. The duty cycle of the carrier will be determined according to the setting of the carrier frequency and the selection of Transmitter Modulation pulse width. <table> <thead> <tr> <th>TXMPW[2:0]</th> <th>HCFS = 0</th> <th>HCFS = 1</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>001</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>010</td> <td>6 μs</td> <td>0.7 μs</td> </tr> <tr> <td>011</td> <td>7 μs</td> <td>0.8 μs</td> </tr> <tr> <td>100</td> <td>8.7 μs</td> <td>0.9 μs (Default)</td> </tr> <tr> <td>101</td> <td>10.6 μs</td> <td>1.0 μs</td> </tr> <tr> <td>110</td> <td>13.3 μs</td> <td>1.16 μs</td> </tr> <tr> <td>111</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	TXMPW[2:0]	HCFS = 0	HCFS = 1	000	Reserved	Reserved	001	Reserved	Reserved	010	6 μ s	0.7 μ s	011	7 μ s	0.8 μ s	100	8.7 μ s	0.9 μ s (Default)	101	10.6 μ s	1.0 μ s	110	13.3 μ s	1.16 μ s	111	Reserved	Reserved
TXMPW[2:0]	HCFS = 0	HCFS = 1																												
000	Reserved	Reserved																												
001	Reserved	Reserved																												
010	6 μ s	0.7 μ s																												
011	7 μ s	0.8 μ s																												
100	8.7 μ s	0.9 μ s (Default)																												
101	10.6 μ s	1.0 μ s																												
110	13.3 μ s	1.16 μ s																												
111	Reserved	Reserved																												

Table 9-17. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS = 0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	38 kHz (default)	480 kHz (default)
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

Table 9-18. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		(Hz)
	CFQ	Min.	Max.	Min.	Max.								
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	35.63	40.38	33.25	42.75	30.88	45.13	28.5	47.5	26.13	49.88	23.75	52.25	38k
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 9-19. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		(Hz)
	CFQ	Min.	Max.	Min.	Max.								
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	480k
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

9.10.6.6 CIR Transmitter Status Register (TSR)

The TSR, an 8-bit **read only** register, provides the Transmitter FIFO status.

Address: Base Address + 5h

Bit	R/W	Default	Description
7-6	R	-	Reserved
5-0	R	000000b	Transmitter FIFO Byte Count (TXFBC[5:0]) Return the number of bytes left in the Transmitter FIFO.

9.10.6.7 CIR Receiver FIFO Status Register (RSR)

The RSR, an 8-bit **read only** register, provides the Receiver FIFO status.

Address: Base Address + 6h

Bit	R/W	Default	Description
7	R	0b	Receiver FIFO Time-out (RXFTO) This bit will be set to "1" when a Receiver FIFO time-out condition occurs. Followings are the conditions required for the occurrence of Receiver FIFO time-out: 1. At least one byte of data are queued in the Receiver FIFO for more than 64 ms. 2. The Receiver has been inactive (RXACT=0) for more than 64 ms.
6	-	-	Reserved
5-0	R	000000b	Receiver FIFO Byte Count (RXFBC) Return the number of bytes left in Receiver FIFO.

9.10.6.8 CIR Baud Rate Divisor Low Byte Register (BDLR)

The BDLR, an 8-bit **read/write** register, is to program the CIR Baud Rate clock.

Address: Base Address + 5h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	Baud Rate Divisor Low Byte (BDLR[7:0]) These bits, for dividing the Baud Rate clock, are the low byte of the register.

9.10.6.9 CIR Baud Rate Divisor High Byte Register (BDHR)

The BDHR, an 8-bit read/write register, is used to program the CIR Baud Rate clock.

Address: Base Address + 6h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	Baud Rate Divisor High Byte (BDHR[7:0]) These bits, for dividing the Baud Rate clock, are the high byte of the register.

Baud rate divisor = 115200 / baud rate

Ex1: 2400 bps → 115200 /2400 = 48 → 48(d) = 0030(h) → BDHR = 00h, BDLR = 30h

Ex2: bit width = 0.565 ms (1770 bps (115200 / 1770 = 65(d) = 0041(h)) (BDHR = 00(h), BDLR = 41(h))

9.10.6.10 CIR Interrupt Identification Register (IIR)

The IIR, an 8-bit register, is to identify the pending interrupt.

Address: Base address + 7h

Bit	R/W	Default	Description
7-3	-	-	Reserved
2-1	R	00b	Interrupt Identification These two bits are to identify the source of the pending interrupt. IIR[1:0] Interrupt Source 00 No interrupt 01 Transmitter Low Data Level Interrupt 10 Receiver Data Stored Interrupt 11 Receiver FIFO Overrun Interrupt
0	R	1b	Interrupt Pending This bit will be set to “1” while an interrupt is pending.

9.11 Shared Memory Flash Interface Bridge (SMFI)

9.11.1 Overview

The bridge provides the host to access the shared memory. It also provides EC code address space mapped into host domain address space, and locking mechanism for read/write protection.

9.11.2 Features

- Behaves as a LPC/FWH memory device (HLPC)
- Supports memory mapping between host domain and EC domain
- Supports read/write(program/erase) flash operations and protection mechanism
- Supports two shared memory access paths: host and EC
- Supports serial flash and up to 16M bytes

9.11.3 Function Description

9.11.3.1 Supported Interface

IT8733/SMFI can behave as a LPC/FWH memory device on LPC bus connected to the host Southbridge and this function is abbreviated as HLPC.

IT8733/SMFI can behave as an SPI memory slave on SPI bus connected to host Southbridge and this function is abbreviated as HSPI.

9.11.3.2 Supported Flash

IT8733 – Serial Flash:

Requirement:

Only one serial flash can be attached.

Table 9-20. SPI Flash Frequency Requirement

PLLREQR= 0011b	PLLREQR= 0101b	PLLREQR= 0111b
33 MHz	48 MHz	66 MHz

Note:

If HSPI is enabled or SPIFR = 00b, the supported frequency of “Read (03h)” instruction of the selected SPI flash device must meet the requirement shown in this table, too.

9.11.3.3 HLPC: Host Translation

The SMFI provides an HLPC interface between the host bus and the M bus. The flash is mapped into the host memory address space for host accesses. The flash is also mapped into the EC memory address space for EC accesses.

An M bus transaction is generated by the host bus translations and has the following three types:

- 8-bit LPC Memory Read/Write
- 8-bit FWH Read/Write
- 8-bit Host-Indirect Memory Read/Write

After the LPC address translation is done, the host memory transaction is forwarded to M-bus (flash interface) if it is accessing an unprotected region. The host side can't issue a write transaction until the firmware write 1 to HOSTWA bit SMECCS register.

9.11.3.4 HLPC: Memory Mapping

The host memory addresses are mapped into the following regions shown in the following table. Some regions are always mapped and some are mapped only when the corresponding register is active. And these regions may be mapped into the same range in the flash space. See also Table 3-1 on page 8.

Table 9-21. Mapped Host Memory Address

Memory Address Range (byte)	Region Description
FFC0_0000h-FFFF_FFFFh	386 Mode BIOS Range This is the memory space whose maximum value is up to 4M bytes. If the flash size defined in FMSSR register is smaller than 4M bytes, the remaining space is treated as “Out of Range”,
000F_0000h-000F_FFFFh	Legacy BIOS Range The total is 64K inside lower 1M legacy BIOS range.
000E_0000h-000E_FFFFh	Extended Legacy BIOS Range The total is 64K inside lower 1M legacy BIOS range.

The following memory transactions are based on LPC, FWH or I/O Cycles which are valid only when corresponding HBREN bit in HCTRL2R register is enabled.

Legacy BIOS Range

Always handle.

Extended Legacy BIOS Range

Handle only when BIOSEXTS bit in SHMC register is active. Otherwise, transactions are ignored.

386 Mode BIOS Range

Always handle.

Host-Indirect Memory Address

Host-Indirect Memory Cycles are memory transactions based on LPC I/O Cycles.

This address specified in SMIMAR3-0 is used as follows:

Translated 32-bit host address = { SMIMAR3[7:0], SMIMAR2[7:0], SMIMAR1[7:0], SMIMAR0[7:0] }

9.11.3.5 HLPC: Host-Indirect Memory Read/Write Transaction

The following I/O mapped registers can be used to perform an M bus transaction using an LPC I/O transaction:

- **Host-Indirect Memory Address registers (SMIMAR 3-0)**

Stand for host address bit 31 to 0.

- **Host-Indirect Memory Data register (SMIMDR)**

Stand for read or write data bit 7 to 0.

When LPC I/O writes to SMIMDR register, SMFI begins a flash read with SMIMAR3-0 as the addresses. IT8733 responds Long-Waits until the transaction on M-bus (flash interface) is completed.

When LPC I/O read cycle from SMIMDR register begins a flash write with using the SMIMAR3-0 as the address. The data back from SMIMDR register is used to complete the LPC I/O read cycle.

Host-Indirect memory read/write transactions use the same memory mapping and protection mechanism as the LPC memory read/write transactions.

9.11.3.6 EC-Indirect Memory Read/Write Transaction

R8032TT in IT8733 can access full flash address range via "MOVX" instruction.

This kind of access is useful to

1. read flash ID for EC BIOS.
2. customize user-defined flash programming interface.
3. put extra BIOS data outside EC 64K.

- **EC-Indirect Memory Address registers (ECINDAR3-0)**

Stand for flash address bit 31 to 0.

- **EC-Indirect Memory Data register (ECINDDR)**

Stand for read or write data bit 7 to 0.

- **EC-Indirect Read Mode**

The EC firmware can read the flash byte located at the flash address combined by ECINDAR2-0 from ECINDDR when ECINDAR3 is 00h

- **EC-Indirect Follow Mode**

For serial flash, the way to access whole flash is performed by EC-Indirect Follow Mode.

EC-Indirect Follow Mode is enabled after

1. Writing 0Fh to ECINDAR3 register.

EC-Indirect Follow Mode is disabled after

1. Writing 00h to ECINDAR3 register.

In EC-Indirect Follow Mode,

1. Writing 00h to EC-Indirect Memory Address FFFF_FExxh generates FSCE# with high level.
2. Writing data to EC-Indirect Memory Address FFFF_FDxxh generates FSCE# with low level and FMOSI with written data.
3. Reading data from EC-Indirect Memory Address FFFF_FDxxh generates FSCE# with low level and read data from FMISO.
4. All of the above actions are clocked by 8 FSCK clock-ticks and FSCK is stopped in other cases.

9.11.3.7 HSPI: Host Translation

HSPI function can behave as an SPI memory slave and it supports the listed instructions below if the attached SPI flash supports it.

For FREAD instruction, it's converted to READ instruction by HSPI function.

For instructions except FREAD, they are not converted by HSPI function.

Unsupported instructions are not certain to be bridged.

Table 9-22. SPI Instruction List Supported by HSPI

Instruction	Hex Code
Write Status (WRSR)	01h
Page Program (PROG)	02h (up to 64B)
Read Data (READ)	03h (up to 64B)
Write Disable (WRDI)	04h
Read Status (RDSR)	05h
Write Enable (WREN)	06h
Fast Read (FREAD)	0Bh
Dual Out Fast Read (DOFR)	3Bh
Enable Write Status (EWSR)	50h
JEDEC ID (3-byte)	9Fh
Chip/Bulk Erase (ERASE)	60h,C7h
Sector/Block Erase (ERASE)	20h,52h,D7h,D8h
Debug Instruction	86h,87h

Table 9-23. Approval HSPI Setting

	HSPI inst./min freq.	SPI flash's required inst./freq. ^{NOTE1}	SPIFR	PLLREQ	SCEMINHW	HSRS
Setting 1	All/20MHz	READ(03h) / 33MHz	00b ^{NOTE2}	0011b	011b (default)	00b (default)
Setting 2	FREAD/33MHz Otherwise/20MHz DOFR isn't supported	1. READ(03h) / 33MHz, and 2. FREAD(0Bh) / 66MHz, and 3. Others / 66MHz	01b ^{NOTE3}	0111b	011b (default)	00b (default)
Setting 3	FREAD/33MHz Otherwise/20MHz DOFR isn't supported	1. READ(03h) / 33MHz, and 2. Dual (BBh) / 33MHz	11b	0011b	011b (default)	00b (default)
Setting 4	DOFR/50MHz Otherwise/20MHz FREAD isn't supported	1. READ(03h) / 33MHz, and 2. DIOFR (BBh) / 66MHz, and 3. Others / 66MHz	11b	0111b	011b (default)	00b (default)
Setting 5	All/20MHz ^{NOTE3}	1. READ(03h) / 33MHz, and 2. FREAD(0Bh) / 66MHz, and 3. Others / 66MHz	01b ^{NOTE2}	0111b	011b (default)	10b
Setting 6	All/20MHz ^{NOTE3}	1. READ(03h) / 33MHz, and 2. Dual (BBh) / 33MHz	11b	0011b	011b (default)	01b
Setting 7	DOFR/33MHz Otherwise/20MHz FREAD isn't supported	1. READ(03h) / 33MHz, and 2. DIOFR (BBh) / 66MHz, and 3. Others / 66MHz	11b	0111b	011b (default)	01b

Note 1: This shown flash frequency is for the external clock.
Note 2: The SPIFR values, 01b, 10b and 11b, are optional.
Note 3: The "Fast Read Support" bit in FLCOMP register of PCH must be set.

In the sleep mode, on-chip PLL is disabled but HSPI function still can work well regardless of the sleep mode.

Followings are the requirements/limitations for the HSPI function:

- The placement of the EC is close to the Southbridge and the placement of the serial flash is close to the EC.
- Supports Mode 0 (clock phase is 0 and data is latched on the rising edge of the clock).
- Supports Southbridge of Intel ICH/PCH.
- HSPI function and HLPC function can not operate simultaneously.
- PCH's "Controller Link Power" must be the same as VSTBY of EC.
- The byte count of PROG instructions must be equal to/less than 64.
- The result of EC-Indirect Follow Mode is uncertain since an HSPI cycle may break a processing EC-Indirect Memory cycle. EC-Indirect Follow Mode can be performed if a WIP instruction is being deferred

- or before HSPI is enabled. EC-Indirect Read Mode works well with HSPI.
- The only valid instruction after a WIP instruction is RDSR instruction until WIP bit is cleared.
- Whether the SPI flash is in the WIP status can only be detected by polling RDSR instruction and can not be detected by a hardware pin (BUSY#) on the SPI flash if it has one.
- Maybe one more GPIO is required to be connected to RSMRST# or CLPWROK in ICH to make sure that the first SPI memory cycle comes after EC finishes initialization.
- If it's in deferred mode and the leading two bytes of JEDEC ID of flash is "BFh 25h", PROG2AAIW is enabled and multiple bytes followed after PROG instruction on HSPI side are translated to AAIW instruction on FSPI side.

9.11.3.8 Flash Shared between Host and EC Domains

A hardware arbiter handles flash read/write translation between the host and EC side.

- HLPC**

IT8733 bridges the memory cycles on LPC bus and bridges them to the attached SPI flash. The SMFI internal flash controller performs interleave mechanism control to let the flash fetch for the host and EC side.

It may respond to Long-Waits on LPC bus or freeze 8032 code-fetch due to interleave mechanism. There is no internal hard-wired mechanism to monitor whether the attached SPI flash is in the WIP (busy) state caused by the WIP instruction from the host.

When the host wants to erase or program the flash via Follow Mode 0, the signaling interface (Semaphore Write or KBC/PMC extended command such as 62h/66h command) notifies the firmware to write 1 to HOSTWA bit in SMECCS register. EC 8032 will fail to code fetch due to the WIP (busy) state caused by erasing/programming so Scratch ROM must be applied. Once the host accessing to the flash is completed, the host should indicate this to the EC, allowing EC to clear HOSTWA bit and resume normal operation. The EC can clear HOSTWA bit at any time, and prevent the host from issuing any erase or program operations.

When the host wants to erase or program the flash via Follow Mode 1, it is not necessary for the firmware to shadow code to the SRAM if the EC code is not modified since there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash. Refer to section 9.11.3.17 HLPC: Serial Flash Programming on page 174 for its description and limitation.

Defer SPI WIP Instruction in Follow Mode:

This WIP instruction received by the EC will not be bridged to the flash immediately.

It returns Long-Waits to the SouthBridge.

It issues INT59 to notify the firmware in default; however, if the start addresses of this WIP and the preceding WIP instruction are within the same 4K block boundary (address bit 23-12 of this and preceding cycle are identical), INT59 will be omitted.

The firmware may check the 8-bit SPI instruction (DSINST register) and SPI address bit 23-12 (DSADR1 and DSADR2 register) then decide to allow/inhibit this WIP instruction by writing 1/0 to DISS bit in HINSTC1 register. This is also known as software write protection of HSPI. The firmware can not modify the programmed data in the deferred mode.

- **HSPI**

IT8733 bridges the memory cycles from the Southbridge interface to the attached SPI flash. For each READ/FREAD instruction, SMFI freezes the code-fetch of 8032 and serves the host request as the highest priority.

For each ERASE/PROG/WRSR instruction (WIP instruction), there are two modes provided to EC, non-deferred mode and deferred mode. The mode switch (ENDI field in HINSTC1 register) must be finished during EC initialization and can not be modified after writing 1 to SMSS bit in HCTRL2R register.

Unlike HLPC follow mode 0, there is an internal hard-wired mechanism to monitor whether the attached SPI flash is in the WIP (busy) state caused by the WIP instruction from the host through HSPI interface. It means that the code-fetch of 8032 is automatically resumed by the hardware circuit.

Non-deferred Mode of WIP Instruction (Default):

This WIP instruction is bridged to the flash without notifying the firmware.

Pending time of code-fetch of 8032 is about “WIP instruction cycle time” + “flash busy time”.

(where “flash busy time” is “erase time” or “programming time” defined on the flash datasheet.)

The firmware doesn't care WIP instructions; however, code-fetch of uC may be stopped for a long time without notification while programming BIOS region, so the host flash utility should notify EC through KBC/PMC extended command such as 62h/66h command.

It is not necessary for the firmware to shadow code to the SRAM if the EC code is not modified since there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash.

Deferred Mode of WIP Instruction (Recommended):

This WIP instruction received by the EC will not be bridged to the flash immediately.

Pending time of code-fetch of 8032 is about “flash busy time”.

It returns the WIP (busy) state to the Southbridge.

It issues INT59 to notify the firmware. If it's in Sleep mode, INT59 will be pended until exiting Sleep mode.

The firmware may check the 8-bit SPI instruction (DSINST register) and SPI address bit 23-12 (DSADR1 and DSADR2 register) and shadow EC firmware to SRAM if necessary, then bridge this WIP instruction by writing 11b to DISS and DISSV bit in HINSTC1 register.

The firmware can not modify the programmed data in the deferred mode.

The firmware can decide when to bridge the WIP instructions, e.g. only bridge them if the firmware isn't executing critical code.

The firmware can know this WIP instruction is initiated by BIOS/ME/GbE... by checking its start address and then decides the corresponding actions (e.g. shadow code to the SRAM).

It is not necessary for the firmware to shadow code to the SRAM if the EC code is not modified since there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash.

Recommended Code during Initialization:

1. Use EC-Indirect Memory cycle to read JEDEC ID of the flash.

Check whether this flash requires EWSR+WRSR instructions to clear BP0, BP1 ... registers in the flash before erase/program instructions, for example, if the leading two bytes of JEDEC ID of flash is “BFh 25h”.

If it's true and it's non-deferred mode, use EC-Indirect Memory cycle to send EWSR+WRSR instructions to the flash.

Refer to 10.1.10.7 Code Snippet of Sending EWSR+WRSR during HSPI Init on page 276.

2. If deferred mode is applied, then

Method A: write 11b to ENDI field in HINSTC1 register, write 1b to DIALWQ bit in HSPICTRL3R, write 1b to DISWRSR bit in HSPICTRL3R, and write 1b to bit 3 in IER7 (Enable INT59).
Method B: write 11b to ENDI field in HINSTC1 register, write 1b to DISWREN bit in HSPICTRL3R, write 1b to DISWRSR bit in HSPICTRL3R, and write 1b to bit 3 in IER7 (Enable INT59).

If non-deferred mode is applied and JEDEC ID is not “BFh 25h”, write 1b to DISWRSR bit in HSPICTRL3R.

3. Set function 1 of GPH3, GPH4, GPH5 and GPH6.
4. Write 0b to SPIFR bit in FLHCTRL1R register (Don't use Fast Read for the flash)
5. Write 0Eh to FMSS field in FMSSR register (2'24 flash size)
6. Write 1b to SMSS bit in HCTRL2R register (Select HSPI)
7. Inactive RSMRST# then ICH may send the first SPI cycle.

Recommended Code in INT59 Interrupt Service Routine for Deferred Mode:

1. Check whether the EC code will be destroyed by this WIP cycle.
If it's true, shadow the EC code to Scratch SRAM.
- 2.

Method A, continued: If JEDEC ID is “BFh 25h”, use EC-Indirect Memory cycle to send EWSR+WRSR+WREN instruction to the flash. If JEDEC ID is not “BFh 25h”, use EC-Indirect Memory cycle to send WREN instruction to the flash. Refer to 10.1.10.8 Code Snippet of Sending WREN within ISR of INT59 on page 277.
Method B, continued: Nothing in this step.

3. Write 11b to DISS and DISSV bit in HINSTC1 register.

9.11.3.9 Host Access Protection

HLPC:

It provides host hardware read protection, hardware write protection and software write protection.

For the hardware write protection, there are two sets of protective ranges provided and each can be up to 512K bytes of protective size.

For the software write protection, it provides a flexible and customized protective range in the full 16M SPI flash address range.

The hardware read/write protection is controlled by two sets of registers.

Set 0: P0ZR, P0BA0R and P0BA1R registers for hardware read/write protection

Set 1: P1ZR, P1BA0R and P1BA1R registers for hardware read/write protection

Common: HINSTC2 for hardware write protection

The software write protection is controlled by the deferred mode of the WIP instruction.

Refer to HINSTC1, DSINST, DSADR1 and DSADR2 registers

HSPI:

The same mechanism as that of HLPC.

9.11.3.10 Serial Flash Performance Consideration

Clock-tick number spent for each cycle = 8

Clock-tick number spent for branching instruction = $M + (4 + N) \times 8$

$M = \text{FSCE\# Min High Width} = 1 + \text{SCEMINHW}$

(SCEMINHW field in FLHCTRL2R register)

$N = 1$ if "Fast Read" (SPIFR bit in FLHCTRL1R register)

The selection of these registers depends on the flash specification.

Note that the flash clock frequency is FreqPLL.

(FreqPLL is listed in Table 12-1. Clock Timing Parameter on page 355)

Host LPC has very poor read performance on M-bus if HOSTWA bit in SMECCS register is set.

9.11.3.11 Response to a Forbidden Access

A forbidden access is generated by a translated host address which is protected.

HLPC:

The response to the host bus is according to HERES field in SMECCS register.

HSPI:

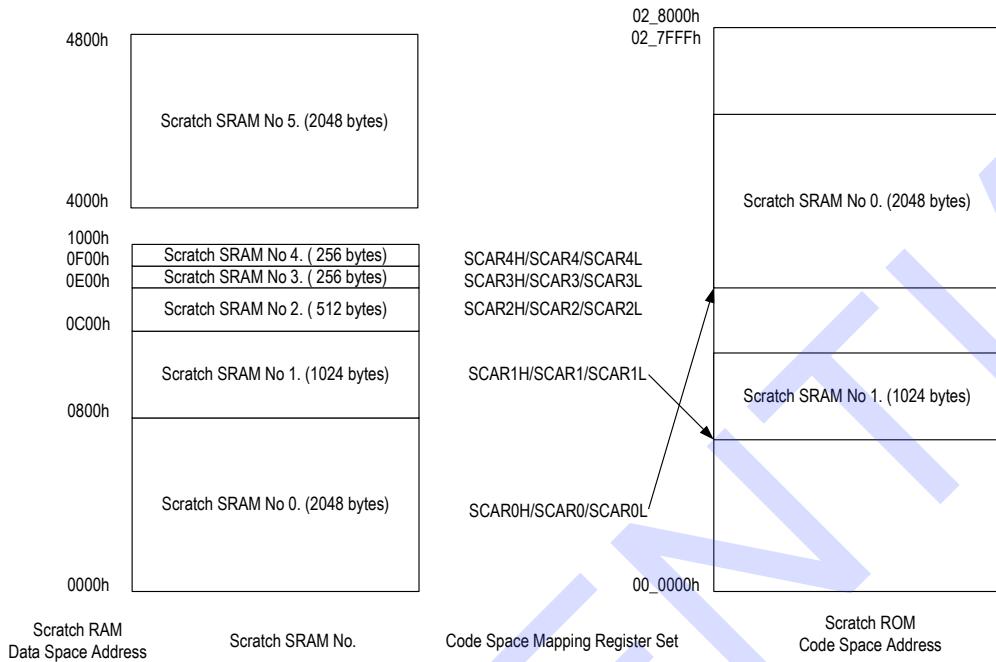
SMFI will not bridge this WIP instruction to the flash.

9.11.3.12 Scratch SRAM

There are five internal Scratch SRAMs No 0-4 which are always mapped into data space and may be mapped into code space if their corresponding code space mapping registers are enabled. It also means that Scratch SRAM may be mapped into data and code space at the same time and the firmware on Scratch ROM can access the same Scratch RAM. It is called Scratch RAM when being located at data space (default after reset) and called Scratch ROM when being located at code space.

Each of these five Scratch SRAM can be mapped into code space with any base addresses without the boundary limit. More than one Scratch SRAM No. can be mapped into code space with an overlay range.

Figure 9-14. Scratch SRAM in Data Space



Each Scratch SRAM No. has three corresponding code space mapping registers in Figure 9-14. Scratch SRAM in Data Space To enable a Scratch SRAM to be mapped into code space, refer to the following steps with code space mapping registers.

Scratch SRAM No.5 supports data R/W only.

For Scratch SRAM No. 0:

SC0A17-0 field (18-bit) is the address of Scratch SRAM No. 0 and has been translated according to “Mapped Flash Address Range” field in Table 3-2. EC/Flash Mapping on page 8. Also refer to ECBB field in FECBSR register on page 181.

The base address in SC0A17-0 field is only valid if it is between 00_0000h and 02_7FFFh.

To enable the code space mapping of Scratch No. 0:

Make SC0A17-0 field is between 00_0000h and 02_7FFFh.

To disable the code space mapping of Scratch No. 0:

Write 11b to SC0A17-16 field.

Scratch SRAM No.0 is always located in data space regardless of mapping into code space.

So is Scratch SRAM No. 1-4.

This SSMC bit in FBCFG register is OBSOLETE. This register bit is only used to be compatible with old IT8510 firmware and should not be used in new firmware.

9.11.3.13 DMA for Scratch SRAM

DMA (Direct Memory Access) is used to shadow flash content of a specified address range inside code space to Scratch SRAM. The performance of DMA is much better than "MOVC-MOVX" steps.

To enable DMA operation to Scratch SRAM No. 0, please follow the steps below:

1. Write data to SCAR0H register with wanted SC0A17-16 field and 1 to NSDMA bit.
2. Write data to SCAR0L register with wanted SC0A7-0 field.
3. Write data to SCAR0M register with wanted SC0A15-8 field.
4. Write data to SCAR0H register with wanted SC0A17-16 field and 0 to NSDMA bit.

DMA operation is started and code space mapping is enabled after DMA operation is finished.

If the firmware wants to modify the mapped base address in code space, more steps below should be taken:

5. Write data to SCAR0H register with 11b to SC0A17-16 field.
Disable code space mapping first since SC0A17-0 are modified in three writings and may be invalid before writing is completed.
6. Write data to SCAR0M/SCAR0L register with wanted SC0A15-0 field.
7. Write data to SCAR0H register with wanted SC0A17-16 field.
Enable code space mapping after this step.

So is Scratch SRAM No. 1-4.

See also 10.1.10.4 Code Snippet of Copying Flash Content to Scratch ROM (DMA) on page 275.

9.11.3.14 HLPC: Flash Programming via Host LPC Interface with Scratch SRAM

When programming flash via HLPC Follow Mode 0 is processing, the flash will be busy and code fetch from flash by 8032 and will be invalid and cause 8032 fail to execute instructions. It means the firmware must copy necessary instructions from code space to Scratch SRAM, enable mapping Scratch SRAM to Scratch ROM, and jump to Scratch ROM before programming flash.

Flash Programming Steps:

- (a) The host side communicates to the EC side via KBC/PMC extended or semaphore registers
- (b) EC side: Write 1 to HOSTWA bit in SMECCS register
- (c) EC side: Copy necessary code to Scratch RAM (by MOVC-MOVX steps or DMA)
- (d) EC side: Enable code space mapping of Scratch SRAM
- (e) EC side: Make the host processor enter SMM mode if necessary
- (f) EC side: Jump instruction to Scratch ROM
- (g) Host side: Set related memory-write registers in South-Bridge
- (h) Host side: Start flash programming
- (i) End flash programming and reset EC domain if necessary.
(Refer to section 5.2 on page 32)

Note: Do not let EC enter Idle/Doze/Sleep mode while processing flash programming flow.

9.11.3.15 Force 8032 to Code Fetch from Internal SRAM

For serial flash, it may not be accessed immediately after issuing "Release Power Down (ABh)" instruction until a time delay is listed on flash specification.

To make sure there is no access cycle on the flash after waking up from the Sleep mode, the firmware must execute a delay routine in Scratch ROM.

It means that "ORL PCON" instruction, delay routine and interrupt entry (e.g.0013h for INT1#) are all required to be code-fetch from internal SRAM (Scratch).

9.11.3.16 Force 8032 to Clear Dynamic Caches

For serial flash, after the flash is modified by the host program, the dynamic caches have to be cleared since they contain old and invalid cache content. Refer to section 10.1.10.9 Code Snippet of Clearing Dynamic Caches on page 279.

9.11.3.17 HLPC: Serial Flash Programming

There is Follow Mode dedicated for serial flash programming through host LPC interface.

There are mode 0 and 1 for Follow Mode and they can not be enabled at the same time.

In mode 0, there is no internal hard-wired mechanism to monitor the WIP (busy) state of the flash.

In mode 1, there is an internal hard-wired mechanism to monitor the WIP (busy) state of the flash; however, the utility in the host side is still required to poll the flash status via RDSR instruction.

In mode 0, it's necessary for the firmware to shadow code to the SRAM and stop all flash access to let the HLPC occupies the flash arbiter.

In mode 1, it's not necessary for the firmware to shadow code to the SRAM and HLPC interleaves with other flash access issued by the firmware.

In mode 0, if the hardware protection is disabled, the program in the host side can construct any SPI cycle.

In mode 0, if the hardware protection is enabled, the WIP instructions listed in Table 9-24. SPI Instruction List Monitored by HLPC Follow Mode 0, Protection Enabled are monitored by protection logic.

Table 9-24. SPI Instruction List Monitored by HLPC Follow Mode 0, Protection Enabled

Instruction	Hex Code	Note
Program Data (PROG)	02h	Monitored by protection logic.
AAI Program Byte (AAIB/AAI)	AFh	Monitored by protection logic.
AAI Program Word (AAIW/AAI)	ADh	Monitored by protection logic.
Chip/Bulk Erase (ERASE)	60h,C7h	Inhibited by protection logic.
Sector/Block Erase (ERASE)	20h,52h,D7h,D8h	Monitored by protection logic.
Otherwise	-	Not monitored by protection logic.

In mode 1, only some specified instructions are supported.

If the leading two bytes of JEDEC ID of flash is "BFh 25h", "50h 01h" will be sent to the flash before bridging a WIP instruction.

Table 9-25. SPI Instruction List Supported by HLPC Follow Mode 1

Instruction	Hex Code	Note
Program Data (PROG)	02h	Monitored by protection logic. Programming single byte supported. Programming multiple bytes isn't supported.
Read Status (RDSR)	05h	Monitored by protection logic. Reading single status byte supported. Reading multiple status bytes isn't supported.
Chip/Bulk Erase (ERASE)	60h,C7h	Not supported
Sector/Block Erase (ERASE)	20h,52h,D7h,D8h	Monitored by protection logic. Supported
Otherwise	-	Not supported

Follow Mode 0 is enabled after

1. Writing 1 to HOSTWA bit in SMECCS register in the EC side.
2. Writing 00h to LPC/FWH Address FFFF_FExxh in the host side

Follow Mode 0 is disabled after

1. Writing 0 to HOSTWA bit in SMECCS register in the EC side.

Follow Mode 1 is enabled after

1. Writing 1 to HFW1EN bit in HCTRL2R register in the EC side.
2. Writing 00h to LPC/FWH Address FFFF_FExxh in the host side
3. Write 1 to ACP80 bit in SPCTRL1 register to enable LPC_IO-to-FSPI function.

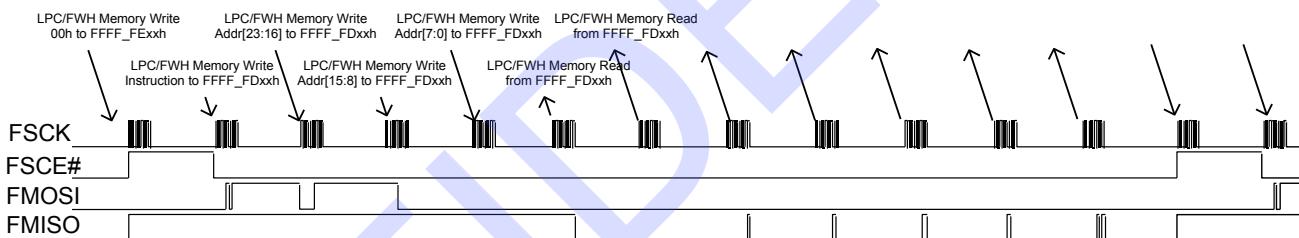
Follow Mode 1 is disabled after

1. Writing 0 to HFW1EN bit in HCTRL2R register in the EC side.

In HLPC Follow Mode,

1. Writing 00h to LPC/FWH Memory Address FFFF_FExxh generates FSCE# with high level.
2. Writing data to LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and FMOSI with written data.
3. Reading data from LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and read data from FMISO.
4. All the above actions are clocked by 8 FSCK clock ticks and FSCK is stopped in other cases.

Figure 9-15. HLPC Follow Mode for Serial Flash (e.g. Fast Read Instruction)



9.11.3.18 LPC_IO-to-FSPI

The “LPC IO-to-FSPI” function is a sub function of HLPC Follow Mode 1. It's enabled if HLPC Follow Mode 1 is enabled and the ACP80 bit in SPCTRL1 register.

Refer to section 0

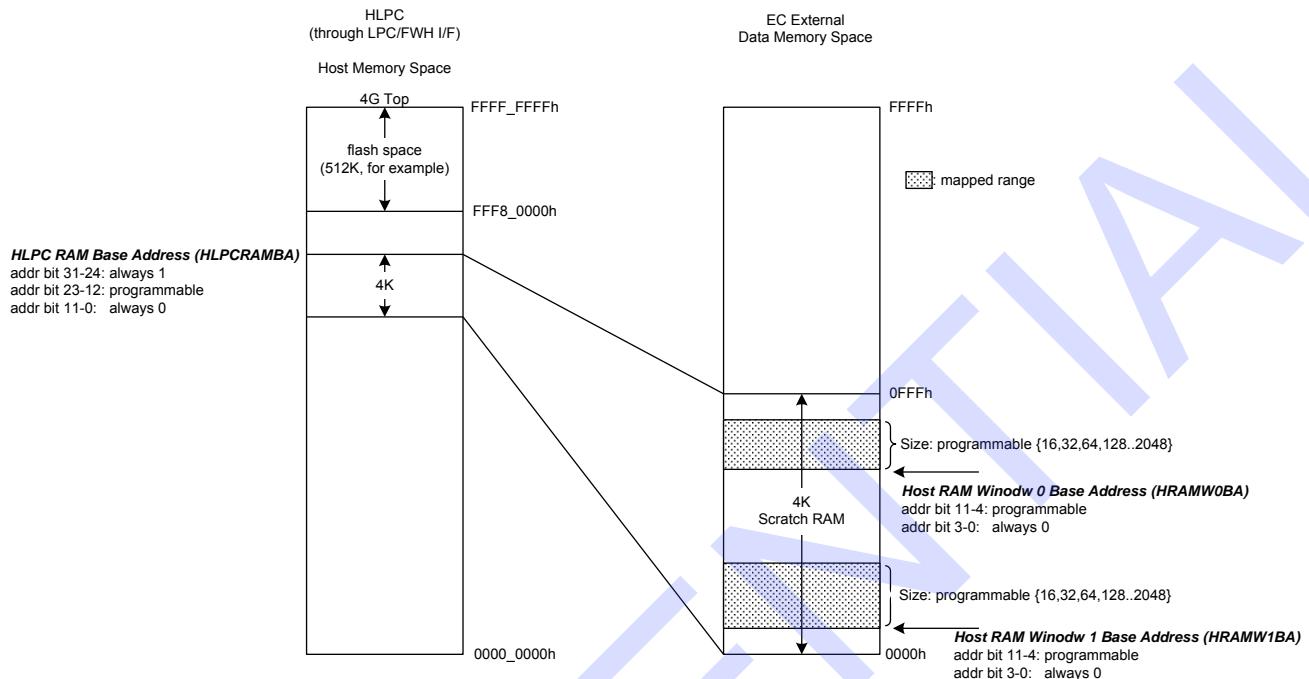
Special Control 3 (SPCTRL3) on page 316.

9.11.3.19 Host Side to EC Scratch RAM (H2RAM)

9.11.3.19.1 HLPC to EC Scratch RAM (H2RAM-HLPC)

- H2RAM can be used by the host side software to access 4K Scratch RAM through LPC Memory/FWH cycles.
- The read/write protection mechanism is also supported by this function.

Figure 9-16. H2RAM-HLPC Mapping



9.11.3.20 SPI Flash Power-on Detection

For some applications (e.g. IT8733 behaves as an SPI memory slave – HSPI), the EC code base address will be located at non-zero address in SPI flash memory.

9.11.3.20.1 16B-signature and Implicit/Explicit EC Code Base Address

A specific 16B-signature is used to locate the EC code base address.

1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th	10 th	11 th	12 th	13 th	14 th	15 th	16 th
A5h	flag	87h	30h	5Ah	5Ah	AAh	AAh	55h or addr	55h or addr						

All contents of the 16 bytes must match those in the table.

8th byte's bit 7:

It must be 1b.

8th byte's bit 6:

0b: Disable.

1b: Suspend internal-to-external clock switching request.

When this bit is set, the internal clock will act as a temporary clock to enable EC to configure some GPIO settings before the external crystal is ready to work.

This bit is available only when the 8th byte's bit 4 is 0.

Refer to section 10.4.3.6 PLL Clock Source Status (PLLCSS) on page 305.

8th byte's bit 5:

It must be 1b.

8th byte's bit 4:

0b: 32.768 kHz is oscillated by the external crystal connected to CK32K and CK32KE pins.

1b: The “Crystal-Free” feature is enabled and 32.768kHz is from the internal clock generator.

8th byte's bit 3:

0b: Use implicit format to describe the EC code base and the 16B-signature must be inside the EC code.

15th and 16th byte must be 55h and 55h and the EC code base is located at the origin of this 4K block of 16B-signature.

For example, let the address of 1st byte be ADDR1[23:0], then the EC code base is located at (ADDR1[23:12] * 2¹²).

1b: Use explicit format to describe the EC code base and the 16B-signature must be outside the EC code.

15th byte indicates the EC code base address bit 23-16.

16th byte indicates the EC code base address bit 15-12.

8th byte's bit 2:

It must be 1b.

8th byte's bit 1-0:

It must be 01b.

1st byte must be located at 16-byte boundary.

For example, let the address of 1st byte be ADDR1[23:0], then ADDR1[3:0] must be 0000b.

The 16B-signature can be located inside or outside the EC code.

If it's inside the EC code, 1st byte must be located at the address 40h, 50h, 60h, ...F0h offset to the EC code base. For example, let the address of 1st byte be ADDR1[23:0], then ADDR1[7:0] must be 40h, 50h, 60h...F0h (interval 10h) and the EC code base is located at (ADDR1[23:12] * 2¹²). Also refer to section 10.1.10.6 Code Snippet of EC Base Signature on page 276.

If it's outside the EC code, 1st byte must be located at the F00h, F10h, F20h, ...FF0h (interval: 10h) in the flash image.

9.11.3.20.2 Detection Sequence

If the EC code base is not at zero, the flash image must match one of the following items (b)-(e), or it is invalid configuration.

The following items are detected step by step and the detection will be aborted if one item is true.

The detection is processed after reset or writing 1 to SCECB bit in HINSTC1 register.

The [addr xxh] represents the 8-bit content at flash address xxh:

- (a) Check the [addr 00h] first. If the content is the jump instruction (LJMP/SJMP/AJMP, or 02h/80h/xxx00001b), then the detection will be finished and the EC code base address will be at flash address 00h.
- (b) Check whether the 16B-signature is found in F00h-FFFh.
- (c) Check the five specific contents of “[addr 00h] = 5Ah, [addr 11h] = A5h, [addr 12h] = F0h, [addr 13h] = 0Fh, [addr 16h] = 04h”. If the expression is true, the EC code base address will be at flash address ([addr 45h] * 100000h + [addr 44h] * 1000h) and 16B-signature must be inside the EC code. It's invalid configuration if it's true but the 16B-signature is not inside the EC code.

For example, if [addr 45h] and [addr 44h] are 12h and 34h respectively, the EC code base address will be at flash address 234000h.

- (d) Scan upward every 4K block to check whether the 16B-signature is within the leading 256 bytes of the 4K block.
If it's true, the EC code base address is the origin of the 4K block and the detection will be aborted, or all flashes will be scanned.

For example, if the 16B-signature is at flash address 2050h, the EC base address will be at flash address 2000h.

(e) If all steps above are not matched, the EC code base address will be at flash address 0000h.

Table 9-26. Corresponding Table of SPI Flash Power-on Detection

	Scanned Address or Scanned Range	Contents	If content is matched, EC code base address wil be at	Note
(a)	[addr 00h]	Jump Instruction (LJMP/SJMP/AJMP, or 02h/80h/xxx00001b)	000000h	It still checks the 16B-signature within 0000h-00FFh, then aborts.
(b)	[addr F00h], [addr F10h], [addr F20h], ... [addr FF0h]	16B-signature with explicit format.	The address described at the 15 th and 16 th byte of the 16B-signature if one of them is true.	Use explicit format.
(c)	[addr 10h] [addr 11h] [addr 12h] [addr 13h] [addr 16h] Leading 256 bytes of ([addr 45h] * 100000h + [addr 44h] * 1000h)	5Ah A5h F0h 0Fh 04h 16B-signature with implicit format.	the base of ([addr 45h] * 100000h + [addr 44h] * 1000h) if all of them are true	Use implicit format.
(d)	Leading 256 bytes of every 4K (1000h) block (e.g. 0000h - 00FFh, 1040h - 10FFh, 2040h - 20FFh, etc.)	16B-signature with implicit format.	the origin of the first matched 4K block if one of them is true.	Use implicit format.
(e)	All 4K blocks	The above contents are not matched.	000000h	

9.11.4 uC Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and uC Interface Registers. This section lists the uC interface. The uC interface can only be accessed by the internal 8032 processor. The base address for SMFI is 1000h.

These registers are listed below.

Table 9-27. uC View Register Map, SMFI

7	0	Offset
	FBIU Configuration (FBCFG)	00h
	Flash Programming Configuration Register (FPCFG)	01h
	Flash EC Code Banking Select Register (FECBSR)	05h
	Flash Memory Size Select Register (FMSSR)	07h
	Shared Memory EC Control and Status (SMECCS)	20h
	Shared Memory Host Semaphore (SMHSR)	22h
	Flash Control Register 1 (FLHCTRL1R)	31h
	Flash Control Register 2 (FLHCTRL2R)	32h
	Reserved	33h
	uC Control Register (UCCTRLR)	34h
	Host Control 2 Register (HCTRL2R)	36h
	HSPI Control Register 2 (HSPICTRL2R)	39h
	HSPI Control Register 3 (HSPICTRL3R)	3Ah
	EC-Indirect Memory Address Register 0 (ECINDAR0)	3Bh
	EC-Indirect Memory Address Register 1 (ECINDAR1)	3Ch
	EC-Indirect Memory Address Register 2 (ECINDAR2)	3Dh
	EC-Indirect Memory Address Register 3 (ECINDAR3)	3Eh
	EC-Indirect Memory Data Register (ECINDDR)	3Fh
	Scratch SRAM 0 Address Low Byte Register (SCAR0L)	40h
	Scratch SRAM 0 Address Middle Byte Register (SCAR0M)	41h
	Scratch SRAM 0 Address High Byte Register (SCAR0H)	42h
	Scratch SRAM 1 Address Low Byte Register (SCAR1L)	43h
	Scratch SRAM 1 Address Middle Byte Register (SCAR1M)	44h
	Scratch SRAM 1 Address High Byte Register (SCAR1H)	45h
	Scratch SRAM 2 Address Low Byte Register (SCAR2L)	46h
	Scratch SRAM 2 Address Middle Byte Register (SCAR2M)	47h
	Scratch SRAM 2 Address High Byte Register (SCAR2H)	48h
	Scratch SRAM 3 Address Low Byte Register (SCAR3L)	49h
	Scratch SRAM 3 Address Middle Byte Register (SCAR3M)	4Ah
	Scratch SRAM 3 Address High Byte Register (SCAR3H)	4Bh
	Scratch SRAM 4 Address Low Byte Register (SCAR4L)	4Ch
	Scratch SRAM 4 Address Middle Byte Register (SCAR4M)	4Dh
	Scratch SRAM 4 Address High Byte Register (SCAR4H)	4Eh
	Protect 0 Base Addr Register 0 (P0BA0R)	4Fh
	Protect 0 Base Addr Register 1 (P0BA1R)	50h
	Protect 0 Size Register (P0ZR)	51h
	Protect 1 Base Addr Register 0 (P1BA0R)	52h
	Protect 1 Base Addr Register 1 (P1BA1R)	53h
	Protect 1 Size Register (P1ZR)	54h
	Deferred SPI Instruction (DSINST)	55h
	Deferred SPI Address 15-12 (DSADR1)	56h
	Deferred SPI Address 23-16 (DSADR2)	57h
	Host Instruction Control 1 (HINSTC1)	58h
	Host Instruction Control 2 (HINSTC2)	59h
	Host RAM Window Control (HRAMWC)	5Ah
	Host RAM Window 0 Base Address (HRAMW0BA[11:4])	5Bh
	Host RAM Window 1 Base Address (HRAMW1BA[11:4])	5Ch
	Host RAM Window 0 Access Allow Size (HRAMW0AAS)	5Dh
	Host RAM Window 1 Access Allow Size (HRAMW1AAS)	5Eh

9.11.4.1 FBIU Configuration Register (FBCFG)

The FBIU (Flash Bus Interface Unit) directly interfaces with the flash device. The FBIU also defines the access time to the flash base address from 00_0000h to 3F_FFFFh (4M bytes).

Address Offset: 00h

Bit	R/W	Default	Description
7	-	0b	Scratch SRAM Map Control (SSMC) 0: Normal 1: Scratch SRAM No. 0, whose size is 2K bytes, is mapped into F800h-FFFFh in code space and overrides the settings in SCAR0H/SCAR0M/SCAR0L register. This bit is OBSOLETE and is only used to be compatible with old IT8510 firmware and should not be used in new firmware. Note that the following is the definition of this register field in IT8510. 0: Scratch RAM (data space). 1: Scratch ROM (code space).
6-2	-	0h	Reserved
1	-	-	Reserved
0	-	-	Reserved

9.11.4.2 Flash Programming Configuration Register (FPCFG)

This register provides general control on banking and flash standby.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	1b	Banking Source Option (BSO) 0: Use 8032 P1[0] and P1[1] as code banking source. 1: Use ECBB[1:0] in FECBSR register as code banking source. Using P1 as banking source has less instruction count since only "MOV" is invoked rather than "MOVX" although T2 and T2EX are used in other bits in P2.
6	R/W	Serial flash: 0b	Auto Flash Standby (AFSTBY) Serial flash: 1: Stop flash access in Idle/Doze/Sleep mode and issue "Deep Power Down (B9h)" instruction before entering Sleep mode and issue "Release Deep Power Down (ABh)" instruction after waking up from Sleep mode. See also section 9.11.3.15 Force 8032 to Code Fetch from Internal SRAM on page 173. 0: Prevent the flash from entering the standby mode
5	R/W	1b	Reserved
4	-	-	Reserved
3-0	R/W	1111b	Reserved

9.11.4.3 Flash EC Code Banking Select Register (FECBSR)

The register is used to select EC banking area Bank 0~3 when BSO =1 in FPCFG register.

Address Offset: 05h

Bit	R/W	Default	Description
7-2	-	0h	Reserved
1-0	R/W	00b	<p>EC Banking Block (ECBB)</p> <p>When ECBB is set to 00, EC code uses conventional code area (maximum 64k) as code memory.</p> <p>Common Bank 32k-byte flash mapping range is from 00_0000h to 00_7FFFh.</p> <p>Bank 0 32k-byte flash mapping range is from 00_8000h to 00_FFFFh.</p> <p>Bank 1 32k-byte flash mapping range is from 01_0000h to 01_7FFFh.</p> <p>Bank 2 32k-byte flash mapping range is from 01_8000h to 01_FFFFh.</p> <p>Bank 3 32k-byte flash mapping range is from 02_0000h to 02_7FFFh.</p> <p>See also Figure 3-1 on page 6.</p> <p>Bits 1-0:</p> <ul style="list-style-type: none"> 00: Select Common Bank + Bank 0 01: Select Common Bank + Bank 1 10: Select Common Bank + Bank 2 11: Select Common Bank + Bank 3 <p>If A15 of 8032 code memory equals to 0, select Common Bank, otherwise select Bank 0, 1, 2 or 3.</p>

9.11.4.4 Flash Memory Size Select Register (FMSSR)

The register provides the selection for the external flash memory size.

Address Offset: 07h

Bit	R/W	Default	Description																																								
7-6	-	0h	Reserved																																								
5-0	R/W	111111b	<p>Flash Memory Size Select (FMSS)</p> <p>These bits select the external flash memory size. These bits only affect the host memory size “seen” by Southbridge and don’t affect address decoder in the EC side. See also Table 3-1. Host/Flash Mapping on page 8.</p> <p>If Southbridge issues LPC Memory Cycles as memory transaction, this field has to be selected so as not to conflict with other memory devices on LPC bus.</p> <p>If Southbridge issues FWH Cycles as memory transaction, there is no conflict issue since each FWH ID has its dedicated 4G memory space.</p> <p>Bits</p> <p>543210 Memory Size (bytes)</p> <table> <tbody> <tr> <td>111111b:</td> <td>4M</td> </tr> <tr> <td>011111b:</td> <td>2M</td> </tr> <tr> <td>001111b:</td> <td>1M</td> </tr> <tr> <td>000111b:</td> <td>512K</td> </tr> <tr> <td>000011b:</td> <td>256K</td> </tr> <tr> <td>000001b:</td> <td>128K</td> </tr> <tr> <td>Or</td> <td></td> </tr> <tr> <td>00h:</td> <td>128K (2^{17})</td> </tr> <tr> <td>02h:</td> <td>256K (2^{18})</td> </tr> <tr> <td>04h:</td> <td>512K (2^{19})</td> </tr> <tr> <td>06h:</td> <td>1M (2^{20})</td> </tr> <tr> <td>08h:</td> <td>2M (2^{21})</td> </tr> <tr> <td>0Ah:</td> <td>4M (2^{22})</td> </tr> <tr> <td>0Ch:</td> <td>8M (2^{23})</td> </tr> <tr> <td>0Eh:</td> <td>16M (2^{24})</td> </tr> <tr> <td>10h:</td> <td>32M (2^{25})</td> </tr> <tr> <td>12h:</td> <td>64M (2^{26})</td> </tr> <tr> <td>14h:</td> <td>128M (2^{27})</td> </tr> <tr> <td>16h:</td> <td>256M (2^{28})</td> </tr> <tr> <td>Otherwise:</td> <td>Reserved</td> </tr> </tbody> </table>	111111b:	4M	011111b:	2M	001111b:	1M	000111b:	512K	000011b:	256K	000001b:	128K	Or		00h:	128K (2^{17})	02h:	256K (2^{18})	04h:	512K (2^{19})	06h:	1M (2^{20})	08h:	2M (2^{21})	0Ah:	4M (2^{22})	0Ch:	8M (2^{23})	0Eh:	16M (2^{24})	10h:	32M (2^{25})	12h:	64M (2^{26})	14h:	128M (2^{27})	16h:	256M (2^{28})	Otherwise:	Reserved
111111b:	4M																																										
011111b:	2M																																										
001111b:	1M																																										
000111b:	512K																																										
000011b:	256K																																										
000001b:	128K																																										
Or																																											
00h:	128K (2^{17})																																										
02h:	256K (2^{18})																																										
04h:	512K (2^{19})																																										
06h:	1M (2^{20})																																										
08h:	2M (2^{21})																																										
0Ah:	4M (2^{22})																																										
0Ch:	8M (2^{23})																																										
0Eh:	16M (2^{24})																																										
10h:	32M (2^{25})																																										
12h:	64M (2^{26})																																										
14h:	128M (2^{27})																																										
16h:	256M (2^{28})																																										
Otherwise:	Reserved																																										

9.11.4.5 Shared Memory EC Control and Status Register (SMECCS)

The following set of registers is accessible only by the EC. The registers are applied to VSTBY. This register provides the flash control and status of a restricted access.

Address Offset: 20h

Bit	R/W	Default	Description
7	R/W	0b	Host Semaphore Interrupt Enable (HSEMIE) It enables interrupt to 8032 via INT22 of INTC. 0: Disable the host semaphore (write) interrupt to the EC. 1: The interrupt is set (level high) if HSEMW bit is set.
6	R/WC	0b	Host Semaphore Write (HSEMW) 0: Host has not written to HSEM3-0 field in SMHSR register. 1: Host has written to HSEM3-0 field in SMHSR register. Writing 1 to this bit to clear itself and clear internal detect logic. Writing 0 has no effect.
5	R/W	0b	Host Write Allow (HOSTWA) This bit is for HLPC only. 0: The SMFI does not generate write transactions on M-bus. 1: The SMFI can generate write transactions on M-bus. The read performance on M-bus will be very poor for Host LPC if this bit is set.
4-3	R	01b	Host Error Response (HERES) These bits control response types on read/write translation from/to a protected address. 01b: Read back FFh; ignoring write Otherwise: Reserved
2	-	-	Reserved
1	-	-	Reserved
0	-	-	Reserved

9.11.4.6 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register is reset on host domain hardware reset.
This is the register the same as the one in section 9.11.5.6 but they are in different views.

Address Offset: 22h

Bit	R/W	Default	Description
7-4	R/W	0h	EC Semaphore (CSEM3-0) These four bits may be written by the EC and read by both the host and the EC
3-0	R	0h	Host Semaphore (HSEM3-0) These four bits may be written by the host and read by both the host and the EC.

9.11.4.7 Flash Control 1 Register (FLHCTRL1R)

Address Offset: 31h

Bit	R/W	Default	Description
7-6	-	-	Reserved
5-4	R/W	01b	SPI Flash Read Mode (SPIFR) For serial flash: 11b: Uses “Fast Read Dual Input/Output” cycle 10b: Uses “Fast Read Dual Output” cycle 01b: Uses “Fast Read” cycle 00b: Uses “Read” cycle (instruction = BBh) (instruction = 3Bh) (instruction = 0Bh) (instruction = 03h) The performance of “Read” cycle is better than “Fast Read” cycle in the same frequency since “Fast Read” cycle request 8 dummy clock ticks in each cycle. The attached must support “Fast Read” cycle since it's the default read instruction to serial flash.
3	R/W	1b	Serial Wait 1T (LFSW1T) For serial flash: Always write 1 to it.
2-0	-	-	Reserved

9.11.4.8 Flash Control 2 Register (FLHCTRL2R)

For serial flash only.

Address Offset: 32h

Bit	R/W	Default	Description
7-3	-	-	Reserved
2-0	R/W	011b	FSCE# Min High Width (SCEMINHW) 000b: 1T 001b: 2T 010b: 3T 011b: 4T 100b: 5T 101b: 6T 110b: 7T It depends on the “FSCE# High Time” on flash specification. Small value gets better performance. This register may needs to be modified before the PLL frequency is changed.

9.11.4.9 uC Control Register (UCCTRLR)

Address Offset: 34h

Bit	R/W	Default	Description
7	R/W	0b	uC Burst Mode (UCBST) 0: default 1: for chipset that issues LPC Abort if LPC Long-wait count during a LPC Memory cycle is greater than 255. This bit can be modified only before VCC power is supplied.
6-3	-	-	Reserved
2-0	R/W	5h	uC Burst Threshold (UCTH) 5h: default 3h: for chipset that issues LPC Abort if LPC Long-wait count during a LPC Memory cycle is greater than 255. Otherwise: reserved. This field can be modified only before VCC power is supplied.

9.11.4.10 Host Control 2 Register (HCTRL2R)

Address Offset: 36h

Bit	R/W	Default	Description
7	R/W	0b	Host Bridge Enable (HBREN) 1: The host memory cycle is decoded 0: Otherwise This bit can be modified only before VCC power is supplied.
6	R/W	0b	Safe HLPC Bridge (SHBR) 1: Host PCI clock is less than 33MHz. 0: Otherwise It has the same affection as SLWPCI bit in MBCTRL register in the host side.
5	R/W	0b	HLPC Follow Mode 1 Enable (HFW1EN) 1: Enable HLPC Follow Mode 1 if HOSTWA bit in SMECCS register isn't set. 0: Otherwise This bit can be modified only before VCC power is supplied.
4	R/W	0b	HSPI Memory Slave Selection (SMSS) 0: IT8733 behaves as a LPC/FWH memory device (HLPC) to host Southbridge. 1: IT8733 behaves as an SPI memory slave (HSPI) to host Southbridge. IT8733 cannot behave the two actions simultaneously.
3	-	-	Reserved
2-0	-	-	Reserved

9.11.4.11 HSPI Control Register 2(HSPICTRL2R)

For HSPI only.

Address Offset: 39h

Bit	R/W	Default	Description
7-6	-	-	Reserved
5	-	-	Reserved
4-3	W	00b	HSPI Request Selection (HSRS) 00b: For setting 1/2/3/4 01b: For setting 6/7 10b: For setting 5 11b: Reserved
2	-	1b	Reserved Always write 1 to it.
1-0	-	-	Reserved

9.11.4.12 HSPI Control Register 3(HSPICTRL3R)

For HSPI only.

Address Offset: 3Ah

Bit	R/W	Default	Description
7	-	-	Reserved
6	R/W	0b	Disable WREN Instruction 06h (DISWREN) WREN Instruction 06h will be inhibited if this bit is set. In deferred mode, if the flash JEDEC ID is “BFh 25h”, EWSR+WRSR+WREN will be injected before each WIP instruction. . In deferred mode, if JEDEC ID is not “BFh 25h”, WREN will be injected before each WIP instruction. This bit should be cleared for non-deferred mode.
5	R/W	0b	Deferred Instruction Always Query (DIALWQ) 1b: INT59 issued for each HSPI deferred instruction. 0b: Reserved. This bit is only valid in HSPI deferred mode. Always write 1 to this bit. If method A is used, it's required to send WREN or EWSR+WRSR+WREN to FSPI by EC-Indirect Memory cycle before writing 1 to this bit.
4	R/W	0b	Disable WRSR Instruction 01h (DISWRSR) WRSR Instruction 01h will be inhibited if this bit is set.
3-2	-	-	Reserved
1-0	-	-	Reserved

9.11.4.13 EC-Indirect Memory Address Register 0 (ECINDAR0)

Address Offset: 3Bh

Bit	R/W	Default	Description
7-0	R/W	00h	EC-Indirect Memory Address (ECINDA7-0) Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

9.11.4.14 EC-Indirect Memory Address Register 1 (ECINDAR1)

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R/W	00h	EC-Indirect Memory Address (ECINDA15-8) Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

9.11.4.15 EC-Indirect Memory Address Register 2 (ECINDAR2)

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R/W	00h	EC-Indirect Memory Address (ECINDA23-16) Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

9.11.4.16 EC-Indirect Memory Address Register 3 (ECINDAR3)

Address Offset: 3Eh

Bit	R/W	Default	Description
7-4	R	Serial flash: 0000b	EC-Indirect Memory Address (ECINDA31-28) Read only.
3-0	R/W	0h	EC-Indirect Memory Address (ECINDA27-24) Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

9.11.4.17 EC-Indirect Memory Data Register (ECINDDR)

Address Offset: 3Fh

Bit	R/W	Default	Description
7-0	R/W	-	EC-Indirect Memory Data (ECINDD7-0) Read/Write to this register will access one byte on the flash with the 32-bit flash address defined in ECINDAR3-0.

9.11.4.18 Scratch SRAM 0 Address Low Byte Register (SCAR0L)

Address Offset: 40h

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 0 Address (SC0A7-0)

9.11.4.19 Scratch SRAM 0 Address Middle Byte Register (SCAR0M)

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 0 Address (SC0A15-8)

9.11.4.20 Scratch SRAM 0 Address High Byte Register (SCAR0H)

Address Offset: 42h

Bit	R/W	Default	Description
7	R/W	0b	Next Start DMA (NSDMA) If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	Reserved
5-2	-	-	Reserved
1-0	R/W	11b	Scratch SRAM 0 Address (SC0A17-16) The default value makes this scratch SRAM not be a scratch ROM.

9.11.4.21 Scratch SRAM 1 Address Low Byte Register (SCAR1L)

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 1 Address (SC1A7-0)

9.11.4.22 Scratch SRAM 1 Address Middle Byte Register (SCAR1M)

Address Offset: 44h

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 1 Address (SC1A15-8)

9.11.4.23 Scratch SRAM 1 Address High Byte Register (SCAR1H)

Address Offset: 45h

Bit	R/W	Default	Description
7	R/W	0b	Next Start DMA (NSDMA) If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	Reserved
5-2	R/W	0h	Reserved
1-0	R/W	11b	Scratch SRAM 1 Address (SC1A17-16) The default value makes this scratch SRAM not be a scratch ROM.

9.11.4.24 Scratch SRAM 2 Address Low Byte Register (SCAR2L)

Address Offset: 46h

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 2 Address (SC2A7-0)

9.11.4.25 Scratch SRAM 2 Address Middle Byte Register (SCAR2M)

Address Offset: 47h

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 2 Address (SC2A15-8)

9.11.4.26 Scratch SRAM 2 Address High Byte Register (SCAR2H)

Address Offset: 48h

Bit	R/W	Default	Description
7	R/W	0b	Next Start DMA (NSDMA) If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	Reserved
5-2	R/W	0h	Reserved
1-0	R/W	11b	Scratch SRAM 2 Address (SC2A17-16) The default value makes this scratch SRAM not be a scratch ROM.

9.11.4.27 Scratch SRAM 3 Address Low Byte Register (SCAR3L)

Address Offset: 49h

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 3 Address (SC3A7-0)

9.11.4.28 Scratch SRAM 3 Address Middle Byte Register (SCAR3M)

Address Offset: 4Ah

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 3 Address (SC3A15-8)

9.11.4.29 Scratch SRAM 3 Address High Byte Register (SCAR3H)

Address Offset: 4Bh

Bit	R/W	Default	Description
7	R/W	0b	Next Start DMA (NSDMA) If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	Reserved
5-2	R/W	0h	Reserved
1-0	R/W	11b	Scratch SRAM 3 Address (SC3A17-16) The default value makes this scratch SRAM not be a scratch ROM.

9.11.4.30 Scratch SRAM 4 Address Low Byte Register (SCAR4L)

Address Offset: 4Ch

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 4 Address (SC4A7-0)

9.11.4.31 Scratch SRAM 4 Address Middle Byte Register (SCAR4M)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-0	R/W	00h	Scratch SRAM 4 Address (SC4A15-8)

9.11.4.32 Scratch SRAM 4 Address High Byte Register (SCAR4H)

Address Offset: 4Eh

Bit	R/W	Default	Description
7	R/W	0b	Next Start DMA (NSDMA) If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	Reserved
5-2	R/W	0h	Reserved
1-0	R/W	11b	Scratch SRAM 4 Address (SC4A17-16) The default value makes this scratch SRAM not be a scratch ROM.

9.11.4.33 Protect 0 Base Addr Register 0 (P0BA0R)

Address Offset: 4Fh

Bit	R/W	Default	Description
7-4	-	-	Reserved
3-0	R/W	-	Protect 0 Address (P0BA23-20) The default value is uncertain.

9.11.4.34 Protect 0 Base Addr Register 1 (P0BA1R)

Address Offset: 50h

Bit	R/W	Default	Description
7-0	R/W	-	Protect 0 Address (P0BA19-12) The default value is uncertain.

9.11.4.35 Protect 0 Size Register (P0ZR)

Address Offset: 51h

Bit	R/W	Default	Description
7-6	R/W	00b	Protect 0 Mode (P0M) It controls the protection mode of set 0. 00b: Read protection 01b: Write protection 10b: Read protection plus write protection 11b: Reserved
5	R/W	0b	Release 4K Protected Part (R4PP) 0b: Disable 1b: The upper 4K part of the range specified by P0Z will be released from protection function. This bit is valid only when P0Z is 5h, 6h, Eh or 7h.
4-3	-	-	Reserved

Bit	R/W	Default	Description
2-0	R/W	0	<p>Protect 0 Size (P0Z)</p> <p>If this field is zero, there is no memory block on SPI flash locked by "Protect 0" configuration.</p> <p>If this field is not zero, it means that read or write cycles from the host side to the specified SPI memory block is locked. The address defined by P0BA0R and P0BA1R is SPI physical address, not host LPC address.</p> <p>If write protection is enabled in P0M field, this size field must be equal to or greater than the allowed sector/block size of ERASE instruction. See also HINSTC2 register.</p> <p>This field returns to the default after warm set, and VSTBY power-up reset.</p> <p>The protected size cannot cross the boundary of the base address.</p> <p>In-system Programming Operation on page 322 is not affected by "Protect 0" configuration.</p> <p>0: Disabled</p> <p>1: The range is from $(P0BA[23..12] << 12)$ to $(P0BA[23..12] << 12) + ((1 << 12) - 1)$ and totally 2^{12} (4K) bytes are locked.</p> <p>2: The range is from $(P0BA[23..13] << 13)$ to $(P0BA[23..13] << 13) + ((1 << 13) - 1)$ and totally 2^{13} (8K) bytes are locked.</p> <p>3: The range is from $(P0BA[23..14] << 14)$ to $(P0BA[23..14] << 14) + ((1 << 14) - 1)$ and totally 2^{14} (16K) bytes are locked.</p> <p>4: The range is from $(P0BA[23..15] << 15)$ to $(P0BA[23..15] << 15) + ((1 << 15) - 1)$ and totally 2^{15} (32K) bytes are locked.</p> <p>5: The range is from $(P0BA[23..16] << 16)$ to $(P0BA[23..16] << 16) + ((1 << 16) - 1)$ and totally 2^{16} (64K) bytes are locked.</p> <p>Otherwise: reserved</p>

9.11.4.36 Protect 1 Base Addr Register 0 (P1BA0R)

Address Offset: 52h

Bit	R/W	Default	Description
7-4	-	-	Reserved
3-0	R/W	-	Protect 1 Address (P1BA23-20) The default value is uncertain.

9.11.4.37 Protect 1 Base Addr Register 1 (P1BA1R)

Address Offset: 53h

Bit	R/W	Default	Description
7-0	R/W	-	Protect 1 Address (P1BA19-12) The default value is uncertain.

9.11.4.38 Protect 1 Size Register (P1ZR)

Address Offset: 54h

Bit	R/W	Default	Description
7-6	R/W	00b	Protect 1Mode (P1) “Protect 1” configuration is the same as “Read Protect 0”.
5-3	-	-	Reserved
2-0	R/W	0	Protect 1 Size (P1Z) “Protect 1” configuration is the same as “Read Protect 0”.

9.11.4.39 Deferred SPI Instruction (DSINST)

Address Offset: 55h

Bit	R/W	Default	Description
7-0	R	-	Deferred SPI Instruction (DSINST) The 8-bit instruction code of deferred SPI WIP instruction. For HSPI only.

9.11.4.40 Deferred SPI Address 15-12 (DSADR1)

Address Offset: 56h

Bit	R/W	Default	Description
7-4	R	-	Deferred SPI Address 15-12 (DSA15-12) The SPI address of deferred SPI WIP instruction. For HSPI only.
3-0	-	-	Reserved

9.11.4.41 Deferred SPI Address 23-16 (DSADR2)

Address Offset: 57h

Bit	R/W	Default	Description
7-0	R	-	Deferred SPI Address 23-16 (DSA23-16) The SPI address of deferred SPI WIP instruction. For HSPI only.

9.11.4.42 Host Instruction Control 1 (HINSTC1)

For HSPI only.

Address Offset: 58h

Bit	R/W	Default	Description
7	-	-	Reserved
6	W	-	<p>Scan EC Base (SCECB) This bit is for HSPI function only. See also section 9.11.3.20 SPI Flash Power-on Detection on page 176.</p> <p>Write 1: Scan the EC code base address. Write 0: Ignored. Read always returns 0.</p> <p>The firmware may write 1 to this bit after the flash is programmed. The firmware must write 1 to this bit only when the HSPI cycle is not presented during the process of scanning for the base address. It may be the followings:</p> <ol style="list-style-type: none"> 1. HSPI is set as the deferred mode and is deferred before writing data to DISS bit in this register. 2. The Southbridge is not activated.
5-4	-	-	Reserved
3	W	-	<p>DISS Valid (DISSV) Write 1: Write DISS bit in this register is valid. Write 0: Write DISS bit in this register is ignored.</p> <p>Only write 1 to this bit while INT59 is active.</p>
2	R/W	-	<p>Deferred Instruction's Succeeding Step (DISS) Always write 1 to this bit.</p> <p>Writing to this bit and writing 1 to DISSV bit must be in the same write cycle, or this writing action to DISS bit is ignored.</p>
1-0	R/W	00b	<p>Enable Deferring WIP Instruction (ENDI) HLPC: Enable deferring an ERASE/PROG instruction in the Follow mode by returning Long-Waits and issuing INT59.</p> <p>HSPI: 11b: Enable deferring a WIP instruction by returning WIP (busy) state and issuing INT59.</p> <p>00b: Disable. Otherwise: Reserved.</p>

9.11.4.43 Host Instruction Control 2 (HINSTC2)

This register is only valid when LPC hardware protection is enabled by setting P0ZR and P1ZR register.

Some SPI flashes provide two or more sector/block ERASE instructions, e.g. 4K and 64K ERASE instruction. If one specified 4K block is set as hardware protection, it may be erased by 64K ERASE instruction.

To accomplish the hardware protectin on the SPI flash, the size defined in P0Z/P1Z field in P0ZR/P1ZR register must be equal to or greater than the allowed sector/block size of ERASE instruction.

For the above example, if an SPI flash provides the 4K ERASE instruction (code 20h) and 64K ERASE instruction (code D8h), the write protection can work well if the size defined in P0Z/P1Z field is equal to or greater than 64K; otherwise, the 64K ERASE instruction should be inhibited by setting DISEID8 bit.

Address Offset: 59h

Bit	R/W	Default	Description
7-4	-	-	Reserved
3	R/W	0b	Disable Erase Instruction D8h (DISEID8) Erase sector/block instruction D8h will be inhibited.
2	R/W	0b	Disable Erase Instruction D7h (DISEID7) Erase sector/block instruction D7h will be inhibited.
1	R/W	0b	Disable Erase Instruction 52h (DISEI52) Erase sector/block instruction 52h will be inhibited.
0	R/W	0b	Disable Erase Instruction 20h (DISEI20) Erase sector/block instruction 20h will be inhibited.

9.11.4.44 Host RAM Window Control (HRAMWC)

Address Offset: 5Ah

Bit	R/W	Default	Description
7-2	-	-	Reserved
1-0	R/W	0b	H2RAM Window 0/1 Enable (H2RAMWE) 00b: Disabled 01b: Window 0 enabled 10b: Window 1 enabled 11b: Both enabled

9.11.4.45 Host RAM Winodw 0 Base Address (HRAMW0BA[11:4])

Address Offset: 5Bh

Bit	R/W	Default	Description
7-0	R/W	00h	Host RAM Window 0 Base Address Bits [11:4] (HRAMW0BA[11:4]) Define RAM window 0 base address.

9.11.4.46 Host RAM Window 1 Base Address (HRAMW1BA[11:4])

Address Offset: 5Ch

Bit	R/W	Default	Description
0	R/W	00h	Host RAM Window 1 Base Address Bits [11:4] (HRAMW1BA[11:4]) Define RAM window 1 base address.

9.11.4.47 Host RAM Window 0 Access Allow Size (HRAMW0AAS)

Address Offset: 5Dh

Bit	R/W	Default	Description
7-6	R/W	0h	Host RAM Window 0 Read Protect Enable (HRAMW0RPE) 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	Host RAM Window 0 Write Protect Enable (HRAMW0WPE) 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	Reserved
2-0	R/W	0h	Host RAM Window 0 Size (HRAMW0S) 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

9.11.4.48 Host RAM Window 1 Access Allow Size (HRAMW1AAS)

Address Offset: 5Eh

Bit	R/W	Default	Description
7-6	R/W	0h	Host RAM Window 1 Read Protect Enable (HRAMW1RPE) 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	Host RAM Window 1 Write Protect Enable (HRAMW1WPE) 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	Reserved
2-0	R/W	0h	Host RAM Window 1 Size (HRAMW1S) 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

9.11.5 Host Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The SMFI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The SMFI logical device number is 0Fh (LDN). These registers are listed below

Table 9-28. Host View Register Map, SMFI

7	0	Offset
	Shared Memory Indirect Memory Address (SMIMAR0-3)	00h-03H
	Shared Memory Indirect Memory Data (SMIMDR)	04h
	Shared Memory Host Semaphore (SMHSR)	0Ch
	M-Bus Control Register (MBCTRL)	0Fh

9.11.5.1 Shared Memory Indirect Memory Address Register 0 (SMIMAR0)

The following set of registers is accessible only by the host. The registers are applied to VCC. This register defines the addresses 7-0 for a read or write transaction to the memory.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	Indirect Memory Address (IMADR7-0)

9.11.5.2 Shared Memory Indirect Memory Address Register 1 (SMIMAR1)

This register defines the addresses 15-8 for a read or write transaction to the memory.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	-	Indirect Memory Address (IMADR15-8)

9.11.5.3 Shared Memory Indirect Memory Address Register 2 (SMIMAR2)

This register defines the addresses 23-16 for a read or write transaction to the memory.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	-	Indirect Memory Address (IMADR23-16)

9.11.5.4 Shared Memory Indirect Memory Address Register 3 (SMIMAR3)

This register defines the addresses 31-24 for a read or write transaction to the memory.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	-	Indirect Memory Address (IMADR31-24)

9.11.5.5 Shared Memory Indirect Memory Data Register (SMIMDR)

This register defines the Data bits 7-0 for a read or write transaction to the memory.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	-	Indirect Memory Data (IMDA7-0)

9.11.5.6 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register reset on host domain hardware reset.

This is the register the same as the one in section 9.11.4.9 on page 185 but they are in different views.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-4	R	0h	EC Semaphore (CSEM3-0) Four bits that may be updated by the EC and read by both the host and the EC.
3-0	R/W	0b	Host Semaphore (HSEM3-0) Four bits that may be updated by the host and read by both the host and the EC.

9.11.5.7 M-Bus Control Register (MBCTRL)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-1	-	-	Reserved
0	R/W	0b	Slow PCI Clock Register (SLWPCI) 1: Host PCI clock is less than 33MHz. 0: Otherwise It has the same affection as SHBR bit in HCTRL2R register in EC side.

9.12 Power Management Channel (PMC)

9.12.1 Overview

The power management channel is defined in ACPI specification and used as a communication channel between the host processor and embedded controller.

9.12.2 Features

- Supports two PM channels
- Supports compatible mode and enhanced mode (all channels)
- Supports shared and private interface
- Supports Command/Status and Data ports
- Supports IRQ/SMI#/SCI# generation

9.12.3 Functional Description

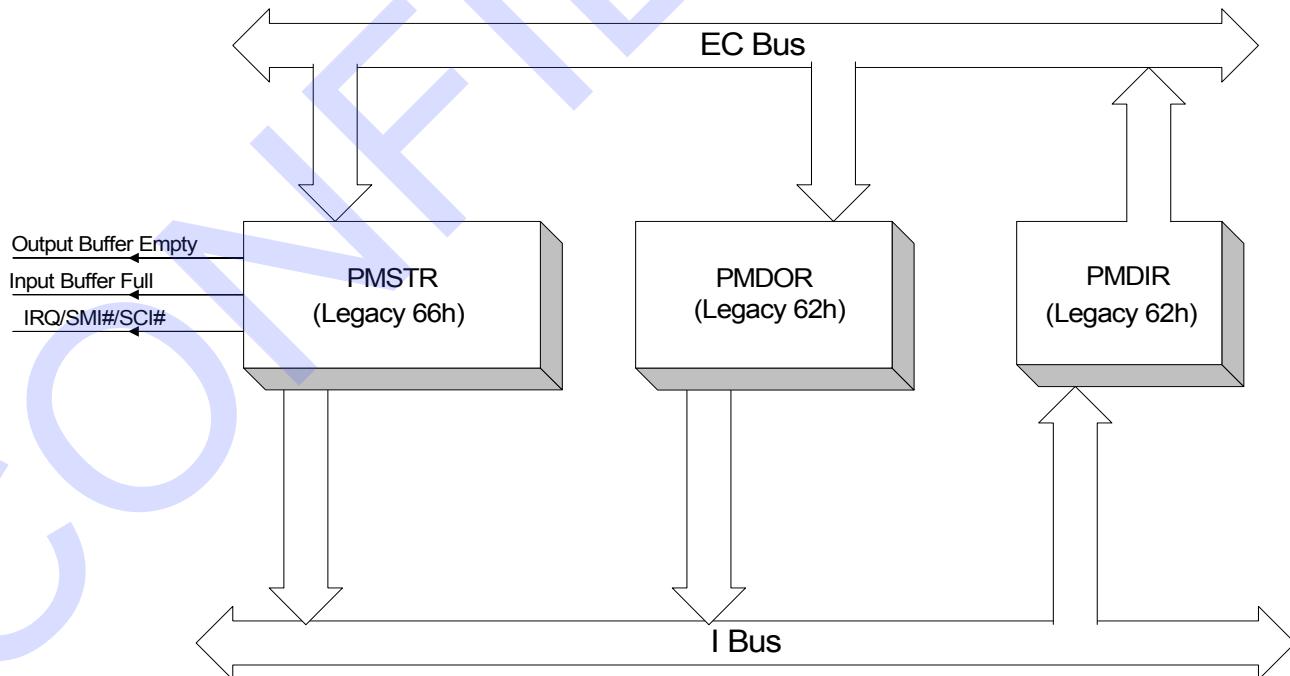
To generate the SCI# and SMI# interrupts to the host

9.12.3.1 General Description

The PM channel supports two operation modes: one is called Compatible mode that is available for channel 1 only. The other is called Enhanced mode. PMC is available for all channels. The PM channel provides four registers: PMDIR, PMDOR, PMCMDR and PMSTR for communication between the EC and host side. The PMDIR register can be written to by the host and read by the EC. The PMDOR register can be written to by the EC and read by the host. The PMCMDR/PMSTR register can be read by both the EC and Host side.

The PMC host interface block diagram is shown below.

Figure 9-16. PMC Host Interface Block Diagram

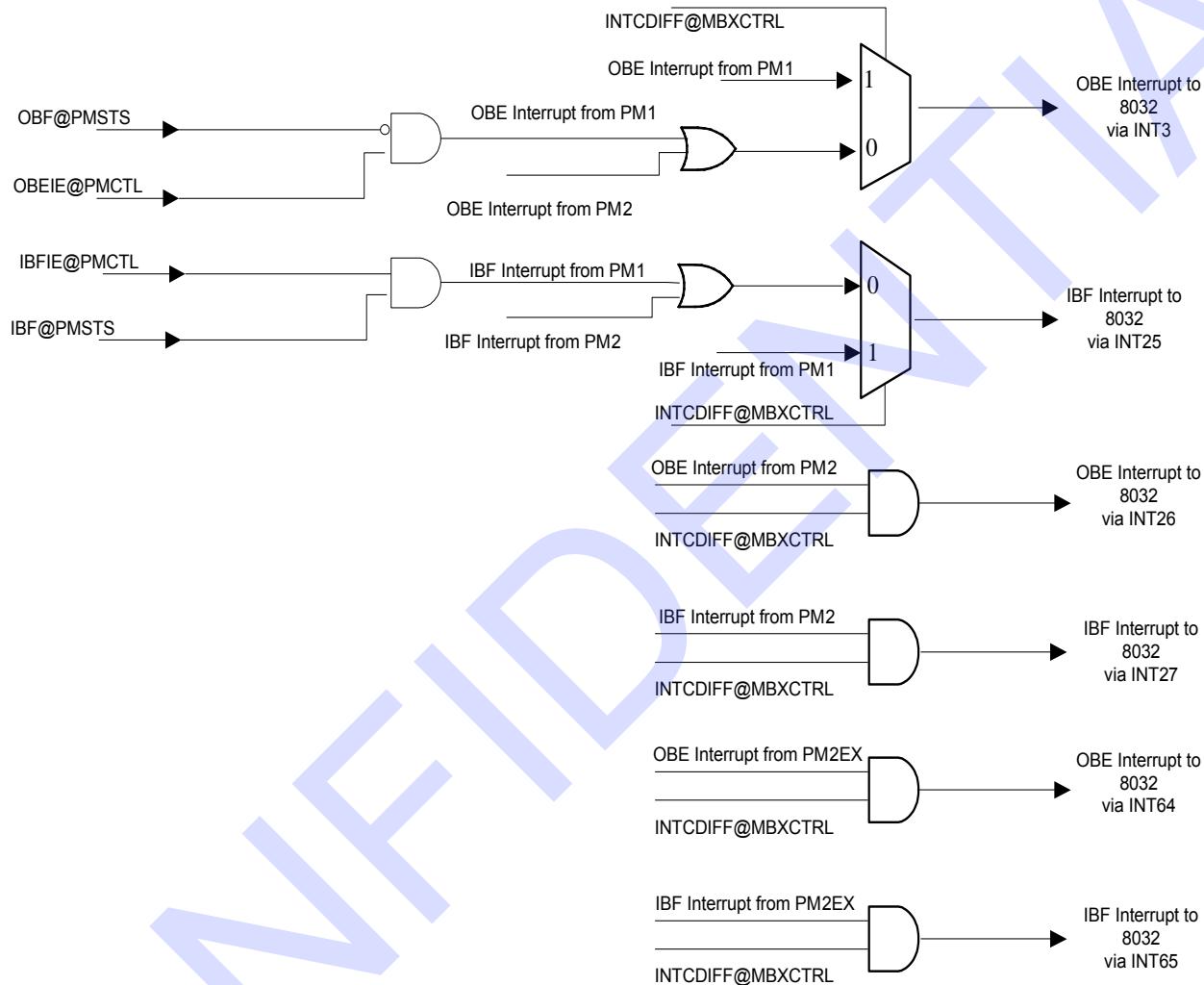


EC Interrupts

Two interrupts (IBF and OBF) are connected to INTC. These interrupts are enabled by OBEIE and IBFIE in PMnCTL register respectively.

The diagram of PMC interrupt to EC 8032 via INT3/INT25/INT26/INT27/INT64/INT65 of INTC is shown below.

Figure 9-17. EC Interrupt Request for PMC



Host Interrupt

The EC can select to access to different address space to generate IRQ, SMI# or SCI# interrupt when either IBF or OBF is set.

The IRQ numbers of PMC are programmable and use IRQ11 as the abbreviation in the following section. The abbreviation, n, represents channel 1 and/or channel 2 of this register.

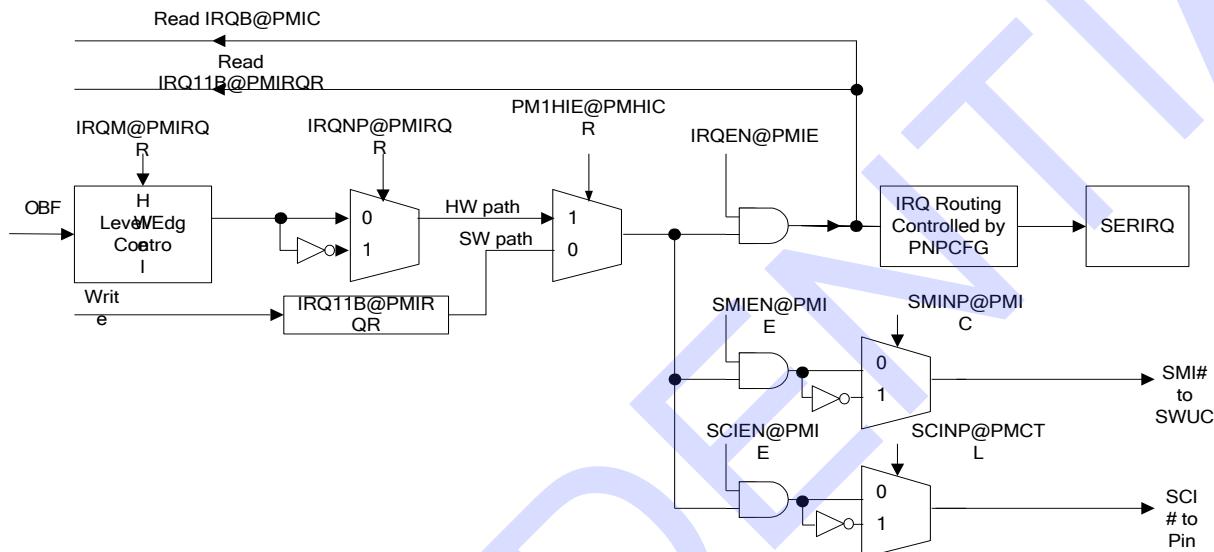
9.12.3.2 Compatible Mode

When IRQ numbers in host configuration register are assigned by host software, and the interrupt can be generated either by hardware via PM1HIE in KBHICR register or by programming KBIRQR register. In Normal Polarity mode (IRQNP in KBIRQR register is cleared), IT8733 supports legacy level for PM compatible mode interrupt. When a level interrupt is selected (IRQM in KBIRQR register is cleared), the interrupt signal is asserted when the OBF flag has been set, which is still asserted until the output buffer is read (i.e., OBF flag is

cleared). The EC can control the interrupts generated by the PM channel to the one as follows:
 IRQ signal to LPC/SERIRQ, when IRQEN bit in PMnIE register is set.
 SMI# output to SWUC, when SMIEN bit in PMnIE register is set.
 SCI# signal, using the SCI# output, when SCIEN bit in PMnIE register is set.

The IRQ/SCI#/SMI# control diagram in PMC compatible mode is shown below.

Figure 9-18. IRQ/SCI#/SMI# Control in PMC Compatible Mode

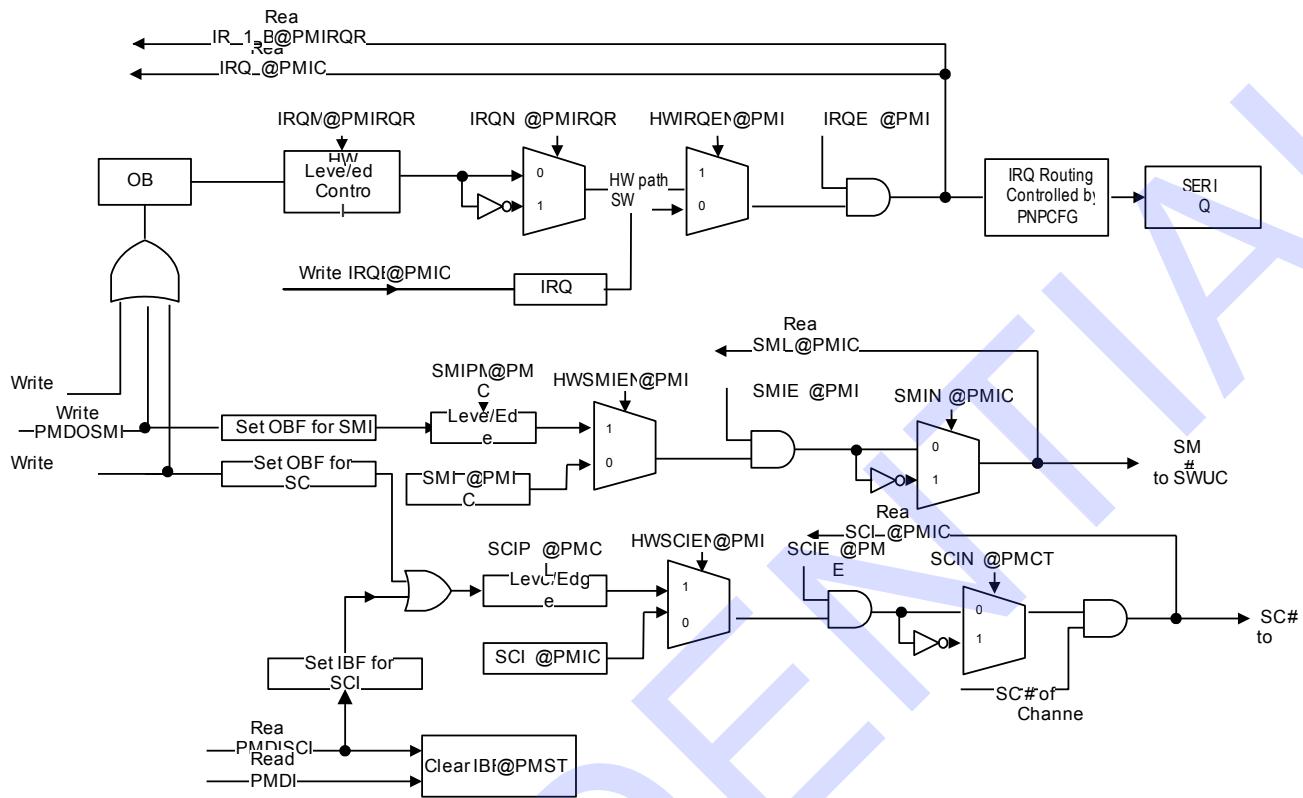


9.12.3.3 Enhanced PM mode

Enhanced PM mode is activated when APM is set to 1 in PMnCTL register. The generated IRQ, SMI# or SCI# interrupt can be selected to output via software control or hardware, which is determined by programming IRQEN bit in PMnIE register. SCI# and SMI# are generated when EC writes to the Data output buffer. SCI# is generated when EC reads the Data Input buffer. Different data register generates different interrupt. The OBF flag in PMnSTS register is set and both SMI# and SCI# interrupts are deasserted when data is written to PMnDO register. The OBF interrupt of SMI# is generated when PMnDOSMI register is written into data. The internal OBF flag of SMI# is cleared when OBF flag is cleared. The OBF interrupt of SCI# is generated When PMnDOSCI register is written into data. OBF_SC# which is cleared when OBF is cleared. The IBF flag is cleared and SCI# interrupt is generated when PMnDISCI register is read out data. The IBF flag is cleared and SCI# interrupt is not asserted when PMnDI register is read out data.

The IRQ/SCI#/SMI# control diagram in PMC enhanced mode is shown below.

Figure 9-19 IRQ/SCI#/SMI# Control in PMC Enhanced Mode



9.12.3.4 PMC2EX

There is a channel 2 extended (PMC2EX) mailbox (MBX) function based on PMC channel 2, which is constructed by a 16-byte mailbox shared with BRAM. See also Figure 10-20. BRAM Mapping Diagram on page 317.

This 16-byte mailbox can be accessed from both the EC side (named MBXEC0-15) and host side (MBXH0-15).

In the EC side, MBXEC0-15 is always located in PMC module offset F0h-FFh and shared with the topmost 16-byte in BRAM.

In the host side, MBXH0-15 address is based on the descriptor 2 of Power Management I/F Channel 2 logic device inside LPC I/O space. (Refer to section 8.16.6 and 8.16.7 on page 86)

The PMC2EX (channel 2 extended) shares the same interrupt generation resource and registers (offset 10h-18h).

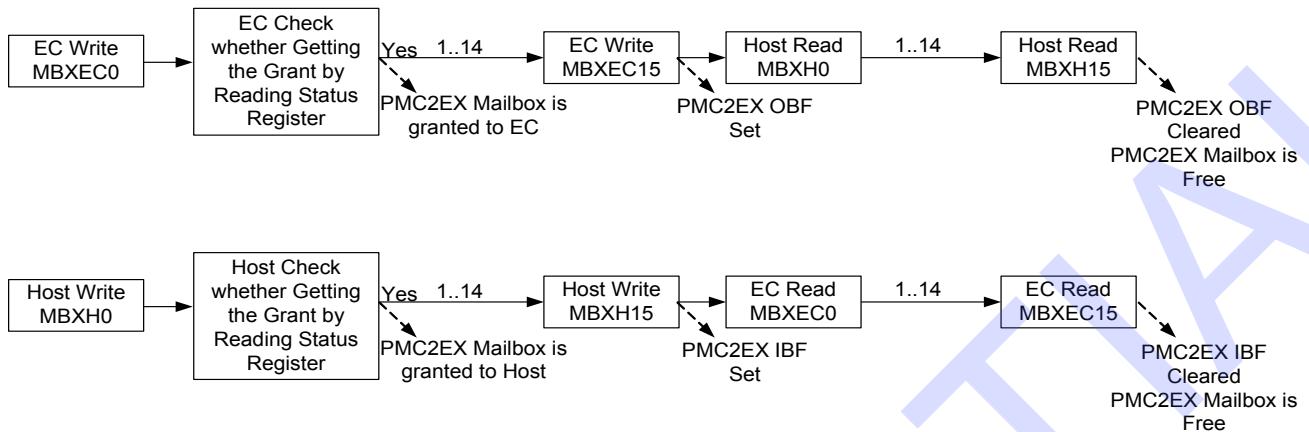
For registers, PMC2EX shares the same registers (offset 10h-18h) and has its dedicated MBXCTRL register (offset 19h).

For interrupt generation, PMC2EX shares the same interrupt logic with channel 2. If MBXEN is set, IBF/OBF interrupt source of PMC2EX is ORed with channel 2.

The EC/host side should check whether to get the grant from the internal arbiter after writing to MBXEC0/MBXH0 (respectively).

The typical PMC2EX mailbox operation is described below.

Figure 9-20 Typical PMC2EX Mailbox Operation



9.12.4 Host Interface Registers

The registers of PMC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The PMC Channel 1 and 2 reside at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The channel 1 logical device number is 11h (LDN) and the channel 2 logical device number is 12h (LDN). For compatibility issue, the two I/O Port Base Addresses of channel 1 are suggested to configure at 62h and 66h.

These registers are listed below.

Table 9-29. Host View Register Map, PMC

7	0	Offset
PMC Data Input Register (PMDIR)		Legacy 62h
PMC Data Output Register (PMDOR)		Legacy 62h
PMC Command Register (PMCMRD)		Legacy 66h
PMC Status Register (PMSTR)		Legacy 66h

Legacy 62h represents (I/O Port Base Address 0) + (Offset 0h)

Legacy 66h represents (I/O Port Base Address 1) + (Offset 0h)

9.12.4.1 PMC Data Input Register (PMDIR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	Data Input Register Bit [7:0] (DIRB) This is the data input register for power management channel data communication between the host and EC side. When the host writes this port, data is written to PMDIR register and EC 8032 can read it. Notice that when the Command/Status register is written, the data is also stored into PMDIR register. Users must read A2 to decide whether the PMDIR data is data or command.

9.12.4.2 PMC Data Output Register (PMDOR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	R	00h	Data Output Register Bit [7:0] (DORB) This is the data output register for power management channel data communication between the host and EC. When the host reads this port, data is read from PMDOR register and EC 8032 can write it.

9.12.4.3 PMC Command Register (PMCMDR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	Command Register Bit [7:0] (CRB) The port is written by the host when A2 = 1 in PMSTR register.

9.12.4.4 Status Register (PMSTR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-4	R/W	0h	Status Register (STS) For channel 1 and channel 2 with MBXEN cleared: This is a general purpose flag used for signaling between the host and EC side. When used as ACPI PM channel, the predefined meaning is burst, SCI# event and SMI# event. For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved
3	R	0b	A2 (A2) This bit is used to indicate the last write (by host) address bit A2. If the bit is 0, it represents that the data written by the host is data. If this bit is 1, it represents that the data written by the host is command.
2	R/W	0b	General Purpose flag (GPF) This bit is used as a general-purpose flag.
1	R	0b	Input Buffer Full (IBF) This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data input register or command register and is cleared when the EC 8032 reads the data input register. Notice that the write to data input register or command register by the host all trigger this flag and EC must use A2 to distinguish whether the write is a command or data.
0	R	0b	Output Buffer Full (OBF) This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data output port and is cleared when the host reads the data out buffer.

9.12.5 EC Interface Registers

The registers of PMC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address is 1500h.

These registers are listed below.

Table 9-30. EC View Register Map, PMC

7	0	Offset
	Host Interface PM Channel 1 Status (PM1STS)	00h
	Host Interface PM Channel 1 Data Out Port (PM1DO)	01h
	Host Interface PM Channel 1 Data Out Port with SCI# (PM1DOSCI)	02h
	Host Interface PM Channel 1 Data Out Port with SMI# (PM1DOSMI)	03h
	Host Interface PM Channel 1 Data In Port (PM1DI)	04h
	Host Interface PM Channel 1 Data In Port with SCI# (PM1DISCI)	05h
	Host Interface PM Channel 1 Control (PM1CTL)	06h
	Host Interface PM Channel 1 Interrupt Control (PM1IC)	07h
	Host Interface PM Channel 1 Interrupt Enable (PM1IE)	08h
	Host Interface PM Channel 2 Status (PM2STS)	10h
	Host Interface PM Channel 2 Data Out Port (PM2DO)	11h
	Host Interface PM Channel 2 Data Out Port with SCI# (PM2DOSCI)	12h
	Host Interface PM Channel 2 Data Out Port with SMI# (PM2DOSMI)	13h
	Host Interface PM Channel 2 Data In Port (PM2DI)	14h
	Host Interface PM Channel 2 Data In Port with SCI# (PM2DISCI)	15h
	Host Interface PM Channel 2 Control (PM2CTL)	16h
	Host Interface PM Channel 2 Interrupt Control (PM2IC)	17h
	Host Interface PM Channel 2 Interrupt Enable (PM2IE)	18h
	Mailbox Control (MBXCTRL)	19h
	PMC Interrupt Control Register (PMIRQR)	20h
	PMC Host Interface Control Register (PMHICR)	21h
	16-byte PMC2EX Mailbox 0 (MBXEC0)	F0h

	16-byte PMC2EX Mailbox 15 (MBXEC15)	FFh

9.12.5.1 PM Status Register (PMSTS)

This register is the same as the Status register in host side but reside in the EC side.

Address Offset: 00h/10h

Bit	R/W	Default	Description
7-4	R/W	0h	<p>Status Register (STS) For channel 1 and channel 2 with MBXEN cleared: This is a general-purpose flag used for signaling between the host and EC. When used as ACPI PM channel, the predefined meaning is burst, SCI# event and SMI# event.</p> <p>For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved</p>
3	R	0b	<p>A2 (A2) This bit is used to indicate the last write (by host) address bit A2. If the bit is 0, it represents that the data written to the data port is data. If this bit is 1, it represents that the data written to the data port is command.</p>
2	R/W	0b	<p>General Purpose Flag (GPF) This bit is used as a general-purpose flag.</p>
1	R	0b	<p>Input Buffer Full (IBF) This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data port or command port whereas cleared when the EC read the data in the buffer.</p>
0	R	0b	<p>Output Buffer Full (OBF) This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port whereas cleared when the host reads the data output buffer.</p>

9.12.5.2 PM Data Out Port (PMDO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 01h/11h

Bit	R/W	Default	Description
7-0	W	00h	<p>PM Data Out (PMDO[7:0]) This is the data output buffer.</p>

9.12.5.3 PM Data Out Port with SCI# (PMDOSCI)

This register is the PMDOR buffer with SCI#. The data written to this register is stored in PMDOR. SCI# is generated upon write.

Address Offset: 02h/12h

Bit	R/W	Default	Description
7-0	W	00h	<p>PM Data Out with SCI# (PMDOSCI[7:0]) This is the data output buffer with SCI#. Writing to this port will generate hardware SCI# if enabled.</p>

9.12.5.4 PM Data Out Port with SMI# (PMDOSMI)

This register is the PMDOR buffer with SMI#. The data written to this register is stored in PMDOR. SMI# is generated upon write.

Address Offset: 03h/13h

Bit	R/W	Default	Description
7-0	W	00h	PM Data Out with SMI# (PMDOSMI[7:0]) This is the data output buffer with SMI#. Writing to this port will generate hardware SMI# if enabled.

9.12.5.5 PM Data In Port (PMDI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 04h/14h

Bit	R/W	Default	Description
7-0	R	00h	PM Data In (PMDI[7:0]) This is the data input buffer.

9.12.5.6 PM Data In Port with SCI# (PMDISCI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer. Reading this register (EC) generates SCI#.

Address Offset: 05h/15h

Bit	R/W	Default	Description
7-0	R	00h	PM Data In with SCI# (PMDISCI[7:0]) This is the data input buffer with SCI#. Reading this port will generate SCI# when enabled.

9.12.5.7 PM Control (PMCTL)

Address Offset: 06h/16h

Bit	R/W	Default	Description
7	R/W	0b	Enhance PM Mode (APM) Setting this bit to '1' enables the enhance PM mode. The interrupts (IRQ, SCI# or SM#) are automatically generated by hardware operations if enabled.
6	R/W	1b	SCI# Negative Polarity (SCINP) Setting this bit to '1' causes the SCI# polarity inversed (low active).
5-3	R/W	0h	SCI# Pulse Mode (SCIPM[2:0]) These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	-	0b	Reserved
1	R/W	0b	Output Buffer Empty Interrupt Enable (OBEIE) Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).
0	R/W	0b	Input Buffer Full Interrupt Enable (IBFIE) Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

9.12.5.8 PM Interrupt Control (PMIC)

Address Offset: 07h/17h

Bit	R/W	Default	Description
7	-	0b	Reserved
6	R/W	1b	SMI# Negative Polarity (SMINP) Setting this bit to '1' causes the SMI# polarity inversed.
5-3	R/W	000b	SMI# Pulse Mode (SMIPM[2:0]) These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000b: Level-triggered mode. 001b: Edge-triggered mode with 1-cycle pulse width. 010b: Edge-triggered mode with 2-cycle pulse width. 011b: Edge-triggered mode with 4-cycle pulse width. 100b: Edge-triggered mode with 8-cycle pulse width. 101b: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	1b	Host SCI# Control Bit (SCIB) This bit is the SCI# generation bit when hardware SCI# is disabled. Read always returns the current value of SCI#.
1	R/W	1b	Host SMI# Control Bit (SMIB) This bit is the SMI# generation bit when hardware SMI# is disabled. Read always returns the current value of SMI#.
0	R/W	0b	Host IRQ Control Bit (IRQB) This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

9.12.5.9 PM Interrupt Enable (PMIE)

Address Offset: 08h/18h

Bit	R/W	Default	Description
7-6	-	00b	Reserved
5	R/W	0b	Hardware SMI# Enable (HWSMIEN) Setting this bit to '1' enables the SMI# generated by hardware control. Writing to the SMIB bit generates the SMI# if this bit is set to '0'.
4	R/W	0b	Hardware SCI# Enable (HWSCIEN) Setting this bit to '1' enables the SCI# generated by hardware control. Writing to the SCIB bit generates the SCI# if this bit is set to '0'.
3	R/W	0b	Hardware IRQ Enable (HWIRQEN) Setting this bit to '1' enables the IRQ generated by hardware control. Writing to the IRQB bit generates the IRQ if this bit is set to '0'.
2	R/W	0b	SMI# Enable (SMIEN) Setting this bit to '1' enables the SMI# generated by this module.
1	R/W	0b	SCI# Enable (SCIEN) Setting this bit to '1' enables the SCI# generated by this module.
0	R/W	0b	IRQ Enable (IRQEN) Setting this bit to '1' enables the IRQ generated by this module.

9.12.5.10 Mailbox Control (MBXCTRL)

Address Offset: 19h

Bit	R/W	Default	Description
7	R/W	0b	Mailbox Enable (MBXEN) 1b: Enable 16-byte PMC2EX mailbox 0b: Otherwise
6	-	-	Reserved
5	R/W	0b	Reserved
4-0	-	-	Reserved

9.12.5.11 PMC Interrupt Control Register (PMIRQR)

Address Offset: 20h

Bit	R/W	Default	Description
7	R	0b	Reserved
6	R/W	0b	Interrupt Negative Polarity (IRQNP) The bit is enabled, and then the interrupt level is inverted.
5-3	R/W	0b	Interrupt Mode (IRQM) These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is high and a negative pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from SCIPM field in PMCTL register and SMIPM field in PMIC register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	1b	IRQ11 Control Bit (IRQ11B) When the PM1HIE bit in PMC Host Interface Control Register (PMHICR) is 0, the bit directly controls the IRQ11 signal. The bit can be used to monitor the status of IRQ11 signal. Reading this bit returns the status of IRQ11 signal, so the read value is not equal to the written value directly.
1-0	R/W	11b	Reserved

9.12.5.12 PMC Host Interface Control Register (PMHICR)

Address Offset: 21h

Bit	R/W	Default	Description
7-5	R	000b	Reserved
4	R/W	0b	PM Channel 1 Host Interface Interrupt Enable (PM1HIE) 0: The IRQ11 is controlled by the IRQ11B bit in PMC Interrupt Control Register (PMIRQR). 1: Enables the interrupt to the host side via SERIRQ for PM channel 1 when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in PMIRQR.
3-0	R/W	0000b	Reserved

9.12.5.13 16-byte PMC2EX Mailbox 0-15 (MBXEC0-15)

Address Offset: F0h-FFh

Bit	R/W	Default	Description
7-0	R/W	-	Mailbox Byte Content This byte is the 16-byte PMC2EX mailbox in the EC side.

9.13 BRAM in Host Domain

9.13.1 Overview

BRAM module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 10.7 BRAM for the EC domain function description on page 317.

CONFIDENTIAL

9.14 SMBus Interface (SMB)

9.14.1 Overview

The SMBus interface includes three SMBus channels. The module can maintain bi-directional communication with the external devices through the interface SMCLK0/SMDAT0, SMCLK1/SMDAT1 and SMCLK2/SMDAT2 pins. It is compatible with ACCESS BUS and I2C BUS.

LPC side: LDN = 19h, ADDR base address = 0215h, and DATA base address = 0216h
uC side: Base address = 1C00h

9.14.2 Features

- Supports SMBus 2.0
- Supports three SMBus channels
- Performs SMBus messages with packet error checking (PEC) either enabled or disabled
- Compatible with I2C cycles
- Two user-defined Slave addresses
- Independently select SMCLK frequency for each channel

9.14.3 Functional Description

The SMBus Channel A contains one SMBus master and one SMBus slave.
The SMBus Channel B contains one SMBus master and one SMBus slave.
The SMBus Channel C contains one SMBus master.

The default interface of the SMBus slave in Channel A is located at SMCLK0/SMDAT0. The default interface of the SMBus slave in Channel B is located at SMCLK1/SMDAT1. The interface of the SMBus slave can be switched to SMCLK1/SMDAT1 or SMCLK2/SMDAT2.

The master supports seven command protocols of the SMBus (see System Management Bus Specification): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, and Block Read/Write. The master also supports the I2C-compatible cycles (see The I2C-Bus Specification). The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.

9.14.3.1 SMBus Master Interface

When an interrupt to INTC (INT9, INT10, and INT16 for slave, B, and C respectively) is detected, software can read the Host Status Register to know the interrupt source. There are 5 interrupt conditions: Byte Done, Failed, Bus Error, Device Error, and Finish.

Quick Command:

In the Quick Command, the Transmit Slave Address Register is sent. Software should force the PEC_EN bit in Host Control Register and I2C_EN bit in Host Control 2 Register to 0 when this command is run.

Send Byte/ Receive Byte:

In the Send Byte command, the Transmit Slave Address and Host Command Registers are sent.
In the Receive Byte command, the Transmit Slave Address Register is sent. The received data is stored in the Host DATA 0 register. Software must force the I2C_EN bit in Host control 2 Register to 0 when this command is run.

Write Byte/ Write Word

In the Write Byte command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Registers are sent.

In the Write Word command, the Transmit Slave Address Register, Host Command Register, Host Data 0, and Host Data 1 Registers are sent.

In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Read Byte/ Read Word

In the Read Byte command, the Transmit Slave Address Register and Host Command Register are sent. Data is received into the Host Data 0 Register.

In the Read Word command, the Transmit Slave Address Register and Host Command Register are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register.

In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Process Call

In the Process Call command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Registers are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register. When the I2C_EN bit in Host Control 2 Register is set to 1, the Host Command Register will not be sent.

Note: The Process Call command with I2C_EN bit set and the PEC_EN bit set produce undefined results.

Block Write/ Block Read

In the Block Write command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 (byte count) register are sent. Data is then sent from the Host Block Data Byte register.

In the Block Read commands, the Transmit Slave Address Register, and Host Command Register are sent. The first byte (byte count) received is stored in the Host Data 0 register, and the remaining bytes are stored in the Host Block Data Byte register.

The Byte Done Status bit in the Host Status Register will be set 1 when the master has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands).

Note: On the block read command, software shall write 1 to LAST BYTE bit in Host Control Register when the next byte will be the last byte to be received.

I2C Block Read

This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.

In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent. Bit 0 of the Transmit Slave Address Register has to be 0. The received data is stored in the Host Block Data Byte register.

I2C-compatible Write Command

In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent and the transmitted data is set in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has completed transmission of a byte.

Note: Software shall write 0 to I2C_EN bit in Host Control Register 2 when the cycle is decided to be finished.

I2C-compatible Read Command

In I2C-compatible Read Command, the Transmit Slave Address Register is sent and the received data is stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has received a byte.

Note: Software shall write 1 to LABY bit in the Host Control Register when the next byte to be received is the last one.

I2C-compatible Combined Command

This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in I2C-compatible cycles.

In I2C-compatible Combined Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent. Bit 0 of the Transmit Slave Address Register is set to decide the direction of the cycle and the received data is also stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set 1 when the host has completed transmission of a byte or received a byte.

Note: Software shall control the I2C_SW_EN bit and I2C_SW_WAIT bit in Host Control Register 2 when the direction switch is decided to be performed.

9.14.3.2 SMBus Slave Interface

The slave supports the following three types of messages: Byte Write, Byte Read, and Host Notify.

When an interrupt to INTC (INT9 for SMBus slave) is detected, software can read the Slave Status Register to know the interrupt source. There are 4 interrupt conditions: STOP Condition Detect Status, Slave Timeout Status, Slave Data Status, and Host Notify Status. In the Byte Write/Byte Read command, software must write/read data in the Slave Data Register twice to release the SMCLK line. For the first time, software would set/get data in the Slave Data Register, but the SMCLK line would not be released. The SMCLK line would be held low until software writes/reads data in the Slave Data Register for the second time, after which the SMCLK line would be released.

Byte Write

In the byte write command, the value of the first received byte (Slave Address) must match the value in Receive Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the Slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time). After the data is read, the third byte (Data) is received and stored in the Slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time).

Byte Read

In the byte read command, the value of the first received byte (Slave Address) must match the value in Receive Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the Slave Data Register and waiting for the software to read the data (for the first time). The SMCLK line will be held low until the data is read (for the second time). After the Repeated Start and Slave Address cycle, the software shall write the data to the Slave Data Register (for the first time) and this register will be sent during the Data Byte Cycle. The SMCLK line will be held low until the data is set in the Slave Data Register for the second time, after which the SMCLK line would be released.

Host Notify Command

In the host notify command, the first received byte must be 0001000b. The second received byte is stored in the Notify Device Address Register. The next two bytes are stored in the Notify Data Low Byte Register and Notify Data High Byte Register.

9.14.3.3 SMBus Porting Guide

(1).SMBus Master Interface:

The SMBus controller requires that various data and command registers be setup for the message to be sent. When the START bit in the Host Control Register is set, the SMBus controller will perform the requested transaction. Any register values needed for computation purposes should be saved prior to issuing of a new command.

The “Timing Registers” (22h~28h, 33h) should be programmed before the transaction starts. In addition, the SMCLK frequency of channel A~C can be switched independently to 50 kHz, 100 kHz, or 400 kHz by setting the registers 41h~42h, which means SMCLK timing doesn’t relate to “Timing Register (22h~28h, 33h).” Besides the 25ms Register, all of the other count numbers are based on EC clock. For example, write the 1Bh

(37 / FreqEC \approx 4.0us) into the 4.0us register.

(FreqEC is listed in Table 12-1. Clock Timing Parameter on page 355 and this example assumes FreqEC = 9.2 MHz.)

The IT8733 SMBus Interface can perform SMBus messages with either packet error checking (PEC) enabled or disabled (PEC_EN bit = 1 or 0 in the Host Control Register). The actual PEC calculation and checking is performed in software.

Here is the steps the software shall follow to program the registers for various command.

1. Quick Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Quick Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register).
- (3). Start the transaction (Write 41h to the Host Control Register, which will select the “Quick Command”, enable the interrupts, and start the transaction).
- (4). When the data transmission was completed, an interrupt is generated. Software can read the Host Status Register to know the source of the interrupt.

Note: After reading the Status Register, the software must write 1 to clear it.

2. Send Byte Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Send Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to the Transmit Slave Address Register and Host Command Register) (Host Command Register is used for transmitting data here). Bit 0 of the Transmit Slave Address Register has to be 0.
- (3). Start the transaction (Write 45h to the Host Control Register, which will select the “Send Byte/Receive Byte Command”, enable the interrupts, and start the transaction).
- (4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

3. Receive Byte Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Receive Byte Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register). Bit 0 of the Transmit Slave Address Register has to be 1.
- (3). Start the transaction (Write 45h to the Host Control Register, which will select the “Send Byte/Receive Byte Command”, enable the interrupts, and start the transaction).
- (4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
- (5). In Receive Byte Command, the received data is stored in the Host Data 0 Register. Software can read this register to get the data.

4. Write Byte Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Write Byte Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register and this register will be sent, too.
- (3). Start the transaction (Write 49h to the Host Control Register, which will select the “Write Byte/Read Byte Command”, enable the interrupts, and start the transaction).

- (4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

5. Write Word Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Write Word Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register. And this register will be sent, too.
- (3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).
- (4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

6. Read Byte Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Read Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
- (3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
- (4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
- (5). In Read Byte Command, the data received is stored in the Host Data 0 Register. Software can read this register to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

7. Read Word Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Read Word Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
- (3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).
- (4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
- (5). In Read Word Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

8. Process Call Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
- (2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Process Call Command will skip the command code.
- (3). In Process Call Command, the Transmit Slave Address Register, Host Command Register (if I2C_EN = 0), Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
- (4). Start the transaction (Write 51h to the Host Control Register, which will select the "Process Call

- Command", enable the interrupts, and start the transaction).
- (5). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
 - (6). In Process Call Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

9. Block Write Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
- (2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Block Write Command will skip sending the byte count (Host Data 0 Register).
- (3). In Block Write Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from the Host Block Data Byte Register (Software shall write data to this register).
- (4). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
- (5). When the data in Host Block Data Byte Register is sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (6). Software writes the data to the Host Block Data Byte Register, then the data is sent from this register by SMBus logic.
- (7). Repeat step (5) and (6) for the other data byte until all of the data were sent.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register and this register will be sent, too.
- (8). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

10. Block Read Command

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In Block Read Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
- (3). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
- (4). When the byte count and the first byte data are received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (5). Software read the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the first data byte.
- (6). When the next data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (7). Software read the data from the Host Block Data Byte Register to get the data.
- (8). Repeat step (6) and (7) until the last byte.
- (9). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
- (10). Get an interrupt and receive the last byte.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

11. I2C Block Read Command

This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.

- (1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
- (2). In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
- (3). Start the transaction (Write 59h to the Host Control Register, which will select the "I2C Block Read Command", enable the interrupts, and start the transaction).
- (4). When the data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (5). Software can read the data from the Host Block Data Byte Register to get the data.
- (6). Repeat step (4) and (5) until the last byte.
- (7). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
- (8). Get an interrupt and receive the last byte.

12. I2C-compatible Write Command

- (1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
- (2). Set the I2C_EN bit in the Host Control Register 2 to 1.
- (3). In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
- (4). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
- (5). When the data in the Host Block Data Byte Register has been transmitted, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (6). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is transmitted from this register by the SMBus logic.
- (7). Repeat step (5) and (6) for the other data bytes until software wants to finish the cycle.
- (8). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
- (9). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
- (10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

13. I2C-compatible Read Command

- (1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
- (2). Set the I2C_EN bit in the Host Control Register 2 to 1.
- (3). In I2C-compatible Read Command, the Transmit Slave Address Register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register.
- (4). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
- (5). When the data has been received from the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
- (7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
- (8). Set the LABY bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.

- (9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
- (10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

14. I2C-compatible Combined Command

This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in the I2C-compatible cycles.

From I2C Write Command to I2C Read Command:

- (1). In the I2C Write Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Read Command.
- (2). After the last transmitted data byte has been sent in the I2C Write Command, the Byte Done interrupt will be generated. Then, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Read Command.
- (3). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
- (4). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Read Command.
- (5). When the data has been received and stored in the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
- (7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
- (8). Set the LABY bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.
- (9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
- (10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

From I2C Read Command to I2C Write Command:

- (1). In the I2C Read Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Write Command.
- (2). In the I2C Read Command, after setting the LABY bit in the Host Control Register, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Write Command.
- (3). Get the Byte Done interrupt of the last byte, and receive the last byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
- (4). Software writes the transmitted data byte in the Host Block Data Byte Register.
- (5). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Write Command.
- (6). When the data in the Host Block Data Byte Register has been sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
- (7). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is sent from this register by the SMBus logic.
- (8). Repeat step (6) and (7) for the other data bytes until software wants to finish the cycle.
- (9). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
- (10). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
- (11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

(2).SMBus Slave Interface:

The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.

Here are the steps the software shall follow to program the registers for various commands.

1. Byte Write

- (1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
- (2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
- (3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the data transmission from the external SMBus device.
- (4). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
- (5). Software can read the data from the Slave Data Register for the first time. (This data byte is the command code.) The SMCLK line would be held low until software reads the data for the second time.
- (6). When the next interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
- (7). Software can read the data from the Slave Data Register for the first time. (This data byte is the Data Byte in SMBus Protocol.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be released.

2. Byte Read

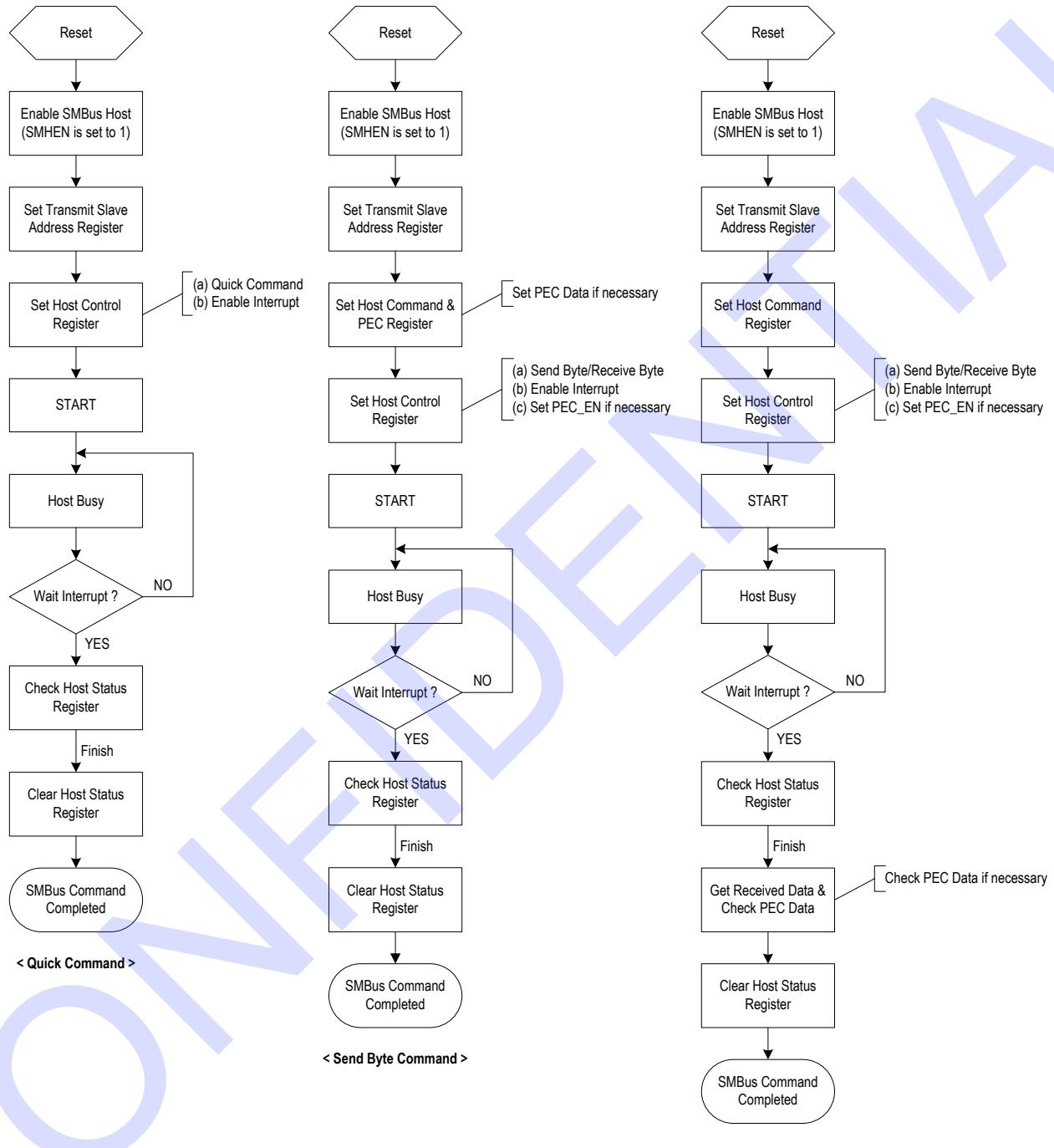
- (1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
- (2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
- (3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the data transmission from the external SMBus device.
- (4). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Read Command).
- (5). Software can read the data from the Slave Data Register for the first time. (This data byte is the command code.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be released.
- (6). When the next interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 0Ah for Byte Read Command).
- (7). Software can write the data to the Slave Data Register for the first time. (This data will be sent to the external device.) The SMCLK line would be held low until software reads the data for the second time, after which the SMCLK line would be released.

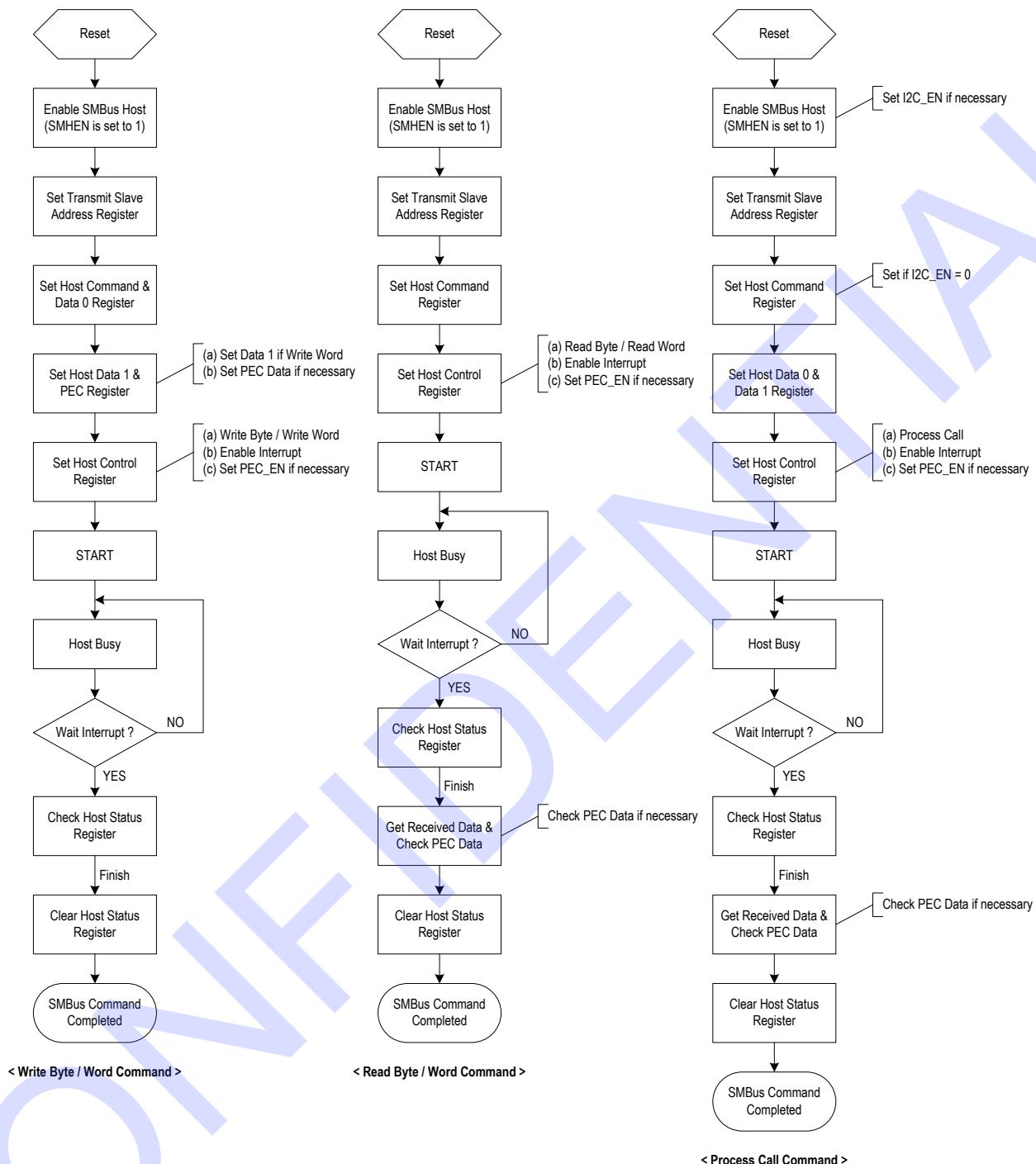
3. Host Notify Command

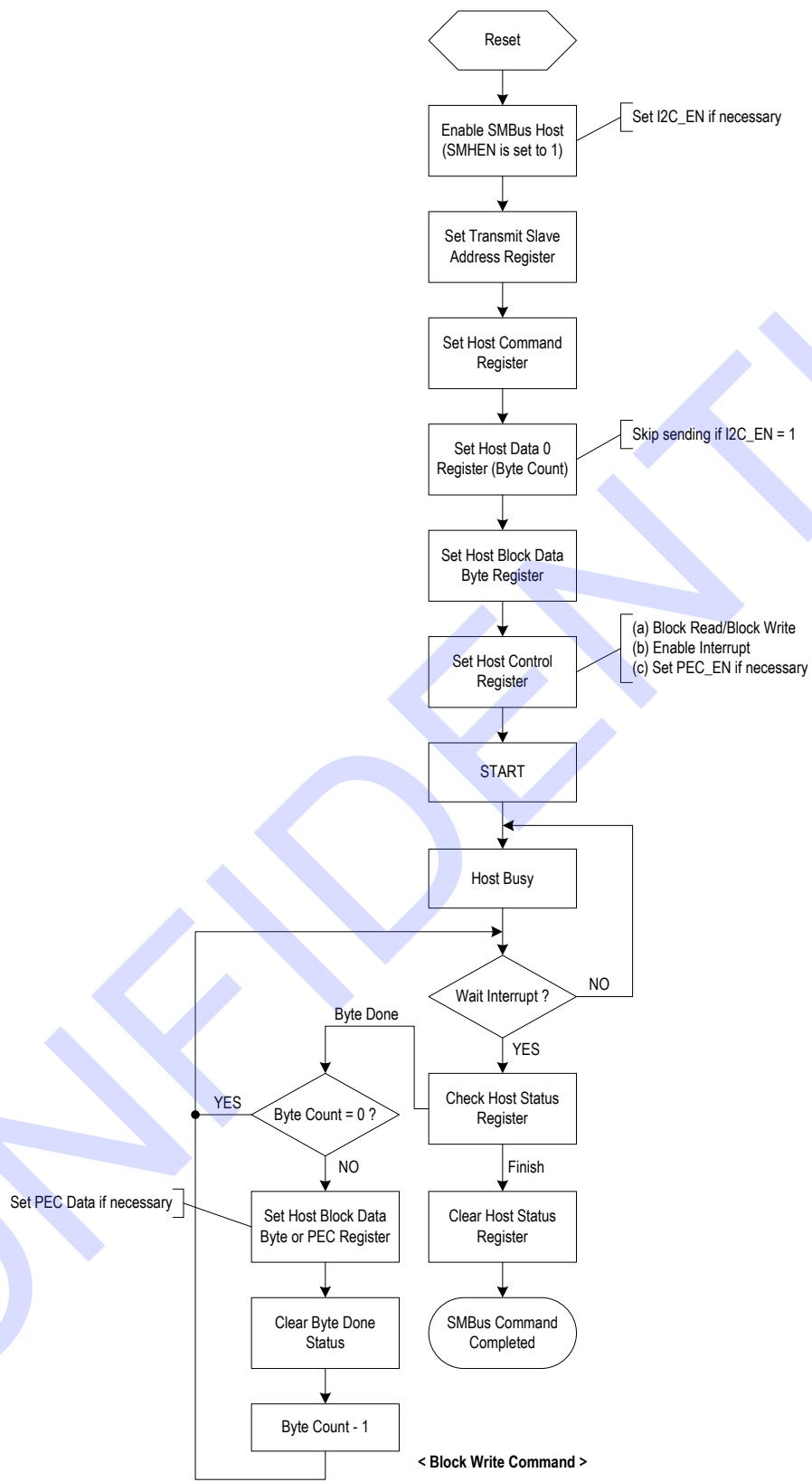
- (1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
- (2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
- (3). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 01h for Host Notify Command).
- (4). Software can read the data from the Notify Device Address Register, Notify Data Low Byte Register, and Notify Data High Byte Register.

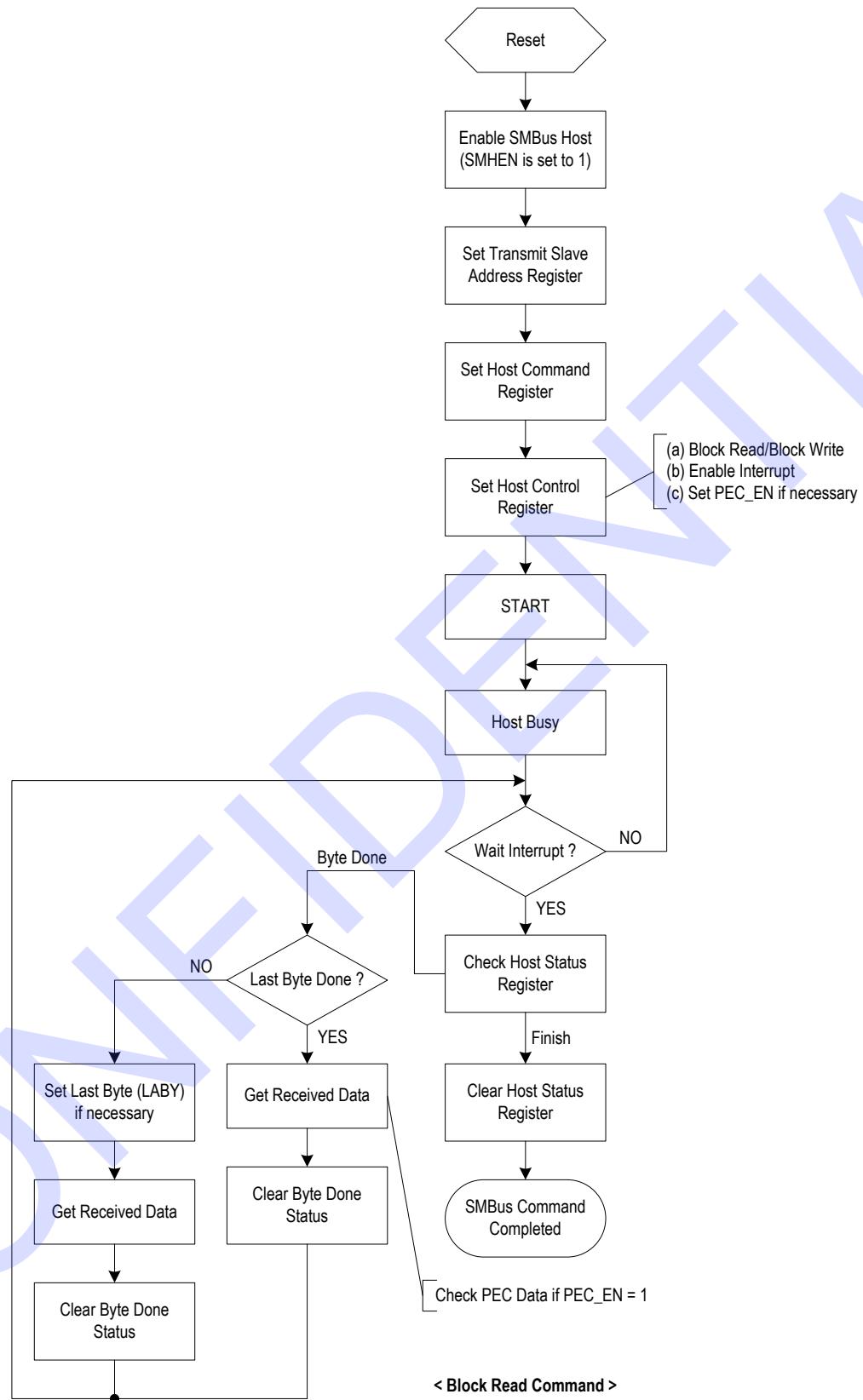
9.14.3.4 SMBus Master Programming Guide

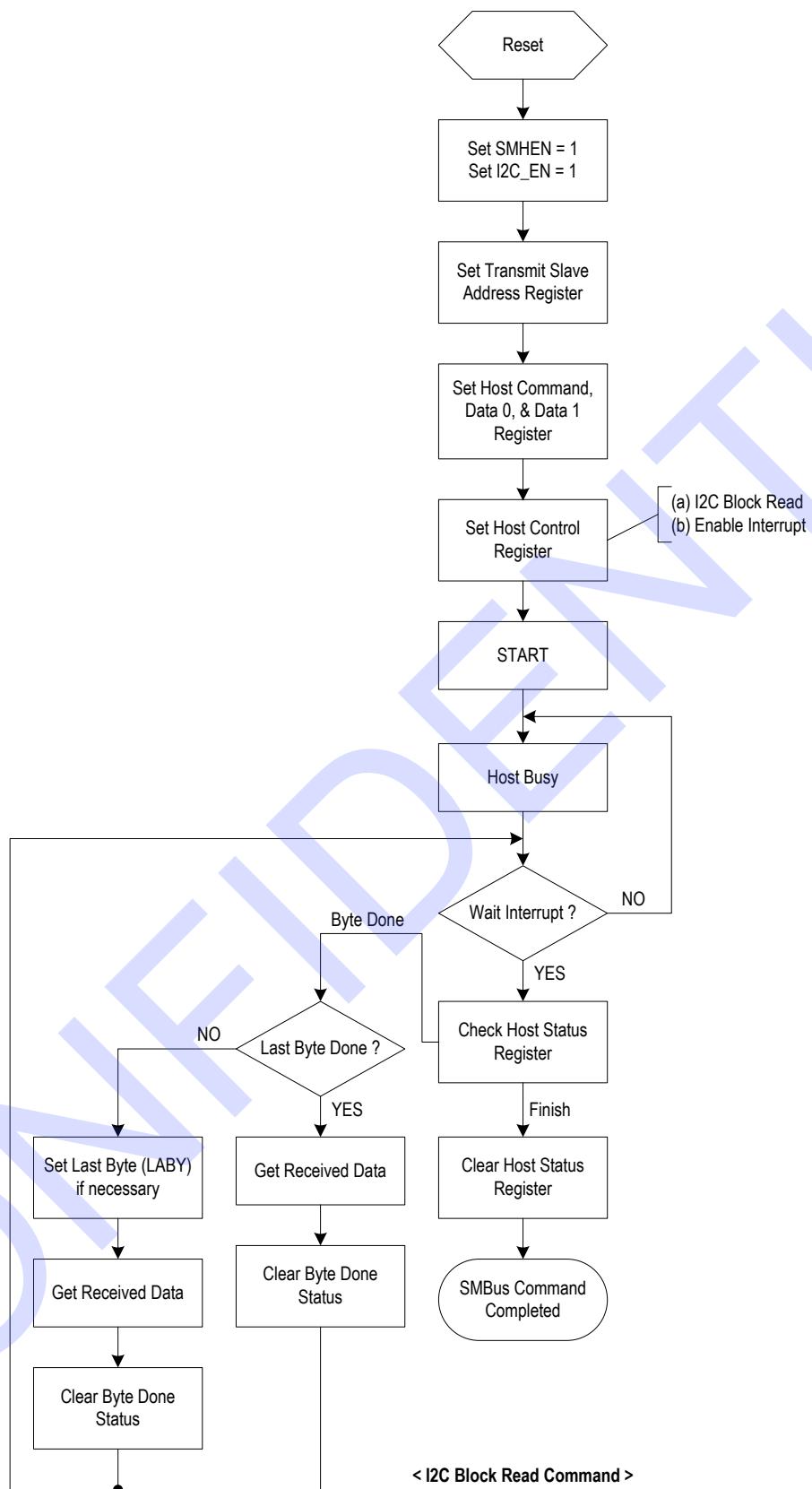
Figure 9-21 Program Flow Chart of SMBus Master Interface

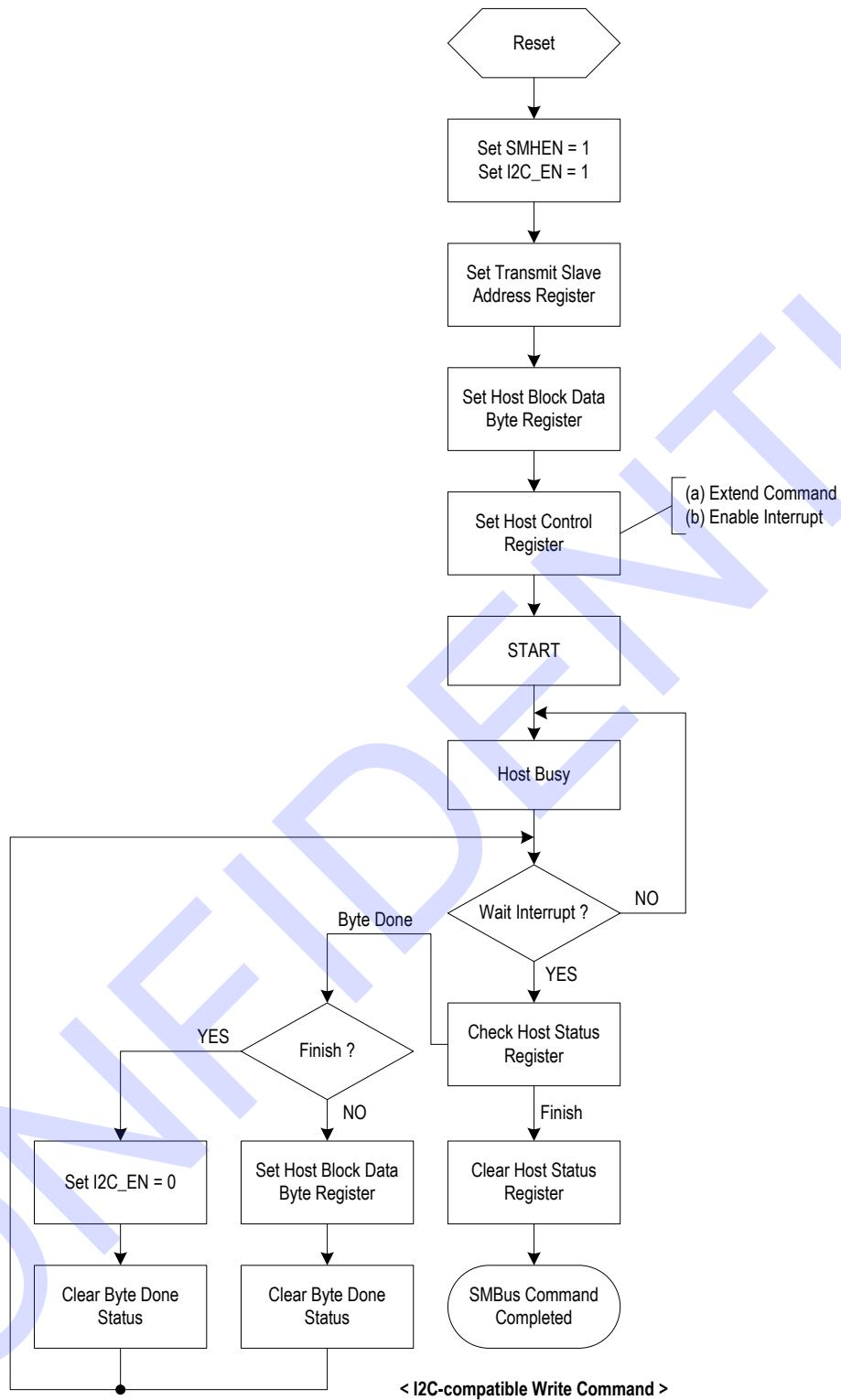


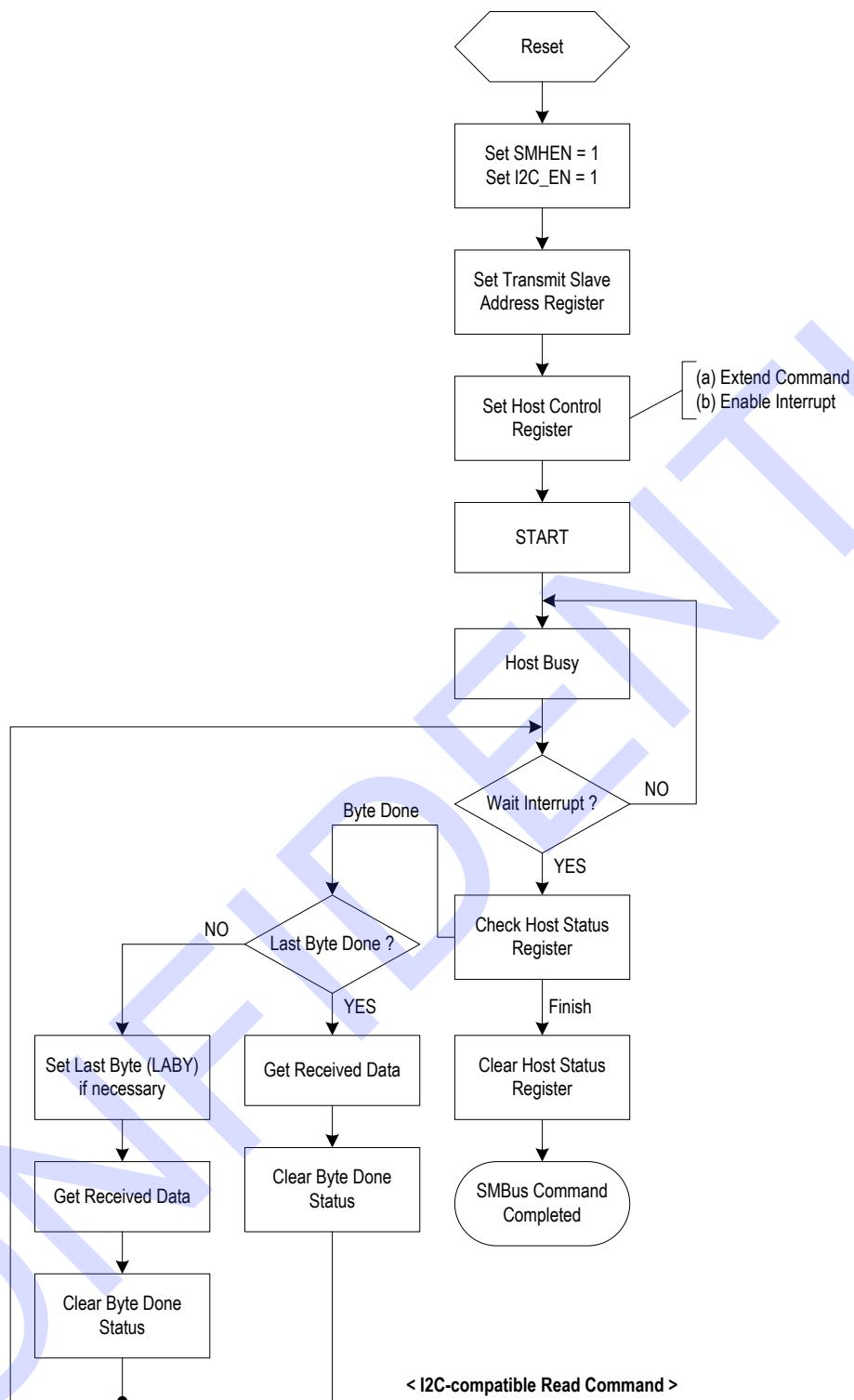


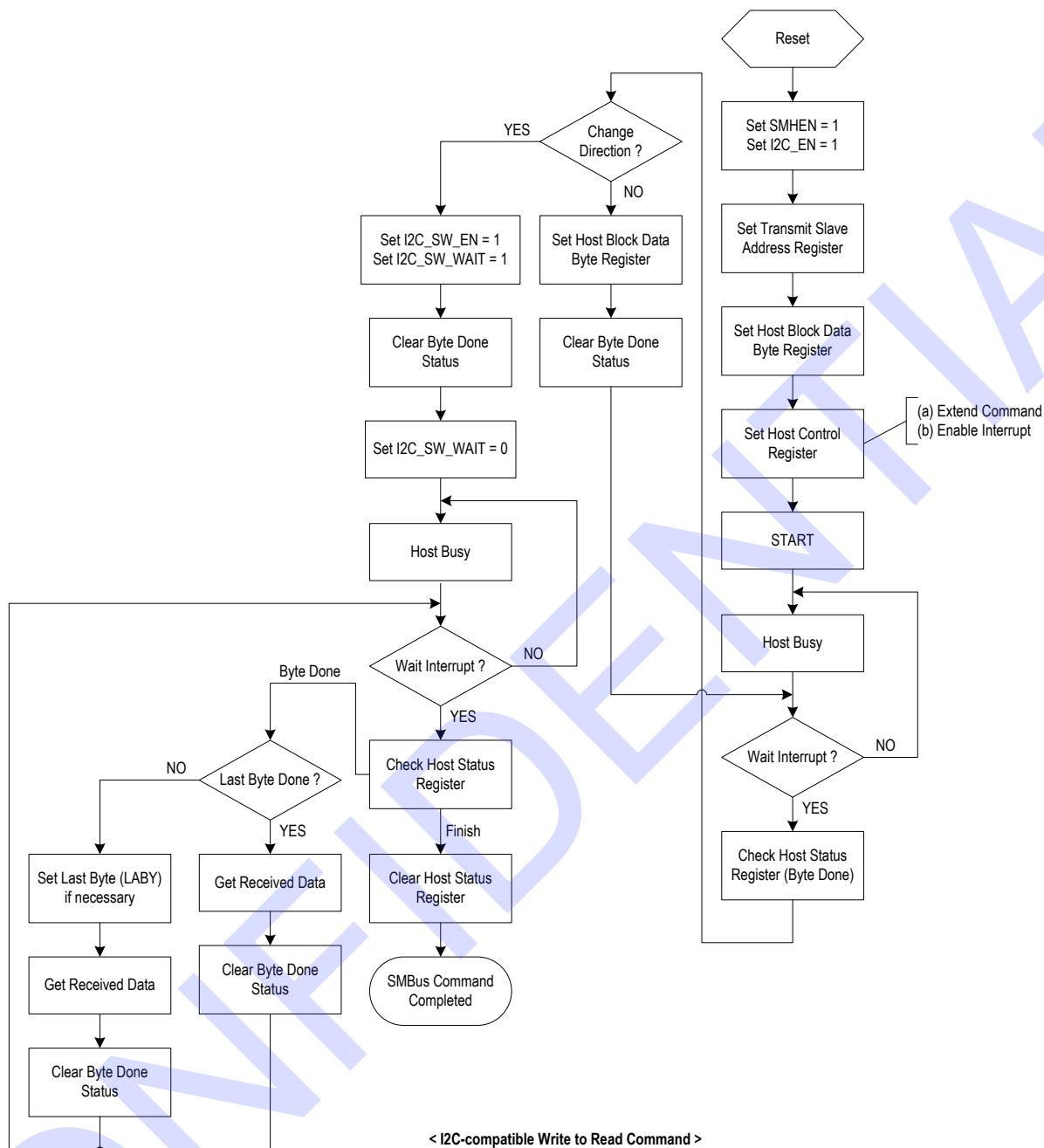




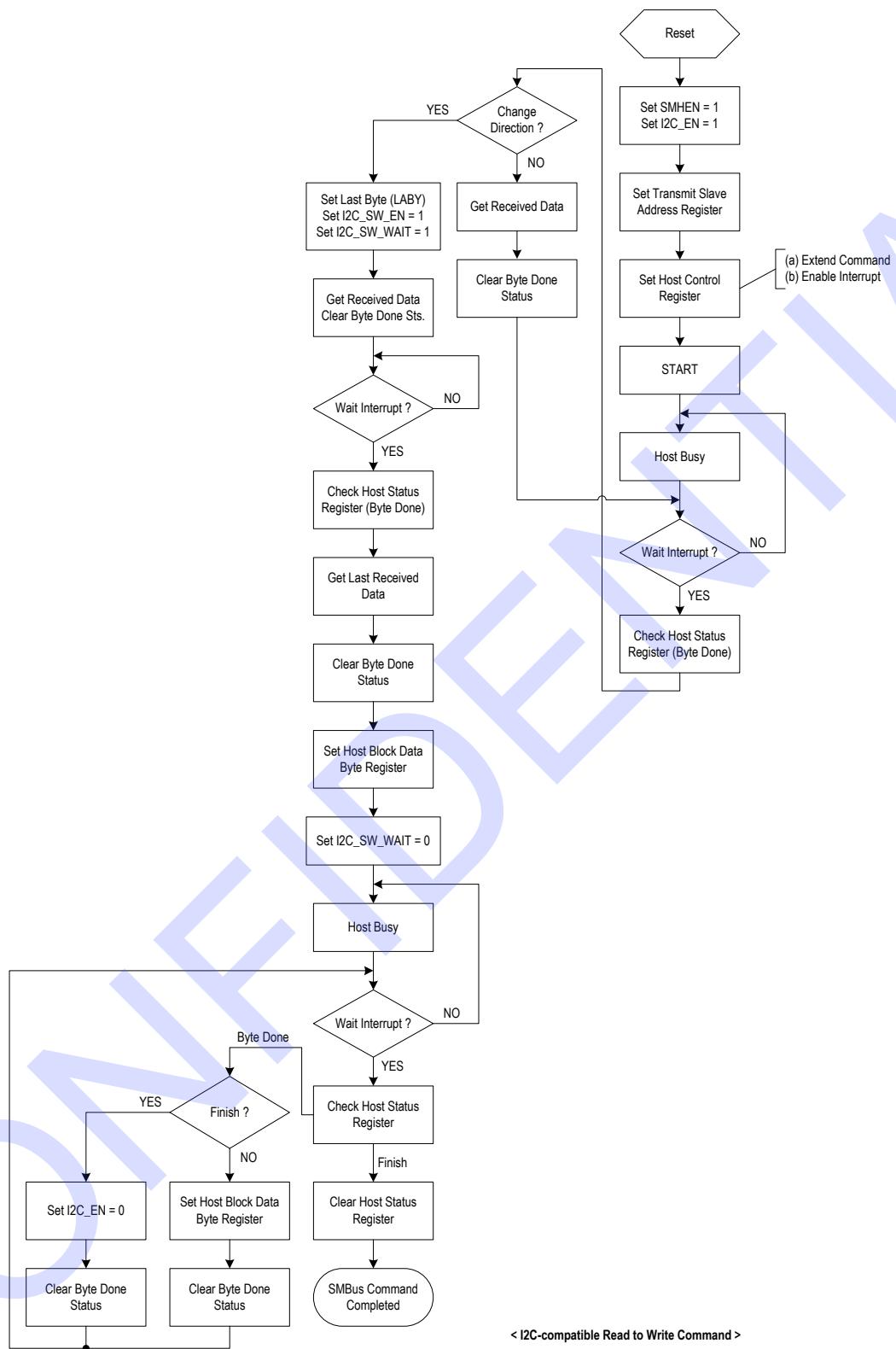








< I2C-compatible Write to Read Command >



9.14.3.5 Description of SMCLK and SMDAT Line Control in Software Mode

- (1) Control the SMCLK and SMDAT line by setting SCLCTL bit, SDACTLE bit, and SDACTL bit in SMBus Pin Control register (a.k.a., in software mode).
- (2) When the SMCLK and SMDAT line are controlled in software mode, the hardware's SMBus logic will be reset, so the hardware will release the SMCLK and SMDAT line.
- (3) The hardware's mechanism of 25 ms time-out will not work in software mode.

Note: It is recommended that SMCLK and SMDAT line should not be controlled in software mode and hardware mode simultaneously.

9.14.3.6 Description of SMBus Slave Interface Select

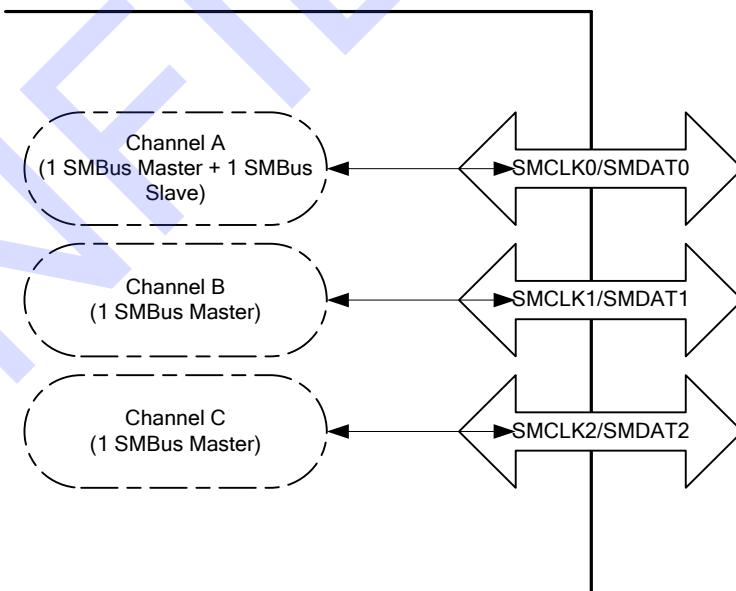
The interface of the SMBus slave can be switched from SMCLK0/SMDAT0 (default) to SMCLK1/SMDAT1 or SMCLK2/SMDAT2 by setting the SLVISEL bits in the Slave Interface Select Register. Followings are the detailed description:

- (1) When the interface of the SMBus slave is switched to SMCLK1/SMDAT1 (set the SLVISEL bit to 01b), it represents that the interface of Channel A and Channel B are exchanged, as shown in Figure 9-22.
- (2) When the interface of the SMBus slave is switched to SMCLK2/SMDAT2 (set the SLVISEL bit to 10b), it represents that the interface of Channel A and Channel C are exchanged, as shown in Figure 9-22.
- (3) When the interface of the SMBus slave is switched to SMCLK3/SMDAT3 (set the SLVISEL bit to 11b), it represents that the interface of Channel A and Channel D are exchanged, as shown in Figure 9-22.
- (4) When the interface of the SMBus slave in channel B is switched to SMCLK2/SMDAT2 (set the SLVISEL[3:2] to 10b), it represents that the interfaces of Channel B and Channel C are exchanged, as shown in Figure 9-22.

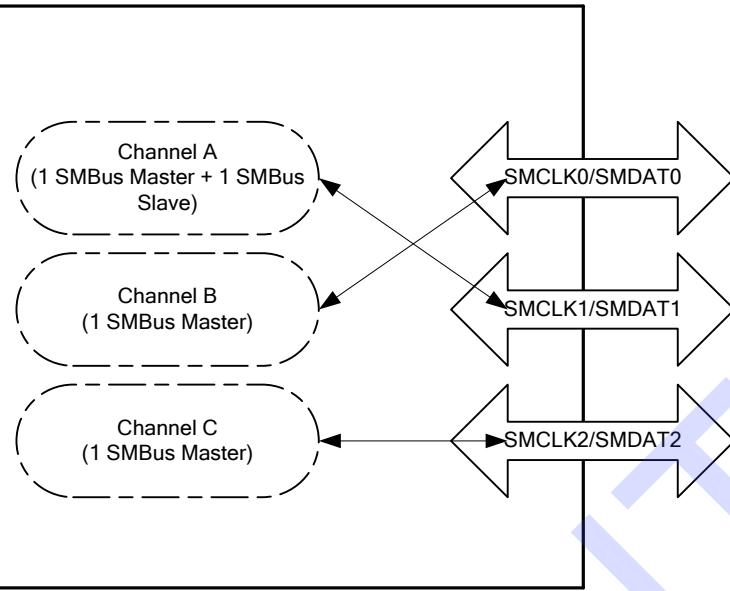
Note: If the interface of the SMBus slave in channel A is switched to SMCLK1/SMDAT1 (the default interface of SMBus slave in channel B), the interface of the SMBus slave in channel B will be automatically switched to SMCLK0/SMDAT0.

Note: Switching the interfaces of the two slaves to the same interface is invalid.

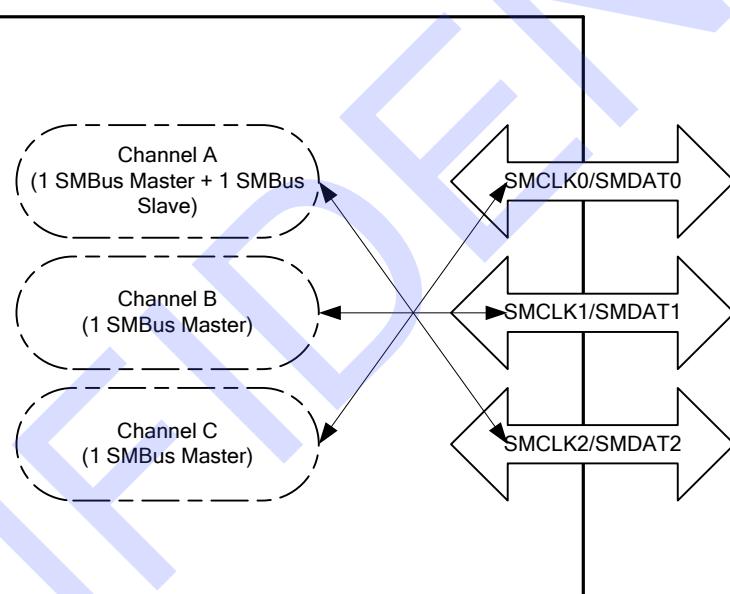
Figure 9-22 Schematic Diagram of SMBus Slave Interface Select



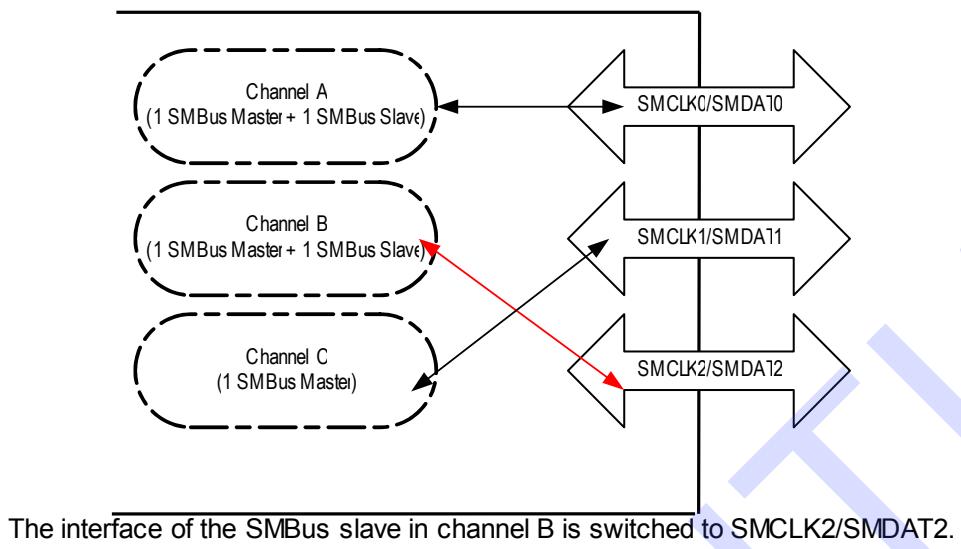
The interface of the SMBus slave is switched to SMCLK0/SMDAT0 (Default).



The interface of the SMBus slave is switched to SMCLK1/SMDAT1.



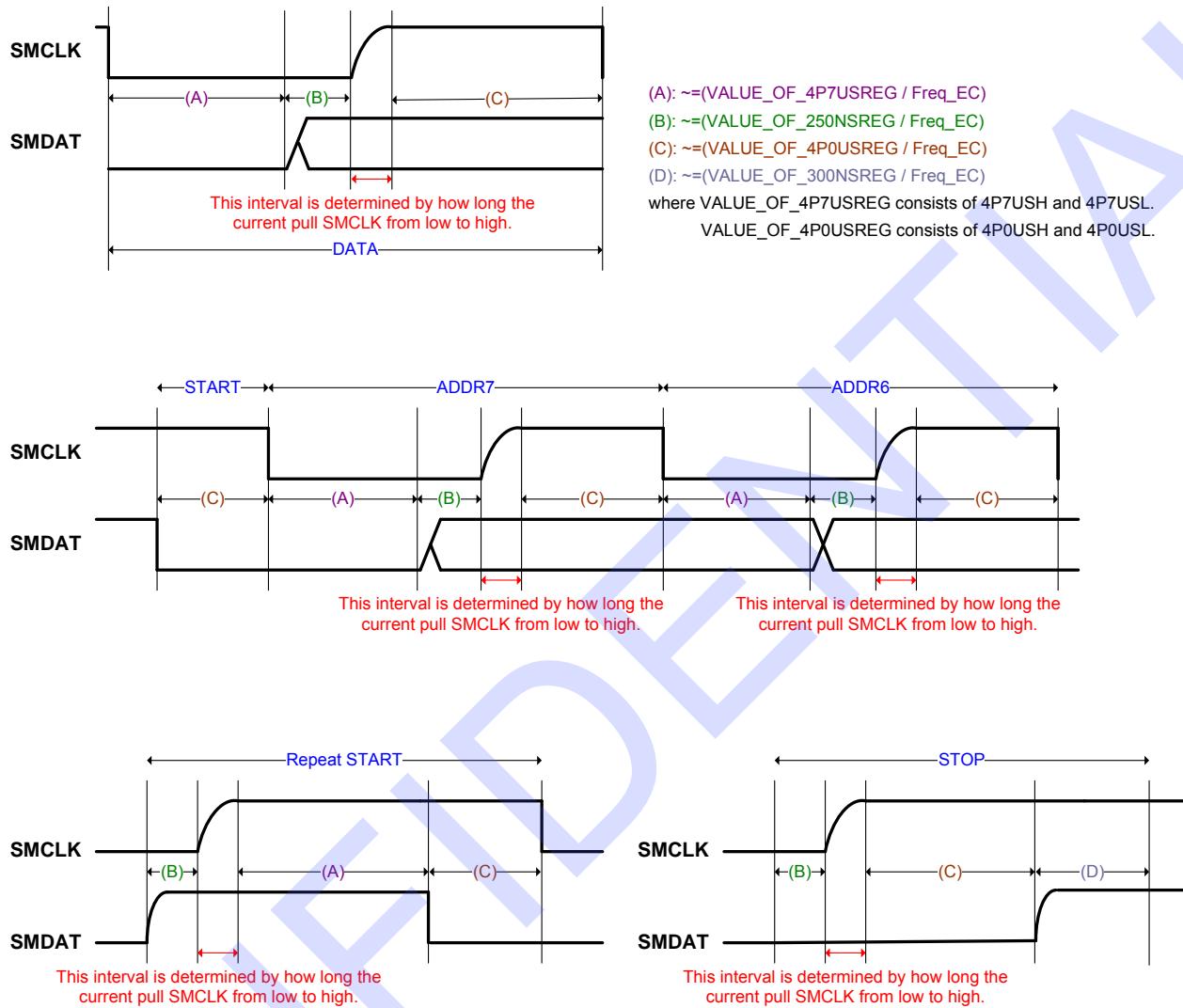
The interface of the SMBus slave is switched to SMCLK2/SMDAT2.



The interface of the SMBus slave in channel B is switched to SMCLK2/SMDAT2.

9.14.3.7 SMBus Waveform

Figure 9-23. SMBus Waveform versus SMBus Timing Registers



9.14.4 EC Interface Registers

The SMBus I/O registers are listed below. The base address for SMBus is 1C00h. A, B, and C are for channel A, B, and C respectively.

Table 9-31. EC View Register Map, SMBus

7	0	Offset
Host Status (HOSTA)(A, B,C)	00h,11h,29h	
Host Control (HOCTL)(A, B,C)	01h,12h,2Ah	
Host Command (HOCMD)(A, B,C)	02h,13h,2Bh	
Transmit Slave Address (TRASLA)(A, B,C)	03h,14h,2Ch	
Host Data 0 (D0REG)(A, B,C)	04h,15h,2Dh	
Host Data 1 (D1REG)(A, B,C)	05h,16h,2Eh	
Host Block Data Byte (HOBDB)(A, B,C)	06h,17h,2Fh	
Packet Error Check (PECERC)(A, B,C)	07h,18h,30h	
Receive Slave Address (RESLADR) (A, B)	08h,19h	
Receive Slave Address 2 (RESLADR_2) (A, B)	3Fh,44h	
Slave Data (SLDA) (A, B)	09h,1Ah	
SMBus Pin Control (SMBPCTL)(A, B,C)	0Ah,1Bh,31h	
Slave Status (SLSTA) (A, B)	0Bh,1Ch	
Slave Interrupt Control (SICR) (A, B)	0Ch,1Dh	
Notify Device Address (NDADR) (A, B)	0Dh,1Eh	
Notify Data Low Byte (NDLB) (A, B)	0Eh,1Fh	
Notify Data High Byte (NDHB) (A, B)	0Fh,20h	
Host Control2 (HOCTL2)(A, B,C)	10h,21h,32h	
4.7 μ s Low Register (4P7USL)	22h	
4.0 μ s High Register (4P0USH)	23h	
300 ns Register (300NS)	24h	
250 ns Register (250NS)	25h	
25 ms Register (25MS)	26h	
45.3 μ s Low Register (45P3USL)	27h	
45.3 μ s High Register (45P3USH)	28h	
4.7 μ s and 4.0 μ s High Register (4P7A4P0H)	33h	
Slave Interface Select Register (SLVISEL)	34h	
SMCLK Timing Setting Register A (SCLKTS_A)	40h	
SMCLK Timing Setting Register B (SCLKTS_B)	41h	
SMCLK Timing Setting Register C (SCLKTS_C)	42h	

9.14.4.1 Host Status Register (HOSTA)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software. Software can read this register to know the source of the interrupt (Master Interface).

Address Offset:

- Channel A: 00h**
- Channel B: 11h**
- Channel C: 29h**

Bit	R/W	Default	Description
7	R/WC	0b	Byte Done Status (BDS) This bit will be set to 1 when the host controller has received a byte (for Block Read commands and I2C-compatible cycles) or if it has completed the transmission of a byte (for Block Write commands and I2C-compatible cycles).
6	R/WC	0b	Time-out Error (TMOE) 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when 25ms time-out error occurs.
5	R/WC	0b	Not Response ACK (NACK) 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when the device does not respond ACK.
4	R/WC	0b	Fail (FAIL) 0: This bit is cleared by writing a 1 to the bit position. 1: Reading this bit will return 1 if KILL is set and a processing transmission is successfully killed.
3	R/WC	0b	Bus Error (BSER) 0: This bit is cleared by writing a 1 to the bit position. 1: The source of the interrupt is that the SMBus has lost arbitration.
2	R/WC	0b	Device Error (DVER) 0: This bit is cleared by writing a 1 to this bit's position. 1: This bit is set in one of the following conditions: (1) 25ms Time-out Error. (2) Not response ACK.
1	R/WC	0b	Finish Interrupt (FINTR) This bit will be set by termination of a command. 0: This bit is cleared by writing 1 to this position. 1: The source of the interrupt is the stop condition detected.
0	R	0b	Host Busy (HOBY) 0: This bit is cleared when the current transaction is completed. 1: This bit is set while the command is in operation.

9.14.4.2 Host Control Register (HOCTL)

Address Offset: Channel A: 01h
 Channel B: 12h
 Channel C: 2Ah

Bit	R/W	Default	Description
7	R/W	0b	PEC Enable (PEC_EN) 0: The transaction without the PEC (Packet Error Checking) phase0 appended 1: The transaction with the PEC phase appended.
6	W	0b	Start (SRT) 0: This bit will always return 0 on reads. 1: When this bit is set, the SMBus host controller will perform the requested transaction.
5	W	0b	Last Byte (LABY) This bit is used for Block Read command and I2C-compatible read cycle. Read returns 1 if the next byte is the last byte to be received for the block read command and I2C-compatible read cycle. The firmware shall write 1 to this bit when the next byte will be the last byte to be received for the block read command and I2C-compatible cycle.
4-2	R/W	000b	SMBus Command (SMCD) These bits indicate which command will be performed. Bit 0 of the Transmit Slave Address Register determines if this is a read or write command. 000:Quick Command 001:Send Byte/ Receive Byte 010:Write Byte/ Read Byte 011:Write Word/ Read Word 100:Process Call 101:Block Read/ Block Write 110:I2C Block Read 111:Extend Command
1	R/W	0b	Kill (KILL) 0: Normal SMBus Host controller functionality. 1: When this bit is set, kill the current host transaction. This bit, once set, has to be cleared by software to allow the SMBus Host controller to function normally.
0	R/W	0b	Host Interrupt Enable (INTREN) 0: Disable. 1: Enable the generation of an interrupt for the master interface

9.14.4.3 Host Command Register (HOCMD)

Address Offset: Channel A: 02h
 Channel B: 13h
 Channel C: 2Bh

Bit	R/W	Default	Description
7-0	R/W	00h	Host Command Register (HCREG) These bits are transmitted in the command field of the SMBus protocol.

9.14.4.4 Transmit Slave Address Register (TRASLA)

Address Offset: Channel A: 03h
 Channel B: 14h
 Channel C: 2Ch

Bit	R/W	Default	Description
7-1	R/W	00h	Address (ADR) Address of the targeted slave.
0	R/W	0b	Direction (DIR) Direction of the host transfer. 0: Write 1: Read

9.14.4.5 Data 0 Register (D0REG)

Address Offset: Channel A: 04h
 Channel B: 15h
 Channel C: 2Dh

Bit	R/W	Default	Description
7-0	R/W	00h	Data 0 (D0) These bits contain the data sent in the DATA0 (The first transaction date byte) field of the SMBus protocol. For block write commands, this register reflects the number (from 1 to 32) of bytes to transfer.

9.14.4.6 Data 1 Register (D1REG)

Address Offset: Channel A: 05h
 Channel B: 16h
 Channel C: 2Eh

Bit	R/W	Default	Description
7-0	R/W	00h	Data 1 (D1) These bits contain the data sent in the DATA1 (Data Byte High) field of the SMBus protocol.

9.14.4.7 Host Block Data Byte Register (HOBDB)

Address Offset: Channel A: 06h
 Channel B: 17h
 Channel C: 2Fh

Bit	R/W	Default	Description
7-0	R/W	00h	Block Data (BLDT) For a block write command, data is sent from this register. On block read command, the received data is stored in this register.

9.14.4.8 Packet Error Check Register (PECERC)

Address Offset: Channel A: 07h
 Channel B: 18h
 Channel C: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	PEC Data (PECD) These bits are written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software.

9.14.4.9 Receive Slave Address Register (RESLADR)

Address Offset: 08h (Only for Channel A)
 19h (Only for Channel B)

Bit	R/W	Default	Description
7	-	0b	Reserved
6-0	R/W	00h	Slave Address (SADR) These bits are the slave address decoded for read and write cycles.

9.14.4.10 Receive Slave Address Register 2 (RESLADR2)

Address Offset: 3Fh (Only for Channel A)
 44h (Only for Channel B)

Bit	R/W	Default	Description
7	R/W	0b	Slave Address 2 Enable 0: SADR2 field is ignored. 1: SADR2 field holds a valid address and enables the function to decode SADR2 for comparison with the received address.
6-0	R/W	00h	Slave Address 2 (SADR2) These bits are the slave address 2 decoded for read and write cycles.

9.14.4.11 Slave Data Register (SLDA)

Address Offset: 09h (Only for Channel A)
 1Ah (Only for Channel B)

Bit	R/W	Default	Description
7-0	R/W	00h	Slave Data Byte0 (SDB0) This register stores the data received from the external master. When this register is served, software must write/read data stored in this register twice to release the SCL line. (See also section 9.14.3.3 SMBus Porting Guide on page 214)

9.14.4.12 SMBus Pin Control Register (SMBPCTL)

Address Offset: Channel A: 0Ah
 Channel B: 1Bh
 Channel C: 31h

Bit	R/W	Default	Description
7-5	-	0h	Reserved
4	W	0b	SMDAT Control Enable (SDACTLE) This bit is used to enable the SMDAT Control (SDACTL) bit setting. It is write-only, and always returns 0 on reads.
3	R/W	1b	SMDAT Control (SDACTL) Only when the SMDAT Control Enable (SDACTLE) bit is set to 1 to 1 at the same time, this bit can be written as the following: 0: The SMDAT0/1/2 pin will be driven low regardless of the other SMBus logic. 1: The SMDAT0/1/2 pin will not be driven low. The other SMBus logic controls this pin.
2	R/W	1b	SMCLK Control (SCLCTL) 0: The SMCLK0/1/2 pin will be driven low regardless of the other SMBus logic. 1: The SMCLK0/1/2 pin will not be driven low. The other SMBus logic controls this pin.
1	R	-	SMDAT Current State (SMBDCS) This bit returns the value of the SMDAT0/1/2 pin. 0: Low 1: High
0	R	-	SMCLK Current State (SMBCS) This bit returns the value of the SMCLK0/1/2 pin. 0: Low 1: High

9.14.4.13 Slave Status Register (SLSTA)

Software can read this register to know the source of the interrupt (Slave Interface).

Address Offset: 0Bh (Only for Channel A)
 1Ch (Only for Channel B)

Bit	R/W	Default	Description
7-6	-	0h	Reserved
5	R/WC	0b	Stop Condition Detect Status (SPDS) 0: Cleared by writing a 1 to this bit. 1: Indicate Stop Condition detected.
4	R	0b	Match Slave Address 2 (MSLA2) 0: The received address is matched with SADR. 1: The received address is matched with SADR2. Don't care when Host notify command.
3	R	0b	Read Cycle Status (RCS) Direction of the slave transfer. 0: Write. 1: Read.
2	R/WC	0b	Slave Timeout Status (STS) 0: Cleared by writing a 1 to this bit. 1: Timeout status occurs.

Bit	R/W	Default	Description
1	R/WC	0b	Slave Data Status (SDS) 0: Cleared by writing a 1 to this bit. 1: Slave Data Register is waiting for read or write. When this bit is set and the Read Cycle Status (RCS) bit is low, the software shall read the data from the Slave Data Register. When this bit is set and the Read Cycle Status (RCS) bit is high, the software shall write the data to the Slave Data Register.
0	R/WC	0b	Host Notify Status (HONOST) This bit will be set to a 1 when a Host Notify Command has been completely received. Software can read this bit to determine that the source of the interrupt is the reception of the Host Notify Command.

9.14.4.14 Slave Interrupt Control Register (SICR)

Address Offset: 0Ch (Only for Channel A)
1Dh (Only for Channel B)

Bit	R/W	Default	Description
7-4	-	00h	Reserved
3	R/W	0b	Slave Detect STOP Condition Interrupt Enable (SDSEN) 0: Disable 1: Enable the generation of an interrupt for STOP detected by slave
2	R/W	0b	Slave SMDAT Low Timeout Enable (SDLTOEN) This bit controls the reset mechanism of SMBus Slave to handle the SMDAT line low if 25ms timeout. 0: SMCLK will be released if timeout. 1: SMCLK/SMDAT will be released if timeout.
1	R/W	0b	Slave Interrupt Enable (SITEN) 0: Disable. 1: Enable the generation of an interrupt for the slave interface.
0	R/W	0b	Host Notify Interrupt Enable (HONOIN) 0: Disable. 1: Enable the generation of an interrupt when Host Notify Status is set and it does not affect the setting of the Host Notify Status bit.

9.14.4.15 Notify Device Address Register (NDADR)

Address Offset: 0Dh (Only for Channel A)
1Eh (Only for Channel B)

Bit	R/W	Default	Description
7-1	R	00h	Device Address (DVADR) These bits contain the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification.
0	-	0b	Reserved

9.14.4.16 Notify Data Low Byte Register (NDLB)

Address Offset: 0Eh (Only for Channel A)
1Fh (Only for Channel B)

Bit	R/W	Default	Description
7-0	R	00h	Data Low Byte (DALB) These bits contain the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

9.14.4.17 Notify Data High Byte Register (NDHB)

Address Offset: **0Fh (Only for Channel A)**
20h (Only for Channel B)

Bit	R/W	Default	Description
7-0	R	00h	Data High Byte (DAHB) These bits contain the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

9.14.4.18 Host Control Register 2 (HOCTL2)

Address Offset: **Channel A: 10h**
Channel B: 21h
Channel C: 32h

Bit	R/W	Default	Description
7-6	-	0h	Reserved
5	-	0b	SMBus Slave Enable (SLVEN) 0: Disable the SMBus Slave Device. 1: Enable the SMBus Slave Device. The SMBus host controller is disabled when this bit is set. This bit only exists in address offset 10h.
4	R/W	0b	SMDAT Timeout Enable (SMD_TO_EN) This bit controls the reset mechanism of SMBus Master to handle the SMDAT line low if 25ms timeout. 0: SMCLK will be released if timeout. 1: SMCLK/SMDAT will be released if timeout.
3	R/W	0b	I2C Switch Direction Enable (I2C_SW_EN) 0: Disable I2C Switch Direction. 1: Enable I2C Switch Direction.
2	R/W	0b	I2C Switch Direction Wait (I2C_SW_WAIT) 0: Disable I2C Switch Direction Wait. 1: Enable I2C Switch Direction Wait.
1	R/W	0b	I2C Enable (I2C_EN) 0: SMBus behavior. 1: Enable to communicate with I2C device and support I2C-compatible cycles. When this bit is set, the SMBus logic will instead be set to communicate with I2C devices and support I2C-compatible cycles. This forces the following changes: (1) The Process Call command will skip the Command code. (2) The Block Write command will skip sending the Byte Count. (3) The Extend command can be used to support I2C-compatible cycles.
0	R/W	0b	SMBus Host Enable (SMHEN) 0: Disable the SMBus Host Controller. 1: The SMBus Host interface is enabled to execute commands.

9.14.4.19 Slave Interface Select Register (SLVISELR)

Address Offset: 34h

Bit	R/W	Default	Description
7-5	-	0h	Reserved
4	R/W	0b	Override Debug Mode through SMBus (OVRSMDBG) This bit overrides Debug Mode function enabled by hardware strap in SMBus interface and disables it.
3-2	-	00b	SMBus Slave B Interface Select (SLVBISEL) These bits are to decide which interface the slave B is located at. 00b: Slave B interface is located at SMCLK0/SMDAT0. 01b: Slave B interface is located at SMCLK1/SMDAT1. 10b: Slave B interface is located at SMCLK2/SMDAT2. 11b: Slave B interface is located at SMCLK3/SMDAT3.
1-0	R/W	00b	SMBus Slave Interface Select (SLVISEL) These bits are to decide which interface the slave is located at. 00b: Reserved 01b: SMCLK1/SMDAT1 is changed to Slave interface. 10b: SMCLK2/SMDAT2 is changed to Slave interface. 11b: Reserved.

9.14.4.20 4.7 μs Low Register (4P7USL)

The following registers (22h-28h, 33h) define the SMCLK1/2 and SMDAT1/2 timing.

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R/W	00h	4.7 μs Low Register (4P7USL) This 4.7 μs Low Register and 4.7 μs high bit (in the 4.7 μs and 4.0 μs High Register) define the count number for the 4.7 μs counter. The 4.7 μs is (count number / FreqEC). (FreqEC is listed in Table 12-1. Clock Timing Parameter on page 355)

9.14.4.21 4.0 μs Low Register (4P0USL)

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R/W	00h	4.0 μs Low Register (4P0USL) This 4.0 μs Low Register and 4.0 μs high bit (in the 4.7 μs and 4.0 μs High Register) define the count number for the 4.0 μs counter. The 4.0 μs is (count number / FreqEC). (FreqEC is listed in Table 12-1. Clock Timing Parameter on page 355)

9.14.4.22 300 ns Register (300NSREG)

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	00h	300ns Register (300NS) This field defines the SMDAT1/2 hold time. This byte is the count number of the counter for 300 ns. The 300 ns is calculated by (count number / FreqEC). (FreqEC is listed in Table 12-1. Clock Timing Parameter on page 355)

9.14.4.23 250 ns Register (250NSREG)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	00h	250ns Register (250NS) This field defines the SMDAT1/2 setup time. This byte is the count number of the counter for 250 ns. The 250 ns is calculated by (count number / FreqEC). (FreqEC is listed in Table 12-1. Clock Timing Parameter on page 355)

9.14.4.24 25 ms Register (25MSREG)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R/W	00h	25 ms Register (25MS) This field defines the SMCLK1/2 clock low timeout. This byte is the count number of the counter for 25 ms. The 25 ms is calculated by (count number *1.024 kHz).

9.14.4.25 45.3 μs Low Register (45P3USLREG)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	45.3 μs Low Register (45P3USLOW) This 45.3 μs Low Register, 45.3 μs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7μs And 4.0 μs High Register) define the SMCLK1/2 high periodic (maximal). (45.3μs + 4.7μs=50μs) This byte is the count number bits [7:0] of the counter for 45.3 μs. The 45.3 μs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table 12-1. Clock Timing Parameter on page 355)

9.14.4.26 45.3 μs High Register (45P3USHREG)

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00h	45.3 μs High Register (45P3USHGH) This 45.3 μs Low Register, 45.3 μs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7μs And 4.0 μs High Register) define the SMCLK1/2 high periodic (maximal). (45.3 μs + 4.7 μs=50 μs). This byte is the count number bits [15:8] of the counter for 45.3 μs. The 45.3 μs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table Table 12-1. Clock Timing Parameter on page 355)

9.14.4.27 4.7 μ s And 4.0 μ s High Register (4p7A4P0H)

Address Offset: 33h

Bit	R/W	Default	Description
7-2	-	-	Reserved
1	R/W	0b	4.0 μs High Bit (4P0USH) This bit is bit 8 of the count number for the 4.0 μ s counter. This 4.0 μ s Low Register and 4.0 μ s High Bit define the count number for the 4.0 μ s counter.
0	R/W	0b	4.7 μs High Bit (4P7USH) This bit is bit 8 of the count number for the 4.7 μ s counter. This 4.7 μ s Low Register and 4.7 μ s High Bit define the count number for the 4.7 μ s counter.

9.14.4.28 SMCLK Timing Setting Register A (SCLKTS_A)

Address Offset: 40h

Bit	R/W	Default	Description
7-5	-	-	Reserved
4	R/W	0b	Fix Repeat Start Setup Time (FRSST) 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 9-23. on page 233 for Repeat Start period (A).
3-2	-	-	Reserved
1-0	R/W	00b	SMCLK Setting (SCLKS) These bits are to determine which SMCLK rate is for channel A. If they are disabled, the SMCLK rate will depend on the setting of original timing registers. 00b: Disable. 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

9.14.4.29 SMCLK Timing Setting Register B (SCLKTS_B)

Address Offset: 41h

Bit	R/W	Default	Description
7-5	-	-	Reserved
4	R/W	0b	Fix Repeat Start Setup Time (FRSST) 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 9-23. on page 233 for Repeat Start period (A).
3-2	-	-	Reserved
1-0	R/W	00b	SMCLK Setting (SCLKS) These bits are to determine which SMCLK rate is for channel B. If Disable, the SMCLK rate depends on the setting of original timing registers. 00b: Disable. 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

9.14.4.30 SMCLK Timing Setting Register C (SCLKTS_C)

Address Offset: 42h

Bit	R/W	Default	Description
7-5	-	-	Reserved
4	R/W	0b	Fix Repeat Start Setup Time (FRSST) 0: Repeat Start period (A) will not be fixed. 1: Repeat Start period (A) will be fixed for around 5us. Please refer to Figure 9-23. on page 233 for Repeat Start period (A).
3-2	-	-	Reserved
1-0	R/W	00b	SMCLK Setting (SCLKS) These bits are to decide which SMCLK rate for the channel C. If Disable, the SMCLK rate depends on the setting of original timing registers. 00b: Disable. 01b: 50 kHz. 10b: 100 kHz. 11b: 400 kHz.

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CONFIDENTIAL

10. EC Domain Functions

10.1 8032 Embedded Controller (EC)

10.1.1 Overview

The embedded controller is an 8032 micro-controller which is an 8051-compatible micro-controller.

10.1.2 Features

- Supports Sleep (a.k.a. power-down) and Idle mode
- Supports two external interrupts and one power fail interrupt
- Supports 64K code/data space
- Supports 256 bytes internal(w.r.t. 8032) RAM, with 128 bytes special function register
- Supports 1xwatch dog timer
- Supports full duplex UART
- Memory mapped I/O configuration

10.1.3 General Description

The 8032TT is a high-performance 8051 family compatible micro-controller based on RISC architecture & Pipeline design. This IP Specification of interface timing, external Data Memory read / write timing and external Program Memory read timing are different from that of the standard 80C52. But instruction-set is fully compatible with standard 8051 family.

Table 10-1. 8032 Port Usage

Signal	Port	Note
8032 External Data Bus	P0[7:0], P2[7:0], P3[7:6]	EC Bus MOVX instruction
INT0#	P3[2]	Driven by INTC
INT1#	P3[3]	Driven by INTC
TXD	P3[1]	TXD signal on pin
RXD	P3[0]	RXD signal on pin
T0 Timer	P3[4]	Unused
T1 Timer	P3[5]	Unused
T2 Timer	P1[0]	Unused
T2EX Timer	P1[1]	Unused

10.1.4 Functional Description

Memory

The 8032 manipulates operands in four memory spaces. There are 64K-byte Program Memory space, 64K-byte External Data Memory space, 256-byte Internal Data Memory, and with a 16-bit Program Counter space. The Internal Data Memory address space is further divided into the 256-byte Internal Data RAM and 128-byte Special Function Register address space. The up 128-bytes RAM can be reached by indirect addressing. Four Register Banks, 128 addressable bits, and the stack reside in the Internal Data RAM.

I/O ports

The 8032 has 8-bit I/O ports. The four ports provide 32 I/O lines to interface to the external world. All four ports are both byte and bit addressable. Port 0 is used as an Address/Data bus and Port 2 is used as the upper 8-bits address when external memory/device is accessed. Port 3 contains special control signals such as the read and write strobes. Port 1 is used for both I/O and external interrupts.

Interrupts

In the 8032 there are six hardware resources that generate an interrupt request. The starting addresses of the interrupt service program for each interrupt source are like standard 8052. The external interrupt request inputs (INT0#, INT1#) can be programmed for either negative edge or low level-activated operation.

Timers / Counters

The 8032 has three 16-bit timers/counters that are the same as the timers of the standard 8051 family. The 8032 has two additional watchdog timers for system failure monitor.

Serial I/O ports

The 8032 has one programmable, full-duplex serial I/O port whose function is the same as that of 8051 family and dependent on the requirement.

Power Management

The 8032 supports Idle and Doze/Sleep modes of operation. In the Idle mode, the EC 8032 is stopped operation while the peripherals continue operating. In the Doze/Sleep mode, all the clocks are stopped. The Doze/Sleep mode can be waked up by INT0# or INT1# external interrupt with level trigger.

Dual Data Pointer

The 8032 has two data pointers (DTPR, DTPR1). These two data pointers can help users enhance lots of block data memory moving. Using dual data pointers to move block data almost saves half of the time spent by original 8051 codes.

Watch Dog Timers Interrupt / Reset

The 8032 creates one programmable watchdog timers to monitor system failure. That is maximum 2^{26} .

Hardware Multiply

8032 includes a hardware multiplier to enhance calculating speed. 8032 can finish one multiply instruction at 1 machine cycle.

10.1.5 Memory Organization

In 8032, the memory is organized as three address spaces and the program counter. The memory spaces are shown in EC Memory Map.

- 16-bit Program Counter
- 64k-byte Program Memory address space
- 64k-byte External Data Memory address space
- 256-byte Internal Data Memory address

The 16-bit Program Counter register provides 8032 with its 64k addressing capabilities. The program Counter allows users to execute calls and branches to any location within the Program Memory space. There are no instructions that permit program execution to move from the Program Memory space to any of the data memory spaces.

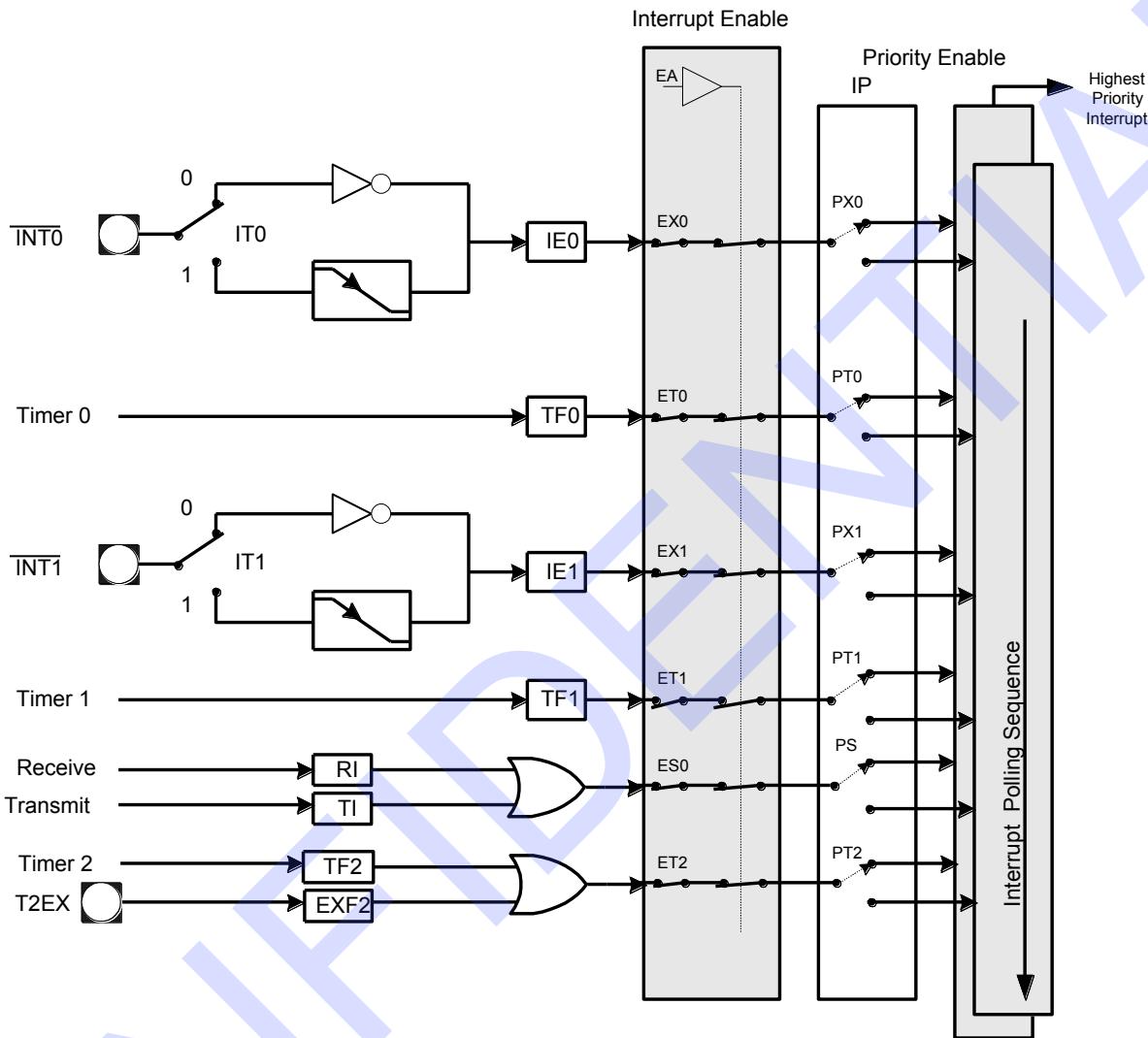
The 64k-byte Program Memory address space is located by dedicated address bus. The 64k-byte External Data Memory address space is automatically accessed when the MOVX instruction is executed. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address Space and a 128-byte Special Function Register address space as shown in the SFRs Map. The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit location ns of the on-chip RAM are accessible through Direct Addressing.

10.1.6 On-Chip Peripherals

Table 10-2. System Interrupt Table

Interrupt Source	Request Flag	Priority Flag	Enable Flag	Vector address	Priority-Within-Level	Flag Cleared by Hardw are?
External Request	IE0/TCON.1	PX0/IP.0	EX0/IE.0	0003h	1	Edge-Yes Level-No
Internal Timer0/Counter0	TF0/TCON.5	PT0/IP.1	ET0/IE.1	000Bh	2	Yes
External Request	IE1/TCON.3	PX1/IP.2	EX1/IE.2	0013h	3	Edge-Yes Level-No
Internal Timer1/Counter1	TF1/TCON.7	PT1/IP.3	ET1/IE.3	001Bh	4	Yes
Internal Serial Port	Tmit	TI/SCON.1	PS/IP.4	ES0/IE.4	5	No
	Rcvr	RI/SCON.0				
Internal Timer2/Counter2	TF2/T2CON.7	PT2/IP.5	ET2/IE.5	002Bh	6	No
	EXF2/T2CON.6					

Figure 10-1. Interrupt Control System Configuration



Note: T2EX is tied to logic high and is not available in IT8733.

External Interrupt

External Interrupt INT0# and INT1# input signal may each be programmed to be level-triggered or edge triggered depending upon bits IT0 and IT1 in the TCON register. If IT0 or IT1 = 0, INT0# or INT1# is triggered by detected low at the input signal. If IT0 or IT1 = 1, INT0# or INT1# is negative-edge triggered. External interrupts are enabled with bits EX0 and EX1 in the IE register. Events on the external interrupt input signals set the interrupt flags IE0 or IE1 in TCON. These request bits are cleared by hardware vectors to service routines only if the interrupt is negative-edge triggered. If the interrupt is level triggered, the interrupt service routine must clear the request bit. External hardware must release INT0# or INT1# before the service routine completes, or an additional interrupt is requested.

External interrupt input signals are sampled once every oscillator clock's rising edge. A level-triggered interrupt input signal held low or high for at least three clocks guarantees detection. Edge-triggered external interrupts only sample the request input signal for one clock time. This ensures edge recognition and sets interrupt request bit EX0 or

EX1. The 8032 clears EX0 or EX1 automatically during service routine fetch cycles for edge-triggered interrupts.

Timer Interrupts

Sources of timer 0, timer 1 and timer 2 are GPE5, TMR10 and TMR11 from pins. Three timer-interrupt request bits TF0, TF1 and TF2 are set by timer 0, timer 1 and timer 2 overflow. When timer 0 and timer 1 interrupts are generated, the bits TF0 and TF1 are cleared by an on-chip hardware vector to an interrupt service routine. Timer 2 is different from timer 0 or timer 1. Timer 2 has to clear TF2 bit by software writing when timer 2 interrupt is generated. Timer interrupts are enabled by bits ET0, ET1, and ET2 in the IE register.

Timer 2 interrupts are generated by a logical OR of bits TF2 and EXF2 in register T2CON. Neither flag is cleared by a hardware vector to a service routine. In fact, the interrupt service routine must determine if TF2 or EXF2 generates the interrupt, and then clear the bit. Timer 2 interrupt is enabled by ET2 in register IE.

Serial Port Interrupt

Serial port interrupts are generated by the logical OR of bits RI and TI in the SCON register. Neither flag is cleared by a hardware vector to the service routine. The service routine resolves RI and TI interrupt generation and clears the serial port request flag. The serial port interrupt is enabled by bit ES0 in the IE register in the same way by using serial port 1.

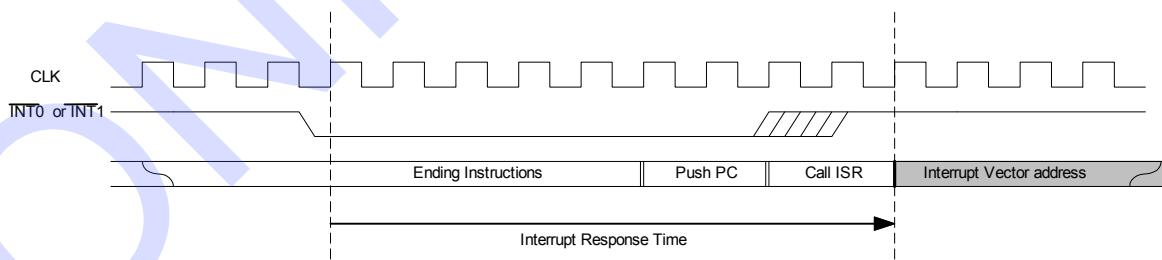
Interrupt Priority

8032 has 2 level priorities. Setting / clearing a bit in the Interrupt Priority register (IP) establish its associated interrupt request as a high / low priority. If a low-priority level interrupt is being serviced, a high-priority level interrupt will interrupt it. However, an interrupt source cannot interrupt a service program of the same or higher level. The interrupt priority is shown on Interrupt Control System Configuration.

Interrupt Response Time

The Figure of Interrupt Response Time shows the response time is between the interrupt request being active and the interrupt service routing being executed. The minimum interrupt response time is eight clocks that when an interrupt request asserts after the ending instruction execution completes. The maximum interrupt response time is 24 clocks when an interrupt request asserts during the ending instruction, DJNZ direct, rel or other instruction sets whose operation period is 16 clocks and is decoded ok. However, a high priority interrupt asserts while a low priority interrupt service program is executing. The minimum and the maximum interrupt response time is 8 clocks and 24 clocks respectively.

Figure 10-2. Interrupt Response Time



10.1.7 Timer / Counter

Timer 0

Timer 0 functions as either a timer or event counter in four modes of operation. Timer 0 is controlled by the four low-order bits of the TMOD register and bits 5, 4, 1 and 0 of the TCON register. The TMOD register selects the method of timer gating (GATE), timer or counter operation (C/T), and mode of operation (M1, M0). The TCON register provides timer 0 control functions: overflow (TF0), run control (TR0), interrupt flag (IE0), and interrupt type control (IT0). For normal timer operation (GATE = 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE and TR0 allows INT0# to control timer operation.

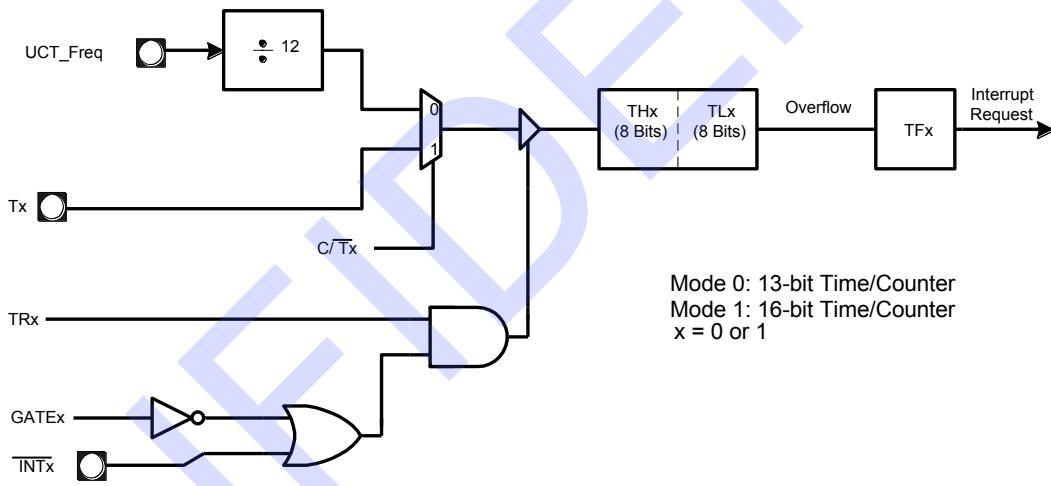
Timer0/Mode 0 (13-bit Timer)

Mode 0 configures timer 0 as a 13-bit timer which is set up as an 8-bit timer (TH0 register) with a module 32 prescaler implemented with the lower five bits of the TL0 register. The upper three bits of TL0 register are indeterminate and should be ignored. Prescaler overflow increments the TH0 register.

Timer 0/ Mode 1 (16-bit Timer)

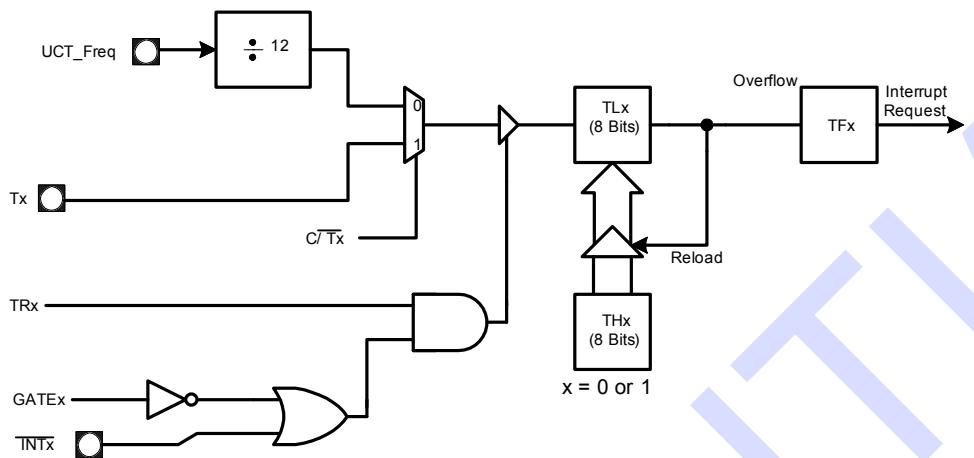
Mode 1 configures timer 0 as a 16-bit timer with TH0 and TL0 connected in cascade. The selected input increases TL0.

Figure 10-3. Timer 0/1 in Mode 0 and Mode 1



Timer 0/ Mode 2 (8-bit Timer With Auto-reload)

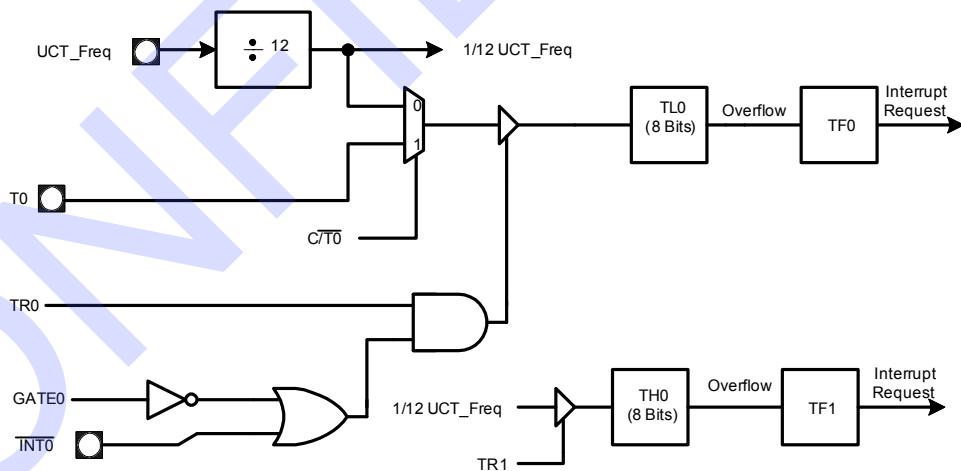
Mode 2 configures timer 0 as an 8-bit timer (TL0 register) that automatically reloads from the TH0 register. TL0 overflow sets the timer overflow flag (TF0) in the TCON register and reloads TL0 with the contents of TH0, which is preset by software. When the interrupt request is serviced, hardware clears TF0. The reload leaves TH0 unchanged.

Figure 10-4. Timer 0/1 in Mode 2, Auto-Reload


Timer 0/ Mode 3(Two 8-bit Timers)

Mode 3 configures timer 0 such that registers TL0 and TH0 operate as separate 8-bit timers. This mode is provided for application requiring an additional 8-bit timer or counter. TL0 uses the timer 0 control bits C/T and GATE in TMOD, and TR0 in TCON in the normal manner. TH0 is locked into a timer function (counting UCT_Freq/12) and takes over use of the timer 1 interrupt (TF1) and run control (TR1) bits. Thus, operation of timer 1 is restricted when timer 0 is in mode 3.

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 12-1. Clock Timing Parameter on page 355).

Figure 10-5. Timer 0 in Mode 3 Two 8-bit Timers


Timer 1

Timer 1 functions as either a timer or event counter in three modes of operation. The logical configuration for modes 0, 1 and 2 is the same as that of Timer 0. Mode 3 of timer 1 is a hold-count mode.

Timer 1 is controlled by the four high-order bits of the TMOD register and bits 7, 6, 3 and 2 of the TCON register. The TMOD register selects the method of timer gating (GATE), timer or counter operation (C/ T), and mode of

operation (M1 and M0). The TCON register provides timer 1 control functions: overflow flag (TF1), run control (TR1), interrupt flag(IE1), and interrupt type control (IT1).

For normal timer operation (GATE = 0), setting TR1 allows timer register TL1 to be incremented by the selected input. Setting GATE and TR1 allows external input signal INT1# to control timer operation. This setup can be used to make pulse width measurements.

Timer 1/ Mode 0 (13-bit Timer)

Mode 0 configures timer 0 as a 13-bit timer, which is set up as an 8-bit timer (TH1 register) with a modulo-32 prescaler implemented with the lower 5 bits of the TL1 register. The upper 3 bits of the TL1 register are ignored. Prescaler overflow increase the TH1 register.

Timer1/ Mode 1 (16-bit Timer)

Mode 1 configures timer 1 as a 16-bit timer with TH1 and TL1 connected in cascade. The selected input increases TL1.

Timer 1/ Mode 2 (8-bit Timer)

Mode 2 configures timer 1 as an 8-bit timer (TL1 register) with automatic reload from the TH1 register on overflow. Overflow from TL1 sets overflow flag TF1 in the TCON register and reloads TL1 with the contents of TH1, which is preprogrammed by software. The reload leaves TH1 unchanged.

Timer 1/ Mode 3 (Halt)

Placing timer in mode 3 causes it to halt and its count. This can be used to halt timer 1 when the TR1 run control bit is not available, i.e., when timer 0 is in mode 3.

Timer 2

Timer 2 is a 16-bit timer/count maintained by two eight-bit timer registers, TH2 and TL2, which are connected in cascade. The timer/counter 2 mode control register T2MOD and the timer /counter control register T2CON control the operation of timer 2.

Timer 2 provides the following operating modes: capture mode, auto-reload mode, baud rate generator mode, and programmable clock-out mode. Select the operating mode with T2MOD and TCON register bits as shown in table of Timer 2 Modes of Operation. Auto-reload is the default mode. Setting RCLK and/or TCLK selects the baud rate generator mode.

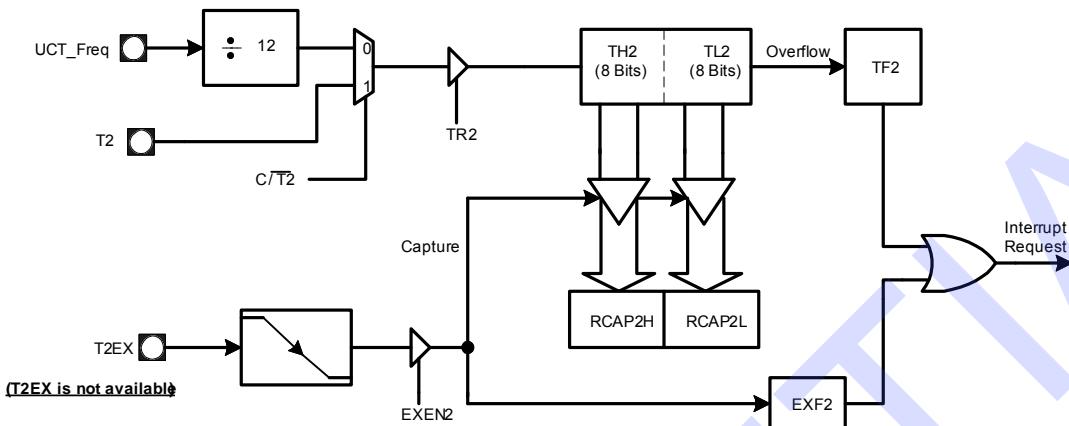
Timer 2 operation is similar to timer 0 and timer 1. C/2 T selects UCT_Freq/12 (timer operation) or external input signal T2 (counter operation) as the timer register input. Setting TF2 to be incremented by the selected input.

Timer 2/ Capture Mode

In the capture mode, timer 2 functions as a 16-bit timer or counter. An overflow condition sets bit TF2, which you can use to request an interrupt. Setting the external enable bit EXEN2 allows the RCAP2H and RCAP2L registers to capture the current value in timer registers TH2 and TL2 in response to a I-to-0 transition at external input T2EX. The transition at T2EX also sets bit EXF2 on T2CON. The EXF2 bit, like TF2, can generate an interrupt. TR2 has to be enabled when this mode is run.

Note: T2EX is tied to logic high and is not available in IT8733.

Figure 10-6. Timer 2: Capture Mode



Note: T2EX is tied to logic high and is not available in IT8733.

Timer 2/ Auto-reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. The timer operates as an up counter or up/down counter, as determined by the down counter enable bit (DCEN). At device reset, DCEN is cleared, so in the auto-reload mode, timer 2 defaults to operation as an up counter. TR2 has to be enabled when this mode is run.

Up Counter Operation

When DCEN = 0, timer 2 operates as an up counter. If EXEN2 = 0, timer 2 counts up to FFFFh and sets the TF2 overflow flag. The overflow condition loads the 16-bit value in the reload/capture registers (RCAP2H, RCAP2L) into the timer registers (TH2, TL2). The values in RCAP2H and RCAP2L are preset by software.

If EXEN2 = 1, the timer registers are reloaded by either a timer overflow or a high-to-low transition at external input T2EX. This transition also sets the EXF2 bit in the T2CON register. Either TF2 or EXF2 bit can generate a timer 2 interrupt request. TR2 has to be enabled when its mode is run.

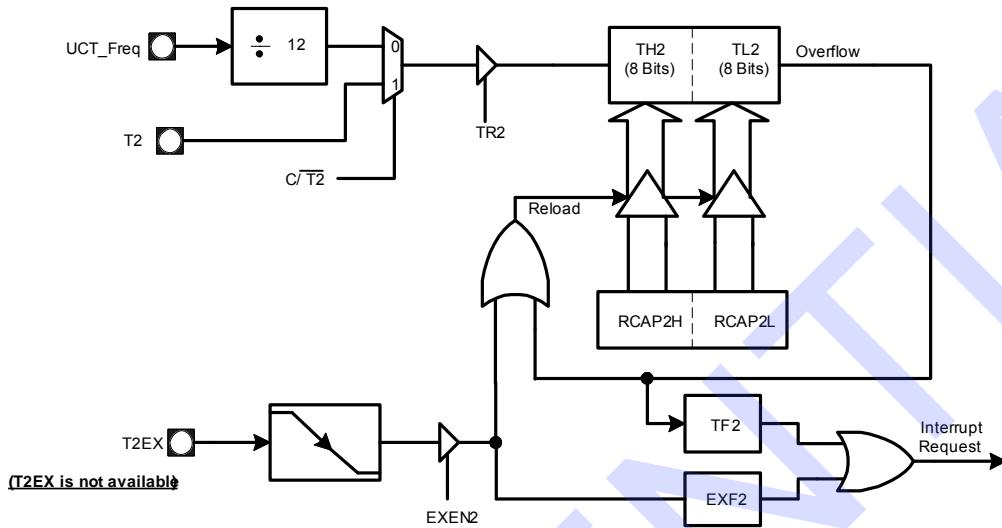
Up/Down Counter Operation

When DCEN = 1, timer 2 operates as an up/down counter. External input signal T2EX controls the direction of the count. When T2EX is high, timer 2 counts up. The timer overflow occurs at FFFFh, which sets the timer 2 overflow flag (TF2) and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers (TH2, TL2) equals the value stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and reloads FFFFh into the timer registers.

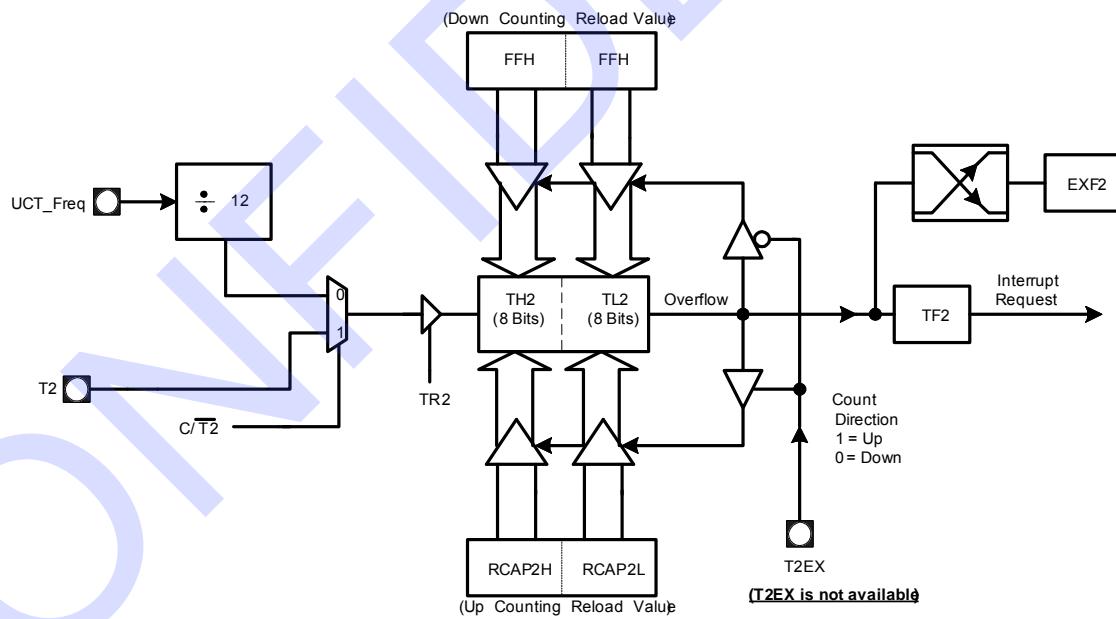
The EXF2 bit toggles when timer 2 overflows or underflows changing the direction of the count. When timer 2 operates as an up/down counter, EXF2 does not generate an interrupt. This bit can be used to provide 17-bit resolution. TR2 has to be enabled when his mode is run.

Figure 10-7. Timer 2: Auto Reload (DCEN = 0)



Note: T2EX is tied to logic high and is not available in IT8733.

Figure 10-8. Timer 2: Auto Reload Mode (DCEN = 1)



Note: T2EX is tied to logic high and is not available in IT8733.

Timer 2/ Baud Rate Generator Mode

This mode configures timer 2 as a baud rate generator for use with the serial port. Select this mode by setting the RCLK and/or TCLK bits in T2CON.

Timer 2/ Clock-out Mode

In the clock-out mode, timer 2 functions as a 50%-duty-cycle, variable-frequency clock. The input clock increments TL0 at frequency UCT_Freq/2. The timer repeatedly counts to overflow from a preloaded value. At overflow, the contents of the RCAP2H and RCAP2L registers are loaded into TH2/TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

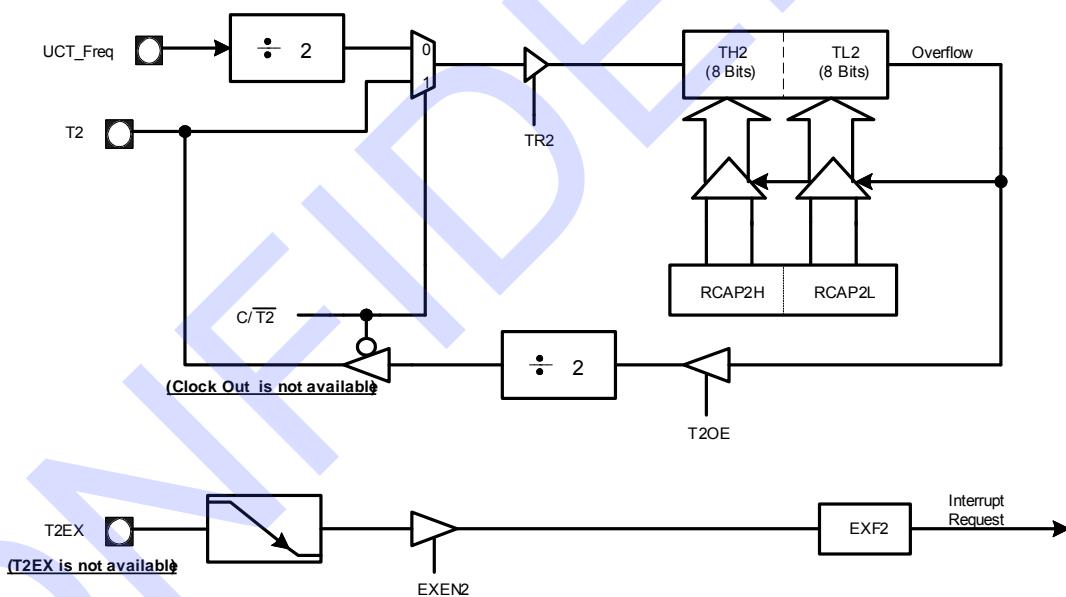
$$\text{Clock-out Frequency} = \text{UCT_Freq} / \{4 \times (65536 - \text{RCAP2H}, \text{RCAP2L})\}$$

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 12-1. Clock Timing Parameter on page 355).

Table 10-3. Timer 2 Modes of Operation

Mode	RCLK OR TCLK (in T2CON)	Cp/rI2# (in T2CON)	T2OE (in T2MOD)
Auto-reload Mode	0	0	0
Capture Mode	0	1	0
Baud Rate Generator Mode	1	X	X
Programmable Clock-Out	X	0	1

Figure 10-9. Timer 2: Clock Out Mode

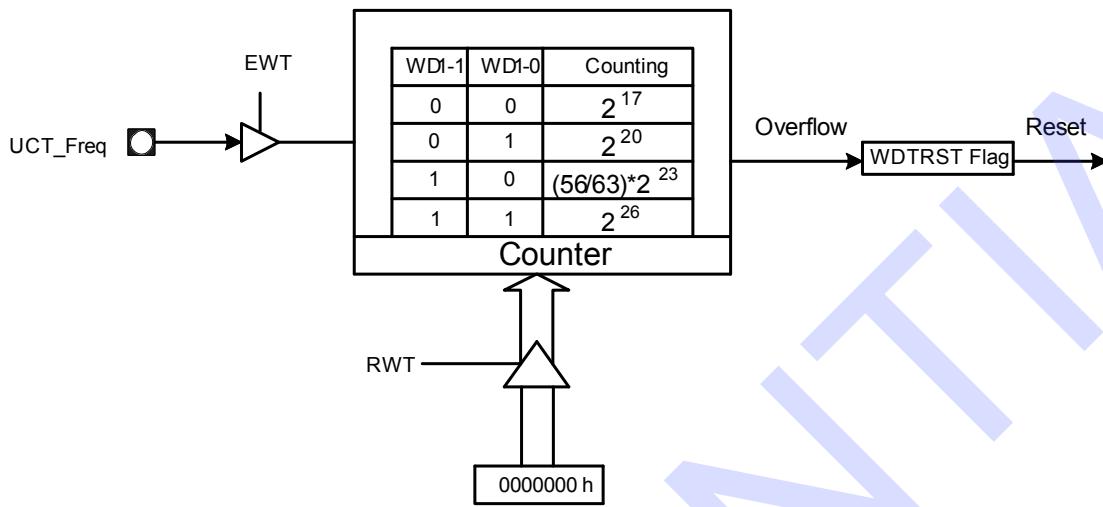


Note: T2EX is tied to logic high and is not available in IT8733.

Watchdog Timer

The watchdog timer has system reset functions. Users can set WD1-1, WD1-0 (in register CKCON, 8Eh) to choose 2^17, 2^20, (56/63)*2^23 or 2^26 counter for Watchdog Timer. After the Watchdog Timer counts the specific counter and an overflow occurs, set WDTRST Flag (in register WDTCON, D8h) and finally reset the 8032. If 8032 has been reset by Watchdog Timer, WDTEN Flag remains one.

Figure 10-10. Watchdog Timer



SERIAL I/O PORT

The serial I/O port provides both asynchronous communication modes. It operates as a universal asynchronous receiver and transmitter (UART) in three full-duplex modes (modes 1, 2, and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates.

Mode 1 and 3 operate over a wide range of baud rates, which are generated by timer 1 and timer 2.

The serial port signals are defined in Table of Serial Port Signals, and the serial port special function registers (SBUF, SCON) are described in the section of Special Function Registers.

For the three asynchronous modes, the UART transmits on the TxD pin and receives on the RxD pin. The SBUF register, which holds received bytes and bytes to be transmitted, actually consists of two physically different registers. To send, software writes a byte to SBUF; to receive, software reads SBUF. The receive shift register allows reception of a second byte before the byte has been read from SBUF. However, if software has not read the first byte by the time the second byte is received, the second byte will overwrite the first. The UART sets interrupt bits TI and RI on transmission and reception respectively. These two bits share a single interrupt request and interrupt vector.

Figure 10-11. Serial Port Block Diagram

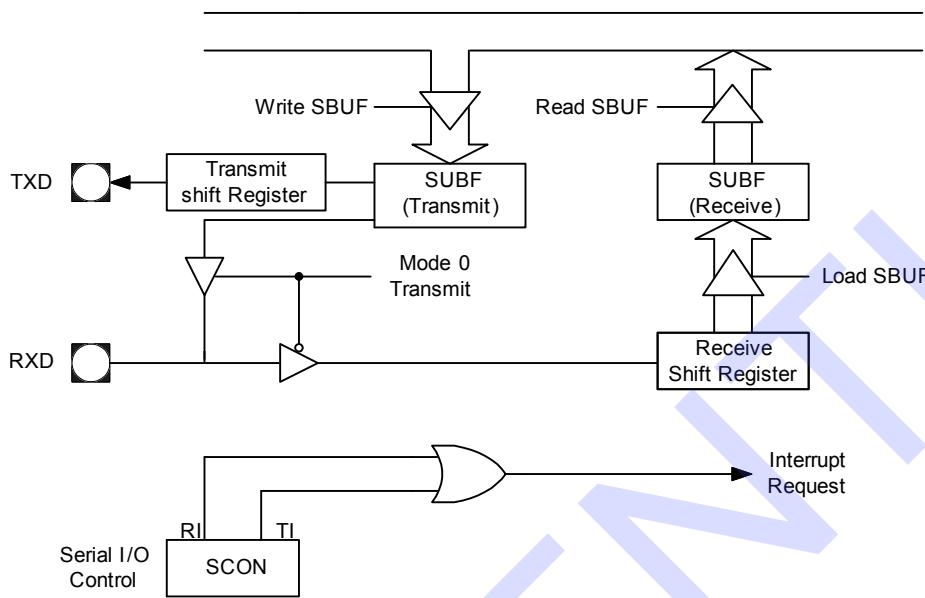


Table 10-4. Serial Port Signals

Function Name	Type	Description	Multiplexed With
TXD	O	Transmit Data. In modes 1, 2 and 3, TXD transmits serial data.	P3.1
RXD	I	Receive Data. In mode 1, 2 and 3, RXD receives serial data.	P3.0

(Mode 0 is not available)

Asynchronous Modes (Modes 1, 2, and 3)

The serial port has three asynchronous modes of operation.

Mode 1

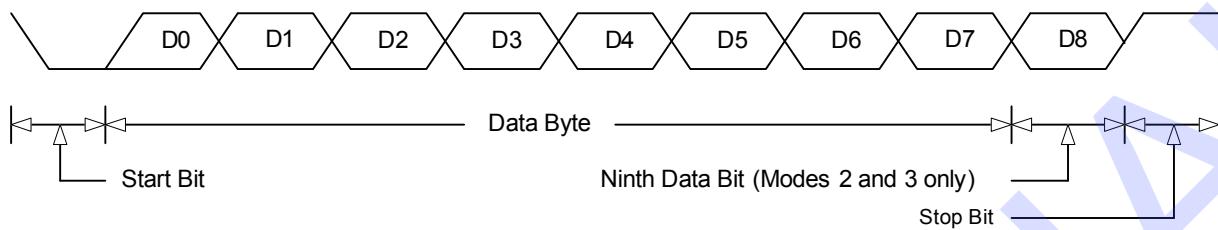
Mode 1 is a full-duplex and asynchronous mode. The data frame consists of 10 bits: one start bit, eight data bits, and one stop bit. Serial data is transmitted on the TXD pin and received on the RXD pin. When a message is received, the stop bit is read in the RB8 bit in the SCON register. The baud rate is generated by overflow of timer 1 or timer 2.

Mode 2 and 3

Mode 2 and 3 are full-duplex and asynchronous modes. The data frame consists of 11 bits: one start bit, eight data bits (transmitted and received LSB first), one programmable ninth data bit, and one stop bit which is read from the RB8 bit in the SCON register. On transmit, the ninth data bit is written to the TB8 bit in the SCON register. Alternatively, you can use the ninth bit as a command/data flag.

- In mode 2, the baud rate is programmable to 1/32 or 1/64 of the oscillator frequency.
- In mode 3, the baud rate is generated by overflow of timer 1 or timer 2.

Figure 10-12. Data Frame (Mode 1, 2 and 3)



Transmission (Mode 1, 2, 3)

Follow these steps below to initiate a transmission:

1. Write to the SCON register. Select the mode with the SM0 and SM1 bits, and clear the REN bit.
For mode 2 and 3, write the ninth bit to the TB8 bit.
2. Write the byte to be transmitted to the SBUF register. This write starts the transmission.

Reception (Mode 1, 2, 3)

To prepare for a reception, set the REN bit in the SCON register. The actual reception is then initiated by a detected high-to-low transition on the RXD pin.

Baud Rates

Baud Rates for Mode 2

Mode 2 has a two-baud rate, which is selected by the SMOD1 bit in the PCON register. The following expression defines the baud rate:

$$\text{Serial I/O Mode 2 Baud Rate} = (2^{\text{SMOD1}}) \times (\text{UCT_Freq} / 64)$$

UCT_Freq equals to EC Clock Frequency (listed in Table 12-1. Clock Timing Parameter on page 355).

Baud Rates for Mode 1 and 3

In mode 1 and 3, the baud rate is generated by overflow of timer (default) and/or timer 2. You may select either or both timers to generate the baud rate(s) for the transmitter and/or the receiver.

Timer 1 Generated Baud Rates (Mode 1 and 3)

Timer 1 is the default baud rate generator for the transmitter and the receiver in mode 1 and 3. The baud rate is determined by the timer 1 overflow rate and the value of SMOD1, as shown in the following formula:

$$\text{Serial I/O Mode 1 and 3 Baud Rate} = (2^{\text{SMOD1}}) \times (\text{Timer 1 Overflow Rate}) / 32$$

Selecting Timer 1 as the Baud Rate Generator

To select timer 1 as the baud rate generator:

- Disable the timer interrupt by clearing the IE0 register.
- Configure timer 1 as a timer or an event counter (set or clear the C/T bit in the TMOD register).
$$\text{Serial I/O Mode 1 and 3 Baud Rate} = (2^{\text{SMOD1}}) \times \text{UCT_Freq} / (32 \times 12 \times (256 - \text{TH1}))$$

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 12-1. Clock Timing Parameter on page 355).

- Select timer mode 0-3 by programming the M1 and M0 bits in the TMOD register.

In most applications, timer 1 is configured as a timer in auto-reload mode (high nibble of TMOD = 0010B). The resulting baud rate is defined by the following expression:

Timer 1 can generate very low baud rates by the following setups:

- Enable the timer 1 interrupt by setting the ET1 bit in the IE register.
- Configure timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B).

- Use the timer 1 interrupt to initiate a 16-bit software reload.

Timer 2 Generated Baud Rates (Mode 1 and 3)

Timer 2 may be selected as the baud rate generator for the transmitter and/or receiver. The baud rate generator mode of timer 2 is similar to the auto-reload mode. A rollover in the TH2 register reloads registers TH2 and TL2 with the 16-bit value on registers RCAP2H and RCAP2L, which are presented by software.

The baud rate of timer 2 is expressed by the following formula:

$$\text{Serial I/O Mode 1 and 3 Baud Rate} = (\text{Timer 2 Overflow Rate}) / 16$$

Selecting Timer 2 as the Baud Rate Generator

To select timer 2 as the baud rate generator for the transmitter and/or receiver, program the RCLK and TCLK bits in the T2CON register. Setting RCLK and/or TCLK puts timer 2 into its baud rate generator mode. In this mode, a rollover in the TH2 register does not set the TF2 bit in the T2CON register. Besides, a high-to-low transition at the T2EX input signal sets the EXF2 bit in the T2CON register but does not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). You can use the T2EX input signal as an additional external interrupt by setting the EXEN2 bit in T2CON.

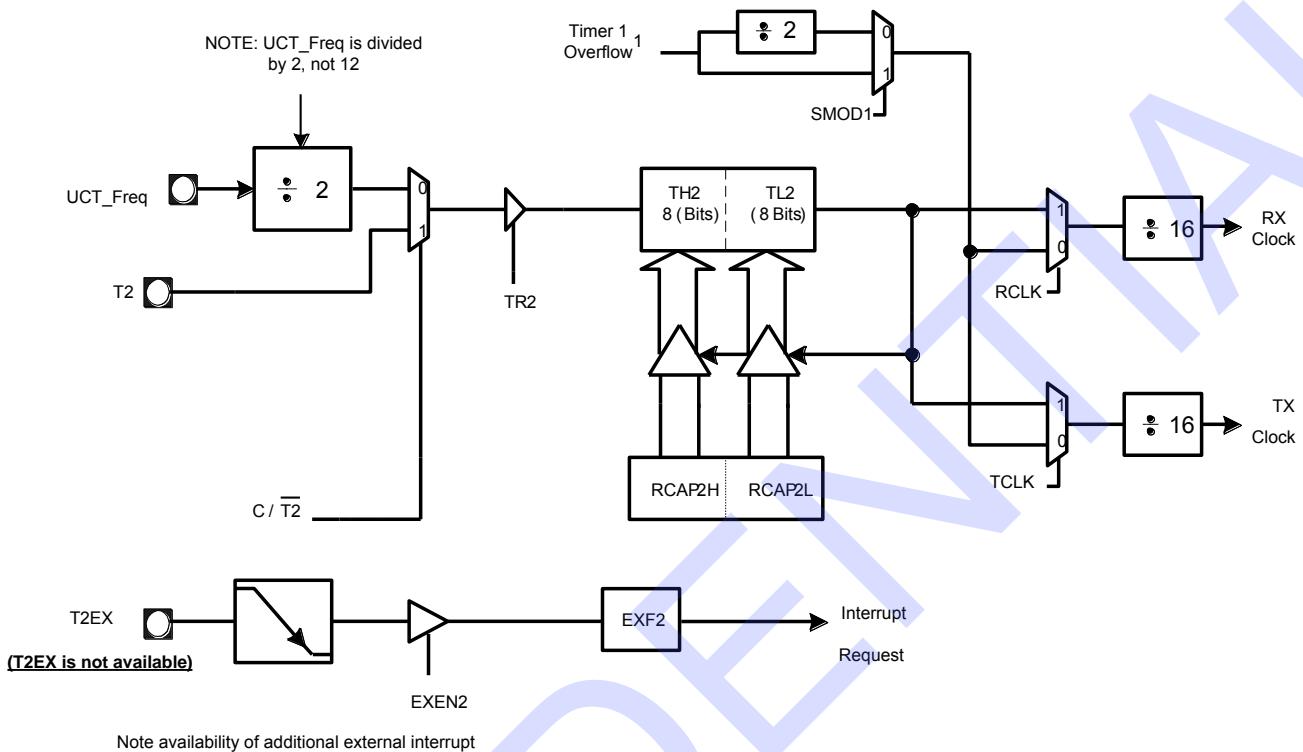
Note: T2EX is tied to logic high and is not available in IT8733.

Note: Turn off the timer (clear the TR2 bit in the T2CON register) before accessing registers TH2, TL2, RCAP2H and RCAP2L. You may configure timer 2 as a timer or a counter. In most applications, it is configured for timer operation (i.e., the C/T2 bit is cleared in the T2CON register).

Table 10-5. Selecting the Baud Rate Generator(s)

PCLK Bit	TCLK Bit	Receiver Baud Rate Generator	Transmitter Baud Rate Generator
0	0	Timer1	Timer1
0	1	Timer1	Timer2
1	0	Timer2	Timer1
1	1	Timer2	Timer2

Figure 10-13. Timer 2 in Baud Rate Generator Mode



Note: T2EX is tied to logic high and is not available in IT8733.

Note that timer 2 increments every state time (2Tosc) when it is in the baud rate generator mode. In the baud rate formula that follows, “RCAP2H, RCAP2L” denoting the contents of RCAP2H and RCAP2L is taken as a 16-bit unsigned integer:

$$\text{Serial I/O Mode 1 and 3 Baud Rate} = \text{UCT_Freq} / (32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})])$$

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 12-1. Clock Timing Parameter on page 355).

When timer 2 is configured as a timer and is in baud rate generator mode, do not read or write the TH2 or TL2 registers. The timer is being incremented every state time, and the result of a read or write may not be accurate. In addition, you may read but not write to the RCAP2H/RCAP2L registers; a write may overlap a reload and cause write and/or reload errors.

10.1.8 Idle and Doze/Sleep Mode

Idle Mode

When set IDL bit in PCON(87h), the 8032 will enter an Idle mode. In the Idle mode, the 8032 is idle while all the on-chip peripherals remain active. The internal RAM and SFRs registers remain unchanged during this mode. The Idle mode can be terminated by any enabled internal/external interrupt or by a hardware reset.

Doze/Sleep Mode

When PD bit is set in PCON(87h), the 8032 will enter a Doze/Sleep mode. In the Doze/Sleep mode, the 8032 clock is stopped, and PLL may be alive or stopped depending on PLLCTRL. The Doze/Sleep mode can be waked up by the hardware reset or by the external enabled interrupt with level trigger activation (ITx in register TCON is

set to 0). The Program Counter, internal RAM and SFRs registers retain their values and will not be changed after the exiting Doze/Sleep mode by external interrupt. The reset will restart the 8032, while the SFRs with initial values and the internal RAM retain their values.

10.1.9 EC Internal Register Description

The embedded 8032 internal memory space and special function registers (F0h-80h) are listed below.

Table 10-6. Internal RAM Map

Index	07h-00h	0Fh-08h	17h-10h	1Fh-18h	2Fh-20h	7Fh-2Fh	FFh-80h
7	Bank 0						
	Bank 1						
	Bank 2						
	Bank 3						
	Addressable Bits						
	General Purpose RAM						
0	Indirect Addressing Register						

SFR Index	80h	88h	90h	98h	A0h	A8h	B0h	B8h	C0h	C8h	D0h	D8h	E0h	E8h	F0h	F8h
PCON	DPS	DPH1	DPL1	DPH	DPL	SP	P0									
	CKCON	TH1	TH0	TL1	TL0	TMOD	TCON									
							P1									
							SBUF	SCON								
									P2							
									IE							
									P3							
									IP							
		STATUS														
		TH2	TL2	RCAP2H	RCAP2L	T2MOD	T2CON									
							PSW									
								WDTCON								
									ACC							
	MPREFC														B	

10.1.9.1 Port 0 Register (P0R)

Address: 80h

Bit	R/W	Default	Description
7-0	R/W	FFh	P0 Register Bit [7:0] (P0) This is the 8-bit 8032 port 0.

10.1.9.2 Stack Pointer Register (SPR)

Address: 81h

Bit	R/W	Default	Description
7-0	R/W	07h	Stack Pointer Bit [7:0] (SP) This is the 8-bit stack pointer.

10.1.9.3 Data Pointer Low Register (DPLR)

Address: 82h

Bit	R/W	Default	Description
7-0	R/W	00h	Data Pointer Low Bit [7:0] (DPL) This is the 8-bit data pointer low byte.

10.1.9.4 Data Pointer High Register (DPHR)

Address: 83h

Bit	R/W	Default	Description
7-0	R/W	00h	Data Pointer High Bit [7:0] (DPH) This is the 8-bit data pointer high byte.

10.1.9.5 Data Pointer 1 Low Register (DP1LR)

Address: 84h

Bit	R/W	Default	Description
7-0	R/W	00h	Data Pointer 1 Low Bit [7:0] (DPL1) This is the 8-bit data pointer 1 low byte.

10.1.9.6 Data Pointer 1 High Register (DP1HR)

Address: 85h

Bit	R/W	Default	Description
7-0	R/W	00h	Data Pointer 1 High Bit [7:0] (DPH1) This is the 8-bit data pointer 1 high byte.

10.1.9.7 Data Pointer Select Register (DPSR)

Address: 86h

Bit	R/W	Default	Description
7-1	-	00h	Reserved
0	R/W	0b	Data Pointer Select (DPS) Setting '1' selects the data pointer 1 (DPL1, DPH1) while setting '0' selects the data pointer (DPL, DPH).

10.1.9.8 Power Control Register (PCON)

Address: 87h

Bit	R/W	Default	Description
7	R/W	0b	Serial Port Double Baud Rate (SMOD1) Setting '1' doubles the baud rate when timer 1 is used and mode 1, 2, or 3 is selected in SCON register.
6	-	0b	Reserved
5-2	-	0h	Reserved
1	R/W	0b	Power Down Mode (PD) Set "1" to enter a Sleep (a.k.a. power-down) or Doze mode immediately. The Sleep or Doze mode is controlled by PPDC bit. Exit Sleep or Doze mode and clear this bit by external interrupt or hardware reset.
0	R/W	0b	Idle Mode (IDL) Set "1" to enter idle mode immediately. Exit idle mode and clear this bit by internal interrupt and external interrupt or hardware reset.

10.1.9.9 Timer Control Register (TCON)

Address: 88h

Bit	R/W	Default	Description
7	R/W	0b	Timer 1 Overflow (TF1) This bit is set by hardware when timer 1 register overflows. This bit is cleared by hardware when the processor vectors to the interrupt service routine.
6	R/W	0b	Timer 1 Run Control (TR1) Setting '1' enables timer 1 operation and setting '0' disables timer 1.
5	R/W	0b	Timer 0 Overflow (TF0) This bit is set by hardware when timer 0 register overflows. This bit is cleared by hardware when the processor vectors to the interrupt service routine.
4	R/W	0b	Timer 0 Run Control (TR0) Setting '1' enables timer 0 operation and setting '0' disables the timer 0.
3	R/W	0b	Interrupt 1 Edge Detect (IE1) This bit is set by hardware when an edge or a level is detected on external INT1 (depends on the setting of IT1). This bit is cleared by hardware when the interrupt service routine is processed if an edge trigger is selected.
2	R/W	0b	Interrupt 1 Type Select (IT1) Setting '1' selects the edge-triggered for INT1. Setting '0' selects a level-triggered. Don't write 1 to this bit because interrupt triggered type is considered in INTC module and needs IT0 and IT1 to be set as level-low triggered.
1	R/W	0b	Interrupt 0 Edge Detect (IE0) Set by hardware when an edge or a level is detected on external INT0 (depends on the setting of IT0). Cleared by hardware when the interrupt service routine is processed if an edge trigger is selected.

Bit	R/W	Default	Description
0	R/W	0b	Interrupt 0 Type Select (IT0) Setting '1' selects the edge-triggered for INT0. Setting '0' selects a level-triggered. Don't write 1 to this bit because interrupt triggered type is considered in INTC module and needs IT0 and IT1 to be set as level-low triggered.

10.1.9.10 Timer Mode Register (TMOD)

Address: 89h

Bit	R/W	Default	Description
7	R/W	0b	Timer 1 Gate (GATE1) 0: Timer 1 will clock when TR1=1, regardless of the state of INT1. 1: Timer 1 will clock only when TR1=1 and INT1 is deasserted.
6	R/W	0b	Timer 1 Source (C/T1#) 0: timer 1 counts the divided-down EC clock. 1: timer 1 counts negative transitions on T1 input of 8032 from TMRI0 pin.
5-4	R/W	0b	Timer 1 Mode (MODE1) 0h: 8-bit timer/counter (TH1) with 5-bit prescaler (TL1) 1h: 16-bit timer/counter 2h: 8-bit auto-reload timer/counter (TL1). Reload from TH1 at overflow. 3h: timer 1 halted. Retains count.
3	R/W	0b	Timer 0 Gate (GATE0) 0: Timer 0 will clock when TR0=1, regardless of the state of INT0. 1: Timer 0 will clock only when TR0=1 and INT0 is deasserted.
2	R/W	0b	Timer 0 Source (C/T0#) 0: timer 0 counts the divided-down EC clock. 1: timer 0 counts negative transitions on T0 input of 8032 from GPE5.
1-0	R/W	0b	Timer 0 Mode (MODE0) 0h: 8-bit timer/counter (TH0) with 5-bit prescaler (TL0) 1h: 16-bit timer/counter 2h: 8-bit auto-reload timer/counter (TL0). Reload from TH0 at overflow. 3h: timer 0 halted. Retains count.

10.1.9.11 Timer 0 Low Byte Register (TL0R)

Address: 8Ah

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 0 Low Byte Bit [7:0] (TL0) Timer 0 low byte register.

10.1.9.12 Timer 1 Low Byte Register (TL1R)

Address: 8Bh

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 1 Low Byte Bit [7:0] (TL1) Timer 1 low byte register.

10.1.9.13 Timer 0 High Byte Register (TH0R)

Address: 8Ch

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 0 High Byte Bit [7:0] (TH0) Timer 0 high byte register.

10.1.9.14 Timer 1 Low Byte Register (TH1R)

Address: 8Dh

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 1 High Byte Bit [7:0] (TH1) Timer 1 high byte register.

10.1.9.15 Clock Control Register (CKCON)

Address: 8Eh

Bit	R/W	Default	Description
7-6	R/W	00b	Watch Dog Time Out Counter Select (WD[1:0]) 0h: 17-bit counter 1h: 20-bit counter 2h: (56/63)*2 ²³ counter 3h: 26-bit counter
5	R/W	0b	Timer 2 Clock (T2M) 0: timer 2 clock is EC clock / 12. 1: timer 2 clock is EC clock / 4.
4	R/W	0b	Timer 1 Clock (T1M) 0: timer 1 clock is EC clock / 12. 1: timer 1 clock is EC clock / 4.
3	R/W	0b	Timer 0 Clock (T0M) 0: timer 0 clock is EC clock / 12. 1: timer 0 clock is EC clock / 4.
2	R/W	0b	Timer 1 Clock II (T1M2) 0: Timer 1 clock depends on T1M bit in this register. 1: Timer 1 clock is EC clock / 5.
1-0	-	-	Reserved

10.1.9.16 Port 1 Register (P1R)

Address: 90h

Bit	R/W	Default	Description
7-0	R/W	FFh	P1 Register Bit [7:0] (P1) This is the 8-bit 8032 port 1.

10.1.9.17 Serial Port Control Register (SCON)

Address: 98h

Bit	R/W	Default	Description
7	R/W	0b	Serial Port Mode 0 (SM0) Serial port mode control is set/cleared by software. Mode 1-3 are supported.
6	R/W	0b	Serial Port Mode 1 (SM1) Serial port mode control is set/cleared by software. Mode 1-3 are supported.
5	-	0b	Reserved
4	R/W	0b	Receive Enable (REN) Receiver enable bit. Setting '1' enables the serial data reception. Setting '0' disables the serial data reception.
3	R/W	0b	Transmit Bit 8 (TB8) Transmit bit 8, set/cleared by hardware to determine the state of the ninth data bit transmitted in 9-bit UART mode.
2	R/W	0b	Receive Bit 8 (RB8) Receive bit 8, set/cleared by hardware to determine the state of the ninth data bit received in 9-bit UART mode.
1	R/W	0b	Transmit Interrupt (TI) Transmit interrupt, set by hardware when the byte is transmitted and cleared by software after serving.
0	R/W	0b	Receive Interrupt (RI) Receive interrupt, set by hardware when the byte is received and cleared by software when data is processed.

10.1.9.18 Serial Port Buffer Register (SBUFR)

Address: 99h

Bit	R/W	Default	Description
7-0	R/W	00h	Serial Port Buffer Bit [7:0] (SBUF) This is the 8-bit 8032 serial port data buffer. Writing to SBUF loads the transmit buffer to the serial I/O port. Reading SBUF reads the receive buffer of the serial port.

10.1.9.19 Port 2 Register (P2R)

Address: A0h

Bit	R/W	Default	Description
7-0	R/W	FFh	P2 Register Bit [7:0] (P2) This is the 8-bit 8032 port 2.

10.1.9.20 Interrupt Enable Register (IE)

Address: A8h

Bit	R/W	Default	Description
7	R/W	0b	Global Interrupt Enable (EA) Setting this bit enables all interrupts that are individually enabled by bit 0-6. Clearing this bit disables all interrupts.
6	R/W	0b	Serial Port 1 Interrupt Enable (ES1) Setting this bit enables the serial port 1 interrupt.
5	R/W	0b	Timer 2 Overflow Interrupt Enable (ET2) Setting this bit enables the timer 2 overflow interrupt.
4	R/W	0b	Serial Port 0 Interrupt Enable (ES0) Setting this bit enables the serial port 0 interrupt.
3	R/W	0b	Timer 1 Overflow Interrupt Enable (ET1) Setting this bit enables the timer 1 overflow interrupt.
2	R/W	0b	External Interrupt 1 Enable (EX1) Setting this bit enables the external interrupt 1.
1	R/W	0b	Timer01 Overflow Interrupt Enable (ET0) Setting this bit enables the timer 0 overflow interrupt.
0	R/W	0b	External Interrupt 0 Enable (EX0) Setting this bit enables the external interrupt 0.

10.1.9.21 Port 3 Register (P3R)

Address: B0h

Bit	R/W	Default	Description
7-0	R/W	FFh	P3 Register Bit [7:0] (P3) This is the 8-bit 8032 port 3.

10.1.9.22 Interrupt Priority Register (IP)

Address: B8h

Bit	R/W	Default	Description
7	-	0b	Reserved
6	-	-	Reserved
5	R/W	0b	Timer 2 Overflow Interrupt Priority (PT2) Setting this bit enables the timer 2 overflow interrupt.
4	R/W	0b	Serial Port 0 Interrupt Priority (PS0) Setting this bit enables the serial port 0 interrupt.
3	R/W	0b	Timer 1 Overflow Interrupt Priority (PT1) Setting this bit enables the timer 1 overflow interrupt.
2	R/W	0b	External Interrupt 1 Priority (PX1) Setting this bit enables the external interrupt 1.
1	R/W	0b	Timer01 Overflow Interrupt Priority (PT0) Setting this bit enables the timer 0 overflow interrupt.
0	R/W	0b	External Interrupt 0 Priority (PX0) Setting this bit enables the external interrupt 0.

10.1.9.23 Status Register (STATUS)

Address: C5h

Bit	R/W	Default	Description
7	-	-	Reserved
6	R/W	0b	High priority interrupt status (HIP)
5	R/W	0b	Low priority interrupt status (LIP)
4-2	-	-	Reserved
1	R/W	0b	Serial Port 0 Transmit Activity Monitor (SPTA0)
0	R/W	0b	Serial Port 0 Receive Activity Monitor (SPRA0)

10.1.9.24 Timer 2 Control Register (T2CON)

Address: C8h

Bit	R/W	Default	Description
7	R/W	0b	Timer 2 Overflow (TF2) Set by hardware when the timer 2 overflows. It has to be cleared by software. TF2 is not set if RCLK=1 or TCLK=1.
6	R/W	0b	Timer 2 External Flag (EXF2) If EXEN2=1, a capture or reload is caused by a negative transition on T2EX sets EXF2. EXF2 dose not cause an interrupt in up/down counter mode (DCEN=1).
5	R/W	0b	Receive Clock (RCLK) Selects timer 2 overflow pulses (RCLK=1) or timer 1 overflow pulses (RCLK=0) as the baud rate generator for port mode 1 and 3.
4	R/W	0b	Receive Clock (RCLK) Selects timer 2 overflow pulses (TCLK=1) or timer 1 overflow pulses (TCLK=0) as the baud rate generator for port mode 1 and 3.
3	R/W	0b	Timer 2 External Enable (EXEN2) Setting EXEN2 causes a capture or reload to occur as a result of a negative transition on T2EX unless timer 2 is being used as the baud rate generator for the serial port. Clearing EXEN2 causes timer 2 to ignore events at T2EX.
2	R/W	0b	Timer 2 Run Control (TR2) Setting this bit starts the timer.
1	R/W	0b	Timer/Counter 2 Select (C/T2#) 0: timer 2 counts the divided-down EC clock. 1: timer 2 counts negative transitions on T2 input of 8032 from TMRI1 pin.
0	R/W	0b	Capture/Reload (CP/RL2#) When this bit is set, captures occur on negative transitions at T2EX if EXEN2=1. When reloads occur o if EXEN2=1, the CP/RL2# bit is ignored and timer 2 is forced to auto-reload on timer 2 overflow if RCLK =1 or TCLK = 1.

10.1.9.25 Timer Mode Register (T2MOD)

Address: C9h

Bit	R/W	Default	Description
7-2	-	-	Reserved
1	R/W	0b	Timer 2 Output Enable (T2OE) In the timer 2 clock-out mode, this bit connects the programmable clock output to External signal T2.
0	R/W	0b	Down Count Enable (DCEN) This bit configures timer 2 as an up/down counter.

10.1.9.26 Timer 2 Capture Low Byte Register (RCAP2LR)

Address: CAh

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 2 Capture Low Byte Bit [7:0] (RCAP2L) Low byte of the timer2 reload/recapture register. This register stores 8-bit value to be loaded into or captured from the timer register TL2 in timer 2.

10.1.9.27 Timer 2 Capture High Byte Register (RCAP2HR)

Address: CBh

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 2 Capture High Byte Bit [7:0] (RCAP2H) High byte of the timer2 reload/recapture register. This register stores 8-bit value to be loaded into or captured from the timer register TH2 in timer 2.

10.1.9.28 Timer 2 Low Byte Register (TL2R)

Address: CCh

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 2 Low Byte Bit [7:0] (TL2) Timer 2 low byte register.

10.1.9.29 Timer 2 High Byte Register (TH2R)

Address: CDh

Bit	R/W	Default	Description
7-0	R/W	00h	Timer 2 High Byte Bit [7:0] (TH2) Timer 2 high byte register.

10.1.9.30 Program Status Word Register (PSW)

Address: D0h

Bit	R/W	Default	Description
7	R/W	0b	Carry Flag (CY) CY is set if the operation result in a carry out of (during addition) or a borrow into (during subtraction) the high-order bit in the result; otherwise CY is cleared.
6	R/W	0b	Auxiliary Carry Flag (AC) AC is set if the operation result in a carry out of the low-order 4 bits of the result (during addition) or a borrow from the high-order bits into the low-order 4 bits (during subtraction); otherwise AC is cleared.
5	R/W	0b	User Flag 0 (F0) General-purpose flag.
4-3	R/W	0b	Register Bank Select Bit [1:0](RS1:0) 0h: bank 0, 00h-07h 1h: bank 1, 08h-0Fh 2h: bank 2, 10h-17h 3h: bank 3, 18h-1Fh
2	R/W	0b	Overflow Flag (OV) This bit is set if an addition or signed variables result in an overflow error (i.e., if the magnitude of the sum or difference is too great for the seven LSBs in 2's – complement representation). The overflow flag is also set if the multiplication product overflows one byte or if a division by zero is attempted.
1	R/W	0b	User Defined Flag (UD) General-purpose flag.
0	R/W	0b	Parity Flag (P) This bit indicates the parity of the accumulator. It is set if an odd number of bits in the accumulator is set. Otherwise, it is cleared. Not all instructions update the parity bit. The parity bit is set or cleared by instructions that change the contents to the accumulator.

10.1.9.31 Watch Dog Timer Control Register (WDTCON)

Address: D8h

Bit	R/W	Default	Description
7	-	-	Reserved
6-2	-	-	Reserved
1	R/W	0b	Watch Dog Timer Enable (WDTEN) Setting '1' enables the watchdog timer.
0	R/W	0b	Watch Dog Timer Reset (WDTRST) Setting '1' resets the watchdog timer.

10.1.9.32 Accumulator Register (ACC)

Address: E0h

Bit	R/W	Default	Description
7-0	R/W	00h	Accumulator Bit [7:0] (ACC[7:0]) The instruction uses the accumulator as both source and destination for calculations and moves.

10.1.9.33 B Register (BR)

Address: F0h

Bit	R/W	Default	Description
7-0	-	00h	B Register (B[7:0]) The B Register is used as both a source and destination in multiply and divide operations.

10.1.9.34 Manual Prefetch Register (MPREFC)

Address: F7h

Bit	R/W	Default	Description
7-6	-	-	Reserved
5-0	W	-	Manually Prefetch Count (MPREFCN) This register is dedicated to clear internal dynamic caches. Refer to section 10.1.10.9 Code Snippet of Clearing Dynamic Caches on page 279.

10.1.10 Programming Guide

10.1.10.1 IT8733 Coding Consideration

Coding consideration is to speed up the 8032 code-fetch performance while fetching from serial flash. There are some recommendations for coding consideration.

- If a code section is usually fetched, consider shadowing it to Scratch SRAM or let it be recognized by on-chip cache mechanism.
- The on-chip cache mechanism automatically recognizes a loop which is constructed with “CJNE” or “DJNZ” instruction.
- If a function contains only few bytes, consider replacing it with macro function.
- R8032TT code-fetch frequency is variable while fetching from serial flash. A delay routine which is formed by a loop routine can have a known delay time even code-fetch frequency is variable since the loop is fetched from loop or not. A delay routine can be implemented by WNCKR register. However, this is a simple way.

10.1.10.2 Code Snippet of Entering Idle/Doze/Sleep Mode

```
; Power-down ADC/DAC analog circuit  
; Disable unnecessary channel of INTC/WUC  
  
nop          ; Reserved  
orl pcon, #01h ; #01h for Idle mode  
              ; #02h for Doze/Sleep mode  
  
; Repeat "nop" eight times immediately  
; for internal bus turn-around  
nop          ; 1st  
nop          ; 2nd  
nop          ; 3rd  
nop          ; 4th  
nop          ; 5th  
nop          ; 6th  
nop          ; 7th  
nop          ; 8th
```

10.1.10.3 Code Snippet of Copying Flash Content to Scratch ROM 0 (PIO)

```
; First copy data from code space to Scratch RAM in data space,  
; then enable code space mapping of Scratch ROM  
  
; copy 256 bytes from code space to scratch RAM  
; code space: FF00h ~ FFFFh (byte)  
; data space: 0700h ~ 07FFh (byte)  
  
copy_loop:  
    mov r6, #00h  
    mov dptr, #0ff00h      ; read from code space from ff00h (byte)  
    mov a, r6  
    movc a, @a+dptr       ; write to data space from 0700h (byte)  
    mov dph, #07h  
    mov dpl, r6  
    movx @dptr, a  
  
    inc r6  
    cjne r6, #00h, copy_loop ; copy 256 bytes  
  
    ; enable mapping Scratch SRAM to Scratch ROM  
    mov dptr, #1042h        ; SCAR0H register  
    mov a, #03h              ; disable code space mapping first  
    movx @dptr, a  
  
    mov dptr, #1040h        ; SCAR0L register  
    mov a, #00h              ;  
    movx @dptr, a  
  
    mov dptr, #1041h        ; SCAR0 register  
    mov a, #0ffh              ;
```

```

movx    @dptr, a
mov      dptr, #1042h          ; SCAR0H register
mov      a, #00h               ;
movx    @dptr, a              ; enable code space mapping

```

10.1.10.4 Code Snippet of Copying Flash Content to Scratch ROM (DMA)

```

; DMA copies 2048 bytes from code space to scratch RAM then
; enable code space mapping
;
; code space: F800h ~ FFFFh (byte)
; data space: 0000h ~ 07FFh (byte)

mov      dptr, #1042h          ; SCAR0H register
mov      a, #80h               ;
movx   @dptr, a
;
mov      dptr, #1040h          ; SCAR0L register
mov      a, #00h               ;
movx   @dptr, a
;
mov      dptr, #1041h          ; SCAR0 register
mov      a, #0f8h               ;
movx   @dptr, a
;
mov      dptr, #1042h          ; SCAR0H register
mov      a, #00h               ;
movx   @dptr, a
; start DMA then enable code space mapping

```

10.1.10.5 Code Snippet of Changing PLL Frequency

```

mov      b,#07h               ; let reg. b = new PLLFREQR value
mov      dptr,#1e06h            ; PLLFREQR reg. addr
movx   a,@dptr               ; check whether PLLFREQR value
cjne   a,b,pll_chgfreq       ;
sjmp   bypass_pll_chgfreq

pll_chgfreq:
xch    a,b                  ; modify PLLFREQR reg.
movx   @dptr,a
;
mov      dptr,#1e03h            ; PLLCTRL reg. addr.
mov      a,#01h               ; 1: Sleep mode; 0: Doze mode
movx   @dptr,a
;
clr    ea                   ; intentionally clear EA
orl    pcon,#02h             ; enter Sleep mode then immediately
                             ; wakeup with new frequency
nop
nop
nop
nop
nop

```

```
nop  
nop  
nop  
  
bypass_pll_chgfreq:  
.....
```

10.1.10.6 Code Snippet of EC Base Signature

```
org      40h           ; available list: 40h, 50h  
          ; ... E0h, F0h (interval 10h)  
  
db      0A5h, 0A5h, 0A5h, 0A5h, 0A5h, 0A5h, 0A5h, 0A5h  
db      085h, 012h, 05Ah, 05Ah, 0AAh, 0AAh, 055h, 055h
```

10.1.10.7 Code Snippet of Sending EWSR+WRSR during HSPI Init

```
; required to put this code snippet in Scratch ROM  
  
mov      dptr,#103bh      ; ECINDADDR0  
mov      a,#0ffh  
movx    @dptr,a  
  
inc      dptr  
movx    @dptr,a      ; ECINDADDR1  
  
inc      dptr  
movx    @dptr,a      ; ECINDADDR2  
  
inc      dptr  
movx    @dptr,a      ; ECINDADDR3  
  
mov      dph,#10h        ; DPH = SMFI  
mov      dpl,#3ch  
mov      85h,#10h        ; DPL = ECINDAR1  
mov      84h,#3fh        ; DPH1  
          ; DPL1 = ECINDDR  
          ;  
          ; in the following code  
          ; dps = 0: ECINDAR1  
          ; dps = 1: ECINDDR  
  
          ; FSCE# high  
mov      a,#0feh  
movx    @dptr,a      ; select FSCE#  
  
inc      dps  
mov      a,#00h  
movx    @dptr,a      ; ECINDAR1->ECINDDR  
inc      dps  
          ; FMOSI = 0 while FSCE# = 1  
          ; ECINDDR->ECINDAR1  
  
          ; toggle FMOSI  
mov      a,#0fdh  
movx    @dptr,a      ; select FMOSI
```

```

inc      dps          ; ECINDAR1->ECINDDR
mov      a,#50h       ; inst EWSR = 50h
movx    @dptr,a
inc      dps          ; ECINDDR->ECINDAR1

; FSCE# high
mov      a,#0feh     ; select FSCE#
movx    @dptr,a

inc      dps          ; ECINDAR1->ECINDDR
mov      a,#00h       ; FMOSI = 0 while FSCE# = 1
movx    @dptr,a
inc      dps          ; ECINDDR->ECINDAR1

; toggle FMOSI
mov      a,#0fdh     ; select FMOSI
movx    @dptr,a

inc      dps          ; ECINDAR1->ECINDDR
mov      a,#01h       ; inst WRSR = 01h
movx    @dptr,a
mov      a,#00h       ; data byte 00h after EWSR
movx    @dptr,a
inc      dps          ; ECINDDR->ECINDAR1

; FSCE# high
mov      a,#0feh     ; select FSCE#
movx    @dptr,a

inc      dps          ; ECINDAR1->ECINDDR
mov      a,#00h       ; FMOSI = 0 while FSCE# = 1
movx    @dptr,a
inc      dps          ; ECINDDR->ECINDAR1

; escape EC-ind follow mode
; write address 31-24
mov      dpl,#3eh    ; ECINDAR3
mov      a,#00h
movx    @dptr,a

```

10.1.10.8 Code Snippet of Sending WREN within ISR of INT59

; required to put this code snippet in Scratch ROM

```

mov      dptr,#103bh   ; ECINDADDR0
mov      a,#0ffh
movx    @dptr,a

inc      dptr         ; ECINDADDR1
movx    @dptr,a

inc      dptr         ; ECINDADDR2
movx    @dptr,a

```

```

inc      dptr          ; ECINDADDR3
movx    @dptr,a

mov      dph,#10h       ; DPH = SMFI
mov      dpl,#3ch       ; DPL = ECINDAR1
mov      85h,#10h       ; DPH1
mov      84h,#3fh       ; DPL1 = ECINDDR
;
; in the following code
; dps = 0: ECINDAR1
; dps = 1: ECINDDR

; FSCE# high
mov      a,#0feh        ; select FSCE#
movx    @dptr,a

inc      dps            ; ECINDAR1->ECINDDR
mov      a,#00h          ; FMOSI = 0 while FSCE# = 1
movx    @dptr,a
inc      dps            ; ECINDDR->ECINDAR1

; toggle FMOSI
mov      a,#0fdh        ; select FMOSI
movx    @dptr,a

inc      dps            ; ECINDAR1->ECINDDR
mov      a,#06h          ; inst WREN = 06h
movx    @dptr,a
inc      dps            ; ECINDDR->ECINDAR1

; FSCE# high
mov      a,#0feh        ; select FSCE#
movx    @dptr,a

inc      dps            ; ECINDAR1->ECINDDR
mov      a,#00h          ; FMOSI = 0 while FSCE# = 1
movx    @dptr,a
inc      dps            ; ECINDDR->ECINDAR1

; escape EC-ind follow mode
; write address 31-24
mov      dpl,#3eh        ; ECINDAR3
mov      a,#00h
movx    @dptr,a

; bridge this deferred WIP cycle now
mov      dptr,#1058h
mov      a,#0fh
movx    @dptr,a

```

10.1.10.9 Code Snippet of Clearing Dynamic Caches

; after flash is modified by the host program, the dynamic caches have to be
; cleared since they contain old and invalid cache content
; uC should execute these lines if the program counter leaves Scratch ROM

```
mov      0f7h, #01h ; MPREFC reg
nop
```

CONFIDENTIAL

10.2 Interrupt Controller (INTC)

10.2.1 Overview

INTC mainly collects several interrupts from modules. Using interrupt driven design has a better performance than polling-driven.

It traps LRESET#, ROM match interrupt and samples interrupt channels, then outputs to the INT0# and INT1# of 8032.

Both interrupts INT0# and INT1# to 8032 are generated by INTC, and don't write 1 to IT0 and IT1 bit in TCON because interrupt triggered type is considered in INTC and needs IT0 and IT1 to be set as level-low triggered.

Note INT0# and INT1# are external interrupts of 8032 and they are controlled by EA, EX0 and EX1 in IE register.

External interrupts can wakeup 8032 from Idle/Doze/Sleep mode, but internal interrupts can wakeup 8032 from Idle mode only.

10.2.2 Features

- Configurable level-triggered and edge-triggered mode
- Configurable interrupt polarity of triggered mode
- Clear registers for edge-triggered interrupts
- Each interrupt source can be enabled/masked individually
- Special handler for power-fail (INT0# of 8032)

10.2.3 Functional Description

10.2.3.1 Power Fail Interrupt

The INTC collects interrupt sources from internal and external (through WUC) and provides two interrupt requests INT0# and INT1# to 8032. 8032 treats INT0# as a higher priority interrupt request than INT1#. INTC uses INT0# as a power-fail interrupt and INT1# as a maskable interrupt. The firmware should enable the IE0 and IE1 bit in TCON before all.

To implement a power-fail application, connect LRESET# to external circuit. To receive an asynchronous external input, and provides related INT0# interrupt routine.

There are two methods to trap a power-fail event: "Trap Enabled" and "Trap Enabled and Locked". Users select "Trap Enabled" by setting TREN bit in PFAILR and select "Trap Enabled and Locked" by setting TRENL bit in PFAILR. If both bits are selected, TREN bit is ignored. If "Trap Enabled" is used, power-fail event is detected by falling edge transition of LRESET#, and INT0# to 8032 is asserted. After INT0# is set, TREN bit is cleared. "Trap Enabled and Locked" method is similar to "Trap Enabled" method but TRENL will not be cleared after INT0# is set.

10.2.3.2 ROM Match Interrupt

Refer to section 10.8 Debugger (DBGR) on page 320.

10.2.3.3 Programmable Interrupts

INTC also collects maskable interrupt sources and make a request on INT1 # of 8032 if triggered. Each channel can be individually enabled or masked by IERx. If an interrupt channel is masked and one interrupt request is triggered, the request is masked (inhibited, not canceled), and will be asserted the request on INT1# if it is enabled.

The ISR_x indicates the status of interrupt regardless of IER_x. In the level-triggered mode, ISR_x is affected by corresponding interrupt sources, and firmware should clear the interrupt status on interrupt sources after its request is handled. In edge-triggered mode, ISR_x is set by selected edge transition (determined by IELMR_x) of corresponding interrupts sources, and firmware should write 1 to clear to ISR_x after this request is handled.

Firmware may use the IVECT to determine which channel is to be serviced first or have its priority rule by reading ISR_x and IER_x. IVECT treats INT1 as the lowest priority interrupt.

The 8032 always wakes up from Idle/Doze/Sleep mode when it detects an enabled external interrupt and it wakes up from Idle mode by internal interrupt, too. Firmware should disable unwanted interrupt sources to prevent from waking up unexpectedly.

Normally interrupts from WUC are high level-triggered. Note that interrupts from WUC are not always level-triggered interrupts since they may be just throughout WUC if the corresponding channels at WUC are disabled (bypassed). If an edge-triggered passes through WUC and INTC with WUC corresponding channel is disabled and INTC corresponding channel is level-trig mode, it may cause 8032 interrupt routine called but finds no interrupt source to service, or it may cause 8032 to wake up from Idle/Doze/Sleep mode and enters interrupt routine but finds no interrupt source to service.

10.2.4 EC Interface Registers

The EC interface registers are listed below. The base address for INTC is 1100h.

Table 10-7. EC View Register Map, INTC

7	0	Offset
Interrupt Status Register 0 (ISR0)		00h
Interrupt Status Register 1 (ISR1)		01h
Interrupt Status Register 2 (ISR2)		02h
Interrupt Status Register 3 (ISR3)		03h
Interrupt Status Register 4 (ISR4)		14h
Interrupt Status Register 5 (ISR5)		18h
Interrupt Status Register 6 (ISR6)		1Ch
Interrupt Status Register 7 (ISR7)		20h
Interrupt Status Register 8 (ISR8)		24h
Interrupt Status Register 9 (ISR9)		28h
Interrupt Enable Register 0 (IER0)		04h
Interrupt Enable Register 1 (IER1)		05h
Interrupt Enable Register 2 (IER2)		06h
Interrupt Enable Register 3 (IER3)		07h
Interrupt Enable Register 4 (IER4)		15h
Interrupt Enable Register 5 (IER5)		19h
Interrupt Enable Register 6 (IER6)		1Dh
Interrupt Enable Register 7 (IER7)		21h
Interrupt Enable Register 8 (IER8)		25h
Interrupt Enable Register 9 (IER9)		29h
Interrupt Edge/Level-Trig Mode Register 0 (IELMR0)		08h
Interrupt Edge/Level-Trig Mode Register 1 (IELMR1)		09h
Interrupt Edge/Level-Trig Mode Register 2 (IELMR2)		0Ah
Interrupt Edge/Level-Trig Mode Register 3 (IELMR3)		0Bh
Interrupt Edge/Level-Trig Mode Register 4 (IELMR4)		16h
Interrupt Edge/Level-Trig Mode Register 5 (IELMR5)		1Ah

7	0	Offset
Interrupt Edge/Level-Trig Mode Register 6 (IELMR6)		1Eh
Interrupt Edge/Level-Trig Mode Register 7 (IELMR7)		22h
Interrupt Edge/Level-Trig Mode Register 8 (IELMR8)		26h
Interrupt Edge/Level-Trig Mode Register 9 (IELMR9)		2Ah
Interrupt Polarity Register 0 (IPOLR0)		0Ch
Interrupt Polarity Register 1 (IPOLR1)		0Dh
Interrupt Polarity Register 2 (IPOLR2)		0Eh
Interrupt Polarity Register 3 (IPOLR3)		0Fh
Interrupt Polarity Register 4 (IPOLR4)		17h
Interrupt Polarity Register 5 (IPOLR5)		1Bh
Interrupt Polarity Register 6 (IPOLR6)		1Fh
Interrupt Polarity Register 7 (IPOLR7)		23h
Interrupt Polarity Register 8 (IPOLR8)		27h
Interrupt Polarity Register 9 (IPOLR9)		2Bh
Interrupt Vector Register (IVECT)		10h
INT0# status (INT0ST)		11h
Power Fail Register (PFAILR)		12h

10.2.4.1 Interrupt Status Register 0 (ISR0)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 00h

Bit	R/W	Default	Description
7-1	R/WC Or R	-	Interrupt Status (IS7-1) It indicates the interrupt input status of INTx. INTST7 to INTST1 correspond to INT7 to INT1 respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, and is R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending. Read 1: Interrupt input to INTC is pending. For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.
0	R	0b	Reserved

10.2.4.2 Interrupt Status Register 1 (ISR1)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS15-8) It indicates the interrupt input status of INTx. INTST15 to INTST8 correspond to INT15 to INT8 respectively.

10.2.4.3 Interrupt Status Register 2 (ISR2)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS23-16) It indicates the interrupt input status of INTx. INTST23 to INTST16 correspond to INT23 to INT16 respectively.

10.2.4.4 Interrupt Status Register 3 (ISR3)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS31-24) It indicates the interrupt input status of INTx. INTST31 to INTST24 correspond to INT31 to INT24 respectively.

10.2.4.5 Interrupt Status Register 4 (ISR4)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS39-32) It indicates the interrupt input status of INTx. INTST39 to INTST32 correspond to INT39 to INT32 respectively.

10.2.4.6 Interrupt Status Register 5 (ISR5)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS47-40) It indicates the interrupt input status of INTx. INTST47 to INTST40 correspond to INT47 to INT40 respectively.

10.2.4.7 Interrupt Status Register 6 (ISR6)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS55-48) It indicates the interrupt input status of INTx. INTST55 to INTST48 correspond to INT55 to INT48 respectively.

10.2.4.8 Interrupt Status Register 7 (ISR7)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS63-56) It indicates the interrupt input status of INTx. INTST63 to INTST56 correspond to INT63 to INT56 respectively.

10.2.4.9 Interrupt Status Register 8 (ISR8)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS71-64) It indicates the interrupt input status of INTx. INTST71 to INTST64 correspond to INT71 to INT64 respectively.

10.2.4.10 Interrupt Status Register 9 (ISR9)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	Interrupt Status (IS79-72) It indicates the interrupt input status of INTx. INTST79 to INTST72 correspond to INT79 to INT72 respectively.

10.2.4.11 Interrupt Enable Register 0 (IER0)

Address Offset: 04h

Bit	R/W	Default	Description
7-1	R/W	0h	Interrupt Enable (IE7-0) Each bit determines whether its corresponding interrupt channel (INT7-0) is masked or enabled. Note that it has no effect on INT0 0: Masked 1: Enabled
0	-	0b	Reserved

10.2.4.12 Interrupt Enable Register 1 (IER1)

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE15-8) Each bit determines whether its corresponding interrupt channel (INT15-8) is masked or enabled.

10.2.4.13 Interrupt Enable Register 2 (IER2)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE23-16) Each bit determines whether its corresponding interrupt channel (INT23-16) is masked or enabled.

10.2.4.14 Interrupt Enable Register 3 (IER3)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE31-24) Each bit determines whether its corresponding interrupt channel (INT31-24) is masked or enabled.

10.2.4.15 Interrupt Enable Register 4 (IER4)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE39-32) Each bit determines whether its corresponding interrupt channel (INT39-32) is masked or enabled.

10.2.4.16 Interrupt Enable Register 5 (IER5)

Address Offset: 19h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE47-40) Each bit determines whether its corresponding interrupt channel (INT47-40) is masked or enabled.

10.2.4.17 Interrupt Enable Register 6 (IER6)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE55-48) Each bit determines whether its corresponding interrupt channel (INT55-48) is masked or enabled.

10.2.4.18 Interrupt Enable Register 7 (IER7)

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE63-56) Each bit determines whether its corresponding interrupt channel (INT63-56) is masked or enabled.

10.2.4.19 Interrupt Enable Register 8 (IER8)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE71-64) Each bit determines whether its corresponding interrupt channel (INT71-64) is masked or enabled.

10.2.4.20 Interrupt Enable Register 9 (IER9)

Address Offset: 29h

Bit	R/W	Default	Description
7-0	R/W	0h	Interrupt Enable (IE79-72) Each bit determines whether its corresponding interrupt channel (INT79-72) is masked or enabled.

10.2.4.21 Interrupt Edge/Level-Trigged Mode Register 0 (IELMR0)

It determines whether its corresponding interrupt channel is level-triggered or edge-triggered.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00000000b	Interrupt Edge/Level-Trigged Mode (IELM7-0) Each bit determines the triggered mode of the corresponding interrupt channel (INT7-0). 0: Level-triggered 1: Edge-triggered Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.

10.2.4.22 Interrupt Edge/Level-Trigged Mode Register 1 (IELMR1)

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00000000b	Interrupt Edge/Level-Trigged Mode (IELM15-8) Each bit determines the triggered mode of the corresponding interrupt channel (INT15-8).

10.2.4.23 Interrupt Edge/Level-Trigged Mode Register 2 (IELMR2)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00011100b	Interrupt Edge/Level-Trigged Mode (IELM23-16) Each bit determines the triggered mode of the corresponding interrupt channel (INT23-16).

10.2.4.24 Interrupt Edge/Level-Trigged Mode Register 3 (IELMR3)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	01100000b	Interrupt Edge/Level-Trigged Mode (IELM31-24) Each bit determines the triggered mode of the corresponding interrupt channel (INT31-24).

10.2.4.25 Interrupt Edge/Level-Trigged Mode Register 4 (IELMR4)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R	11111111b	Interrupt Edge/Level-Trigged Mode (IELM39-32) Each bit determines the triggered mode of the corresponding interrupt channel (INT39-32).

10.2.4.26 Interrupt Edge/Level-Trigged Mode Register 5 (IELMR5)

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R	00000000b	Interrupt Edge/Level-Trigged Mode (IELM47-40) Each bit determines the triggered mode of the corresponding interrupt channel (INT47-40).

10.2.4.27 Interrupt Edge/Level-Trigged Mode Register 6 (IELMR6)

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	00000000b	Interrupt Edge/Level-Trigged Mode (IELM55-48) Each bit determines the triggered mode of the corresponding interrupt channel (INT55-48).

10.2.4.28 Interrupt Edge/Level-Trigged Mode Register 7 (IELMR7)

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R	00000000b	Interrupt Edge/Level-Trigged Mode (IELM63-56) Each bit determines the triggered mode of the corresponding interrupt channel (INT63-56).

10.2.4.29 Interrupt Edge/Level-Trigged Mode Register 8 (IELMR8)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R	00000000b	Interrupt Edge/Level-Trigged Mode (IELM71-64) Each bit determines the triggered mode of the corresponding interrupt channel (INT71-64).

10.2.4.30 Interrupt Edge/Level-Trigged Mode Register 9 (IELMR9)

Address Offset: 2Ah

Bit	R/W	Default	Description
7-0	R	00000000b	Interrupt Edge/Level-Trigged Mode (IELM79-72) Each bit determines the triggered mode of the corresponding interrupt channel (INT79-72).

10.2.4.31 Interrupt Polarity Register 0 (IPOLR0)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	0h	<p>Interrupt Polarity (IPOL7-0) Each bit determines the active high/low of the corresponding interrupt channel (INT7-0). 0: level-high-triggered or rising-edge-triggered 1: level-low-triggered or falling-edge-triggered</p> <p>Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.</p>

10.2.4.32 Interrupt Polarity Register 1 (IPOLR1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R/W	0h	<p>Interrupt Polarity (IPOL15-8) Each bit determines the active high/low of the corresponding interrupt channel (INT15-8).</p>

10.2.4.33 Interrupt Polarity Register 2 (IPOLR2)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	0h	<p>Interrupt Polarity (IPOL23-16) Each bit determines the active high/low of the corresponding interrupt channel (INT23-16)</p>

10.2.4.34 Interrupt Polarity Register 3 (IPOLR3)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	0h	<p>Interrupt Polarity (IPOL31-24) Each bit determines the active high/low of the corresponding interrupt channel (INT31-24).</p>

10.2.4.35 Interrupt Polarity Register 4 (IPOLR4)

Address Offset: 17h

Bit	R/W	Default	Description
7-0	R	0h	<p>Interrupt Polarity (IPOL39-32) Each bit determines the active high/low of the corresponding interrupt channel (INT39-32).</p>

10.2.4.36 Interrupt Polarity Register 5 (IPOLR5)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-0	R	0h	Interrupt Polarity (IPOL47-40) Each bit determines the active high/low of the corresponding interrupt channel (INT47-40).

10.2.4.37 Interrupt Polarity Register 6 (IPOLR6)

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	0h	Interrupt Polarity (IPOL55-48) Each bit determines the active high/low of the corresponding interrupt channel (INT55-48).

10.2.4.38 Interrupt Polarity Register 7 (IPOLR7)

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R	0h	Interrupt Polarity (IPOL63-56) Each bit determines the active high/low of the corresponding interrupt channel (INT63-56).

10.2.4.39 Interrupt Polarity Register 8 (IPOLR8)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R	0h	Interrupt Polarity (IPOL71-64) Each bit determines the active high/low of the corresponding interrupt channel (INT71-64).

10.2.4.40 Interrupt Polarity Register 9 (IPOLR9)

Address Offset: 2Bh

Bit	R/W	Default	Description
7-0	R	0h	Interrupt Polarity (IPOL79-72) Each bit determines the active high/low of the corresponding interrupt channel (INT79-72).

10.2.4.41 Interrupt Vector Register (IVCT)

Address Offset: 10h

Bit	R/W	Default	Description
7	R	0b	Reserved
6-0	R	0010000b	Interrupt Vector (IVECT) It contains the interrupt number, which is the highest priority, enabled and pending interrupt. The valid values range from 10h. Note that INT1 has the lowest priority. If no enabled interrupt is pending, it returns 10h.

10.2.4.42 8032 INT0# Status (INT0ST)

INT0PF is set when falling edge transition of LRESET# with TREN or TRENL bit in PFAILR is set, and it is clear when being reset or read its content.

INT0RM is set when the trigger address matches the 8032 program counter.

Address Offset: 11h

Bit	R/W	Default	Description
7-1	-	00h	Reserved
1	R	-	INT0# from ROM Match Status (INT0RM) 0: INT0# is deasserted by an 8032 ROM match. 1: INT0# is asserted by an 8032 ROM match.
0	R	-	INT0# from LRESET# Status (INT0PF) 0: INT0# is deasserted by a LRESET#. 1: INT0# is asserted by a LRESET#.

10.2.4.43 Power Fail Register (PFAILR)

It provides two methods to trap the LRESET# event.
This register can't be reset by WDT Reset.

Address Offset: 12h

Bit	R/W	Default	Description
7-3	-	00h	Reserved
2	R/W	0b	LRESET# Trap Enabled and Locked (TRENL) Firmware sets this bit to enable LRESET# trap. When trap is enabled, INT0 bit in INT0ST will be set if the falling edge transition of LRESET# is detected. This bit can't be cleared by writing 0 to it until reset. 0: No LRESET# Trap 1: LRESET# Trap
1	R	-	LRESET# Status (PFAILST) 0: LRESET# is low (asserted) 1: LRESET# is high (deasserted)
0	R/W	0b	LRESET# Trap Enabled (TREN) Firmware sets this bit to enable LRESET# trap. When trap is enabled, INT0 bit in INT0ST will be set if the falling edge transition of LRESET# is detected, and TREN will be cleared. This bit is ignored when TRENL bit is set. 0: No LRESET# Trap 1: LRESET# Trap

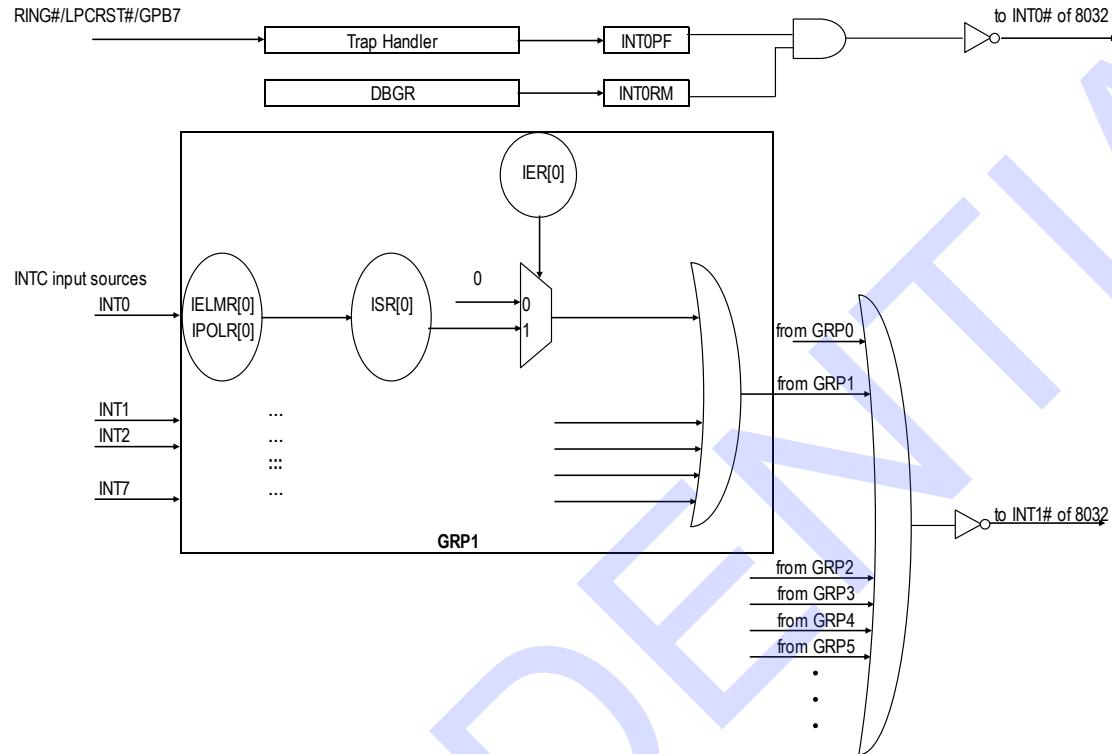
10.2.5 INTC Interrupt Assignments

Table 10-8. INTC Interrupt Assignments

Interrupt	Source	Default Type (Adjustable)	Description	Reference
INT0	Reserved	-	-	-
INT1	External/WUC	High-Level Trig	WKO[10]	Figure 10-16, p280
INT2	Internal	High-Level Trig	SWKBC OBE Interrupt	Section 10.9, pxxx
INT3	Internal	High-Level Trig	PMC1 Output Buffer Empty Intr.	Section 9.10.5.1, p185
INT4	Reserved	-	-	-
INT5	Reserved	-	-	-
INT6	External/WUC	High-Level Trig	WKO[11]	Figure 10-16, p280
INT7	Internal	High-Level Trig	USB Interrupt	-
INT8	Reserved	-	-	-
INT9	Internal	High-Level Trig	SMBus A Interrupt	Section 9.12.4.1, p214
INT10	Internal	High-Level Trig	SMBus B Interrupt	Section 9.12.4.1, p214
INT11	Internal	High-Level Trig	KB Matrix Scan Interrupt	Section 10.9, pxxx
INT12	External/WUC	High-Level Trig	WKO[12]	Figure 10-16, p280
INT13	External/WUC	High-Level Trig	WKO[13]	Figure 10-16, p280
INT14	External/WUC	High-Level Trig	WKO[14]	Figure 10-16, p280
INT15	Internal	High-Level Trig	IO_CIR Interrupt	Section 9.8.6.2, p149
INT16	Internal	High-Level Trig	SMBus C Interrupt	Section 9.12.4.1, p214
INT17	External/WUC	High-Level Trig	WKO[15]	Figure 10-16, p280
INT18	Reserved	-	-	-
INT19	Reserved	-	-	-
INT20	Reserved	-	-	-
INT21	External/WUC	High-Level Trig	WKO[16]	Figure 10-16, p280
INT22	Internal	High-Level Trig	SMFI Semaphore Interrupt	Section 9.9.4.5, p169
INT23	Reserved	-	-	-
INT24	Interrupt	High-Level Trig	SWKBC IBF Interrupt	Section 10.9, pxxx
INT25	Internal	High-Level Trig	PMC1 Input Buffer Full Interrupt	Section 9.10.5.1, p185
INT26	Internal	High-Level Trig	PMC2 Output Buffer Empty Intr.	Section 9.10.5.1, p185
INT27	Internal	High-Level Trig	PMC2 Input Buffer Full Intr.	Section 9.10.5.1, p185
INT28	Reserved	-	-	-
INT29	Reserved			
INT30	Internal	Rising-Edge Trig	External Timer 1 Interrupt	Section 10.5.3, p284
INT31	External/WUC	High-Level Trig	WKO[17]	Figure 10-16, p280

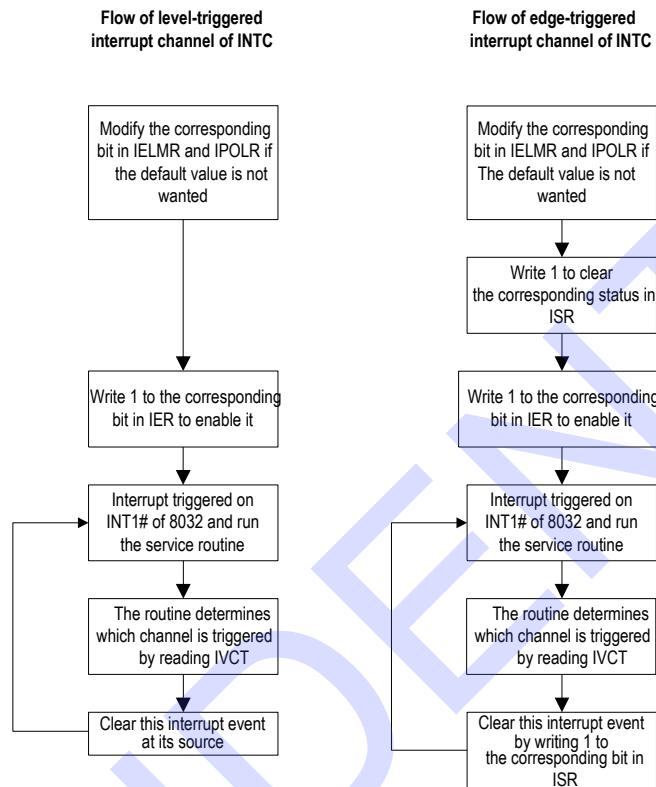
Interrupt	Source	Default Type (Adjustable)	Description	Reference
INT32	Internal	Rising-Edge Trig (Not Adjustable)	GPINT0	Section 8.14.9, p89
INT33	Internal		GPINT1	Section 8.14.9, p89
INT34	Internal		GPINT2	Section 8.14.9, p89
INT35	Internal		GPINT3	Section 8.14.9, p89
INT36	Reserved		-	-
INT37	Reserved		-	-
INT38	Internal		IO_UART1 Interrupt	Section 9.6.2.1, p136
INT39	Internal		IO_UART2 Interrupt	Section 9.6.2.1, p136
INT40	External/WUC	High-Level Trig (Not Adjustable)	WKO[20]	Figure 10-16, p280
INT41	External/WUC		WKO[21]	Figure 10-16, p280
INT42	External/WUC		WKO[22]	Figure 10-16, p280
INT43	External/WUC		WKO[23]	Figure 10-16, p280
INT44	External/WUC		WKO[24]	Figure 10-16, p280
INT45	External/WUC		WKO[25]	Figure 10-16, p280
INT46	External/WUC		WKO[26]	Figure 10-16, p280
INT47	External/WUC		WKO[27]	Figure 10-16, p280
INT48	External/WUC		WKO[30]	Figure 10-16, p280
INT49	External/WUC		WKO[31]	Figure 10-16, p280
INT50	External/WUC		WKO[32]	Figure 10-16, p280
INT51	External/WUC	High-Level Trig	WKO[33]	Figure 10-16, p280
INT52	External/WUC	(Not Adjustable)	WKO[34]	Figure 10-16, p280
INT53	External/WUC		WKO[35]	Figure 10-16, p280
INT54	External/WUC		WKO[36]	Figure 10-16, p280
INT55	External/WUC		WKO[37]	Figure 10-16, p280
INT64	Internal	High-Level Trig (Not Adjustable)	PMC2EX Output Buffer Empty Intr.	Section 9.10.5.1, p185
INT65	Internal		PMC2EX Input Buffer Full Intr.	Section 9.10.5.1, p185
INT66	Reserved		-	-
INT67	Reserved		-	-
INT68	Reserved		-	-
INT69	Reserved		-	-
INT70	internal		Parallel Port Interrupt	Section 9.7, pxxx
INT71	Internal	High-Level Trig	IO_ECBLK Interrupt	Section 9.5.2.2.1,p104
INT72	External/WUC		WKO[40]	Figure 10-16, p280
INT73	External/WUC		WKO[41]	Figure 10-16, p280
INT74	External/WUC		WKO[42]	Figure 10-16, p280
INT75	External/WUC	High-Level Trig	WKO[43]	Figure 10-16, p280
INT76	External/WUC	(Not Adjustable)	WKO[44]	Figure 10-16, p280
INT77	External/WUC		WKO[45]	Figure 10-16, p280
INT78	External/WUC		WKO[46]	Figure 10-16, p280
INT79	External/WUC		WKO[47]	Figure 10-16, p280

Figure 10-14. INTC Simplified Diagram



10.2.6 Programming Guide

Figure 10-15. Program Flow Chart for INTC



Note: The routine may has its own interrupt priority by reading ISR register.

Note: If this channel source comes from WUC, the corresponding bit in WUESR needs to be cleared, too

10.3 Wake-Up Control (WUC)

10.3.1 Overview

WUC groups internal and external inputs, and asserts wake-up signals to INTC that allows 8032 to exit an Idle/Doze/Sleep mode.

10.3.2 Features

- Supports internal and external interrupt inputs.
- Supports both the rising-edge and falling-edge triggered mode.
- Input can be connected to INTC directly.

10.3.3 Functional Description

Input sources of WUC are external inputs such as pins about PS/2 and GPIO, or inputs from internal module such as LPC and SMBus that handle external inputs.

Each channel can be selected to be rising or falling edge triggered mode. If one channel is disabled, the input bypasses WUC pending logic and is connected directly to INTC.

10.3.4 EC Interface Registers

The EC interface registers are listed below. The base address for WUC is 1B00h.

Table 10-9. EC View Register Map, WUC

7	0	Offset
		00h
		01h
		02h
		03h
		04h
		05h
		06h
		07h
		08h
		09h
		0Ah
		0Bh

Wake-Up Edge Mode Register 1 (WUEMR1)
Wake-Up Edge Mode Register 2 (WUEMR2)
Wake-Up Edge Mode Register 3 (WUEMR3)
Wake-Up Edge Mode Register 4 (WUEMR4)
Wake-Up Edge Sense Register 1 (WUESR1)
Wake-Up Edge Sense Register 2 (WUESR2)
Wake-Up Edge Sense Register 3 (WUESR3)
Wake-Up Edge Sense Register 4 (WUESR4)
Wake-Up Enable Register 1 (WUENR1)
Wake-Up Enable Register 2 (WUENR2)
Wake-Up Enable Register 3 (WUENR3)
Wake-Up Enable Register 4 (WUENR4)

10.3.4.1 Wake-Up Edge Mode Register 1 (WUEMR1)

This register configures the trigger mode of input signals WU10 to WU17.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Edge Mode (WUEM17-10) 0: Rising-edge triggered is selected. 1: Falling-edge triggered is selected. Always write-1-clear to the corresponding bit in WUESR register after modifying these bits.

10.3.4.2 Wake-Up Edge Mode Register 2 (WUEMR2)

This register configures the trigger mode of input signals WU20 to WU27.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Edge Mode (WUEM27-20)

10.3.4.3 Wake-Up Edge Mode Register 3 (WUEMR3)

This register configures the trigger mode of input signals WU30 to WU37.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Edge Mode (WUEM37-30)

10.3.4.4 Wake-Up Edge Mode Register 4 (WUEMR4)

This register configures the trigger mode of input signals WU40 to WU47.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Edge Mode (WUEM47-40)

10.3.4.5 Wake-Up Edge Sense Register 1 (WUESR1)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU10 to WU17.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/WC	-	Wake-Up Sense (WUES17-10) For each bit: Read 1: It indicates a trigger condition occurs on the corresponding input. Read 0: Otherwise For each bit: Write 1: Clear this bit Write 0: No action

10.3.4.6 Wake-Up Edge Sense Register 2 (WUESR2)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU20 to WU27.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/WC	-	Wake-Up Sense (WUES27-20)

10.3.4.7 Wake-Up Edge Sense Register 3 (WUESR3)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU30 to WU37.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/WC	-	Wake-Up Sense (WUES37-30)

10.3.4.8 Wake-Up Edge Sense Register 4 (WUESR4)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU40 to WU47.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/WC	-	Wake-Up Sense (WUES47-40)

10.3.4.9 Wake-Up Enable Register 1 (WUENR1)

This register enables a wake-up function of the corresponding input signal WU10 to WU17.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Enable (WUEN17-10) 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal; it is canceled but not pending.

10.3.4.10 Wake-Up Enable Register 2 (WUENR2)

This register enables a wake-up function of the corresponding input signal WU20 to WU27.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Enable (WUEN27-20)

10.3.4.11 Wake-Up Enable Register 3 (WUENR3)

This register enables a wake-up function of the corresponding input signal WU30 to WU37.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Enable (WUEN37-30)

10.3.4.12 Wake-Up Enable Register 4 (WUENR4)

This register enables a wake-up function of the corresponding input signal WU40 to WU47.

Address Offset: 0Bh

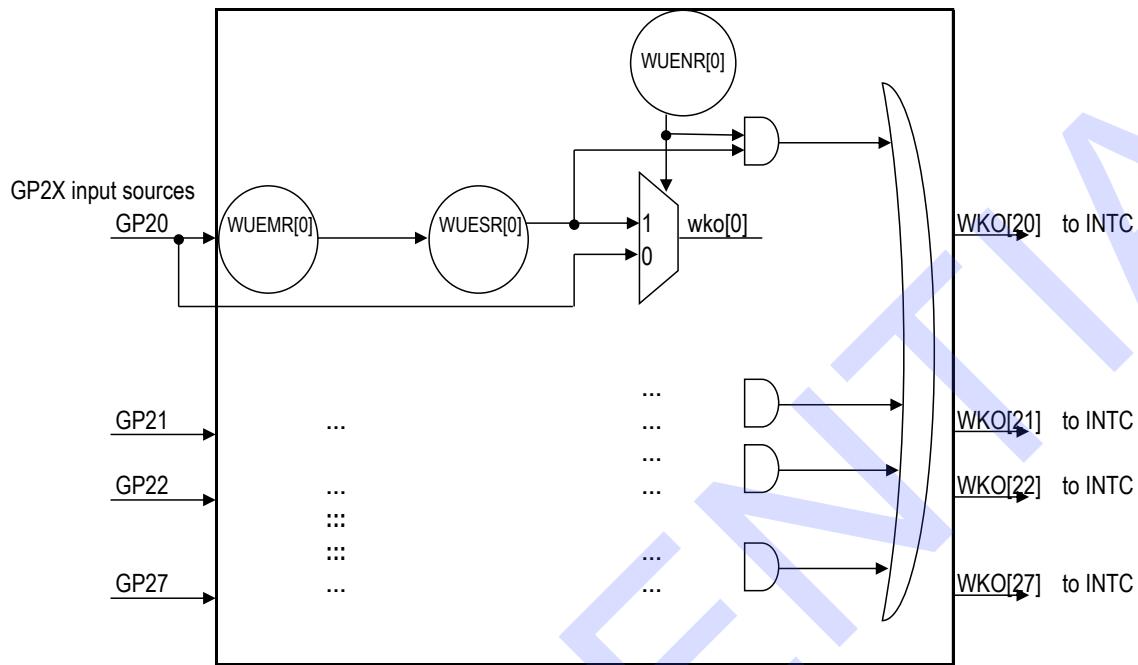
Bit	R/W	Default	Description
7-0	R/W	0h	Wake-Up Enable (WUEN47-40)

10.3.5 WUC Input Assignments

Table 10-10. WUC Input Assignments

WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
WU10	MCLK	External Source from Pin	WKO[10], to INT1	Rising Edge Trig
WU11	MDAT	External Source from Pin	WKO[11], to INT6	Rising Edge Trig
WU12	KCLK	External Source from Pin	WKO[12], to INT12	Rising Edge Trig
WU13	KDAT	External Source from Pin	WKO[13], to INT13	Rising Edge Trig
WU14	LPC Access	LPC Cycle with Address Recognized See also Section 6.1.6, p38	WKO[14], to INT14	Rising Edge Trig
WU15	SMDAT0	External Source from Pin	WKO[15], to INT17	Rising Edge Trig
WU16	SMDAT1	External Source from Pin	WKO[16], to INT21	Rising Edge Trig
WU17	SMDAT2	External Source from Pin	WKO[17] to INT31	Rising Edge Trig
WU20	GP20	External Source from GP20	WKO[20], to INT40	Rising EdgeTrig
WU21	GP21	External Source from GP21	WKO[21], to INT41	Rising EdgeTrig
WU22	GP22	External Source from GP22	WKO[22], to INT42	Rising EdgeTrig
WU23	GP23	External Source from GP23	WKO[23], to INT43	Rising EdgeTrig
WU24	GP24	External Source from GP24	WKO[24], to INT44	Rising EdgeTrig
WU25	GP25	External Source from GP25	WKO[25], to INT45	Rising EdgeTrig
WU26	GP26	External Source from GP26	WKO[26], to INT46	Rising EdgeTrig
WU27	GP27	External Source from GP27	WKO[27], to INT47	Rising EdgeTrig
WU30	GP30	External Source from GP30	WKO[30], to INT48	Rising EdgeTrig
WU31	GP31	External Source from GP31	WKO[31], to INT49	Rising EdgeTrig
WU32	GP32	External Source from GP32	WKO[32], to INT50	Rising EdgeTrig
WU33	GP33	External Source from GP33	WKO[33], to INT51	Rising EdgeTrig
WU34	GP34	External Source from GP34	WKO[34], to INT52	Rising EdgeTrig
WU35	GP35	External Source from GP35	WKO[35], to INT53	Rising EdgeTrig
WU36	GP36	External Source from GP36	WKO[36], to INT54	Rising EdgeTrig
WU37	GP37	External Source from GP37	WKO[37], to INT55	Rising EdgeTrig
WU40	GP70	External Source from GP70	WKO[40], to INT72	Rising EdgeTrig
WU41	GP71	External Source from GP71	WKO[41], to INT73	Rising EdgeTrig
WU42	GP72	External Source from GP72	WKO[42], to INT74	Rising EdgeTrig
WU43	GP73	External Source from GP73	WKO[43], to INT75	Rising EdgeTrig
WU44	GP74	External Source from GP74	WKO[44], to INT76	Rising Edge Trig
WU45	GP75	External Source from GP75	WKO[45], to INT77	Rising Edge Trig
WU46	GP76	External Source from GP76	WKO[46], to INT78	Rising Edge Trig
WU47	GP77	External Source from GP77	WKO[47], to INT79	Rising Edge Trig

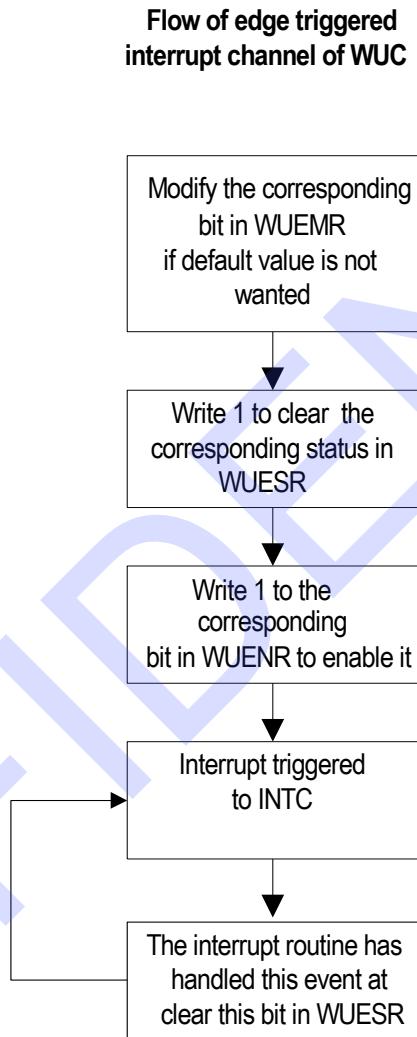
Figure 10-16. WUC Simplified Diagram



10.3.6 Programming Guide

If the WUC source is from GPIO port, the firmware should not enable the corresponding channel when this GPIO is not in alternate function.

Figure 10-17. Program Flow Chart for WUC



10.4 EC Clock and Power Management Controller (ECPM)

10.4.1 Overview

The EC Clock and Power Management module provide the EC clock control and power management.

10.4.2 Features

- Supports programmable EC clock frequency
- Supported by module power-down mode control
- Supports PLL power-down when 8032 enters a Sleep mode

10.4.3 EC Interface Registers

The clock generation and power management registers are listed below. The base address is 1E00h.

Table 10-11. EC View Register Map, ECPM

7	0	Offset
	Reserved	00h
	Clock Gating Control 1 (CGCTRL1R)	01h
	Clock Gating Control 2 (CGCTRL2R)	02h
	Clock Gating Control 3 (CGCTRL3R)	05h
	PLL Control (PLLCTRL)	03h
	PLL Frequency (PLLREQR)	06h
	PLL Clock Source Status (PLLCSS)	08h

10.4.3.1 Clock Gating Control 1 Register (CGCTRL1R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	0b	Reserved
6	R/W	0b	ETWD Clock Gating (ETWDCG) 0: Operation 1: Clock to this module is gated
5	R/W	0b	SMB Clock Gating (SMBCG) 0: Operation 1: Clock to this module is gated
4	R/W	0b	Keyboard Scan Clock Gating (KBSCG) 0: Operation 1: Clock to this module is gated
3	R/W	0b	Reserved
2	R/W	0b	PWM/TMR Clock Gating (PWMCG) 0: Operation 1: Clock to this module is gated
1-0	R/W	00b	Reserved

10.4.3.2 Clock Gating Control 2 Register (CGCTRL2R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 02h

Bit	R/W	Default	Description
7-4	-	-	Reserved
3	R/W	0b	PMC Clock Gating (PMCCG) 0: Operation 1: Clock to this module is gated
2-1	R/W	00b	Reserved
0	R/W	0b	SMFI Clock Gating (SMFICG) 0: Operation 1: Clock to this module is gated

10.4.3.3 Clock Gating Control 3 Register (CGCTRL3R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 05h

Bit	R/W	Default	Description
7	W	0b	Reserved
6	W	1b	Reserved Always write 1 to this bit.
5-4	-	-	Reserved
3	-	-	Reserved
2	-	-	Reserved
1	-	-	Reserved
0	R/W	1b	DBGR Clock Gating (DBGRCG) 0: Operation 1: Clock to this module is gated.

10.4.3.4 PLL Control (PLLCTRL)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 03h

Bit	R/W	Default	Description
7-1	-	-	Reserved
0	R/W	1b	PLL Power Down Control (PPDC) 0: PLL will not be powered down by software until VSTBY is not supplied. Setting PD bit in PCON will enter an EC Doze mode. 1: PLL will be powered down after setting PD bit in PCON and enter an EC power-down mode.

10.4.3.5 PLL Frequency(PLLREQR)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 06h

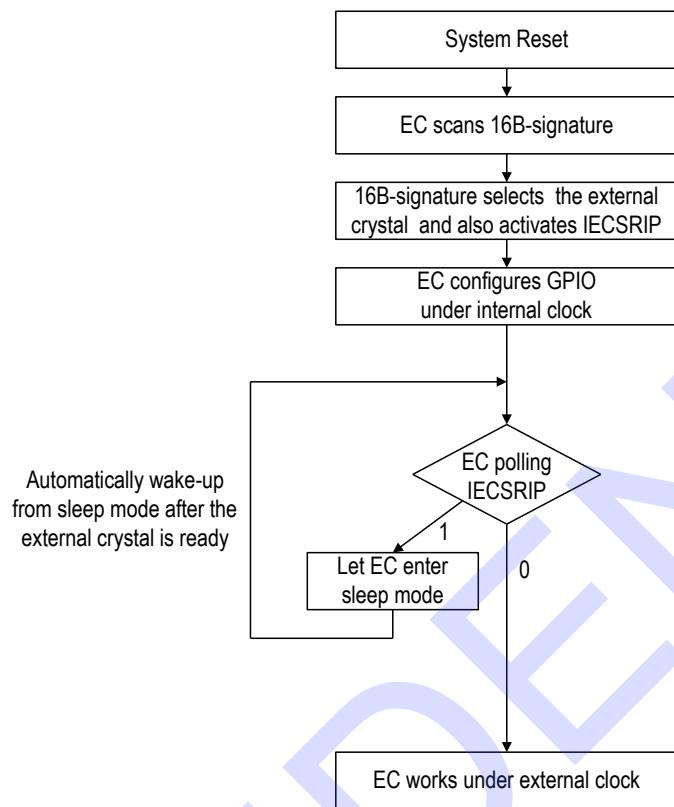
Bit	R/W	Default	Description
7-4	-	-	Reserved
3-0	R/W	0011b	<p>PLL Frequency(PLLREQ)</p> <p>0011b: Select 32.3MHz as PLL frequency. 0101b: Select 48.0MHz as PLL frequency. 0111b: Select 64.5MHz as PLL frequency. Otherwise: Reserved</p> <p>Read returns the current PLL frequency setting. Writing to this register doesn't change PLL frequency immediately until wakeup from the Sleep mode. Refer to section 10.1.10.5 Code Snippet of Changing PLL Frequency on page 275. SCEMINHW field in FLHCTRL2R register may be required before the PLL frequency is changed.</p>

10.4.3.6 PLL Clock Source Status (PLLCSS)

Address Offset: 08h

Bit	R/W	Default	Description
7	R	0b	<p>PLL Clock Source (PLLCSS)</p> <p>0b: PLL currently sources the reference clock from internal clock generator. 1b: PLL currently sources the reference clock from external crystal via CK32K and CK32KE.</p>
6-1	-	-	Reserved
0	R	0b	<p>Internal-to-External Clock Switching Request Is Postponing (IECSRIP)</p> <p>The EC scan the 16B-signature by internal clock and switch to external clock if 8th byte's bit 4 in 16B-signature is 0b. However, the switching time-point can be postponed by setting 8th byte's bit 6 in 16B-signature to 1 until sleep mode. It's useful to toggle GPIO in early time.</p> <p>0b: Otherwise. 1b: Internal-to-external clock switching is postponed. Let EC enter the sleep mode to finish this clock switching request.</p> <p>Refer to Figure 10-18. Program Flow Chart of IECSRIP Refer to section 9.11.3.20.1 16B-signature and Implicit/Explicit EC Code Base Address on page 176.</p>

Figure 10-18. Program Flow Chart of IECSRIP



10.5 External Timer and External Watchdog (ETWD)

10.5.1 Overview

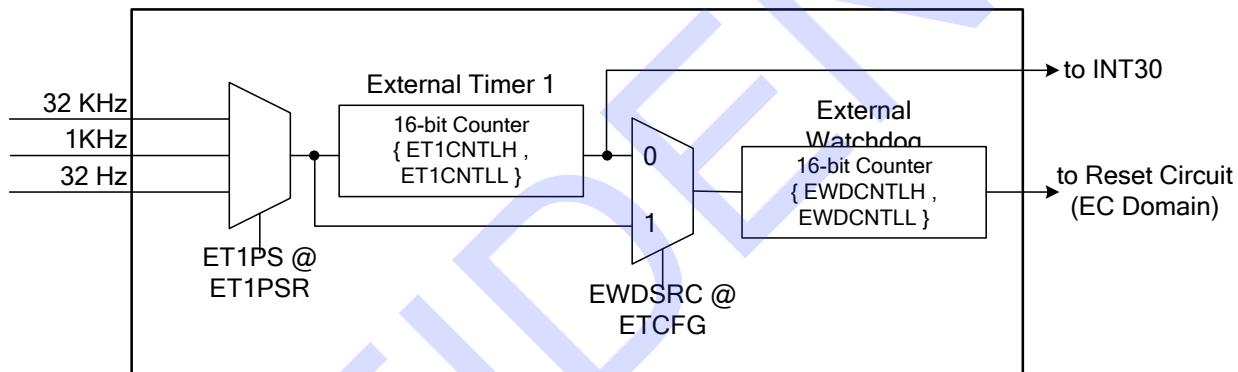
Besides the internal timer 0, 1, 2 and WDT inside the 8032, there is External Timer 1 with WDT outside the 8032. External Timer 1 with WDT is based on 30 k Clock and still works when EC is in Idle/Doze/Sleep mode. The external timer is recommended to replace internal timer for periodical wakeup task.

External Timer 1 with WDT has less power consumption than internal Timer/WDT due to the low frequency.

10.5.2 Features

- 32 kHz, 1kHz and 32 Hz prescaler for External Timer 1
- 16-bit count-down External Timer 1
- 16-bit count-down External WDT

Figure 10-19. Simplified Diagram



10.5.3 Functional Description

10.5.3.1 External Timer Operation

The External Timer 1 is a 16-bit counter down timer. Its clock source is based on 32 k Clock and can be selected by a prescaler defined at ET1PS field in ET1PSR register.

The count number of External Timer 1 is defined in ET1CNTLH and ET1CNTLL registers. External Timer 1 is stopped after reset and started after writing data to ET1CNTLL register and never stops until reset. It asserts an interrupt to INTC (INT30 for External Timer 1) when it counts to zero every time.

The External Timer 1 re-starts when

- it counts to zero periodically.
- data is written to ET1CNTLL register.
- 1 is written to ET1RST bit in ETWCTRL register.

External Timer 1 asserts periodical interrupt to EC 8032 via INT30 of INTC.

10.5.3.2 External WDT Operation

External WDT is a 16-bit counter down timer. Its clock source is either External Timer 1 output or the same clock source of External Timer 1, and it is controlled by EWDSRC bit in ETWCFG register.

The count number is defined in EWDCNTLH and EWDCTLL registers. External WDT is stopped after reset and started after writing data to EWDCTLL register and can be stopped by setting EWDSCE bit and EWDSCMS bit in ETWCTRL register. It asserts an External Watchdog Reset to EC domain when it counts to zero. External WDT requires starting External Timer 1 regardless of EWDSRC field in ETWCFG register. External WDT cannot be started until External Timer 1 is started.

The External WDT re-starts when it is touched by the firmware.

There are two following ways to touch (re-start) External WDT:

- Writing data to EWDCTLL register (if LEWDCNTL bit in ETWCFG register is not set)
- Writing 5Ch to EWDKEYR register, called key-match

External WDT asserts an External Watchdog Reset to EC domain when

- it counts to zero.
- data except 5Ch is written to EWDKEYR register.

10.5.4 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is 1F00h.

Table 10-12. EC View Register Map, ETWD

7	0	Offset
External Timer 1/WDT Configuration Register (ETWCFG)		01h
External Timer 1 Prescaler Register (ET1PSR)		02h
External Timer 1 Counter High Byte (ET1CNTLHR)		03h
External Timer 1 Counter Low Byte (ET1CNTLLR)		04h
External Timer/WDT Control Register (ETWCTRL)		05h
External WDT Counter High Byte (EWDCTLHR)		09h
External WDT Counter Low Byte (EWDCTLLR)		06h
External WDT Key Register (EWDKEYR)		07h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”

10.5.4.1 External Timer 1/WDT Configuration Register (ETWCFG)

Address Offset: 01h

Bit	R/W	Default	Description
7	-	0b	Reserved
6	-	0b	Reserved
5	R/W	0b	External WDT Key Enabled (EWDKEYEN) 1: Enable the key match function to touch the WDT. 0: Otherwise.
4	R/W	0b	External WDT Clock Source (EWDSRC) 1: Select clock after prescaler of the external timer 1. 0: Select clock from the output of the external timer 1.

Bit	R/W	Default	Description
3	R/W	0b	Lock EWDCNTLx Register (LEWDCNTL) 1: Writing to EWDCNTL is ignored. 0: Writing to EWDCNTL is allowed.
2	R/W	0b	Lock ET1CNTLx Registers (LET1CNTL) 1: Writing to ET1CNTLL is ignored. 0: Writing to ET1CNTLL is allowed.
1	R/W	0b	Lock ET1PS Register (LET1PS) 1: Writing to ET1PS is ignored. 0: Writing to ET1PS is allowed.
0	R/W	0b	Lock ETWCFG Register (LETWCFG) 1: Writing to ETWCFG itself is ignored, and this bit can't be cleared until reset. 0: Writing to ETWCFG itself is allowed.

10.5.4.2 External Timer 1 Prescaler Register (ET1PSR)

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	0h	Reserved
1-0	R/W	00b	External Timer 1 Prescaler Select (ET1PS) These bits control the clock input source to the external timer 1. 00b: 32 kHz 01b: 1kHz 10b: 32 Hz 11b: Reserved Note the prescaler will not output clock until data is written to ET1CNTLLR register.

10.5.4.3 External Timer 1 Counter High Byte (ET1CNTLHR)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	FFh	External Timer 1 Counter High Byte (ET1CNTLH) Define the count number of high byte of the 16-bit count-down timer.

10.5.4.4 External Timer 1 Counter Low Byte (ET1CNTLLR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	FFh	External Timer 1 Counter Low Byte (ET1CNTLL) Define the count number of low byte of the 16-bit count-down timer. The external timer 1 starts or re-starts after writing this register.

10.5.4.5 External Timer/WDT Control Register (ETWCTRL)

Address Offset: 05h

Bit	R/W	Default	Description
7-6	-	00b	Reserved
5	R/W	0b	External WDT Stop Count Enable (EWDSCEN) 1: External WDT is stopped counting. 0: Otherwise. This bit cannot be set until EWDSCMS bit is set to 1.
4	R/W	0b	External WDT Stop Count Mode Select (EWDSCMS) 1: External WDT can be stopped by setting EWDSCEN bit. 0: External WDT cannot be stopped. Writing data to this bit is ignored after writing data to EWDCNTLL register, and this bit cannot be cleared until being reset.
3-2	-	00b	Reserved
1	R	0b	External Timer 1 Terminal Count (ET1TC) 1: Indicates the external timer 1 has counted down to zero, and it is cleared after reading it. 0: Otherwise Writing to this bit is ignored.
0	W	-	External Timer 1 Reset (ET1RST) Writing 1 forces the external timer 1 to re-start. Writing 0 is ignored. Read always returns zero.

10.5.4.6 External WDT Counter High Byte (EWDCNTLHR)

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	External WDT Counter High Byte (EWDCNTL) Define the count number of high byte of the 16-bit count-down WDT.

10.5.4.7 External WDT Counter Low Byte (EWDCNTLLR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0Fh	External WDT Counter Low Byte (EWDCNTLL) Define the count number of 16-bit count-down WDT.

10.5.4.8 External WDT Key Register (EWDKEYR)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	W	-	External WDT Key (EWDKEY) External WDT is re-started (touched) if 5Ch is written to this register. Writing with other values causes an External Watchdog Reset. This function is enabled by EWDKEYEN bit. Read returns unpredictable value.

10.6 General Control (GCTRL)

10.6.1 Overview

This module controls EC function that doesn't belong to the specified module.

10.6.2 Features

- By module reset

10.6.3 Functional Description

Wait Next Clock Rising:

When writing 0 to WNCKR register, the R8032TT will be paused and wait for a low to high transition of the internal 60 kHz clock. This may be useful to get a delay.

For a loop that writing 0 to WNCKR register for N times, the delay value will be
 $(N-1) / 60 \text{ kHz}$ to $(N / 60 \text{ kHz})$

e.g.

Consecutively writing 0 to WNCKR register for 33 times get 0.5ms delay with $-2.3\% \sim +0.7\%$ tolerance.

Consecutively writing 0 to WNCKR register for 66 times get 1ms delay with $-0.8\% \sim +0.7\%$ tolerance.

Consecutively writing 0 to WNCKR register for 132 times get 2ms delay with $-0.05\% \sim +0.7\%$ tolerance.

10.6.4 EC Interface Registers

The following set of the registers is accessible only by EC. They are listed below and the base address is 2000h.

Table 10-13. EC View Register Map, GCTRL

7	0	Offset
Chip ID Byte 1 (ECHIPID1)		00h
Chip ID Byte 2 (ECHIPID2)		01h
Chip Version (ECHIPVER)		02h
Reserved		03h
Reserved		05h
Reset Status (RSTS)		06h
Reset Control 1 (RSTC1)		07h
Reset Control 2 (RSTC2)		08h
Reset Control 3 (RSTC3)		09h
Wait Next Clock Rising (WNCKR)		0Bh
Special Control 1 (SPCTRL1)		0Dh
Generate IRQ (GENIRQ)		0Fh
Reset Control 4 (RSTC4)		11h
Special Control 2 (SPCTRL2)		12h
Port I2EC High-Byte Register (PI2ECH)		14h
Port I2EC Low-Byte Register (PI2ECL)		15h
Special Control 3 (SPCTRL3)		16h

For a summary of the abbreviations used for the register type, see "Register Abbreviations and Access Rules".

10.6.4.1 Chip ID Byte 1 (ECHIPID1)

The content of this EC side register is the same as that of the CHIPID1 register in the host side.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R	87h	Chip ID Byte 1 (ECHIPID1) This register contains the Chip ID byte 1.

10.6.4.2 Chip ID Byte 2 (ECHIPID2)

The content of this EC side register is the same as that of the CHIPID2 register in the host side.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R	33h	Chip ID Byte 2 (ECHIPID2) This register contains the Chip ID byte 2.

10.6.4.3 Chip Version (ECHIPVER)

This register contains revision ID of this chip.

The content of this EC side register is the same as that of the CHIPVER register in the host side.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R	03h	Chip Version (ECHIPVER)

10.6.4.4 Reset Status (RSTS)

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R/W	10b	VCC Detector Option (VCCDO) 10b: The VCC power status is detected by internal circuit. 00b: The VCC power status is treated as power-off. 01b: The VCC power status is treated as power-on. otherwise: reserved No matter which option is selected, the VCC power status is always recognized as power off if LPCPD# input is level low. The VCC power status is used as internal “power good” signal to prevent current leakage while VCC is off. Intentionally toggling this field when VCC is supplied can reset logic VCC domain in EC.
5	-	-	Reserved
4	-	-	Reserved

Bit	R/W	Default	Description
3	R/W	1b	Host Global Reset (HGRST) 0: The reset source of PNPCFG is RSTPNP bit in RSTCH register and WRST#. 1: The reset source of PNPCFG are RSTPNP bit in RSTCH register, internal VCC status controlled by VCCDO bit in RSTS register, LPCPD#, LPCRST# and WRST#.
2	R/W	1b	Global Reset (GRST) This bit controls whether to reset EC domain globally during Internal/External Watchdog Reset. 0: Only reset 8032, and each module can be reset by RSTCn register 1: Reset all the EC domain
1-0	R	-	Last Reset Source (LRS) If this register field is used, it is required to read this field once and only one time after reset. 00b, 01b: VSTBY Power-Up Reset or Warm Reset 10b: Internal Watchdog Reset 11b: External Watchdog Reset

10.6.4.5 Reset Control 1 (RSTC1)

Write 1 to the selected bit(s) to possibly reset corresponding module(s). Refer to VCCDO field in RSTS register to reset logic in VCC domain in EC.

Address Offset: 07h

Bit	R/W	Default	Description
7	W	-	Reset SMFI (RSMFI)
6	W	-	Reset INTC (RINTC)
5-3	-	-	Reserved
2	W	-	Reset PMC (RPMC)
1-0	-	-	Reserved

10.6.4.6 Reset Control 2 (RSTC2)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 08h

Bit	R/W	Default	Description
7-6	-	-	Reserved
5	W	-	Reset WUC (RWUC)
4-0	-	-	Reserved

10.6.4.7 Reset Control 3 (RSTC3)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 09h

Bit	R/W	Default	Description
7-3	-	-	Reserved
2	W	-	Reset SMBus Channel C (RSMBC)
1	W	-	Reset SMBus Channel B (RSMBB)
0	-	-	Reset SMBus Channel B (RSMBB) To reset the logic of SMBus shared with all channels, write 1111b to bit 3-0 at the same time and writing 0111b is reserved.

10.6.4.8 Wait Next Clock Rising (WNCKR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	W	-	Wait Next 65K Rising (WN65K) Writing 00h to this register and the R8032TT program counter will be paused until the next low to high transition of 65.536 kHz clock. Writing other values is reserved.

10.6.4.9 Special Control 1 (SPCTRL1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7	R/W	0b	P80L Enable (P80LEN) This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. Refer to section 10.7.3.1 P80L on page 317. 1b: Enable P80L function. 0b: Otherwise
6	R/W	0b	Accept Port 80h Cycle (ACP80) This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. Refer to section Refer to section 10.7.3.1 P80L on page 317. 1b: The host LPC I/O cycle with address 80h will be accepted by EC. If P80LEN is set, enabling this bit to guarantee LPC I/O port 80h data can be latched even though there is a transaction cycle to BRAM. 0b: Otherwise
5-4	-	-	Reserved
3	R/W	0b	KRST# Control This register is one source of KRST#. If the bit is 1, KRST# will be low. If the bit is 0, the value of KRST# depends on other sources. 1b: Set KRST# low 0b: Disable

Bit	R/W	Default	Description
2	R/W	0b	GA20 Control This register is one source of GA20. If the bit is 1, GA20 will be high. If the bit is 0, the value of GA20 depends on other sources. 1b: Set GA20 high 0b: Disable
1-0	R/W	00b	I2EC Control (I2ECCTRL) 00b: I2EC is disabled. 10b: I2EC is read-only. 11b: I2EC is read-write. 01b: Reserved Refer to section 10.8.3.6 EC Memory Snoop (ECMS) on page 322.

10.6.4.10 Generate IRQ (GENIRQ)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-4	-	-	Reserved
3-0	W	-	Generate IRQ Number (GENIRQNUM) Writing to this field will generate SERIRQ with a specified number. This field is valid only when it is between 1-12 or 14-15.

10.6.4.11 Special Control 2 (SPCTRL2)

Address Offset: 12h

Bit	R/W	Default	Description
7	-	-	Reserved
6	-	-	Reserved
5	R/W	0b	LRESET Gating Write Data 0b: Enable LRESET gating 1b: Disable LRESET gating
4	R/W	0b	uC UART1 Enable (uC_UART1_EN) 1b: Set QFP:Pin-124 (LQFP:Pin:-121), and QFP:Pin-125 (LQFP:Pin:122) to uC UART function. 0b: Disable uC UART1. Bit 4 and bit 3 can't be set to 1 at the same time.
3	R/W	0b	uC UART0 Enable (uC_UART0_EN) 1b: Set QFP:Pin-66 (LQFP:Pin-63), and QFP:Pin-70 (LQFP:Pin:67) to uC UART function. 0b: Disable uC UART0.
2	R/W	0b	Reserved
1	R/W	0b	Reserved
0	R/W	0b	Port I2EC Enable (PI2ECEN) 1b: Decode I2EC cycles via address I2EC_XADDR. 0b: Otherwise Refer to section 10.8.3.6 EC Memory Snoop (ECMS) on page 322.

10.6.4.12 Special Control 3 (SPCTRL3)

Address Offset: 16h

Bit	R/W	Default	Description
7	R/W	0b	Forwarded as FSPI Inst. 86h/87h (F8687) 0b: Forwarded as SPI instruction 86h on FSPI. 1b: Forwarded as SPI instruction 87h on FSPI.
6-4	-	-	Reserved
3	-	-	Reserved
2	R/W	1b	I/O Port 80h to FSPI Enable (P80FEN) 1b: Written byte data on LPC I/O port 80h will be forwarded to FSPI. If this bit is set, ACP80 bit in SPCTRL1 register must be set to let EC decode I/O port 80h. The forwarded instruction plus data will be “86h/87h 00h XXh”, where XXh is the written byte. 0b: Otherwise
1	R/W	0b	I/O Port 90h to FSPI Enable (P90FEN) 1b: Written byte data on LPC I/O port 90h will be forwarded to FSPI. If this bit is set, EC will decode I/O port 90h. The forwarded instruction plus data will be “86h/87h 90h XXh”, where XXh is the written byte. 0b: Otherwise
0	R/W	0b	I/O Port 84h to FSPI Enable (P84FEN) 1b: Written word data on LPC I/O port 84h will be forwarded to FSPI. If this bit is set, EC will decode I/O port 84h/85h. The forwarded instruction plus data will be “86h/87h YYh XXh”, where (YYh*100h+XXh) is the written word. 0b: Otherwise

10.6.4.13 Port I2EC High-Byte Register (PI2ECH)

LPC I/O port with address equal to PORT_I2EC[15:0] + 1: I2EC_XADDR_H

LPC I/O port with address equal to PORT_I2EC[15:0] + 2: I2EC_XADDR_L

LPC I/O port with address equal to PORT_I2EC[15:0] + 3: I2EC_XDATA

EC only accepts the LPC I/O cycle with PORT_I2EC address if PI2ECEN bit in SPCTRL2 register is set.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/W	03h	Port I2EC[15:8] (PORT_I2EC[15:8]) High-byte address of I/O port for I2EC purpose. Bit 7-4 (PORT_I2EC[15:12]) are forced to 0000b and can't be written.

10.6.4.14 Port I2EC Low-Byte Register (PI2ECL)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	80h	Port I2EC[7:0] (PORT_I2EC[7:0]) Low-byte address of I/O port for I2EC purpose. Bit 1-0 (PORT_I2EC[1:0]) are forced to 00b and can't be written.

10.7 BRAM

10.7.1 Overview

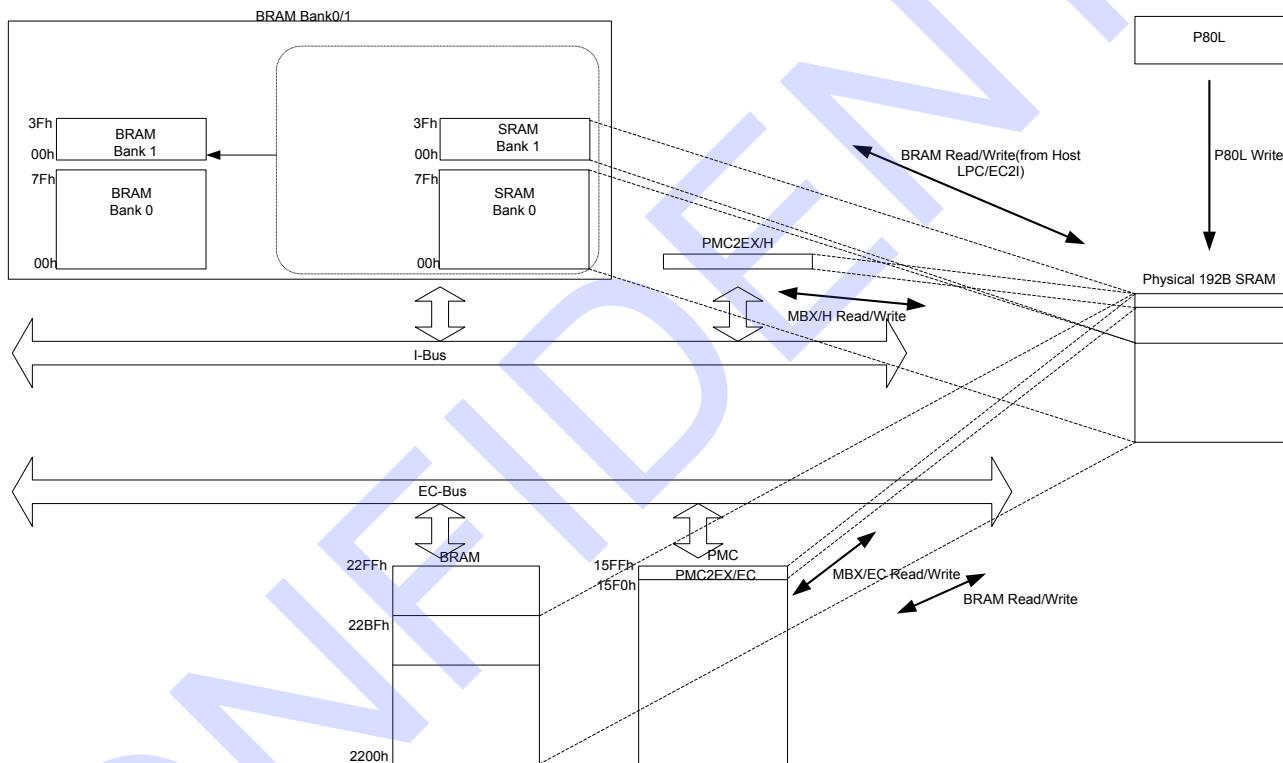
This module provides 192 bytes of battery-backed memory area and power-switching circuit.

10.7.2 Features

- 192 bytes of battery-backed SRAM mapped into the host and EC side.
- Power-switching circui.

10.7.3 Functional Description

Figure 10-20. BRAM Mapping Diagram



10.7.3.1 P80L

If this function is enabled by P80LEN bit in SPCTRL1 register, LPC I/O port 80h written data will be latched into SRAM of BRAM bank 1.

The data may fail to latch data if there is a transaction cycle to BRAM in the EC side at the same time unless ACP80 bit in SPCTRL1 register is set, which guarantees written data is latched into SRAM by issuing Long Wait Sync on host LPC bus.

The destination address range in BRAM Bank 1 is determined by P80LB, P80LE register in the host side, which constructs a queue.

P80LB: It indicates the start index of the queue. Readable/Writable.
P80LE: It indicates the end index of the queue. Readable/Writable.
P80LC: It indicates the current index of the queue. Read-only.
These three registers are supplied by VSTBY power and not affected by VCC status

Whenever written data is latched, P80LC increases one. If it reaches P80LE (queue end), it will wrap back to P80LB (queue begin).

10.7.4 Host Interface Registers

The registers of BRAM can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.

The BRAM resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The BRAM logical device number is 10h (LDN).

These registers are listed below.

Table 10-14. Host View Register Map, BRAM

7	0	Offset
		Legacy
	70h	70h
	71h	Legacy
	72h	Legacy
	73h	Legacy

Legacy 70h represents (I/O Port Base Address 0) + (Offset 0h)

Legacy 71h represents (I/O Port Base Address 0) + (Offset 1h)

Legacy 72h represents (I/O Port Base Address 1) + (Offset 0h)

Legacy 73h represents (I/O Port Base Address 1) + (Offset 1h)

Table 10-15. Host View Register Map via Index-Data I/O Pair, BRAM Bank 0

7	0	Offset
		00h

	7Fh	SBT0

Table 10-16. Host View Register Map via Index-Data I/O Pair, BRAM Bank 1

7	0	Offset
		00h
	...	3Fh

10.7.5 EC Interface Registers

The base address is 2200h.

Table 10-17. EC View Register Map

7	0	Offset
SRAM Byte n Registers (SBT0)	80h	...
...	...	
SRAM Byte n Registers (SBT63)	BFh	

10.7.5.1 SRAM Byte n Registers (SBTn, n= 0-191).

Address Offset: 80h – BFh for byte 0 – byte 191

Bit	R/W	Default	Description
7-0	R/W	-	SRAM Data (SD) When data is written to this register, it will be saved in the corresponding memory space. When this register is read, the contents of the corresponding memory space can be read.

10.8 Debugger (DBGR)

10.8.1 Overview

This EC side module provides three 18-bit 8032 ROM trigger addresses and issues an INT0#, In-system Programming (ISP) and In-system Debugging (ISD).

DBGR can be performed by one of the two interfaces below.

- DBGR/EPP
- DBGR/SMB

Both ISP and ISD can be performed by either DBGR/EPP or DBGR/SMB.

10.8.2 Features

- 3 trigger addresses
- ISP and ISD
- EC Memory Snoop (ECMS = I2EC)

10.8.3 Functional Description

10.8.3.1 ROM Address Match Interrupt

The trigger address, where an instruction is constructed by one, two or three bytes, has to be the first byte of each instruction.

INT0RM is set when the trigger address matches the 8032 program counter except that the trigger address is equal to zero.

If Parallel Port cable is detected by internal hardware strap, this function is disabled.

Note that DBGR module is clock-gated in default and cannot work until 0 is written to DBGRCG bit in the CGCTRL3R register.

10.8.3.2 DBGR/EPP

IT8733 supports IEEE 1284 parallel port interface to allow in-system programming (ISP) or in-system debugging (ISD) regardless of running firmware code.

If Parallel Port cable is detected by internal hardware strap, the following functions will be disabled.

1. ROM Address Match Interrupt
2. Internal/External Watchdog

The DBGR/EPP debug mode takes place when VSTBY is supplied (other types of power are don't-care) and both EC chip and the flash are soldered on PCB.

It can be disabled by OVRPPK bit in the KSICTRLR register.

10.8.3.3 DBGR/SMBus

Debug Mode through SMBus Slave Interface

The SMBus slave would enter Debug Mode when it detects a specific waveform from SMCLKx/SMDATx line, as shown in Figure 1. It can be disabled by OVRSMDBG bit in the Slave Interface Select Register.

When Debug Mode through SMBus slave interface is enabled, the external device can use a specific protocol to communicate with the SMBus slave, and the slave would decode this protocol to access D2EC utility. The specific protocol is described as below:

Address Read Cycle/Data Read Cycle must be decoded to SMBus Receive Byte Command.

Address Write Cycle/Data Write Cycle must be decoded to SMBus Send Byte Command.

(The Receive Byte Command / Send Byte Command protocol is shown in Figure 2.)

SMBus Slave Address for Address Read/Write Cycle: 1011010b + (R/W bit)

SMBus Slave Address for Data Read/Write Cycle: 0110101b + (R/W bit)

Data Byte in the command is an 8-bit data according to the desired cycle.

SMBus Specific Waveform for Entering Debug Mode



◆ How to match:

1. The Frequency of SMCLK and SMDAT equals to 120KHz.
2. The Duty Cycle of SMCLK and SMDAT equals to 50%.
3. The Phase Difference between SMCLK and SMDAT equals to 180.
4. Match correct waveform Continuously up to 25 periods.

SMBus Receive Byte/Send Byte Command Protocol (Referred to SMBus Spec. 2.0)

Receive Byte Command

1	7	1	1	8	1	1
START	Slave Address	Rd	ACK	Data Byte	NACK	STOP

Send Byte Command

1	7	1	1	8	1	1
START	Slave Address	Wr	ACK	Data Byte	ACK	STOP

Refer to section 9.12 SMBus Interface (SMB).

It can be disabled by OVRSMDBG bit in SLVISELR register.

10.8.3.4 In-system Programming Operation

It provides flash read and program function.

10.8.3.5 In-system Debugging Operation

It's performed by the utility provided by ITE and contains two features below.

1. D2EC described in section 10.8.3.6 EC Memory Snoop (ECMS).
2. Breakpoints, stepping, etc. and reset functions supported.

10.8.3.6 EC Memory Snoop (ECMS)

ECMS is available through one of the two ways:

1. I2EC (I-bus to EC Memory)

Local machine snoops EC memory through the LPC I/O cycle.

Here are two registers to provide the way to perform the I2EC access.

- I2EC_XADDR_H/ I2EC_XADDR_L/I2EC_XDATA register, with programmable address and defined in section 10.6.4.13 Port I2EC High-Byte Register (PI2ECH) on page 316.

Figure 10-21. I2EC through 2Eh/2Fh I/O Port Operation Flow

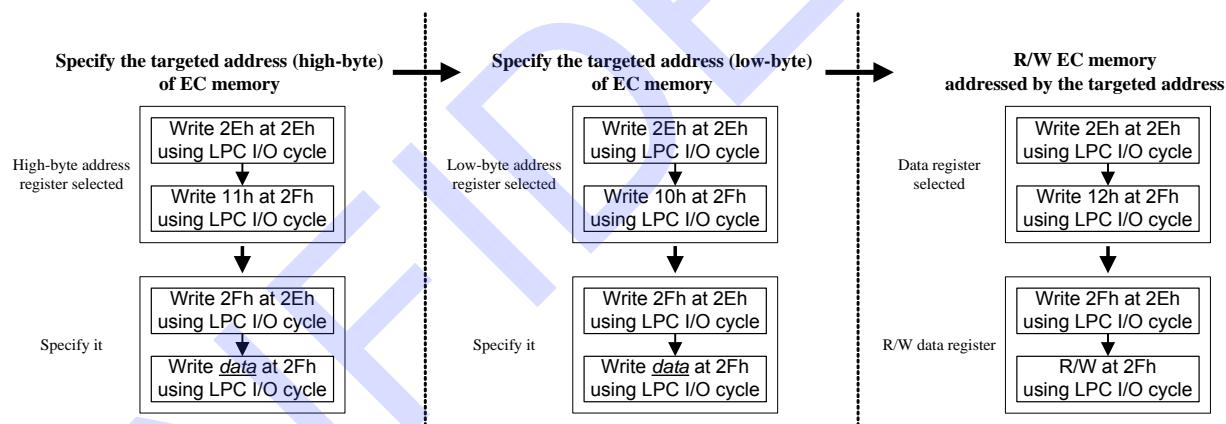
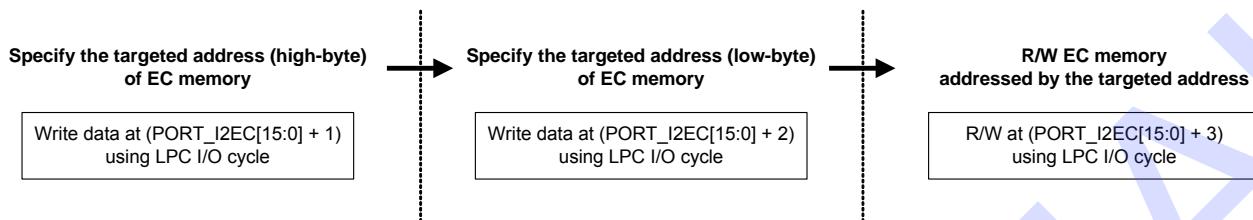


Figure 10-22. I2EC through Dedicated I/O Port Operation Flow



2. D2EC (DBG to EC Memory)

Remote machine snoops EC memory through EPP cycle.

I2EC/D2EC utility is provided by ITE.

I2EC is not enabled until its controlled register in the EC side register is written.

I2EC can be configured as read-only for all targets.

If D2EC is enabled by the utility, I2EC will be disabled until reset.

I2EC/D2EC will not affect any register content of read-clear registers.

The writing action of I2EC/D2EC to F/F based register is okay; however, the result of writing to non-F/F based register is not expected. Such registers may be write-clear, or writing to start internal state-machine, etc.

If D2EC is enabled, PLL will not be power-down in the Sleep mode.

Table 10-18. I2EC/D2EC Accessible Target

	I2EC	D2EC
uC SFR (except Acc reg.)	R	R
uC SFR - Acc reg.	R	R/W
uC External Memory (except DMM)	R/W controlled by I2ECCTRL field in SPCTRL1 reg.	R/W
uC External Memory – DMM	Not Accessible	R

Note: DMM denotes double-mapping module.

10.8.3.7 Other Debug Topics

Here some debug features not covered in this DBGR section but may be useful for users.

1. Section 10.7.3.1 P80L on page 317
2. Section 9.11.3.18 LPC_IO-to-FSPI on page 175.

10.8.4 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is 2500h.

Table 10-19. EC View Register Map, DBGR

7	0	Offset
		10h
		11h
		12h
		13h
		14h
		15h
		16h
		17h
		18h

Trigger 1 Address Low Byte Register (BKA1L)
Trigger 1 Address Middle Byte Register (BKA1M)
Trigger 1 Address High Byte Register (BKA1H)
Trigger 2 Address Low Byte Register (BKA2L)
Trigger 2 Address Middle Byte Register (BKA2M)
Trigger 2 Address High Byte Register (BKA2H)
Trigger 3 Address Low Byte Register (BKA3L)
Trigger 3 Address Middle Byte Register (BKA3M)
Trigger 3 Address High Byte Register (BKA3H)

For a summary of the abbreviations used for the register type, see "Register Abbreviations and Access Rules".

10.8.4.1 Trigger 1 Address Low Byte Register (BKA1L)

Address Offset: 10h

Bit	R/W	Default	Description
7-0	W	00h	Trigger 1 Address (BK1A7-0)

10.8.4.2 Trigger 1 Address Middle Byte Register (BKA1M)

Address Offset: 11h

Bit	R/W	Default	Description
7-0	W	00h	Trigger 1 Address (BK1A15-8)

10.8.4.3 Trigger 1 Address High Byte Register (BKA1H)

Address Offset: 12h

Bit	R/W	Default	Description
7-2	-	00h	Reserved
1-0	W	00b	Trigger 1 Address (BK1A17-16)

10.8.4.4 Trigger 2 Address Low Byte Register (BKA2L)

Address Offset: 13h

Bit	R/W	Default	Description
7-0	W	00h	Trigger 2 Address (BK2A7-0)

10.8.4.5 Trigger 2 Address Middle Byte Register (BKA2M)

Address Offset: 14h

Bit	R/W	Default	Description
7-0	W	00h	Trigger 2 Address (BK2A15-8)

10.8.4.6 Trigger 2 Address High Byte Register (BKA2H)

Address Offset: 15h

Bit	R/W	Default	Description
7-2	-	00h	Reserved
1-0	W	00b	Trigger 2 Address (BK2A17-16)

10.8.4.7 Trigger 3 Address Low Byte Register (BKA3L)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	W	00h	Trigger 3 Address (BK3A7-0)

10.8.4.8 Trigger 3 Address Middle Byte Register (BKA3M)

Address Offset: 17h

Bit	R/W	Default	Description
7-0	W	00h	Trigger 3 Address (BK3A15-8)

10.8.4.9 Trigger 3 Address High Byte Register (BKA3H)

Address Offset: 18h

Bit	R/W	Default	Description
7-2	-	00h	Reserved
1-0	W	00b	Trigger 3 Address (BK3A17-16)

10.9 Keyboard Matrix Scan Controller and Software KBC for Scan Code (KBS/SWKBC)

10.9.1 Overview

The module provides control for keyboard matrix scan and software KBC for Scan Code.

10.9.2 Features

- Supports 6 x scan output
- Supports 2 x scan input
- Supports Schmitt trigger input pin
- Supports programmable pull-up on all output/input pins
- Supports one interrupt (connected to INT11 of INTC) for any KSI inputs to go low to wake up the system
- Supports two standard registers for programming: KBC Command/Data Register and Status Register
- Automatically generates interrupts to the host side and EC side when KBC status changed

10.9.3 Functional Description

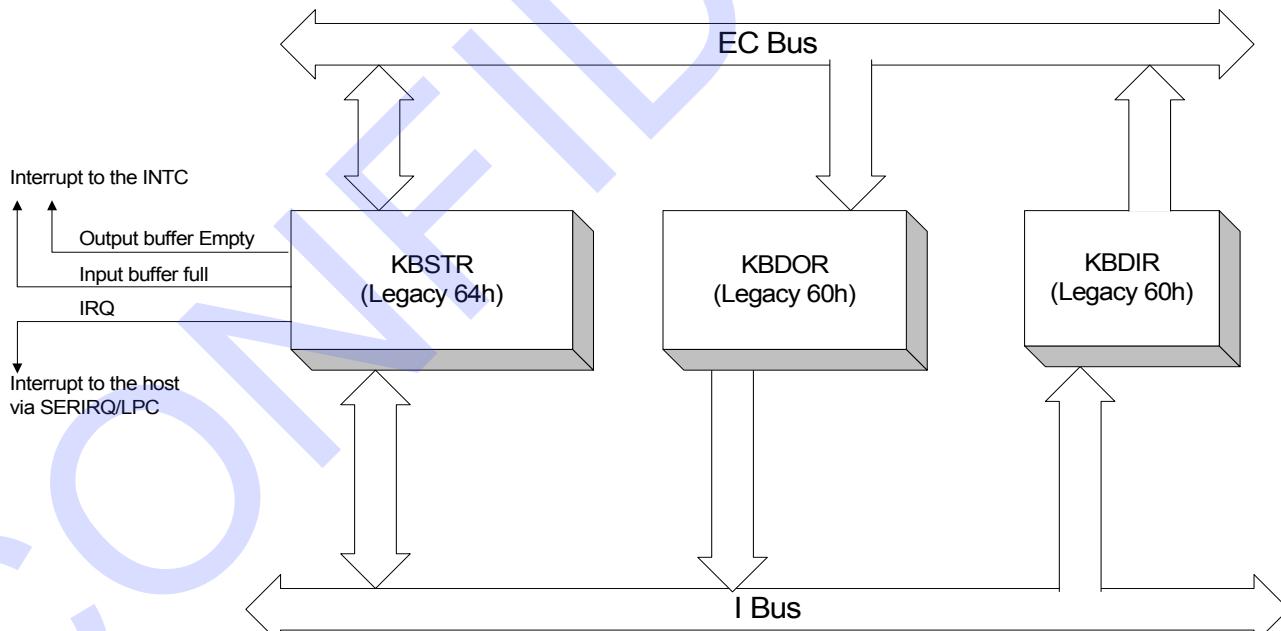
- **KSI/KSO Used as Keyboard Matrix**

Normal usage.

- **Software KBC**

After writing 1 to SCSTART and SCEN = 1, KBC will change to Software KBC and pull KCLK/MCLK low. This keyboard controller is compatible with the legacy 8042 interface keyboard controller.

Figure 10-23. KBC Host Interface Block Diagram



Status

The host processor can read the status of KBC from the KBC Status Register. The internal 8032 can read the status of KBC from the KBC Host Interface Keyboard Status Register.

Host Write Data to KBC Interface

When data was written to address 60h or 64h (programmable), the IBF bit in the KBC Status Register is set and A2 bit in the KBC Status Register indicates 8032 whose address was written. When data was written to address 60h, A2 bit is 0. When data was written to address 64h, A2 bit is 1.

EC 8032 can identify that the input buffer is full by either polling IBF bit in the Status register or detecting an interrupt (INT24) if the interrupt is enabled. EC 8032 can read the data from the KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR), and the IBF bit in the Status Register is cleared.

EC 8032 Write Data to KBC Interface

EC 8032 can write data to the KBC when it needs to send data to the host. When EC 8032 writes data to the KBC Host Interface Keyboard Data Output Register (KBHKDOR), the OBF bit in the Status Register is set. If the IRQ1 interrupt is enabled, the IRQ1 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. The host can read the Data Output Register when it detects the Output Buffer Full condition. When the Output Buffer Empty interrupt to INTC (INT2) is enabled, the interrupt signal is set high if the output buffer is empty.

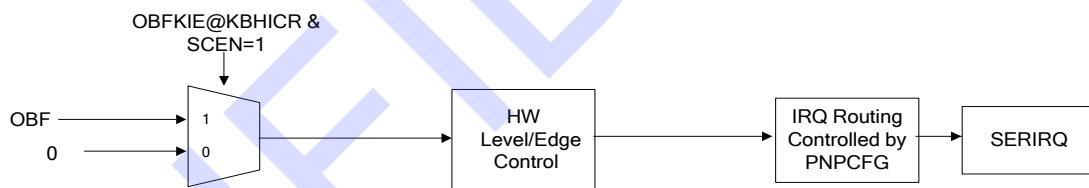
Interrupts

There are two interrupts (Input Buffer Full Interrupt and Output Buffer Empty) connected to the INTC.

There is one interrupt (IRQ1) connected to the host side (SERIRQ).

The IRQ numbers of KBC are programmable and use IRQ1 as abbreviations in this section.

Figure 10-24. IRQ Control in SWKBC Module



10.9.4 Host Interface Registers

The registers of SWKBC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the host interface registers, which can be accessed by the host processor only.

The KBC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. For compatibility issue, the two I/O Port Base Addresses of KBC/Keyboard are suggested to configure at 60h and 64h.

Here are the host interface registers:

Table 10-20. Host View Register Map, KBC

7	0	Offset
	KBC Data Input Register (KBDIR)	Legacy 60h
	KBC Data Output Register (KBDOR)	Legacy 60h
	KBC Command Register (KBCMDR)	Legacy 64h
	KBC Status Register (KBSTR)	Legacy 64h

Legacy 60h represents (I/O Port Base Address 0) + (Offset 0h).

Legacy 64h represents (I/O Port Base Address 1) + (Offset 0h).

10.9.4.1 KBC Data Input Register (KBDIR)

When the host processor is writing data to this register, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be cleared. If the IBFCIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the write action will cause one interrupt to 8032 processor via INT24 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	W	-	KBC Data Input (KBDI) The data is used to output for Keyboard.

10.9.4.2 KBC Data Output Register (KBDOR)

When the host processor is reading data from this register, the OBF bit in KBC Status Register (KBSTR) will be cleared. The reading access will also clear the interrupt for the host processor. If the OBECIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the reading action will cause one interrupt to 8032 processor via INT2 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	R	-	KBC Data Output (KBDO) The data comes from the Keyboard.

10.9.4.3 KBC Command Register (KBCMDR)

When data is written to this register, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be set.

Address Offset: 00h for I/O Port Base Address 1, Legacy 64h

Bit	R/W	Default	Description
7-0	W	-	KBC Command (KBCMD) The command data is used to output for Keyboard.

10.9.4.4 KBC Status Register (KBSTR)

The host processor uses the register to monitor the status of KBC. The same information is similar to the KBC Host Interface Keyboard Status Register (KBHISR). It is used by the internal 8032.

Address Offset: 01h for I/O Port Base Address 0, Legacy 64h

Bit	R/W	Default	Description
7-4	R	0h	Programming Data 3-0 (PD3-0) The data is used by the 8032 firmware for the general-purpose setting.
3	R	0b	A2 Address (A2) The bit is used to keep the A2 address information of the write operation while the host processor accesses the KBC.
2	R	0b	Programming Data II (PDII) The function of this bit is the same as that of the PD3-0.
1	R	0b	Input Buffer Full (IBF) This bit is set when the host processor is writing data to KBDIR or KBCMDR whereas cleared when data is read from KBDIR or KBCMDR by the 8032 firmware.
0	R	0b	Output Buffer Full (OBF) The bit is set when the EC 8032 is writing data to KBDOR whereas cleared when data is read from KBDOR by the host processor.

10.9.5 EC Interface Registers

The keyboard matrix scan registers are listed below. The base address is 1D00h.

Table 10-21. EC View Register Map, KB Scan

7	0	Offset
Keyboard Scan Out [5:0] (KS0R)		00h
Keyboard Scan Out Control (KS0CTRL)		01h
Keyboard Scan In [1:0] (KS1R)		02h
Keyboard Scan In Control (KS1CTRLR)		03h
Scan Code Control Register (SCCTRL)		04h
KBC Host Interface Control Register (KBHICR)		07h
KBC Host Interface Keyboard Status Register (KBHISR)		08h
KBC Host Interface Keyboard Data Output Register (KBHIKDOR)		09h
KBC Host Interface Keyboard Data Input Register (KBHIDIR)		0Ah

10.9.5.1 Keyboard Scan Out Data Register (KSOR)

Address Offset: 00h

Bit	R/W	Default	Description
7-6	-	-	Reserved
5-0	R/W	00h	Keyboard Scan Out Low Data [5:0] (KSOL) This is the 6-bit keyboard scan output register which controls the KSO[5:0] pins.

10.9.5.2 Keyboard Scan Out Control Register (KSOCTRL)

Address Offset: 01h

Bit	R/W	Default	Description
7-6	-	-	Reserved
5-3	-	-	Reserved
2	R/W	0b	KSO Pull Up (KSOPU) Setting this bit to 1 enables the internal pull-up of the KSO[5:0] pins.
1	-	-	Reserved
0	R/W	0b	KSO Open Drain (KSOOD) Setting this bit to 1 enables the open-drain mode of the KSO[5:0] pins. Setting this bit to 0 selects the push-pull mode.

10.9.5.3 Keyboard Scan In Data Register (KSIR)

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	-	Reserved
1-0	R	00h	Keyboard Scan In High Data [1:0] (KSI) This is the 2-bit keyboard scan input register which shows the value of the KSI[1:0] pins.

10.9.5.4 Keyboard Scan In Control Register (KSICTRLR)

Address Offset: 03h

Bit	R/W	Default	Description
7-5	-	000b	Reserved
4	-	-	Reserved
3	-	-	Reserved
2	R/W	0b	KSI Pull Up (KSIPU) Setting this bit to 1 enables the internal pull-up of the KSI[1:0] pins.
1	-	-	Reserved
0	-	-	Reserved

10.9.5.5 Scan Code Control Register (SCCTRL)

Address Offset: 04h

Bit	R/W	Default	Description
7-2	-	-	Reserved
1	R/W	0b	Scan Code Start (SCSTART) 0: Scan code idle - 1: Scan code start Writing 1 to the bit will change KBC to Software KBC and pull KCLK and MCLK low to disable KB/MS.
0	R	0b	Scan Code Enable (SCEN) - The bit indicates whether Scan Code function is enabled or not, and the control bit is bit7 of index F7 with LDN 7.

10.9.5.6 KBS Pin Enable Control Register (KBSEN)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W -	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-120 / LQFP:Pin-117) 0: GP77 1: KSO5
6	R/W	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-119 / LQFP:Pin-116) 0: GP76 1: KSO4
5	R/W	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-118 / LQFP:Pin-115) 0: GP75 1: KSO3
4	R/W	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-117 / LQFP:Pin-114) 0: GP74 1: KSO2
3	R/W	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-116 / LQFP:Pin-113) 0: GP73 1: KSO1
2	R/W	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-115 / LQFP:Pin-112) 0: GP72 1: KSO0
1	R/W	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-114 / LQFP:Pin-111) 0: GP71 1: KSI1

Bit	R/W	Default	Description
0	R/W	0b	Set Pin to Keyboard Matrix Function or GPIO Function (QFP:Pin-113 / LQFP:Pin-110) 0: GP70 1: KSI0

10.9.5.7 KBC Host Interface Control Register (KBHICR)

Address Offset: 07h

Bit	R/W	Default	Description
7	-	0b	Reserved
6	-	0b	Reserved
5	-	0b	Reserved
4	-	0b	Reserved
3	R/W	0b	Input Buffer Full 8032 Interrupt Enable (IBFCIE) The bit is used to enable the interrupt to 8032 for Keyboard when the input buffer is full via INT24 of INTC.
2	R/W	0b	Output Buffer Empty 8032 Interrupt Enable (OBECIE) The bit is used to enable the interrupt to 8032 for Keyboard when the output buffer is empty via INT2 of INTC.
1	-	0b	Reserved
0	-	0b	Reserved

10.9.5.8 KBC Host Interface Keyboard Status Register (KBHISR)

The 8032 firmware uses the register to monitor the status of KBC. It can use bit 7-4 and bit 2 to send the information to the host processor. The data of this register is the same as that of KBC Status Register (KBSTR).

Address Offset: 08h

Bit	R/W	Default	Description
7-4	R/W	0h	Programming Data 3-0 (PD3-0) The data is used by the 8032 firmware for the general-purpose setting.
3	R	0b	A2 Address (A2) The bit is used to keep the A2 address information of the write operation while the host processor accesses the KBC.
2	R/W	0b	Programming Data II (PDII) The function of this register is the same as that of PD3-0.
1	R	0b	Input Buffer Full (IBF) The bit is set when the host processor is writing data to KBDIR or KBCMDR whereas cleared when data is read from KBHIDIR by the 8032 firmware.
0	R	0b	Output Buffer Full (OBF) The bit is set when 8032 is writing data to KBHIKDOR and KBHIMDOR whereas cleared when data is read from KBDOR by the host.

10.9.5.9 KBC Host Interface Keyboard Data Output Register (KBHKDOR)

The 8032 firmware can write data to this register to send the data of the KBC Data Output Register (KBDOR). Besides, this action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	W	-	KBC Keyboard Data Output (KBKDO) The data is output to the KBC Data Output Register (KBDOR).

10.9.5.10 KBC Host Interface Keyboard Data Input Register (KBHIDIR)

The 8032 firmware can read data from this register to get the data of the KBC Data Input Register (KBDIR). Besides, this action will clear the IBF bit in the KBC Status Register (KBSTR). If the IBFCIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	KBC Keyboard Data Input (KBKDI) The data is the same as that of KBC Data Input Register (KBDIR).

10.10 USB Host Controller and Charger

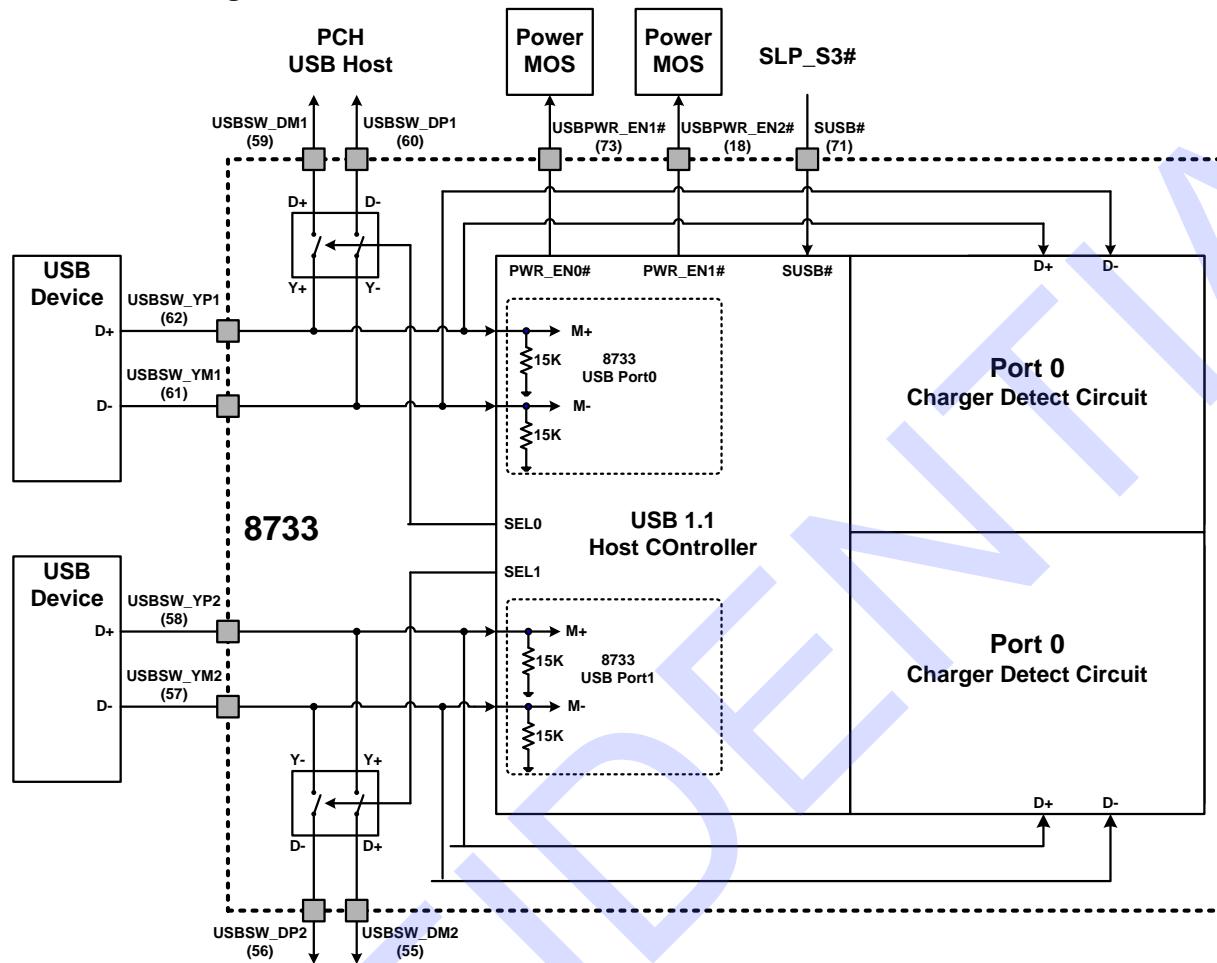
10.10.1 Overview

This module provides USB 1.1 host functions and charger is supported as well.

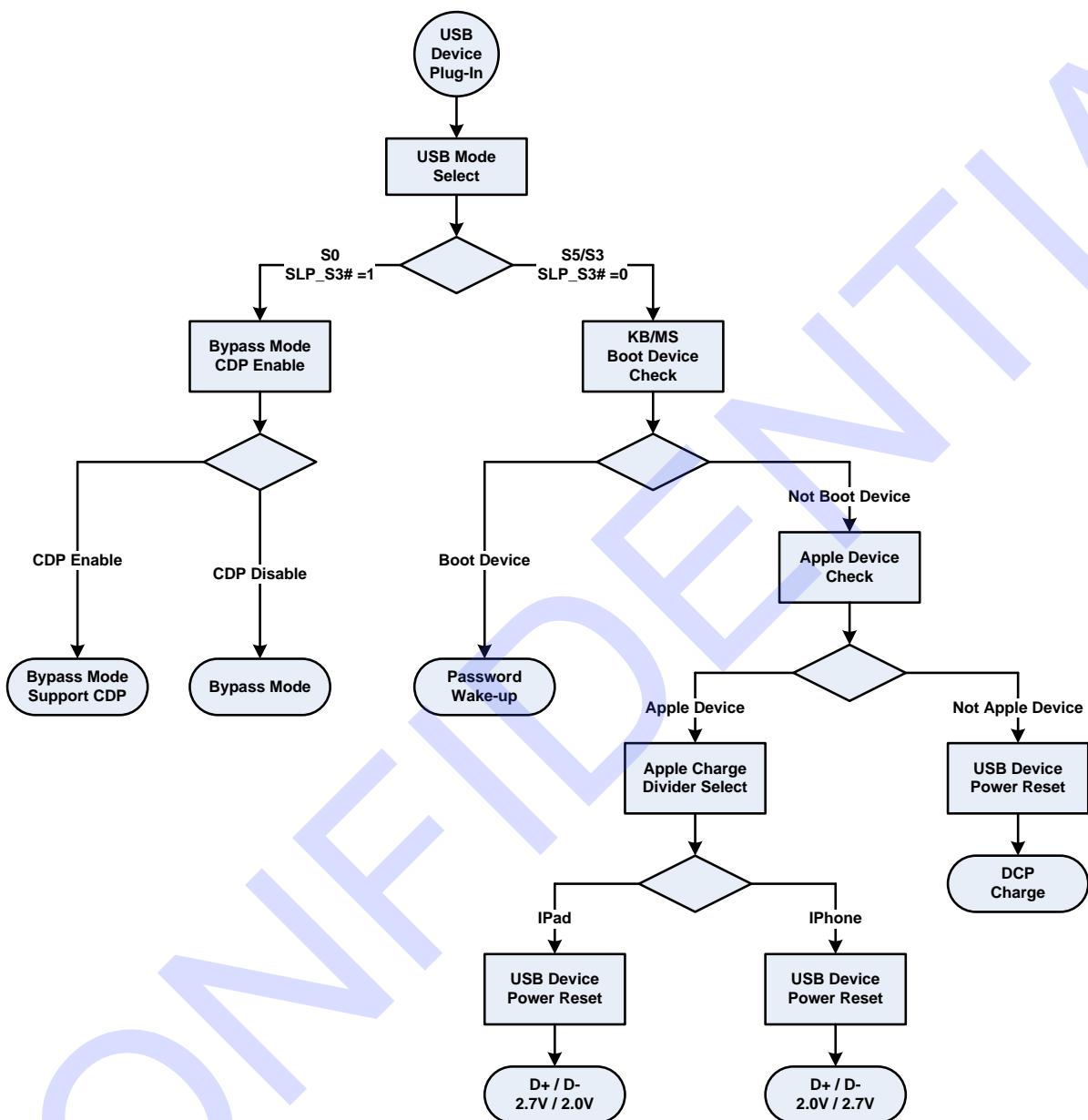
10.10.2 Features

- Supports the USB 1.1 protocol layer
- On transmit path sync insertion, CRC calculation and insertion, parallel to serial conversion, bit stuffing, and NRZI encoding
- On receive path connection state detection, sync detection and stripping, clock recovery, NRZI decoding, bit de-stuffing, CRC calculation and checking, and serial to parallel conversion
- Supports all USB 1.1 transaction types, bulk, setup, interrupt, and isochronous
- Supports automatic preamble insertion, and automatic SOF generation and transmission
- D+/D- CDP/DCP Modes per USB Battery Charging Specification 1.2
- D+/D- Shorted Mode per Chinese Telecommunication Industry Standard YD/T 1591-2009
- D+/D- Divider Modes 2.0V/2.7V and 2.7/2.0V Compliant with 1A and 2A Apple Mobile Digital Devices
- Supports Sleep-Mode Charging and Mouse/Keyboard (Low-Speed Only) Password Wake Up

10.10.3 Block Diagram of USB Host Controller



10.10.4 USB Charger Programming Flowchart



10.10.5.1 List of USB Host Controller Registers

The USB controller registers are listed below and the base address is 2F00h.

Table 10-22. List of USB Controller Register

Register Name	R/W	Address	Default
Host TX Control Register	R/W	0x00	00h
Host TX Transaction Type Register	R/W	0x01	00h
Host TX Line Control Register	R/W	0x02	00h
Host TX SOF Enable Register	R/W	0x03	00h
Host TX Address Register	R/W	0x04	00h
Host TX Endpoint Number Register	R/W	0x05	00h
Host Frame Number MSP Register	RO	0x06	00h
Host Frame Number LSP Register	RO	0x07	00h
Host Interrupt Status Register	RW1C	0x08	00h
Host Interrupt Mask Register	R/W	0x09	00h
Host RX Status Register	RO	0x0A	00h
Host RX PID Register	RO	0x0B	00h
MISC Control Register	R/W	0x0C	00h
MISC Status Register	RO	0x0D	00h
Host RX Connect State Register	RO	0x0E	00h
Host SOF Timer MSB Register	RO	0x0F	00h
Host RX FIFO Data Port Register	RO	0x20	00h
Host RX FIFO Data Count MSB Register	RO	0x22	00h
Host RX FIFO Data Count LSB Register	RO	0x23	00h
Host TX FIFO Data Port Register	WO	0x30	00h
Host/Slave Control Register	R/W	0xE0	01h
Host/Slave Version Register	RO	0xE1	22h
PME# Wake Up Register	WO	0xE2	00h
RX Resume Detection Time Register	R/W	0xE3	20h
Port1 MISC Control Register	R/W	0xE4	10h
Port2 MISC Control Register	R/W	0xE6	00h
Port1 MISC Status Register	RO	0xE8	10h
Port2 MISC Status Register	RO	0xEA	00h
SUSB Control Register	R/W	0xEC	00h
SUSB Status Register	RO	0xED	00h

10.10.5.2 Host TX Control Register

Address Offset: 00h

Bit	R/W	Default	Description
7-4	RO	0h	Reserved
3	R/W	0b	ISO_ENABLE_BIT Set to 1 to enable isochronous mode. In isochronous mode, no acknowledgements are sent or received. Note, the TRANS_TYPE_REG must be set to either IN_TRANS or OUTDATA0_TRANS. Isochronous mode is not allowed with any other transaction types.
2	R/W	0b	PREAMBLE_ENABLE_BIT Set to 1 to enable preamble. Should only be enabled when the host is connected to a low speed device via a hub. The preamble is a token which is prefixed to all packet transmissions, and is transmitted at full speed irrespective of the state of the FULL_SPEED_LINE_RATE_BIT.
1	R/W	0b	SOF_SYNC_BIT Set to 1 to synchronize transaction with the end of SOF transmission. Transaction will be scheduled for transmission immediately after SOF transmission.
0	R/W	0b	TRANS_REQ_BIT Set to 0 to disable transaction. Set to 1 to enable transaction, automatically cleared when transaction complete.

10.10.5.3 Host TX Transaction Type Register

Address Offset: 01h

Bit	R/W	Default	Description
7-2	RO	0h	Reserved
1-0	R/W	0h	TRANSACTION_TYPE These are the four basic types of transaction. The transaction types detailed in USB 1.1 (Setup, bulk, and isochronous) are composed of a series of one or more of these basic atomic transactions. SETUP_TRANS = 0 IN_TRANS = 1 OUTDATA0_TRANS = 2 OUTDATA1_TRANS = 3

10.10.5.4 Host TX Line Control Register

Address Offset: 02h

Bit	R/W	Default	Description
7-5	RO	0h	Reserved
4	R/W	0b	FULL_SPEED_LINE_RATE_BIT Set to 1 to enable full speed line rate of 12Mbps. Clear to 0 to enable low speed line rate of 1.5Mbps. If the host is communicating with a full speed device, then full speed line rate should be enabled. If the host is communicating with a low speed device full speed line rate should be disabled.
3	R/W	0b	FULL_SPEED_LINE_POLARITY_BIT Set to 1 to enable full speed line polarity. That is J= differential 1, K= differential 0. Clear to zero to enable low speed line polarity. That is J= differential 0, K= differential 1. If the host is communicating with a full speed device, then full speed line polarity should be enabled. If the host is communicating with a low speed device directly then full speed line polarity should be disabled. If the host is communicating with a low speed device via a hub, then full speed line polarity should be enabled.
2	R/W	0b	DIRECT_CONTROL_BIT Set to 1 to allow direct control the state of the USB physical wires. Clear to 0 for normal operation.
1-0	R/W	0h	TX_LINE_STATE When DIRECT_CONTROL_BIT=1, TX_LINE_STATE directly controls the state of the USB physical wires, where; TX_LINE_STATE [1] = D+ TX_LINE_STATE [0] = D-

10.10.5.5 Host TX SOF Enable Register

Address Offset: 03h

Bit	R/W	Default	Description
7-1	RO	0h	Reserved
0	R/W	0h	SOF_EN_BIT If FULL_SPEED_LINE_POLARITY_BIT is set, then setting this bit to 1 to enables automatic transmission of SOF tokens every 1mS. Note that SOF tokens will be transmitted at full speed line rate irrespective of the state of FULL_SPEED_LINE_RATE_BIT. If FULL_SPEED_LINE_POLARITY_BIT is clear, then setting this bit to 1 to enables automatic transmission of low speed EOP keep alive every 1ms. Transition from 0 to 1 causes transmission of resume state prior to EOP transmission. Note that this mode is only used when the host is connected directly to a low speed device. Clear to 0 to disable automatic SOF/EOP transmission, and allow any devices attached to the host to enter the suspend state

10.10.5.6 Host TX Address Register

Address Offset: 04h

Bit	R/W	Default	Description
7	RO	0b	Reserved
6-0	R/W	0h	DEVICE_ADDRESS

10.10.5.7 Host TX Endpoint Number Register

Address Offset: 05h

Bit	R/W	Default	Description
7-4	RO	0h	Reserved
3-0	R/W	0h	ENDPOINT_NUMBER

10.10.5.8 Host Frame Number MSP Register

Address Offset: 06h

Bit	R/W	Default	Description
7-3	RO	0h	Reserved
2-0	RO	0h	FRAME_NUM_MSP Most significant part of the frame number used for SOF transmission. That is FRAME_NUM_MSP = FRAME_NUM[10:8].

10.10.5.9 Host Frame Number LSP Register

Address Offset: 07h

Bit	R/W	Default	Description
7-0	RO	0h	FRAME_NUM_LSP Least significant part of the frame number used for SOF transmission. That is FRAME_NUM_LSP = FRAME_NUM[7:0].

10.10.5.10 Host Interrupt Status Register

Address Offset: 08h

Bit	R/W	Default	Description
7	R/W1C	0b	PORT1_CONNECTION_EVENT_BIT Automatically set to 1 when a connection or disconnection occurs for port0. Must be cleared by writing 1.
6	R/W1C	0b	PORT0_CONNECTION_EVENT_BIT Automatically set to 1 when a connection or disconnection occurs for port0. Must be cleared by writing 1.
5	R/W1C	0b	PORT1_RESUME_INT_BIT Automatically set to 1 when resume state is detected for port1. Must be cleared by writing 1.
4	R/W1C	0b	PORT0_RESUME_INT_BIT Automatically set to 1 when resume state is detected for port0. Must be cleared by writing 1.

Bit	R/W	Default	Description
3	R/W1C	0b	SOF_SENT_BIT Automatically set to 1 when a SOF transmission occurs. Must be cleared by writing 1.
2	R/W1C	0b	CONNECTION_EVENT_BIT Automatically set to 1 when a connection or disconnection occurs. Must be cleared by writing 1. This bit only works on 2PORT_MODE_EN = 0;
1	R/W1C	0b	RESUME_INT_BIT Automatically set to 1 when resume state is detected. Must be cleared by writing 1. This bit only works on 2PORT_MODE_EN = 0;
0	R/W1C	0b	TRANS_DONE_BIT Automatically set to 1 when a transaction is completed. Must be cleared by writing 1.

10.10.5.11 Host Interrupt Mask Register

Address Offset: 09h

Bit	R/W	Default	Description
7	R/W	0b	PORT1_CONNECTION_EVENT_INT Set to 1 to enable interrupt on connection or disconnection event for port1.
6	R/W	0b	PORT0_CONNECTION_EVENT_INT Set to 1 to enable interrupt on connection or disconnection event for port0.
5	R/W	0b	PORT1_RESUME_INT Set to 1 to enable interrupt on resume detected for port1.
4	R/W	0b	PORT0_RESUME_INT Set to 1 to enable interrupt on resume detected for port0.
3	R/W	0b	SOF_SENT_INT Set to 1 to enable interrupt on SOF transmission.
2	R/W	0b	CONNECTION_EVENT_INT Set to 1 to enable interrupt on connection or disconnection event.
1	R/W	0b	RESUME_INT Set to 1 to enable interrupt on resume detected.
0	R/W	0b	TRANS_DONE_INT Set to 1 to enable interrupt on transaction completion.

10.10.5.12 Host RX Status Register

Address Offset: 0Ah

Bit	R/W	Default	Description
7	RO	0b	DATA_SEQUENCE_BIT If the last transaction was of type IN_TRANS, then this bit indicates the sequence number of the last receive packet. DATA0 = 0, DATA1 = 1.
6	RO	0b	ACK_RXED_BIT When set to 1, indicates ACK received from USB device.
5	RO	0b	STALL_RXED_BIT When set to 1, indicates STALL received from USB device.
4	RO	0b	NAK_RXED_BIT When set to 1, indicates NAK received from USB device.

Bit	R/W	Default	Description
3	RO	0b	RX_TIME_OUT_BIT When set to 1, indicates no response from USB device.
2	RO	0b	RX_OVERFLOW_BIT When set to 1, indicates insufficient free space in RX fifo to accept entire data packet.
1	RO	0b	BIT_STUFF_ERROR_BIT When set to 1, indicates bit stuff error detected on the last transaction.
0	RO	0b	CRC_ERROR_BIT When set to 1, indicates CRC error detected on the last transaction.

10.10.5.13 Host RX PID Register

Address Offset: 0Bh

Bit	R/W	Default	Description
7-4	RO	0h	Reserved
3-0	RO	0h	RECEIVE_PID Packet identifier for the last packet received.

10.10.5.14 MISC Control Register

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/W	0b	2PORT_DUPLICATED_SOF Set to 1 to enable sending SOF for unselected port while 2PORT_MODE_ENABLE = 1.
6	R/W	0b	Reserved
5	R/W	0b	PORT1_SPEED Set to 1 to enable full speed line rate of 12Mbps. Clear to 0 to enable low speed line rate of 1.5Mbps.
4	R/W	0b	PORT0_SPEED Set to 1 to enable full speed line rate of 12Mbps. Clear to 0 to enable low speed line rate of 1.5Mbps.
3	R/W	0b	HOST_PORT_SEL When set to 1, indicates host controller controlling port 1. When set to 0, indicates host controller controlling port 0.
2	R/W	0b	2PORT_MODE_ENABLE When set to 1, the two resume detection and port connection logic is enabled.
1	R/W	0b	PORT1 Hardware CDP_DET to VSRC_EN When set to 1, the port 1 CDP_DET direct control to VSRC_EN.
0	R/W	0b	PORT0 Hardware CDP_DET to VSRC_EN When set to 1, the port 0 CDP_DET direct control to VSRC_EN.

10.10.5.15 MISC Status Register

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	RO	0h	Reserved
5-4	RO	0h	PORT1_RX_LINE_STATE The contents of RX_CONNECT_STATE_REG reflect the current connection state of port 1, where; DISCONNECT = 0 LOW_SPEED_CONNECT = 1 FULL_SPEED_CONNECT = 2
3-2	RO	0h	Reserved
1-0	RO	0h	PORT0_RX_LINE_STATE The contents of RX_CONNECT_STATE_REG reflect the current connection state of port 0, where; DISCONNECT = 0 LOW_SPEED_CONNECT = 1 FULL_SPEED_CONNECT = 2

10.10.5.16 Host RX Connect State Register

Address Offset: 0Eh

Bit	R/W	Default	Description
7-2	RO	0h	Reserved
1-0	RO	0h	RX_LINE_STATE The contents of RX_CONNECT_STATE_REG reflect the current connection state, where; DISCONNECT = 0 LOW_SPEED_CONNECT = 1 FULL_SPEED_CONNECT = 2

10.10.5.17 Host SOF Timer MSB Register

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	RO	0h	HOST_SOF_TIMER_MSB Most significant byte of the SOF timer used for SOF transmission. Timer is incremented at 48MHz, thus there are 48000 ticks in a 1mS frame. This register can be used to calculate the number of ticks remaining in a frame. Trem = 0xbb - HOST_SOF_TIMER_MSB

10.10.5.18 Host RX FIFO Data Port Register

Address Offset: 20h

Bit	R/W	Default	Description
7-0	RO	0h	RX_FIFO_DATA If the last transaction was an IN_TRANS, then the receive payload can be retrieved by reading RX_FIFO_DATA.

10.10.5.19 Host RX FIFO Data Count MSB Register

Address Offset: 22h

Bit	R/W	Default	Description
7-0	RO	0h	FIFO_DATA_COUNT_MSB MSByte of FIFO_DATA_COUNT. Indicates the number of data entries within the fifo.

10.10.5.20 Host RX FIFO Data Count LSB Register

Address Offset: 23h

Bit	R/W	Default	Description
7-0	RO	0h	FIFO_DATA_COUNT_LSB LSByte of FIFO_DATA_COUNT. Indicates the number of data entries within the fifo.

10.10.5.21 Host TX FIFO Data Port Register

Address Offset: 30h

Bit	R/W	Default	Description
7-0	WO	0h	TX_FIFO_DATA Prior to requesting an OUTDATA0_TRANS or an OUTDATA1_TRANS , load transmit fifo with data by writing to TX_FIFO_DATA.

10.10.5.22 Host/Slave Control Register

Address Offset: E0h

Bit	R/W	Default	Description
7-2	RO	0h	Reserved
1	WO	0b	RESET_CORE Write only. Value is not latched. Set to 1 to reset all the logic including registers. Must wait 10 usbClk cycles for reset to complete.
0	RO	1b	HOST_MODE Set to 1 to enable host mode.

10.10.5.23 Host/Slave Version Register

Address Offset: E1h

Bit	R/W	Default	Description
7-4	RO	2h	VERSION_NUM_MAJOR
3-0	RO	2h	VERSION_NUM_MINOR

10.10.5.24 PME# Wake Up Register

Address Offset: E2h

Bit	R/W	Default	Description
7-1	RO	0h	Reserved
0	WO	0b	ASSERT_PME# Set to 1 to enable PME# status and assert PME#.

10.10.5.25 RX Resume Detection Time Register

Address Offset: E3h

Bit	R/W	Default	Description
7-0	R/W	20h	RX_RESUME_DETECTION_TIME

10.10.5.26 Port0 MISC Control Register

Address Offset: E4h

Bit	R/W	Default	Description
7	RO	0b	Reserved
6	R/W	0b	SWITCH_SEL
5	R/W	0b	IPAD_SWITCH
4	R/W	1b	PULL_DOWN_EN
3	R/W	0b	DCP_EN
2	R/W	0b	CHG_EN
1	R/W	0b	PWR_EN
0	R/W	0b	VSRC_EN

10.10.5.27 Port0 MISC Status Register

Address Offset: E6h

Bit	R/W	Default	Description
7-4	RO	0h	Reserved
3	RO	0b	DCP_DETECT2
2	RO	0b	DCP_DETECT1
1	RO	0b	DCP_CLR
0	RO	0b	CDP_DET

10.10.5.28 Port1 MISC Control Register

Address Offset: E8h

Bit	R/W	Default	Description
7	RO	0b	Reserved
6	R/W	0b	SWITCH_SEL
5	R/W	0b	IPAD_SWITCH
4	R/W	1b	PULL_DOWN_EN
3	R/W	0b	DCP_EN
2	R/W	0b	CHG_EN
1	R/W	0b	PWR_EN
0	R/W	0b	VSRC_EN

10.10.5.29 Port1 MISC Status Register

Address Offset: EAh

Bit	R/W	Default	Description
7-4	RO	0h	Reserved
3	RO	0b	DCP_DETECT2
2	RO	0b	DCP_DETECT1
1	RO	0b	DCP_CLR
0	RO	0b	CDP_DET

10.10.5.30 SUSB Control Register

Address Offset: ECh

Bit	R/W	Default	Description
7-1	RO	0h	Reserved
0	R/W	1b	SUSB#_INTERRUPT_MASK

10.10.5.31 SUSB Status Register

Address Offset: EDh

Bit	R/W	Default	Description
7-2	RO	0h	Reserved
1	R/W1C	0h	SUSB#_Interrupt_Status
0	RO	0b	SUSB#

10.11 PWM

10.11.1 Overview

The PWM module generates one 8-bit PWM output, which may have different duty cycles. The fan speed is controlled by software.

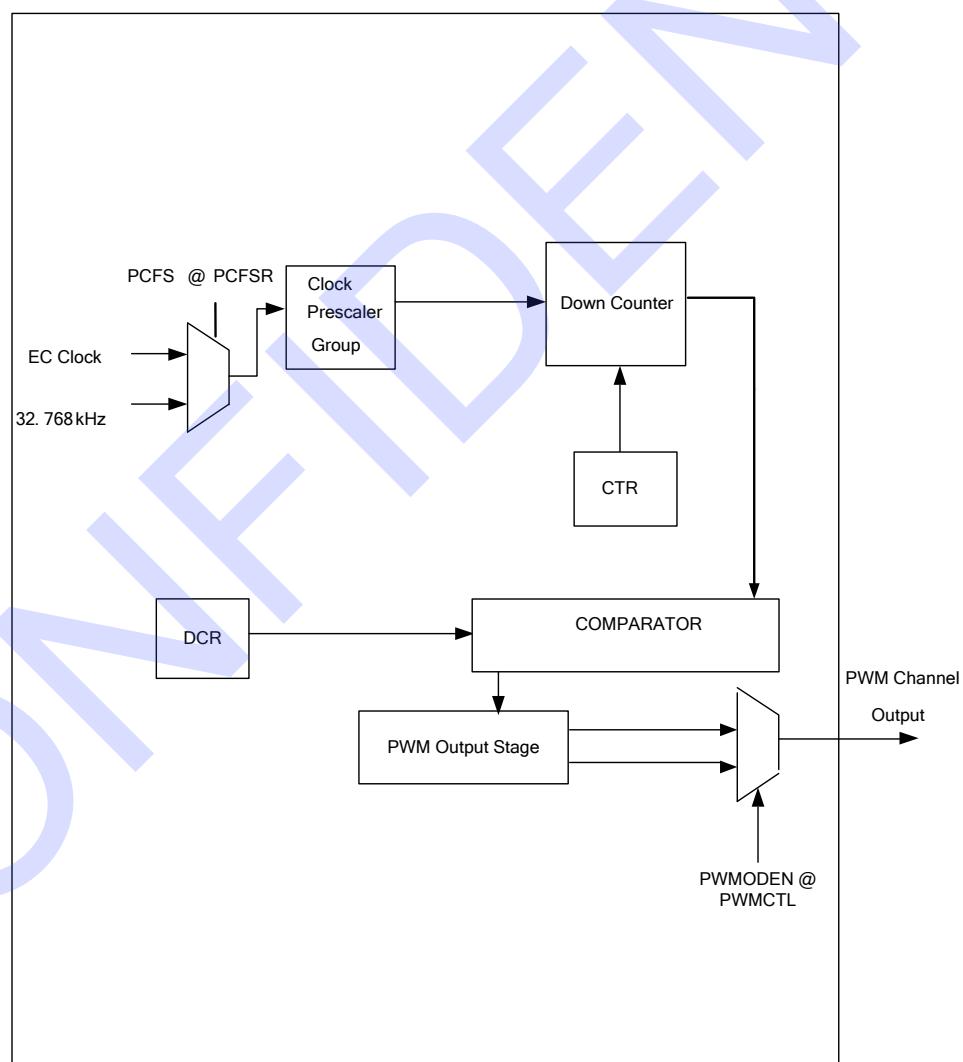
10.11.2 Features

- Supports one PWM output
- Supports PWM open-drain output

10.11.3 Functional Description

10.11.3.1 General Description

Figure 10-25. PWM Diagram



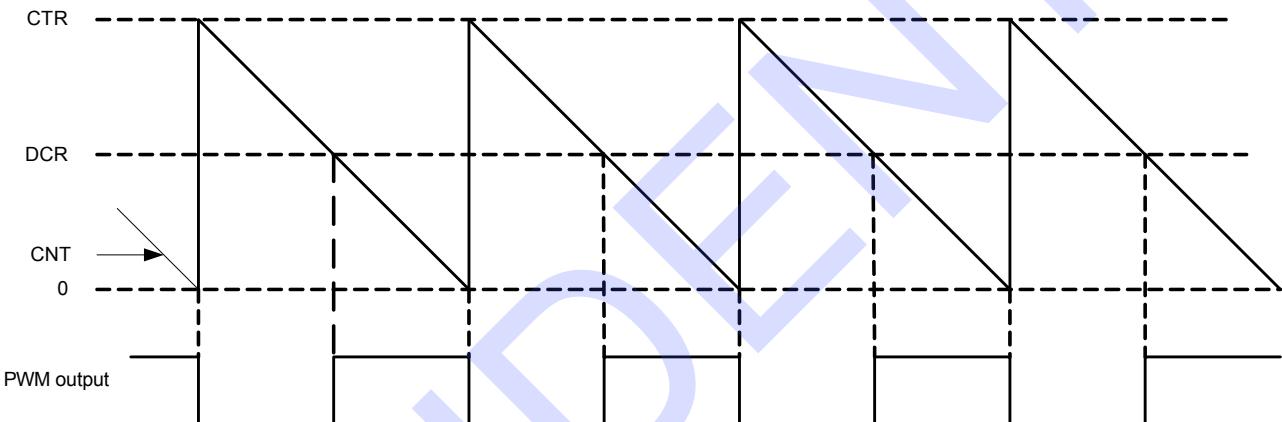
The 32.768 kHz clock and EC clock are used as a reference for PWM output. The prescaler divider values in CRPS register, which divides the PWM input clock into its working clock respectively. The prescaler divider CPRS register has a 8-bit counter value. The PWM provides one 8-bit PWM output. PWM output is controlled by the duty cycle registers (DCR).

When the PWM working clock is enabled, the PWM cycle output will be high if the value in the DCR register is greater than the value in the down-counter. If not, the PWM cycle output will be low and PWM cycle output polarity can be inverted by the INVP register.

When the value in the down-counter reaches 0, the value in the counter will be reloaded then start down-counter until the PWM working clock is disabled.

Cycle Time and Duty Cycle

Figure 10-26. PWM Output Waveform



The PWM module supports duty cycles ranging from 0% to 100%.

The PWM_i output signal cycle time is:

$$n(\text{CPRS} + 1) \times 256 \times T_{\text{clk}}$$

Where:

- T_{clk} is the period of PWM input clock = $(1 / 32.768 \text{ kHz})$ or $(1 / \text{FreqEC})$, which is selected by PCFS in PCFSR register. (FreqEC is listed in Table 12-1. Clock Timing Parameter on page 355)
- The PWM output signal duty cycle (in %, when INVP_i is 0) is:
$$(\text{DCR}) / 256 \times 100.$$

In the following cases, the PWM output is hold at a state (low or high):

- PWM output is still high when the content of DCR is equal to 255.
- PWM output is still low when the content of DCR = 0 & INVP = 0 is in PWMPOL register.

10.11.4 EC Interface Registers

These registers are mapped in the address space of EC. The registers are listed below and the base address is 1800h.

Table 10-23. EC View Register Map, PWM

7	0	Offset
		00h
		01h
		03h

10.11.4.1 Clock Prescaler Register (CPRS)

This register controls the cycle time and the minimal pulse width.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	Prescaler Divider Value (PSDV) The PWM input clock is divided by the number of (CPRS+ 1). For example, the value of 01h results in a division by 2. The value of FFh results in a division by 256.

10.11.4.2 PWM Duty Cycle Register (DCR)

This register (DCR) controls the duty cycle of PWM output signal.

Address Offset: 01h

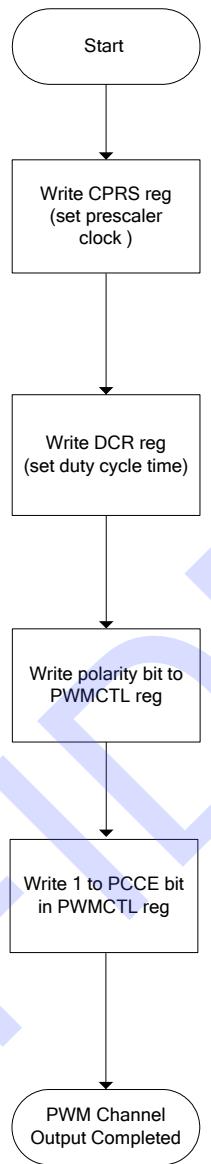
Bit	R/W	Default	Description
7-0	R/W	00h	Duty Cycle Value (DCV) The value of the DCVi register indicates the number of clocks for which PWM is high when the INVP bit in the PWMCTL register is 0. The PWM Duty Cycle output = (DCR)/256 If DCR value = 255, PWM signal is still high. When Inverse PWM bit is 1, the value of PWM is inversed.

10.11.4.3 PWM Control Register (PWMCTL)

This register controls PWM.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	-	Reserved
5	R/W	0b	PWM Output Open-Drain Enable (PWMODEN) This bit controls the output open-drain function of PWM. 0b: PWM output is set to push-pull mode. 1b: PWM output is set to open-drain mode.
4	R/W	0b	Prescaler Clock Frequency Select (PCFS) This bit is for the selection of the clock source of the prescaler. 0b: Select 32.768 kHz 1b: Select FreqEC (EC Clock). (FreqEC and FreqPLL are listed in Table 12-1. Clock Timing Parameter on page 355)
3	R/W	0b	PWM Clock Counter Enable (PCCE) 1: Enable PWM's clock counter. Set this bit to 1 after all other registers have been set. 0: Disable PWM's clock counter
2	-	-	Reserved
1	R/W	0h	Prescaler Clock Source Gating (PCSG) This bit is used to gate prescaler clock source for PWM. 0: Not gating clock source 1: Gating clock source PWM channel output is 0 when INVP bit is set to 0.
0	R/W	0h	Inverse PWM Outputs (INVP) The bit controls the polarity of PWM. 0: Non-inverting. 1: Inverting.

10.11.5 PWM Programming Guide**Figure 10-27. Program Flow Chart for PWM Channel Output**

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11. DC Electrical Characteristics

Operating Conditions

3VSB/SYS_3VSB/A3VSB	$3.3V \pm 0.15V$
VBAT	2.3V to 3.6V
Operation Temperature (Topt).....	0°C to +70°C

Absolute Maximum Ratings*

Applied Voltage	-0.3V to 3.6V
Operation Temperature (Topt).....	0°C to +70°C
Storage Temperature	-55°C to +125°C
Output Voltage (Vo)	-0.3V to VCC3 + 0.3V
Input Voltage (Vi)	-0.3V to VCC3 + 0.3 V

DC Electrical Characteristics(VCC3=3.3V±5%, Ta=0°C~70°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DO8 Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 8 \text{ mA}$			0.4	V
V_{OH}	High Output Voltage	$I_{OH} = -8 \text{ mA}$	2.4			V
DOD8 Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 8 \text{ mA}$			0.4	V
DIO8 Type Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 8 \text{ mA}$			0.4	V
V_{OH}	High Output Voltage	$I_{OH} = -8 \text{ mA}$	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	$V_{IN} = 0$			10	μA
I_{IH}	High Input Leakage	$V_{IN} = \text{VCC3}$			-10	μA
I_{OZ}	3-state Leakage				20	μA
DIOD8 Type Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 8 \text{ mA}$			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	$V_{IN} = 0$			10	μA
I_{IH}	High Input Leakage	$V_{IN} = \text{VCC3}$			-10	μA
I_{OZ}	3-state Leakage				20	μA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DIO16 Type Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 16 \text{ mA}$			0.4	V
V_{OH}	High Output Voltage	$I_{OH} = -16 \text{ mA}$	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	$V_{IN} = 0$			10	μA
I_{IH}	High Input Leakage	$V_{IN} = VCC3$			-10	μA
I_{OZ}	3-state Leakage				20	μA
DIOD16 Type Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 16 \text{ mA}$			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	$V_{IN} = 0$			10	μA
I_{IH}	High Input Leakage	$V_{IN} = VCC3$			-10	μA
I_{OZ}	3-state Leakage				20	μA
DO24L Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 24 \text{ mA}$			0.4	V
V_{OH}	High Output Voltage	$I_{OH} = -8 \text{ mA}$	2.4			V
DIO24 Type Buffer						
V_{OL}	Low Output Voltage	$I_{OL} = 24 \text{ mA}$			0.4	V
V_{OH}	High Output Voltage	$I_{OH} = -16 \text{ mA}$	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	$V_{IN} = 0$			10	μA
I_{IH}	High Input Leakage	$V_{IN} = VCC3$			-10	μA
I_{OZ}	3-state Leakage				20	μA
DI Type Buffer						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
V_{IH}	High Input Voltage(clock)		2.2			V
I_{IL}	Low Input Leakage	$V_{IN} = 0$				μA
I_{IH}	High Input Leakage	$V_{IN} = VCC3$				μA

12. AC Characteristics

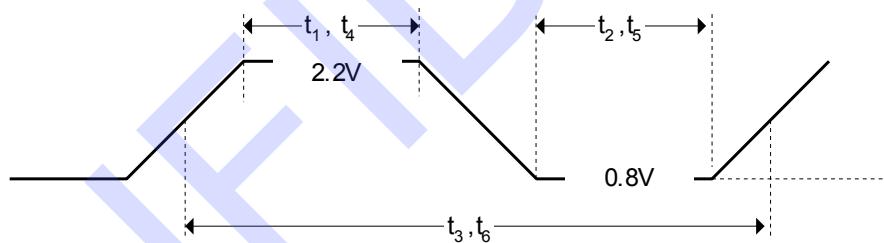
12.1 Clock Input Timings

Table 12-1. Clock Timing Parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock High Pulse Width when CLKIN=48 MHz ¹	8			nsec
t_2	Clock Low Pulse Width when CLKIN=48 MHz ¹	8			nsec
t_3	Clock Period when CLKIN=48 MHz ¹	20	21	22	nsec
t_4	Clock High Pulse Width when CLKIN=24 MHz ¹	18			nsec
t_5	Clock Low Pulse Width when CLKIN=24 MHz ¹	18			nsec
t_6	Clock Period when CLKIN=24 MHz ¹	40			nsec
t_{PLL1}	PLL stabilization time hardware		5		ms
t_{PLL2}	PLL stabilization time after waking up from Sleep mode		5		ms
t_{PER}	PLL clock period			1/Freq PLL	ns
FreqPLL	PLL clock frequency		32.3		MHz
FreqEC	EC Clock Frequency		9.2		MHz

Not tested. Guaranteed by design.

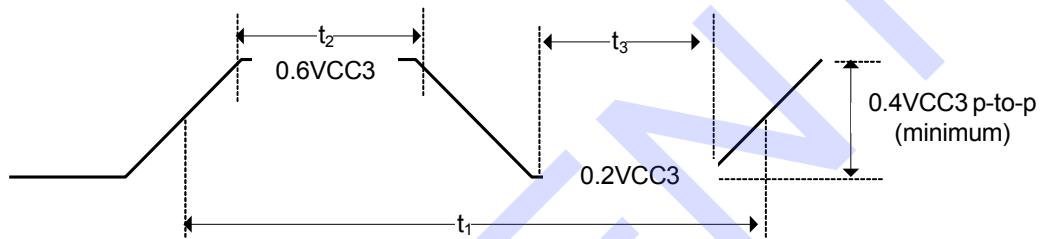
Figure 12-1. Clock Input Timings



12.2 LCLK (PCICLK) and LRESET Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			μsec

Figure 12-2. LCLK (PCICLK) and LRESET Timings

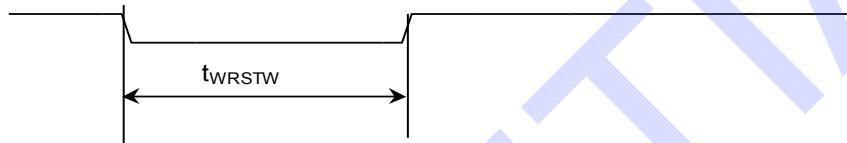


12.3 WARMRESET Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WRSTW}	Warm reset width	10	—	—	μs

Figure 12-3. Warm Reset Timing

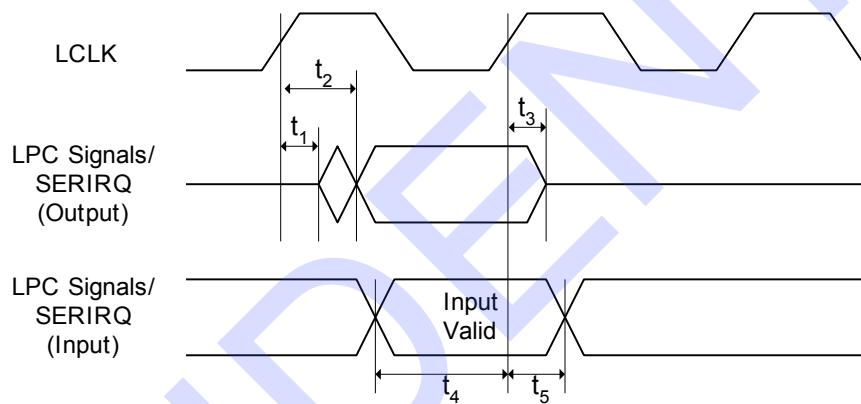
WRST#



12.4 LPC and SERIRQ Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			13	nsec
t_3	Active to Float Delay			20	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

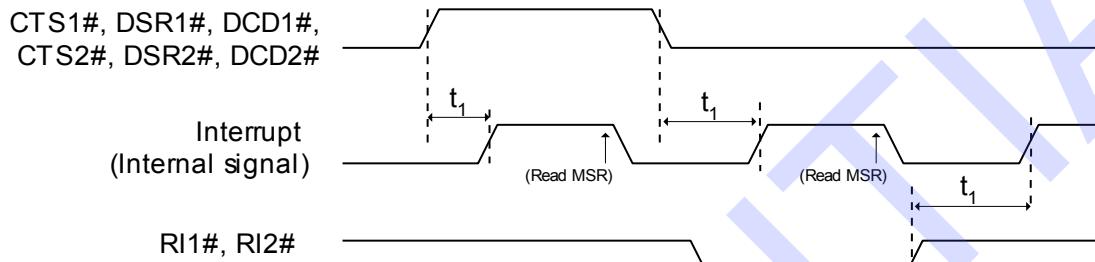
Figure 12-4. LPC and SERIRQ Timings



12.5 Modem Control Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec

Figure 12-5. Modem Control Timings



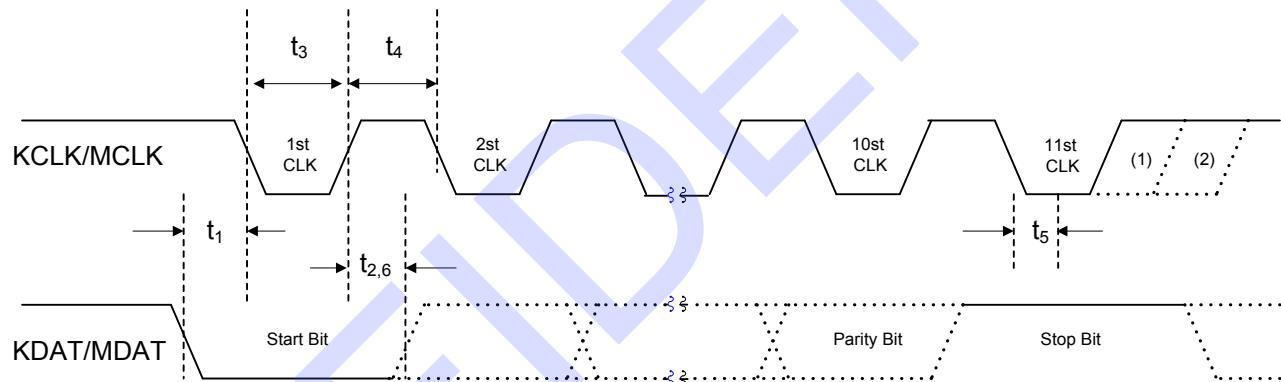
12.6 Keyboard/Mouse Receive/Send Data Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Time from DATA transition to falling edge of CLK (Receive)	5		25	μsec
t_2	Time from rising edge of CLK to DATA transition (Receive)	5		T4-5	μsec
t_3	Duration of CLK inactive (Receive/Send)	30		50	μsec
t_4	Duration of CLK active (Receive/Send)	30		50	μsec
t_5	Time to keyboard inhibit after clock 11 to ensure the keyboard device does not start another transmission (Receive)	>0	50		μsec
t_6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	μsec

Note: (1) The system can hold the 'clock' signal inactive to inhibit the next transmission.

(2) The system raises the 'clock' line to allow the next transmission.

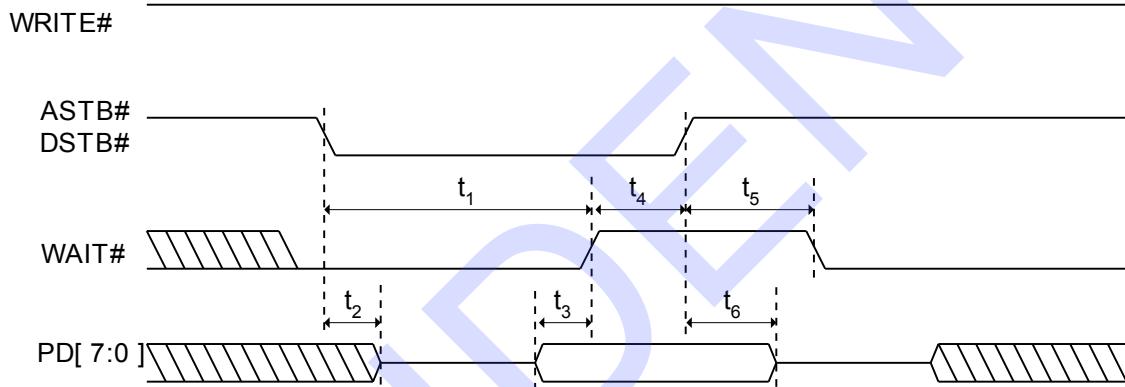
Figure 12-6. Keyboard/Mouse Receive/Send Data Timings



12.7 EPP Address or Data Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	nsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec

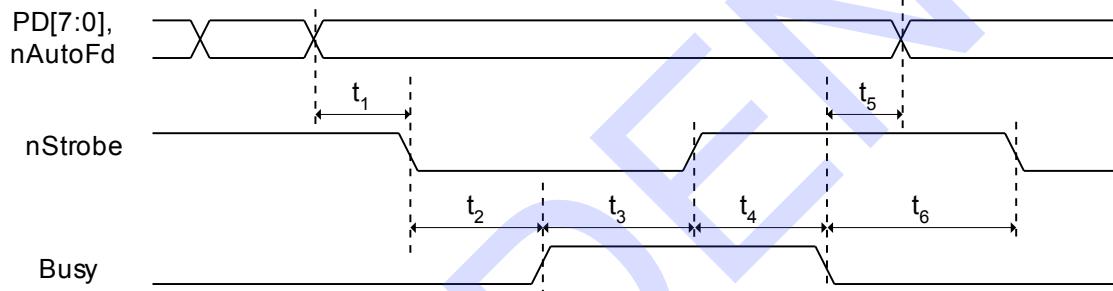
Figure 12-7. EPP Address or Data Read Cycle Timings



12.8 ECP Parallel Port Forward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec

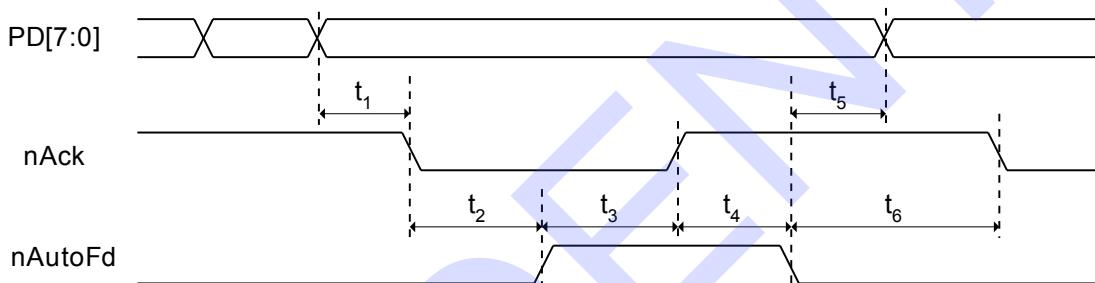
Figure 12-8. ECP Parallel Port Forward Timings



12.9 ECP Parallel Port Backward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec

Figure 12-9. ECP Parallel Port Backward Timings



12.10 RSMRST#, PWROK1/2, and ACPI Power Control Signal Timings

Symbol	Parameter	Typ.			Unit
t_1	RSMRST# de-actives delay from 3VSB=3V	75			msec
t_2 *Note1	PWROK1/2 active delay from $0.8 * VCC3$	23h<3:2> =00b	23h<3:2> =01b	23h<3:2> =10b	
		400	15	200	msec
t_3	Overlap of PSON# and 3VSBSW#	10			msec
t_4	Delay time of 3VSBSW# falling edge to PWROK1/2 falling edge	<1			msec
t_5	Delay time of 3VSBSW# rising edge to PWROK1/2 rising edge	1 Note:2A<Bit 0>=0			usec
t_5'	Delay time of 3VSBSW# rising edge to PWROK1/2 rising edge	139 Note:2A<Bit 0>=1			msec

Figure 12-10. PWROK1/2 Signal Conditions

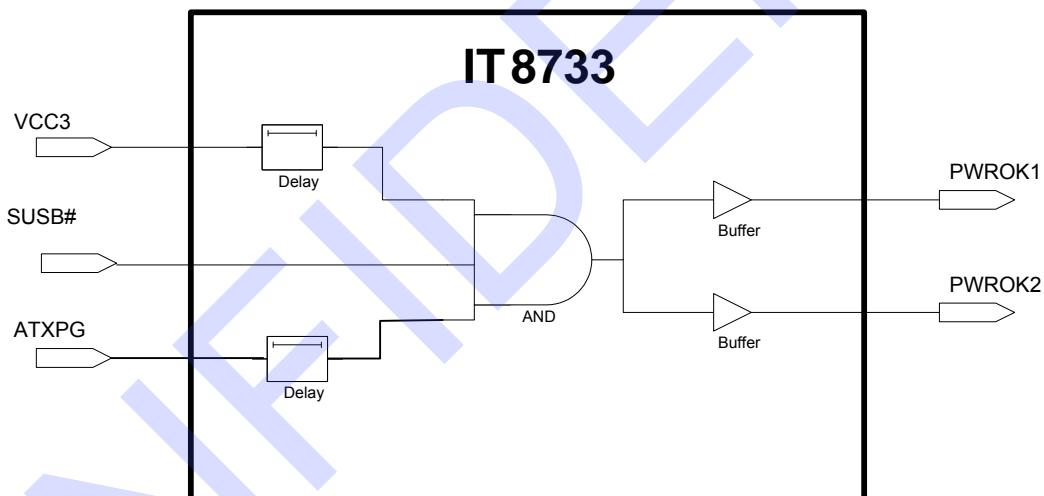


Figure 12-11. RSMRST# Timings

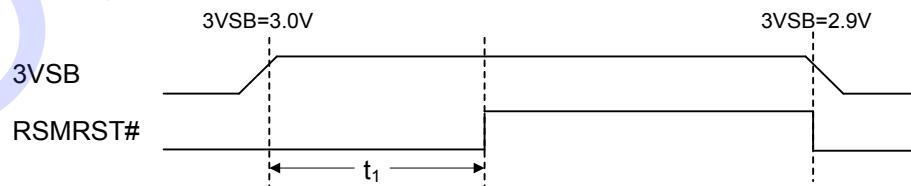


Figure 12-12. PWROK1/2 Timings

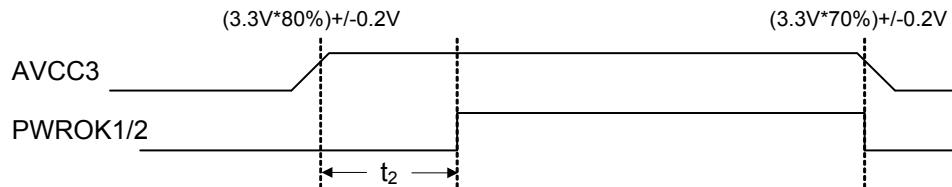
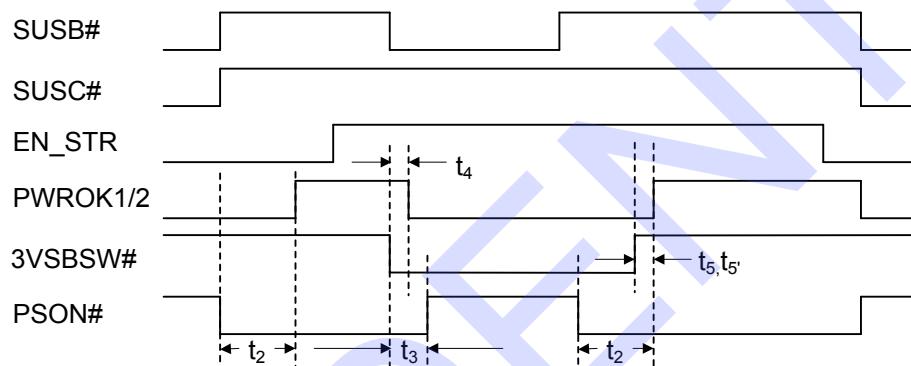


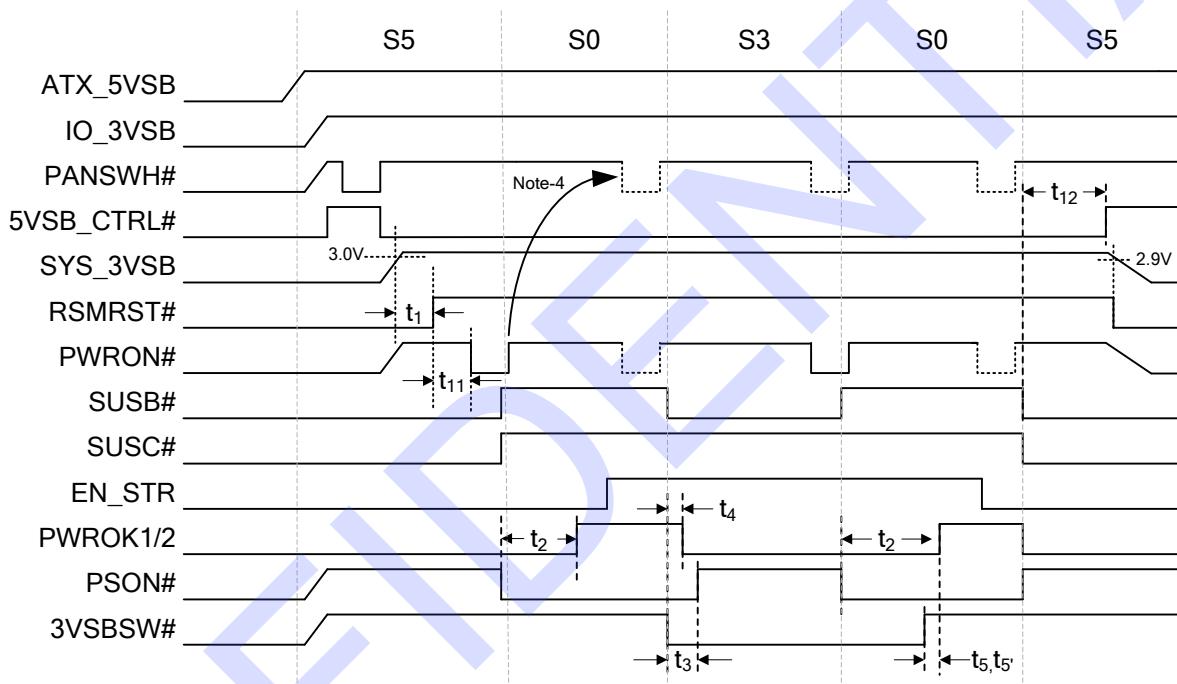
Figure 12-13. ACPI Power Signal Timings



12.11 Energy-using Product (EuP) Power Control Signal Timings

Symbol	Parameter	Min.	Typ.	Max.
t_{11}	Delay time of RSMRST# rising to first PWRON# pulse.	-	200ms	-
t_{12}	Delay time of AVCC3 falling edge to 5VSB_CTRL# rising edge.	-	3.8s	-

Figure 12-14. EuP Function Signal Timings



12.12 Serial Flash (FSPI) Cycle Timings

Figure 12-15. Serial Flash (FSPI) Cycle Timings

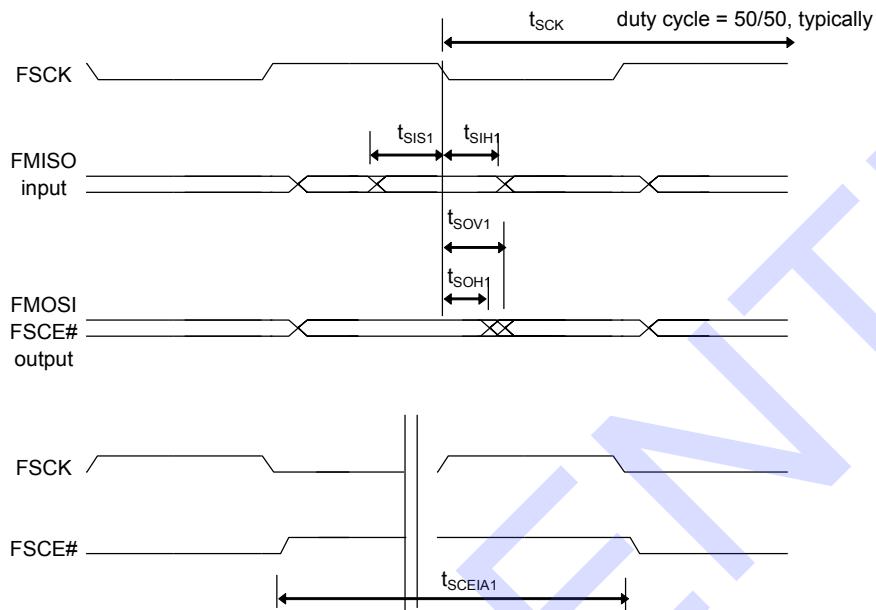


Table 12-2. Serial Flash (FSPI) Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t _{SCK}	FSCK period	—	1/33MHz	—	ns
t _{SIS1}	Input setup time	3	—	—	ns
t _{SIH1}	Input hold time	0	—	—	ns
t _{SOV1}	Clock low to output valid	—	—	5	ns
t _{SOH1}	Output hold time	0	—	—	ns
t _{SCEIA1}	FSCE# high time	(SCEMINHW + 1) * t _{SCK}	—	—	ns

12.13 PMC Timings

Figure 12-16. PMC SMI#/SCI# Timings

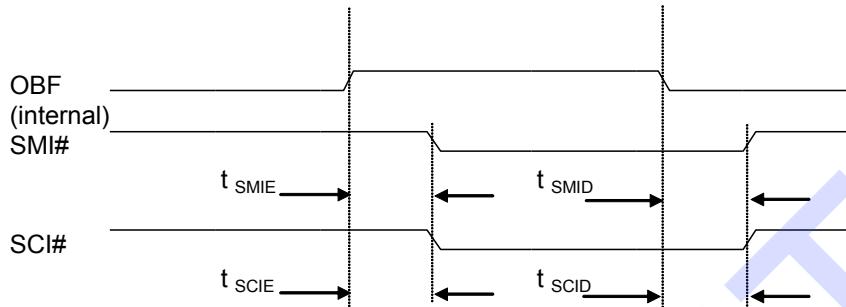


Table 12-3. PMC SMI#/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SMIE}	OBF asserted to SMI# asserted time	—	10	—	ns
t_{SMID}	OBF de-asserted to SMI# de-asserted time	—	5	—	ns
t_{SCIE}	OBF asserted to SCI# asserted time	—	10	—	ns
t_{SCID}	OBF de-asserted to SCI# de-asserted time	—	5	—	ns

Figure 12-17. PMC IBF/SCI# Timings

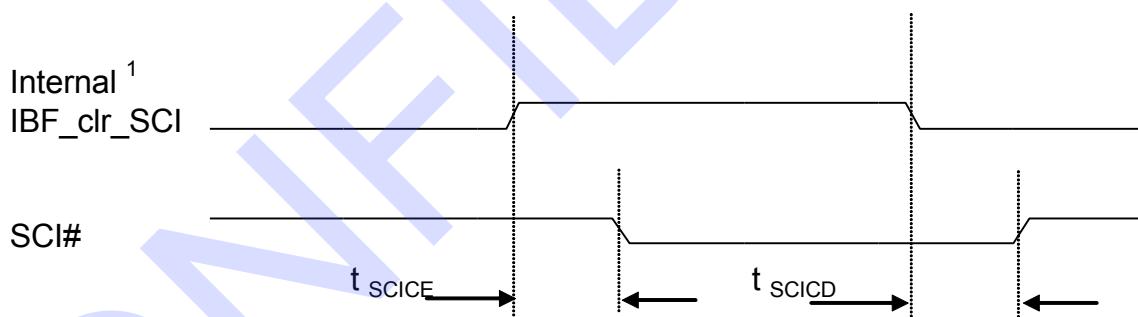


Table 12-4. PMC IBF/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCICIE}	IBF_clr_SCI# asserted to SCI# asserted time	—	70	—	ns
t_{SCICD}	IBF_clr_SCI# de-asserted to SCI# de-asserted time	—	40	—	ns

Note 1: IBF_clr_SCI# means the invert signal of IBF, IBF_clr_SCI# set to one when EC read PMDI or PMDISCI.

12.14 SMBus Timings

Figure 12-18. SMBus Timings

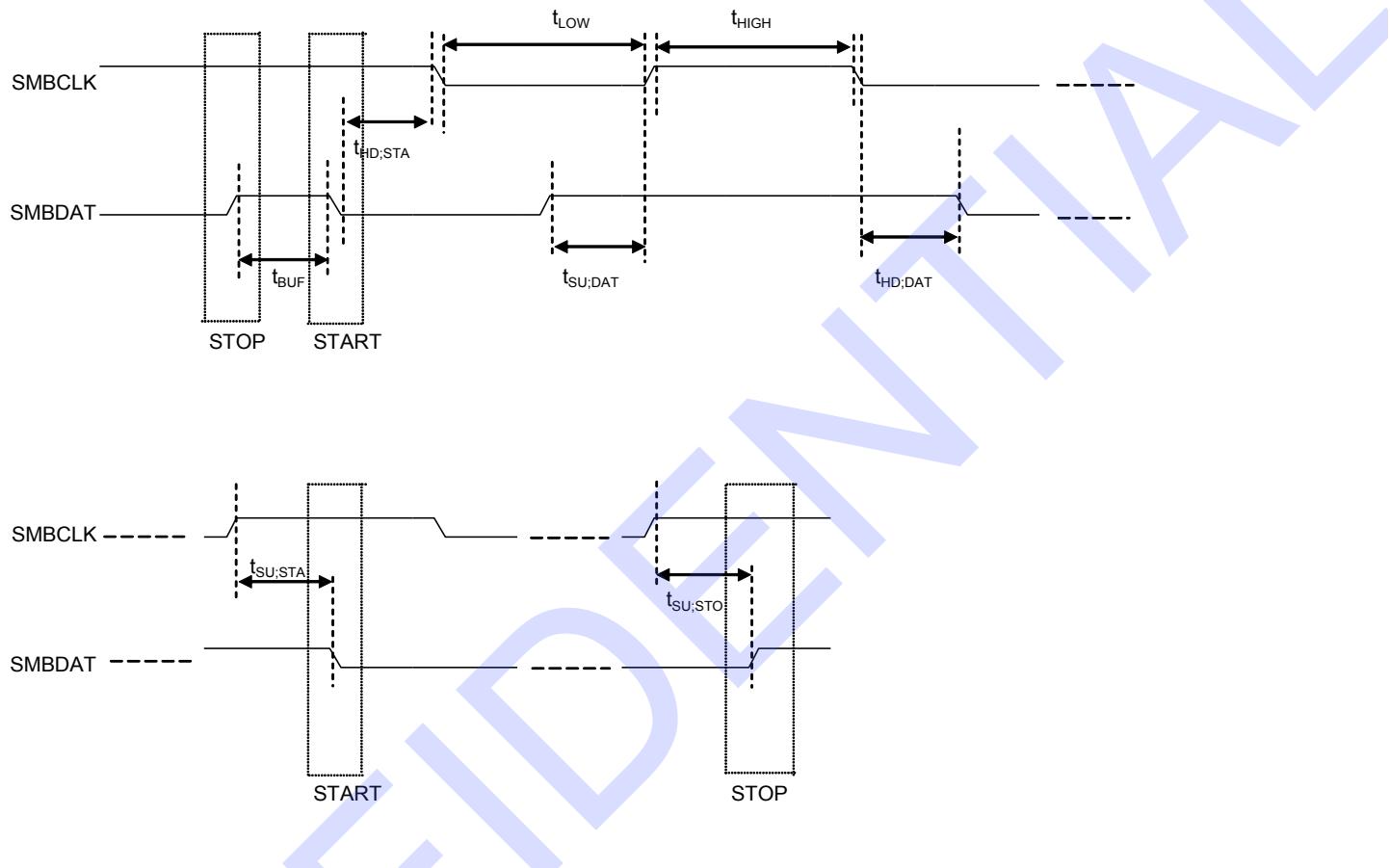


Table 12-5. SMBus AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{BUFS}	Bus free time between Stop and Start condition	4.7	—	—	μs
$t_{HD;STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	4.0	—	—	μs
t_{LOW}	Clock low period	4.7	—	—	μs
t_{HIGH}	Clock high period	4.0	—	50	μs
$t_{SU;DAT}$	Data setup time	250	—	—	ns
$t_{HD;DAT}$	Data hold time	300	—	—	ns
$t_{SU;STA}$	Repeated Start condition setup time	4.7	—	—	μs
$t_{SU;STO}$	Stop condition setup time	4.0	—	—	μs

12.15 DSW Timings

Figure 12-19. DPWORK Timings

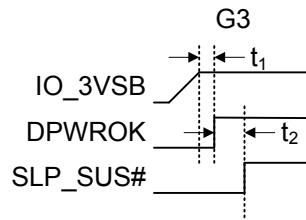


Figure 12-20. DSW Timings

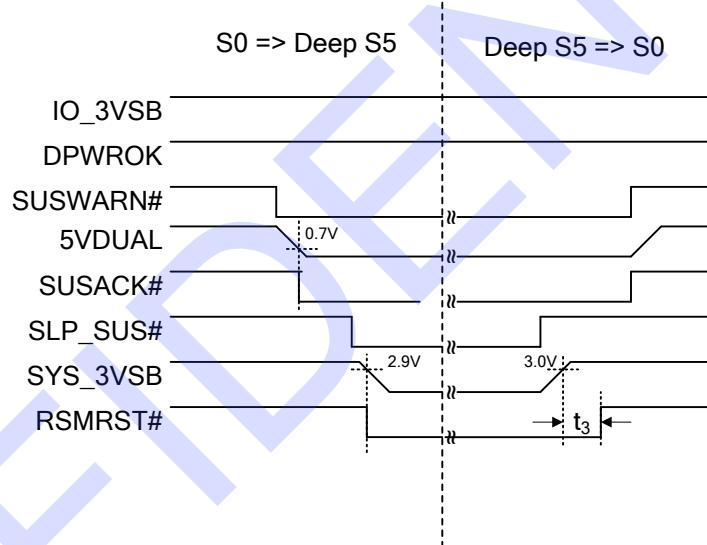


Table 12-6. DSW Timings Parameter

Symbol	Typ.	Description
t ₁	26ms	The rising edge of IO_3VSB to rising edge of DPWORK
t ₂	by SB	The rising edge of IO_3VSB to rising edge of SLP_SUS#
t ₃	75ms	SYS_3VSB voltage over 3.0V to the rising edge of RSMRST#

12.16 AMD K8 Power Sequence

Figure 12-21. AMD K8 Power Sequence Timings

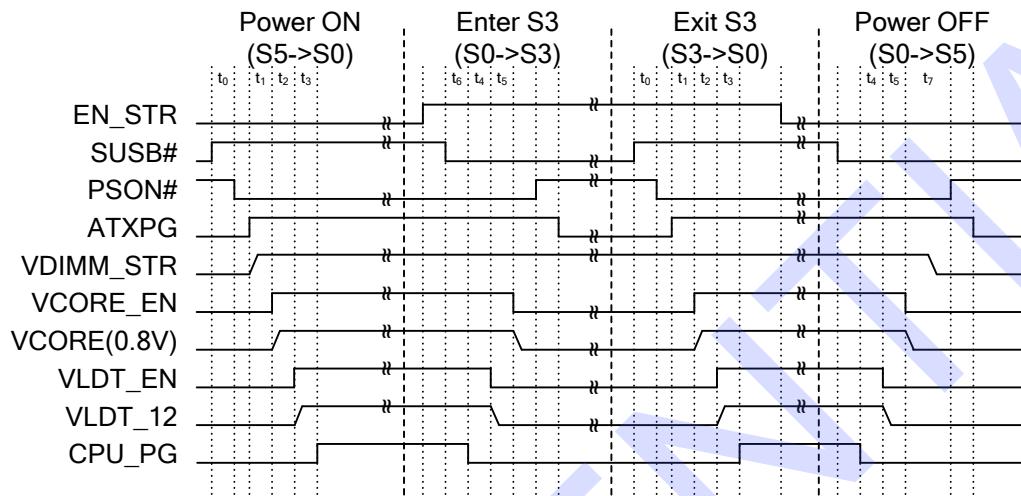


Table 12-7. Power Sequence AC Timing Parameter

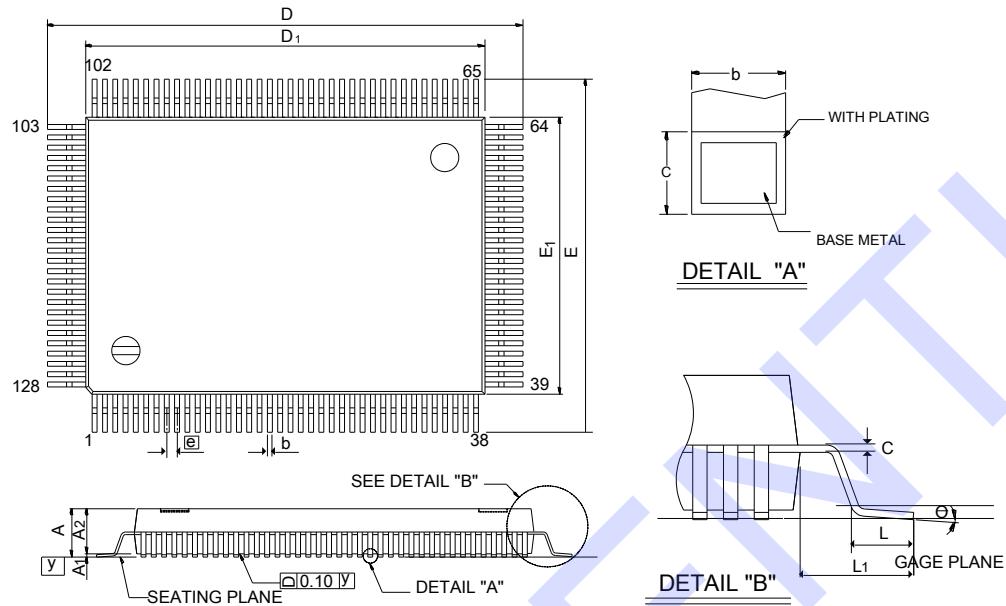
Symbol	Typ.	Description
t_0	1.5ms	The rising edge of SUSB# to the assertion of PSON#.
t_1	$2\text{ms} + t_{\text{vdimm_gd}}$	Both ATXPG & VDIMM_STR ready to the rising edge of VCORE_EN. The $t_{\text{vdimm_gd}}$ is the rise time of the VDIMM_STR voltage from 0V to 1.2V.
t_2	$50\mu\text{s} + t_{\text{vcore_gd}}$	The rising edge of VCORE_EN to the rising edge of VLDT_EN. The $t_{\text{vcore_gd}}$ is the rise time of the VCORE(0.8V) voltage from 0V to 0.6V.
t_3	$2\text{ms} + t_{\text{vldt_gd}}$	The rising edge of VLDT_EN to the rising of CPU_PG. The $t_{\text{vldt_gd}}$ is the rise time of the VLDT voltage from 0V to 1.0V.
t_4	50us	The de-assertion of CPU_PG to the de-assertion of VLDT_EN.
t_5	10ms	The de-assertion of VLDT_EN to the de-assertion of VCORE_EN.
t_6	1.5ms	The falling edge of SUSB# to the de-assertion of CPU_PG.
t_7	210ms	The falling edge of VCORE(0.8V) to the rising edge of PSON#.

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13. Package Information

QFP 128 Outline Dimensions



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A ₁	0.010	-	-	0.25	-	-
A ₂	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D ₁	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E ₁	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L ₁	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

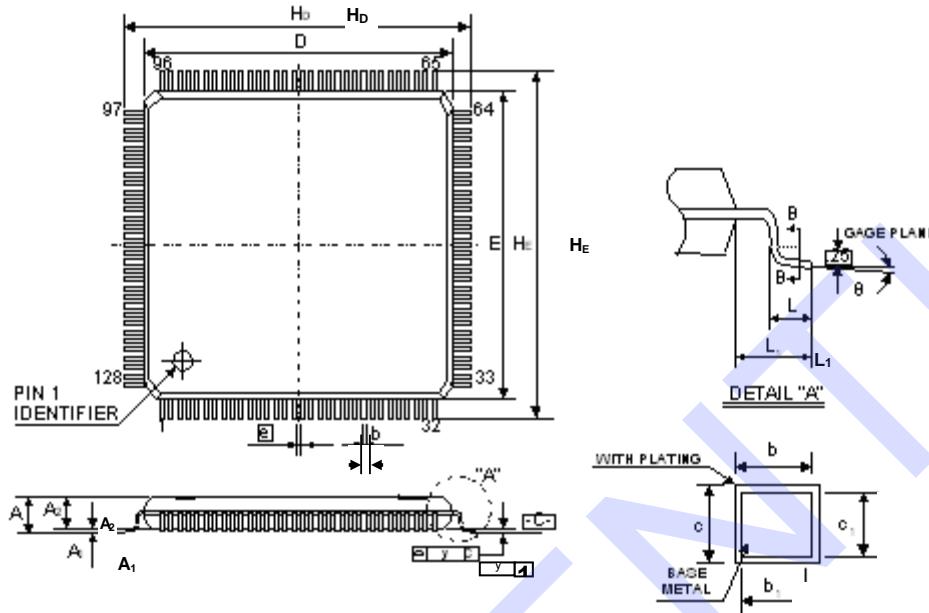
Notes:

- Dimensions D₁ and E₁ do not include mold protrusion.
But mold mismatch is included.
- Dimensions b does not include dambar protrusion.
- Controlling dimension: millimeter

DI-QFP128(14*20)v2

LQFP 128 Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	-	0.05	-	-
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.547	0.551	0.555	13.90	14.00	14.10
e	0.016 BSC			0.40 BSC		
H _D	0.624	0.630	0.636	15.85	16.00	16.15
H _E	0.624	0.630	0.636	15.85	16.00	16.15
L	0.018	0.024	0.030	0.45	0.60	0.75
L ₁	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:

1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
Total in excess of the b dimension at maximum material condition.
Dambar cannot be located on the lower radius of the foot.
3. Controlling dimension : Millimeter
4. Reference document : JEDEC MS-026

DI-LQFP128(14*14)v4

14. Ordering Information

Part No.	Package
IT8733F	QFP 128
IT8733E	LQFP 128

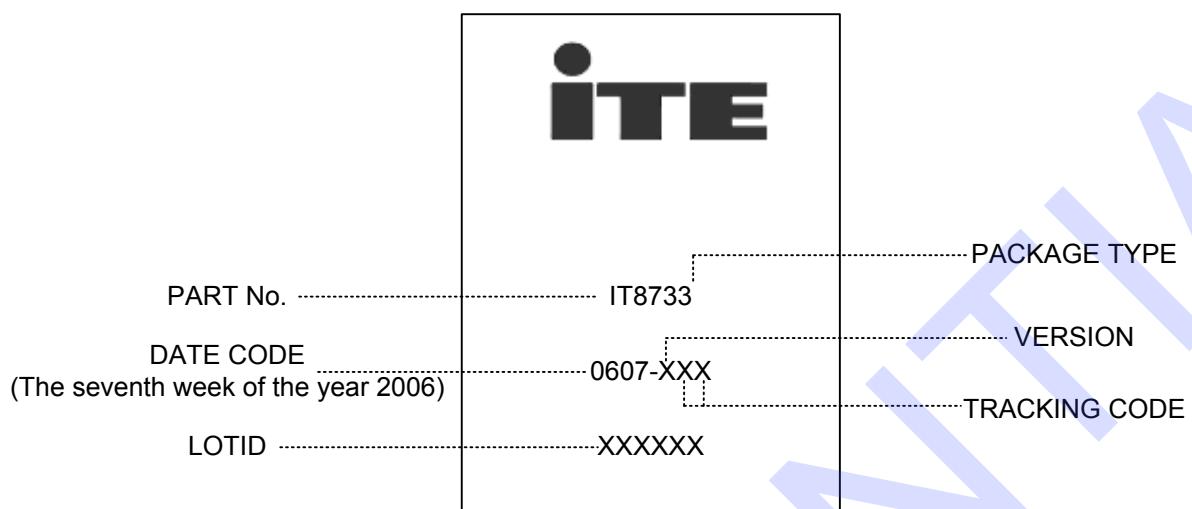
All components provided are RoHS-compliant (100% Green Available).

CONFIDENTIAL

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CONFIDENTIAL

15. Top Marking Information



*PACKAGE TYPE :

- E: LQFP
- F: QFP
- FN: QFN
- R: SSOP

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China. Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (I) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (II) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

- (a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
- (b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
- (c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

- (a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
- (b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
- (c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
- (d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
- (e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
- (f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

- (a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
- (b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
- (c) Buyer will not return any goods without first obtaining a customer return order number.
- (d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.
- (e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
- (f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

- (a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in writing and signed by an officer of Seller.
- (b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.