Quiz 6
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ME333

1. Use the IO SFRs to make pin CN14 an input and enable the pullup resistor:

TRISDbits.TRISD5 = 1;
CNPUEbits.CNPUE14 = 1;

2. List two differences between the CoreTimer and Timer2:

1.) The CoreTimer is integral to the CPU on the PIC32 while Timer2 and the other Timerx timers are all peripherals. CoreTimer uses the SYSCLOCK to keep track of time and Timer2 uses PBCLOCK.

2). The CoreTimer always counts in the same way, with the SYSCLOCK fixed at 80MHz and the timer always incrementing after two ticks. Timer2 is much more flexible since it uses an adjustable period and prescaler to determine time between rollovers.

3. Timer1 has been setup to count external pulses, and can have a prescaler of N = 1, 8, 64, or 256. What is the largest number of input pulses that can be counted before the timer rolls over, and what prescaler N and period register PR1 are used to count to this number?

If we use N = 256 as our prescaler and the maximum period of 62,499, we can count 256 * 62,499 = 15,999,744 pulses. We would use the prescaler N = 256 and PR1 = 62499.

4. OC4 and Timer2 are used to create 2000 Hz PWM with 20% duty cycle.
a. Assuming you use a prescaler of N = 2 and a PBCLK of 80 MHz, what is the value of PR2?

2000 Hz = (1 + PR2) * 2 * 12.5 Ns
2000 Hz = 0.0005 seconds

$$\frac{0.0005\ seconds}{12.5 * 10^{-9} * 2\ seconds} - 1 = PR2$$

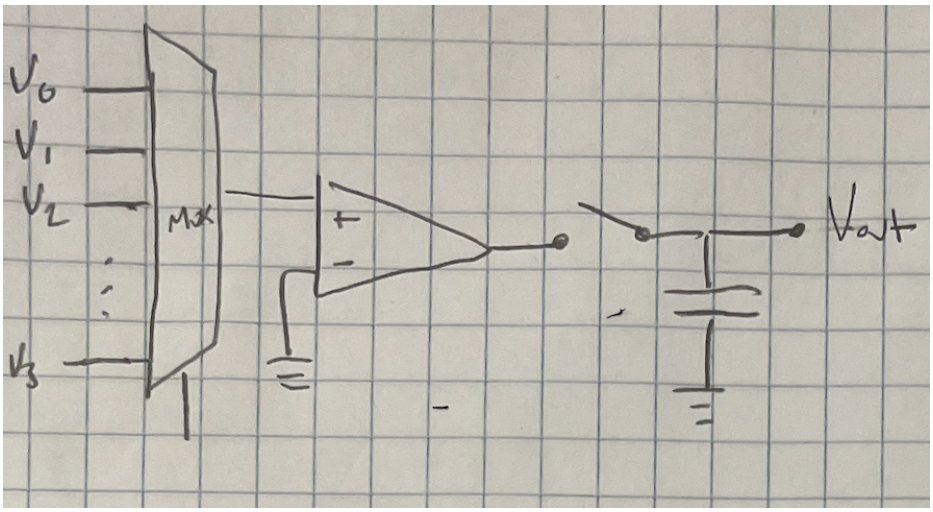
PR2 = 19999

b. What is the value of OC4RS?

OC4RS = 0.2 * 20000 = 4000

5. Describe and draw a picture of the two steps in the process of reading an analog input.

The ADC works in two stages. The first stage is a sampling stage. In this stage a mux selects the analog signal that is fed into a differential amp. A switch is then closed and the signal charges a capacitor to the same potential as the signal.



In the second stage, the signal is digitized. First the capacitor is opened. Then the DAC generates a signal that is halfway between Vmax and Vref. A comparator then compares the analog signal and the generated signal and determines if the signal is higher or lower. The ADC will then use a binary search method to find the value from the DAC that is the closest to the analog sample, and the value will the be the final digitized signal.