PSoC® Creator™
Project Datasheet for RPPSOC-GPIO18Blink

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Table of Contents

1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C52LP series member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C52LP Device Series Block Diagram

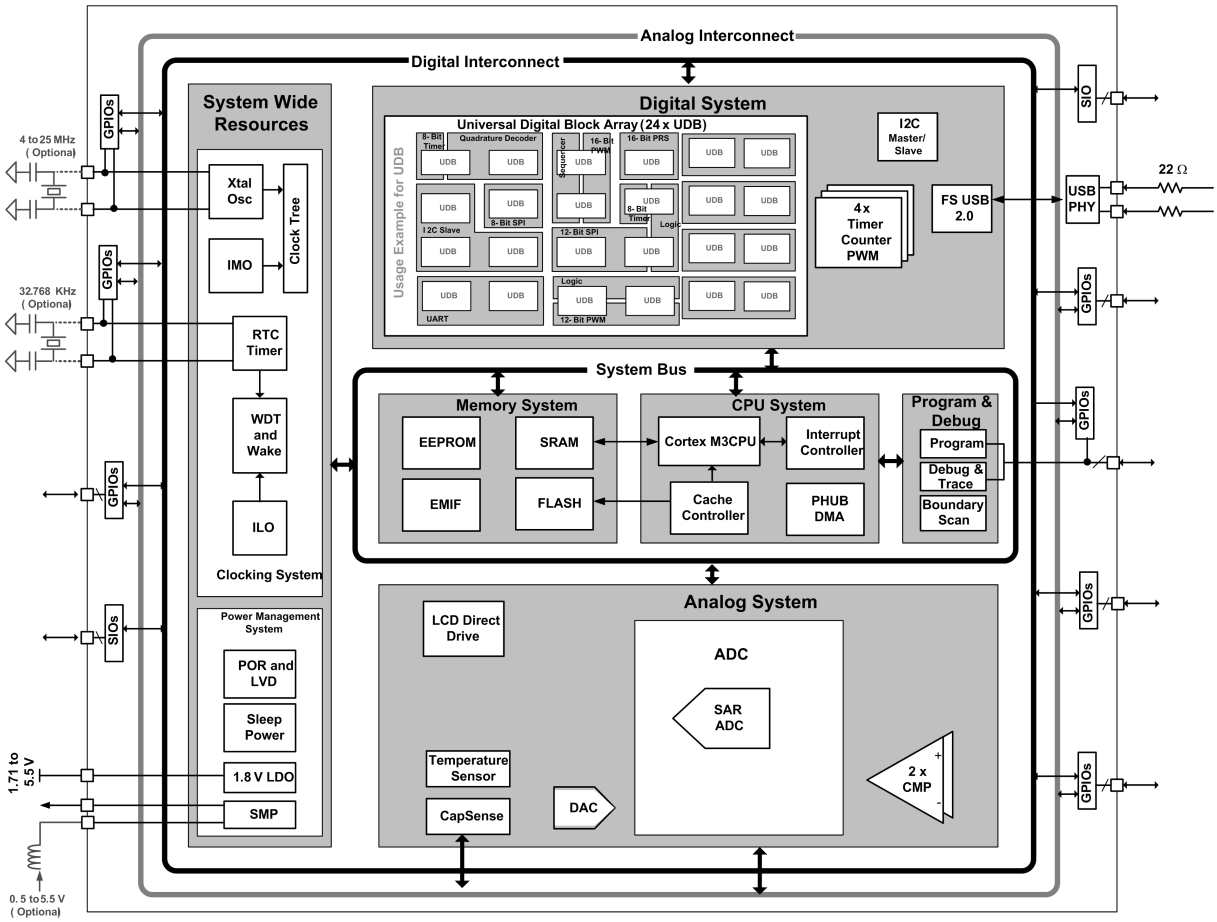


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5267AXI-LP051
Package Name	100-TQFP
Family	PSoC 5LP
Series	CY8C52LP
Max CPU speed (MHz)	0
Flash size (kB)	128
SRAM size (kB)	32
EEPROM size (bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85
JTAG ID	0x2E133069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

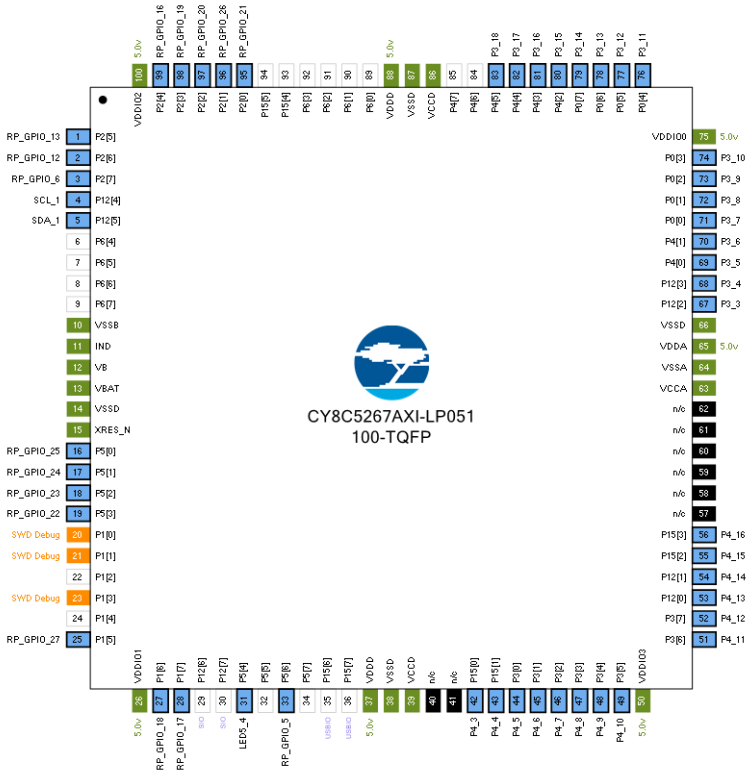
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	1	7	8	12.50 %
Analog Clocks	0	4	4	0.00 %
CapSense Buffers	0	2	2	0.00 %
Interrupts	1	31	32	3.13 %
IO	52	20	72	72.22 %
Segment LCD	0	1	1	0.00 %
I2C	1	0	1	100.00 %
USB	0	1	1	0.00 %
DMA Channels	0	24	24	0.00 %
Timer	0	4	4	0.00 %
UDB				
Macrocells	56	136	192	29.17 %
Unique P-terms	176	208	384	45.83 %
Total P-terms	177			
Datapath Cells	0	24	24	0.00 %
Status Cells	0	24	24	0.00 %
Control Cells	0	24	24	0.00 %
Comparator	0	2	2	0.00 %
Delta-Sigma ADC	0	1	1	0.00 %
LPF	0	2	2	0.00 %
SAR ADC	0	1	1	0.00 %
DAC				
VIDAC	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	RP_GPIO_13	Dgtl In	Res pull up	HiZ Analog Unb
2	P2[6]	RP_GPIO_12	Dgtl In	Res pull up	HiZ Analog Unb
3	P2[7]	RP_GPIO_6	Dgtl In	Res pull up/down	HiZ Analog Unb
4	P12[4]	SCL_1	Dgtl I/O	OD, DL	HiZ Analog Unb
5	P12[5]	SDA_1	Dgtl I/O	OD, DL	HiZ Analog Unb
6	P6[4]	GPIO [unused]			HiZ Analog Unb
7	P6[5]	GPIO [unused]			HiZ Analog Unb
8	P6[6]	GPIO [unused]			HiZ Analog Unb
9	P6[7]	GPIO [unused]			HiZ Analog Unb
10	VSSB	VSSB	Dedicated		
11	IND	IND	Dedicated		
12	VB	VB	Dedicated		
13	VBAT	VBAT	Dedicated		
14	VSSD	VSSD	Power		
15	XRES_N	XRES_N	Dedicated		
16	P5[0]	RP_GPIO_25	Dgtl In	Res pull up	HiZ Analog Unb
17	P5[1]	RP_GPIO_24	Dgtl In	HiZ digital	HiZ Analog Unb
18	P5[2]	RP_GPIO_23	Dgtl In	Res pull up	HiZ Analog Unb
19	P5[3]	RP_GPIO_22	Dgtl In	Res pull up	HiZ Analog Unb
20	P1[0]	Debug:SWD_IO	Reserved		
21	P1[1]	Debug:SWD_CK	Reserved		
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	Debug:SWV	Reserved		
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	RP_GPIO_27	Dgtl In	Res pull up	HiZ Analog Unb
26	VDDIO1	VDDIO1	Power		
27	P1[6]	RP_GPIO_18	Dgtl In	Res pull up	HiZ Analog Unb
28	P1[7]	RP_GPIO_17	Dgtl In	Res pull up	HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	LED5_4	Dgtl Out	Strong drive	HiZ Analog Unb
32	P5[5]	GPIO [unused]			HiZ Analog Unb
33	P5[6]	RP_GPIO_5	Dgtl In	HiZ digital	HiZ Analog Unb
34	P5[7]	GPIO [unused]			HiZ Analog Unb
35	P15[6]	USB IO [unused]			HiZ Analog Unb
36	P15[7]	USB IO [unused]			HiZ Analog Unb
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	P4_3	Dgtl Out	Strong drive	HiZ Analog Unb
43	P15[1]	P4_4	Dgtl Out	Strong drive	HiZ Analog Unb
44	P3[0]	P4_5	Dgtl Out	Strong drive	HiZ Analog Unb
45	P3[1]	P4_6	Dgtl Out	Strong drive	HiZ Analog Unb
46	P3[2]	P4_7	Dgtl Out	Strong drive	HiZ Analog Unb
47	P3[3]	P4_8	Dgtl Out	Strong drive	HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
48	P3[4]	P4_9	Dgtl Out	Strong drive	HiZ Analog Unb
49	P3[5]	P4_10	Dgtl Out	Strong drive	HiZ Analog Unb
50	VDDIO3	VDDIO3	Power		
51	P3[6]	P4_11	Dgtl Out	Strong drive	HiZ Analog Unb
52	P3[7]	P4_12	Dgtl Out	Strong drive	HiZ Analog Unb
53	P12[0]	P4_13	Dgtl Out	Strong drive	HiZ Analog Unb
54	P12[1]	P4_14	Dgtl Out	Strong drive	HiZ Analog Unb
55	P15[2]	P4_15	Dgtl Out	Strong drive	HiZ Analog Unb
56	P15[3]	P4_16	Dgtl Out	Strong drive	HiZ Analog Unb
63	VCCA	VCCA	Power		
64	VSSA	VSSA	Power		
65	VDDA	VDDA	Power		
66	VSSD	VSSD	Power		
67	P12[2]	P3_3	Dgtl Out	Strong drive	HiZ Analog Unb
68	P12[3]	P3_4	Dgtl Out	Strong drive	HiZ Analog Unb
69	P4[0]	P3_5	Dgtl Out	Strong drive	HiZ Analog Unb
70	P4[1]	P3_6	Dgtl Out	Strong drive	HiZ Analog Unb
71	P0[0]	P3_7	Dgtl Out	Strong drive	HiZ Analog Unb
72	P0[1]	P3_8	Dgtl Out	Strong drive	HiZ Analog Unb
73	P0[2]	P3_9	Dgtl Out	Strong drive	HiZ Analog Unb
74	P0[3]	P3_10	Dgtl Out	Strong drive	HiZ Analog Unb
75	VDDIO0	VDDIO0	Power		
76	P0[4]	P3_11	Dgtl Out	Strong drive	HiZ Analog Unb
77	P0[5]	P3_12	Dgtl Out	Strong drive	HiZ Analog Unb
78	P0[6]	P3_13	Dgtl Out	Strong drive	HiZ Analog Unb
79	P0[7]	P3_14	Dgtl Out	Strong drive	HiZ Analog Unb
80	P4[2]	P3_15	Dgtl Out	Strong drive	HiZ Analog Unb
81	P4[3]	P3_16	Dgtl Out	Strong drive	HiZ Analog Unb
82	P4[4]	P3_17	Dgtl Out	Strong drive	HiZ Analog Unb
83	P4[5]	P3_18	Dgtl Out	Strong drive	HiZ Analog Unb
84	P4[6]	GPIO [unused]			HiZ Analog Unb
85	P4[7]	GPIO [unused]			HiZ Analog Unb
86	VCCD	VCCD	Power		
87	VSSD	VSSD	Power		
88	VDDD	VDDD	Power		
89	P6[0]	GPIO [unused]			HiZ Analog Unb
90	P6[1]	GPIO [unused]			HiZ Analog Unb
91	P6[2]	GPIO [unused]			HiZ Analog Unb
92	P6[3]	GPIO [unused]			HiZ Analog Unb
93	P15[4]	GPIO [unused]			HiZ Analog Unb
94	P15[5]	GPIO [unused]			HiZ Analog Unb
95	P2[0]	RP_GPIO_21	Dgtl In	Res pull up	HiZ Analog Unb
96	P2[1]	RP_GPIO_26	Dgtl In	Res pull up	HiZ Analog Unb
97	P2[2]	RP_GPIO_20	Dgtl In	Res pull up	HiZ Analog Unb
98	P2[3]	RP_GPIO_19	Dgtl In	Res pull up	HiZ Analog Unb
99	P2[4]	RP_GPIO_16	Dgtl In	Res pull up	HiZ Analog Unb
100	VDDIO2	VDDIO2	Power		

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Res pull up/down = Resistive pull up/down
- Dgtl I/O = Digital In/Out

- OD, DL = Open drain, drives low
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	71	P3_7	Dgtl Out	Strong drive	HiZ Analog Unb
P0[1]	72	P3_8	Dgtl Out	Strong drive	HiZ Analog Unb
P0[2]	73	P3_9	Dgtl Out	Strong drive	HiZ Analog Unb
P0[3]	74	P3_10	Dgtl Out	Strong drive	HiZ Analog Unb
P0[4]	76	P3_11	Dgtl Out	Strong drive	HiZ Analog Unb
P0[5]	77	P3_12	Dgtl Out	Strong drive	HiZ Analog Unb
P0[6]	78	P3_13	Dgtl Out	Strong drive	HiZ Analog Unb
P0[7]	79	P3_14	Dgtl Out	Strong drive	HiZ Analog Unb
P1[0]	20	Debug:SWD_IO	Reserved		
P1[1]	21	Debug:SWD_CK	Reserved		
P1[2]	22	GPIO [unused]			HiZ Analog Unb
P1[3]	23	Debug:SWV	Reserved		
P1[4]	24	GPIO [unused]			HiZ Analog Unb
P1[5]	25	RP_GPIO_27	Dgtl In	Res pull up	HiZ Analog Unb
P1[6]	27	RP_GPIO_18	Dgtl In	Res pull up	HiZ Analog Unb
P1[7]	28	RP_GPIO_17	Dgtl In	Res pull up	HiZ Analog Unb
P12[0]	53	P4_13	Dgtl Out	Strong drive	HiZ Analog Unb
P12[1]	54	P4_14	Dgtl Out	Strong drive	HiZ Analog Unb
P12[2]	67	P3_3	Dgtl Out	Strong drive	HiZ Analog Unb
P12[3]	68	P3_4	Dgtl Out	Strong drive	HiZ Analog Unb
P12[4]	4	SCL_1	Dgtl I/O	OD, DL	HiZ Analog Unb
P12[5]	5	SDA_1	Dgtl I/O	OD, DL	HiZ Analog Unb
P12[6]	29	SIO [unused]			HiZ Analog Unb
P12[7]	30	SIO [unused]			HiZ Analog Unb
P15[0]	42	P4_3	Dgtl Out	Strong drive	HiZ Analog Unb
P15[1]	43	P4_4	Dgtl Out	Strong drive	HiZ Analog Unb
P15[2]	55	P4_15	Dgtl Out	Strong drive	HiZ Analog Unb
P15[3]	56	P4_16	Dgtl Out	Strong drive	HiZ Analog Unb
P15[4]	93	GPIO [unused]			HiZ Analog Unb
P15[5]	94	GPIO [unused]			HiZ Analog Unb
P15[6]	35	USB IO [unused]			HiZ Analog Unb
P15[7]	36	USB IO [unused]			HiZ Analog Unb
P2[0]	95	RP_GPIO_21	Dgtl In	Res pull up	HiZ Analog Unb
P2[1]	96	RP_GPIO_26	Dgtl In	Res pull up	HiZ Analog Unb
P2[2]	97	RP_GPIO_20	Dgtl In	Res pull up	HiZ Analog Unb
P2[3]	98	RP_GPIO_19	Dgtl In	Res pull up	HiZ Analog Unb
P2[4]	99	RP_GPIO_16	Dgtl In	Res pull up	HiZ Analog Unb
P2[5]	1	RP_GPIO_13	Dgtl In	Res pull up	HiZ Analog Unb
P2[6]	2	RP_GPIO_12	Dgtl In	Res pull up	HiZ Analog Unb
P2[7]	3	RP_GPIO_6	Dgtl In	Res pull up/down	HiZ Analog Unb
P3[0]	44	P4_5	Dgtl Out	Strong drive	HiZ Analog Unb
P3[1]	45	P4_6	Dgtl Out	Strong drive	HiZ Analog Unb
P3[2]	46	P4_7	Dgtl Out	Strong drive	HiZ Analog Unb
P3[3]	47	P4_8	Dgtl Out	Strong drive	HiZ Analog Unb
P3[4]	48	P4_9	Dgtl Out	Strong drive	HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P3[5]	49	P4_10	Dgtl Out	Strong drive	HiZ Analog Unb
P3[6]	51	P4_11	Dgtl Out	Strong drive	HiZ Analog Unb
P3[7]	52	P4_12	Dgtl Out	Strong drive	HiZ Analog Unb
P4[0]	69	P3_5	Dgtl Out	Strong drive	HiZ Analog Unb
P4[1]	70	P3_6	Dgtl Out	Strong drive	HiZ Analog Unb
P4[2]	80	P3_15	Dgtl Out	Strong drive	HiZ Analog Unb
P4[3]	81	P3_16	Dgtl Out	Strong drive	HiZ Analog Unb
P4[4]	82	P3_17	Dgtl Out	Strong drive	HiZ Analog Unb
P4[5]	83	P3_18	Dgtl Out	Strong drive	HiZ Analog Unb
P4[6]	84	GPIO [unused]			HiZ Analog Unb
P4[7]	85	GPIO [unused]			HiZ Analog Unb
P5[0]	16	RP_GPIO_25	Dgtl In	Res pull up	HiZ Analog Unb
P5[1]	17	RP_GPIO_24	Dgtl In	HiZ digital	HiZ Analog Unb
P5[2]	18	RP_GPIO_23	Dgtl In	Res pull up	HiZ Analog Unb
P5[3]	19	RP_GPIO_22	Dgtl In	Res pull up	HiZ Analog Unb
P5[4]	31	LED5_4	Dgtl Out	Strong drive	HiZ Analog Unb
P5[5]	32	GPIO [unused]			HiZ Analog Unb
P5[6]	33	RP_GPIO_5	Dgtl In	HiZ digital	HiZ Analog Unb
P5[7]	34	GPIO [unused]			HiZ Analog Unb
P6[0]	89	GPIO [unused]			HiZ Analog Unb
P6[1]	90	GPIO [unused]			HiZ Analog Unb
P6[2]	91	GPIO [unused]			HiZ Analog Unb
P6[3]	92	GPIO [unused]			HiZ Analog Unb
P6[4]	6	GPIO [unused]			HiZ Analog Unb
P6[5]	7	GPIO [unused]			HiZ Analog Unb
P6[6]	8	GPIO [unused]			HiZ Analog Unb
P6[7]	9	GPIO [unused]			HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Dgtl I/O = Digital In/Out
- OD, DL = Open drain, drives low
- Res pull up/down = Resistive pull up/down
- HiZ digital = High impedance digital

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
GPIO [unused]	P5[5]		HiZ Analog Unb
GPIO [unused]	P5[7]		HiZ Analog Unb
GPIO [unused]	P1[2]		HiZ Analog Unb
GPIO [unused]	P4[6]		HiZ Analog Unb
GPIO [unused]	P1[4]		HiZ Analog Unb
GPIO [unused]	P6[2]		HiZ Analog Unb
GPIO [unused]	P6[7]		HiZ Analog Unb
GPIO [unused]	P6[0]		HiZ Analog Unb
GPIO [unused]	P6[1]		HiZ Analog Unb
GPIO [unused]	P6[4]		HiZ Analog Unb
GPIO [unused]	P6[5]		HiZ Analog Unb
GPIO [unused]	P6[6]		HiZ Analog Unb
GPIO [unused]	P15[4]		HiZ Analog Unb
GPIO [unused]	P4[7]		HiZ Analog Unb
GPIO [unused]	P15[5]		HiZ Analog Unb
GPIO [unused]	P6[3]		HiZ Analog Unb
LED5_4	P5[4]	Dgtl Out	HiZ Analog Unb
P3_10	P0[3]	Dgtl Out	HiZ Analog Unb
P3_11	P0[4]	Dgtl Out	HiZ Analog Unb
P3_12	P0[5]	Dgtl Out	HiZ Analog Unb
P3_13	P0[6]	Dgtl Out	HiZ Analog Unb
P3_14	P0[7]	Dgtl Out	HiZ Analog Unb
P3_15	P4[2]	Dgtl Out	HiZ Analog Unb
P3_16	P4[3]	Dgtl Out	HiZ Analog Unb
P3_17	P4[4]	Dgtl Out	HiZ Analog Unb
P3_18	P4[5]	Dgtl Out	HiZ Analog Unb
P3_3	P12[2]	Dgtl Out	HiZ Analog Unb
P3_4	P12[3]	Dgtl Out	HiZ Analog Unb
P3_5	P4[0]	Dgtl Out	HiZ Analog Unb
P3_6	P4[1]	Dgtl Out	HiZ Analog Unb
P3_7	P0[0]	Dgtl Out	HiZ Analog Unb
P3_8	P0[1]	Dgtl Out	HiZ Analog Unb
P3_9	P0[2]	Dgtl Out	HiZ Analog Unb
P4_10	P3[5]	Dgtl Out	HiZ Analog Unb
P4_11	P3[6]	Dgtl Out	HiZ Analog Unb
P4_12	P3[7]	Dgtl Out	HiZ Analog Unb
P4_13	P12[0]	Dgtl Out	HiZ Analog Unb
P4_14	P12[1]	Dgtl Out	HiZ Analog Unb
P4_15	P15[2]	Dgtl Out	HiZ Analog Unb
P4_16	P15[3]	Dgtl Out	HiZ Analog Unb
P4_3	P15[0]	Dgtl Out	HiZ Analog Unb
P4_4	P15[1]	Dgtl Out	HiZ Analog Unb

Name	Port	Type	Reset State
P4_5	P3[0]	Dgtl Out	HiZ Analog Unb
P4_6	P3[1]	Dgtl Out	HiZ Analog Unb
P4_7	P3[2]	Dgtl Out	HiZ Analog Unb
P4_8	P3[3]	Dgtl Out	HiZ Analog Unb
P4_9	P3[4]	Dgtl Out	HiZ Analog Unb
RP_GPIO_12	P2[6]	Dgtl In	HiZ Analog Unb
RP_GPIO_13	P2[5]	Dgtl In	HiZ Analog Unb
RP_GPIO_16	P2[4]	Dgtl In	HiZ Analog Unb
RP_GPIO_17	P1[7]	Dgtl In	HiZ Analog Unb
RP_GPIO_18	P1[6]	Dgtl In	HiZ Analog Unb
RP_GPIO_19	P2[3]	Dgtl In	HiZ Analog Unb
RP_GPIO_20	P2[2]	Dgtl In	HiZ Analog Unb
RP_GPIO_21	P2[0]	Dgtl In	HiZ Analog Unb
RP_GPIO_22	P5[3]	Dgtl In	HiZ Analog Unb
RP_GPIO_23	P5[2]	Dgtl In	HiZ Analog Unb
RP_GPIO_24	P5[1]	Dgtl In	HiZ Analog Unb
RP_GPIO_25	P5[0]	Dgtl In	HiZ Analog Unb
RP_GPIO_26	P2[1]	Dgtl In	HiZ Analog Unb
RP_GPIO_27	P1[5]	Dgtl In	HiZ Analog Unb
RP_GPIO_5	P5[6]	Dgtl In	HiZ Analog Unb
RP_GPIO_6	P2[7]	Dgtl In	HiZ Analog Unb
SCL_1	P12[4]	Dgtl I/O	HiZ Analog Unb
SDA_1	P12[5]	Dgtl I/O	HiZ Analog Unb
SIO [unused]	P12[6]		HiZ Analog Unb
SIO [unused]	P12[7]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- Dgtl I/O = Digital In/Out

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

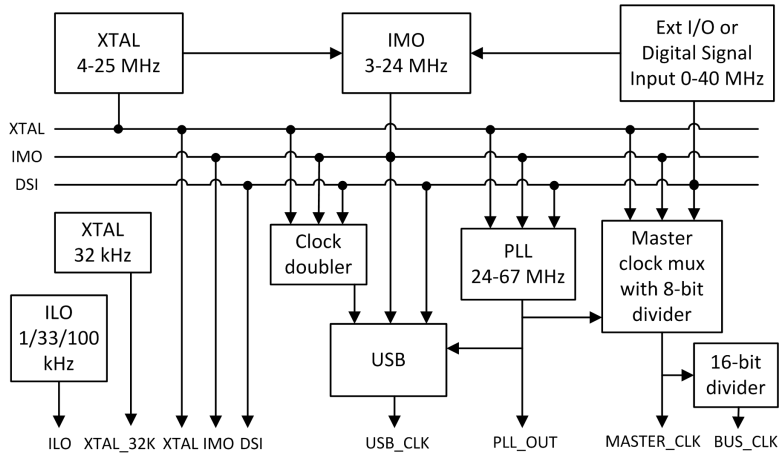
Name	Value
VDDA (V)	5.0
VDDD (V)	5.0
VDDIO0 (V)	5.0
VDDIO1 (V)	5.0
VDDIO2 (V)	5.0
VDDIO3 (V)	5.0
Variable VDDA	False
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	24 MHz	±1	True	True
PLL_OUT	DIGITAL	IMO	24 MHz	24 MHz	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	24 MHz	±1	True	True
IMO	DIGITAL		3 MHz	3 MHz	±1	True	True
ILO	DIGITAL		? MHz	1 kHz	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48 MHz	? MHz	±0	False	False
XTAL	DIGITAL		24 MHz	? MHz	±0	False	False
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

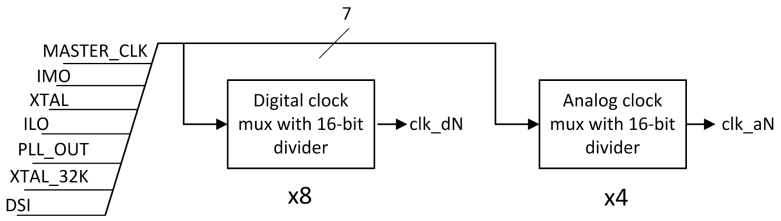


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
I2C_1_BusClock	DIGITAL	BUS_CLK	? MHz	24 MHz	±1	True	True
Clock_1	DIGITAL	ILO	4 Hz	4 Hz	-50,+100	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
I2C_1_I2C_IRQ	15	15	7

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x1FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

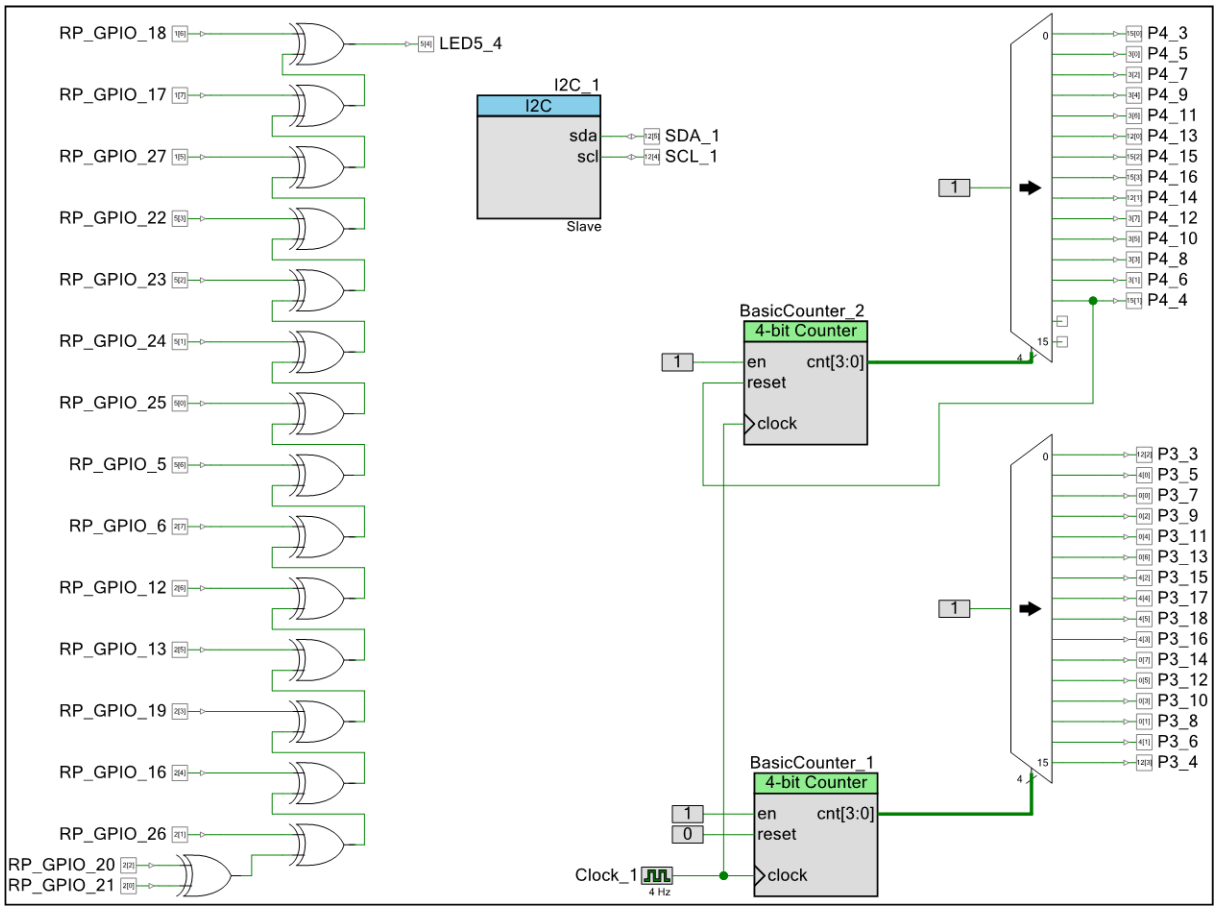
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance BasicCounter_1 (type: BasicCounter_v1_0)
- Instance BasicCounter_2 (type: BasicCounter_v1_0)
- Instance demux_1 (type: demux_v1_10)
- Instance demux_2 (type: demux_v1_10)
- Instance I2C_1 (type: I2C_v3_50)

8 Components

8.1 Component type: BasicCounter [v1.0]

8.1.1 Instance BasicCounter_1

Description: Basic Counter
Instance type: BasicCounter [v1.0]
Datasheet: online component datasheet for BasicCounter

Table 13. Component Parameters for BasicCounter_1

Parameter Name	Value	Description
User Comments		Instance-specific comments.
Width	4	Width of the counter. Must be between 2 and 32.

8.1.2 Instance BasicCounter_2

Description: Basic Counter
Instance type: BasicCounter [v1.0]
Datasheet: online component datasheet for BasicCounter

Table 14. Component Parameters for BasicCounter_2

Parameter Name	Value	Description
User Comments		Instance-specific comments.
Width	4	Width of the counter. Must be between 2 and 32.

8.2 Component type: demux [v1.10]

8.2.1 Instance demux_1

Description: De-Multiplexer with configurable number of output terminals and terminal width.
Instance type: demux [v1.10]
Datasheet: online component datasheet for demux

Table 15. Component Parameters for demux_1

Parameter Name	Value	Description
NumOutputTerminals	16	Number of output terminals of the De-Multiplexer. Acceptable values are 2, 4, 8 and 16.
TerminalWidth	1	Width of each terminal
User Comments		Instance-specific comments.

8.2.2 Instance demux_2

Description: De-Multiplexer with configurable number of output terminals and terminal width.
Instance type: demux [v1.10]
Datasheet: online component datasheet for demux

Table 16. Component Parameters for demux_2

Parameter Name	Value	Description
NumOutputTerminals	16	Number of output terminals of the De-Multiplexer. Acceptable values are 2, 4, 8 and 16.
TerminalWidth	1	Width of each terminal
User Comments		Instance-specific comments.

8.3 Component type: I2C [v3.50]

8.3.1 Instance I2C_1

Description: Standard I2C communication interface
Instance type: I2C [v3.50]
Datasheet: online component datasheet for I2C

Table 17. Component Parameters for I2C_1

Parameter Name	Value	Description
Address_Decode	Hardware	Determines either hardware or software address match logic.
BusSpeed_kHz	100	I2C Data Rate in kbps. Standard settings are 50, 100, 400 or 1000. The value must be between 1 and 1000.
EnableWakeup	false	Determines if I2C is selected as wakeup source.
ExternalBuffer	false	Exposes scl and sda in and out terminals outside the component.
Externi2cIntrHandler	false	Allows I2C interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
ExternTmoutIntrHandler	false	Allows I2C timeout interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
Hex	true	Indicates that address has been input in hexadecimal format.
I2C_Mode	Slave	Determines I2C mode (Slave/Master/Multi-Master/Multi-Master-Slave).
I2cBusPort	I2C0	Determines which I2C pins have been selected. Select I2C0/I2C1 and connect to corresponding pins to be able use I2C as wakeup source.
Implementation	FixedFunction	Determines either I2C implementation Fixed Function or UDB.
NotSlaveClockMinusTolerance	25	Internal component clock negative tolerance value in Master, Multi-Master or Multi-Master-Slave mode.

Parameter Name	Value	Description
NotSlaveClockPlusTolerance	5	Internal component clock positive tolerance value in Master, Multi-Master or Multi-Master-Slave mode.
PrescalerEnabled	false	Enables prescaler (7-bit counter) to expand timeout timer range.
PrescalerPeriod	3	Prescaler period of timeout timer.
SclTimeoutEnabled	false	Enables low time monitoring of scl line.
SdaTimeoutEnabled	false	Enables low time monitoring of sda line.
Slave_Address	32	7-bits I2C slave address.
SlaveClockMinusTolerance	5	Internal component clock negative tolerance value in Slave mode.
SlaveClockPlusTolerance	50	Internal component clock positive tolerance value in Slave mode.
TimeoutImplementation	UDB	Determines either timeout timer feature implementation as UDB or Fixed Function. The Fixed Function implementation only available for PSoC5LP.
TimeOutms	25	Determines maximum time allowed for scl or sda to be low state (in mS). The timeout timer generates interrupt after timeout expires.
TimeoutPeriodff	39999	Period of timeout timer (Fixed Function).
TimeoutPeriodUdb	39999	Period of timeout timer (UDB).
UdbInternalClock	false	Determines either internal or external clock source for I2C UDB.
UdbSlaveFixedPlacementEnable	false	Enables fixed placement for I2C UDB. Only available in slave mode.
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine