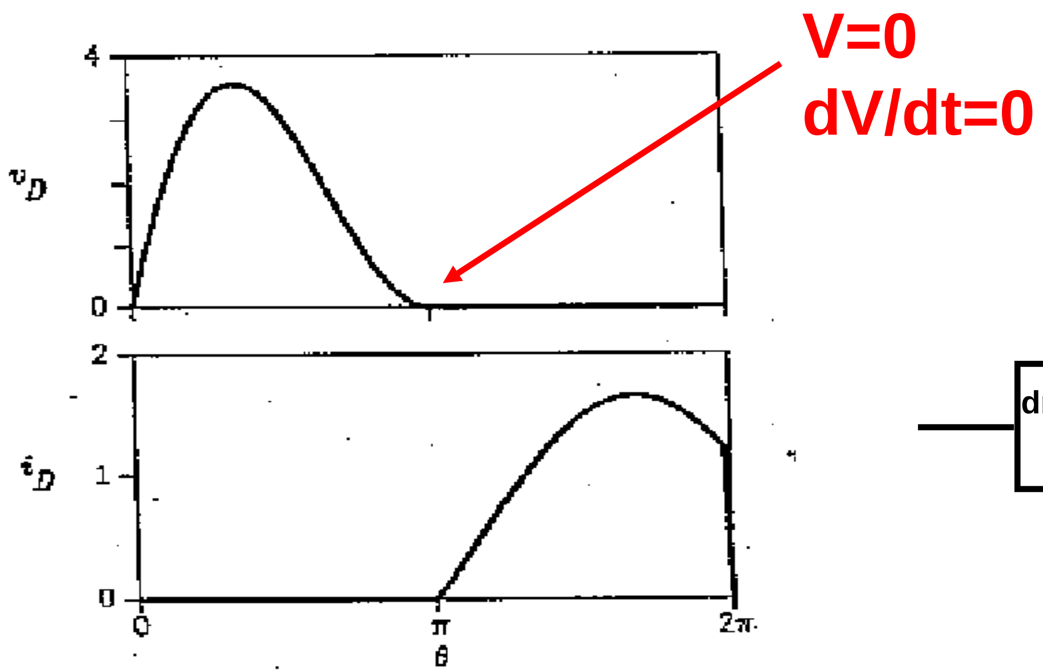
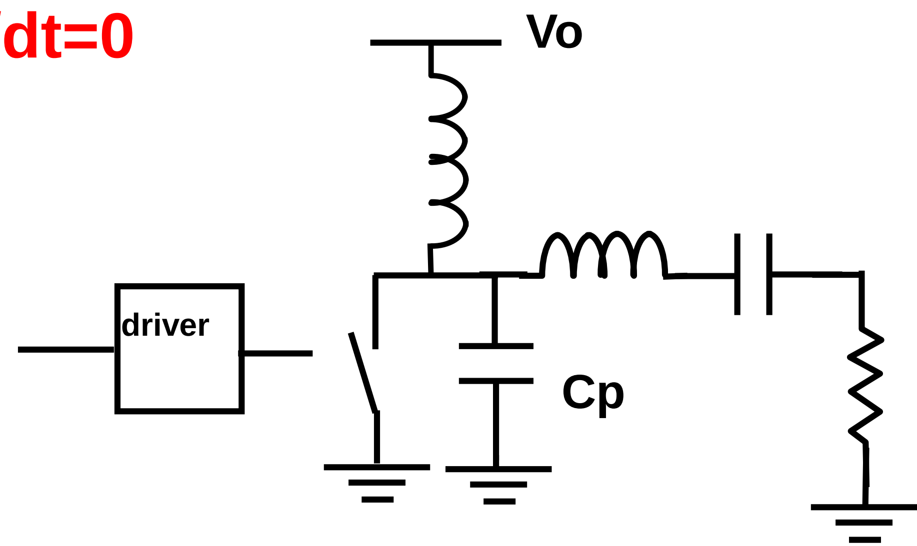
Class E Amplifier

Clever resonant load is constructed so that V(t)=0 when the switch closes!! This avoids $1/2CV^2f$ loss.





- **Voltage across switch is brought to zero when switch closes**

- **dV/dt is also zero when switch closes. This makes operation relatively insensitive to rise time of input.**

Class E Amplifier

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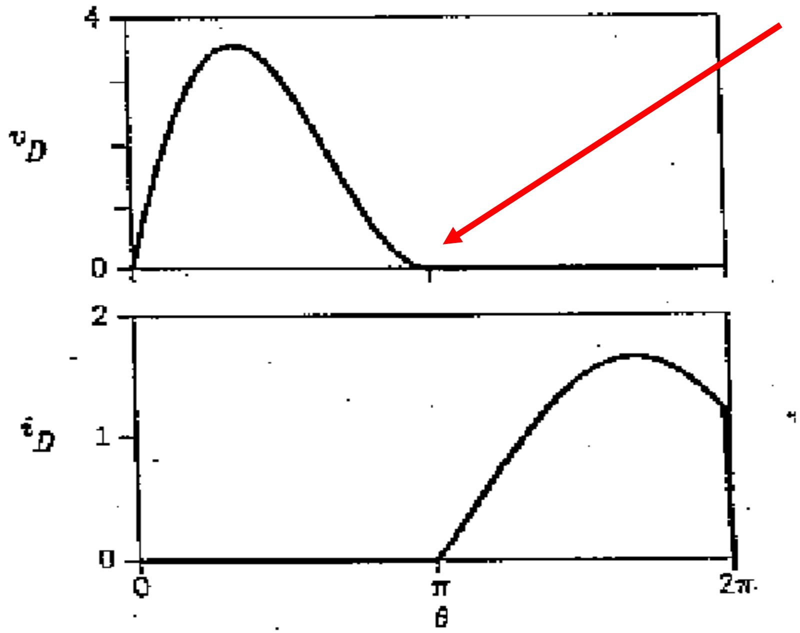
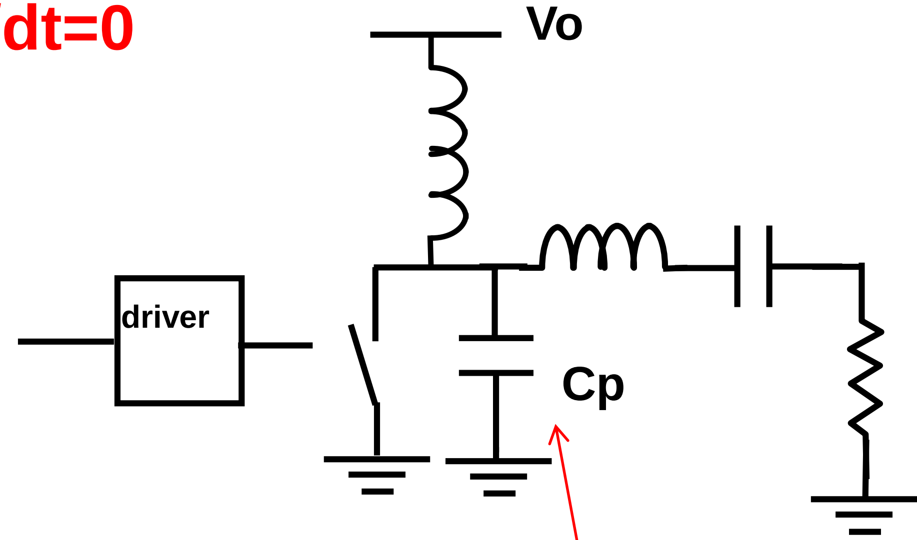


V=0
dV/dt=0



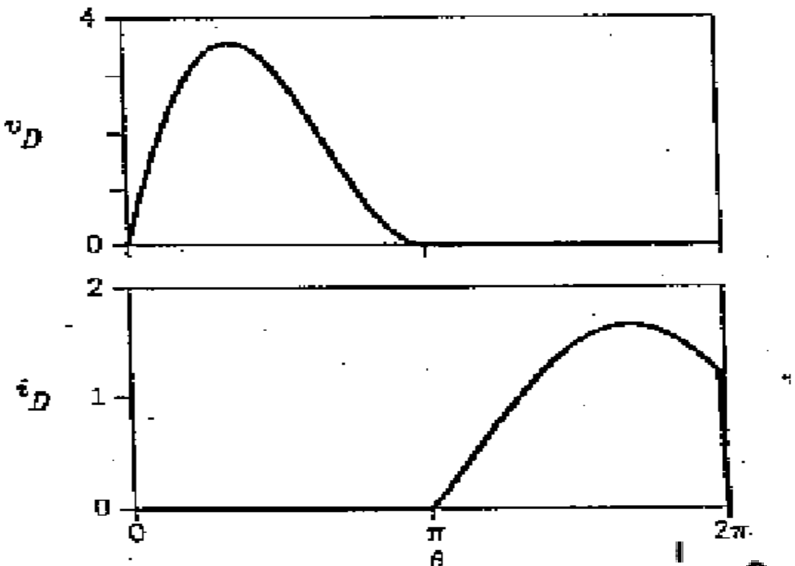
- **Voltage across switch is brought to zero when switch closes**

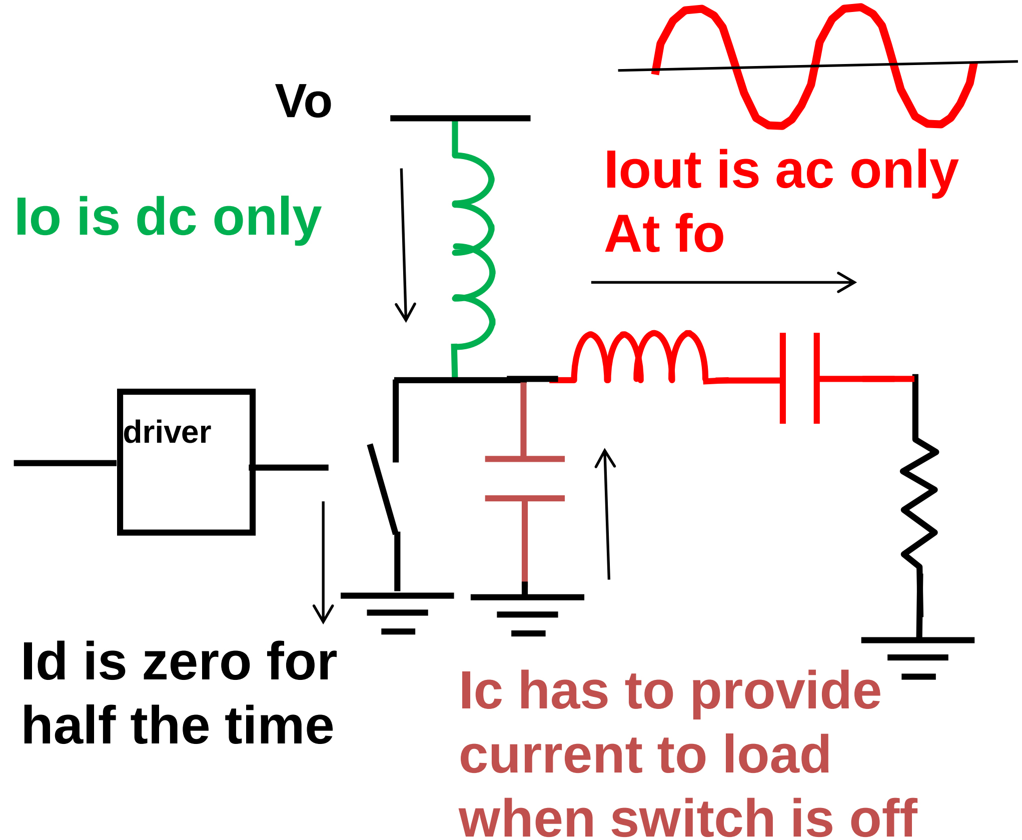
- **dV/dt is also zero when switch closes. This makes operation relatively insensitive to rise time of input.**

This is essential
If device does not have enough Cds then you must add this

Class E Amplifier

- Load current is sinusoidal (just fo) due to filter
- Switch and capacitor provide current during different phases

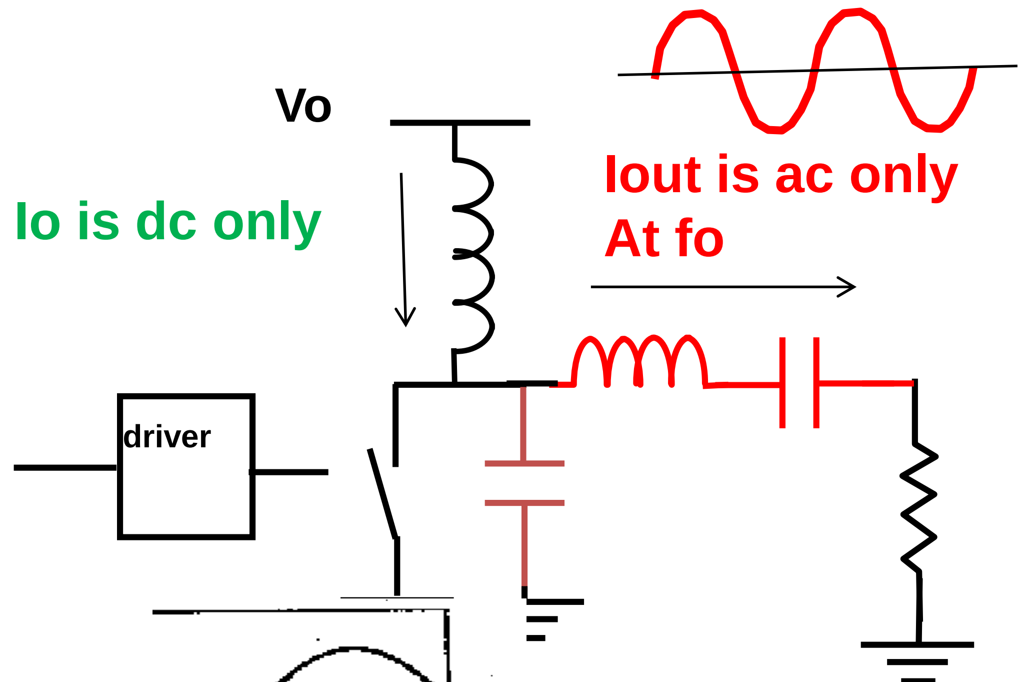


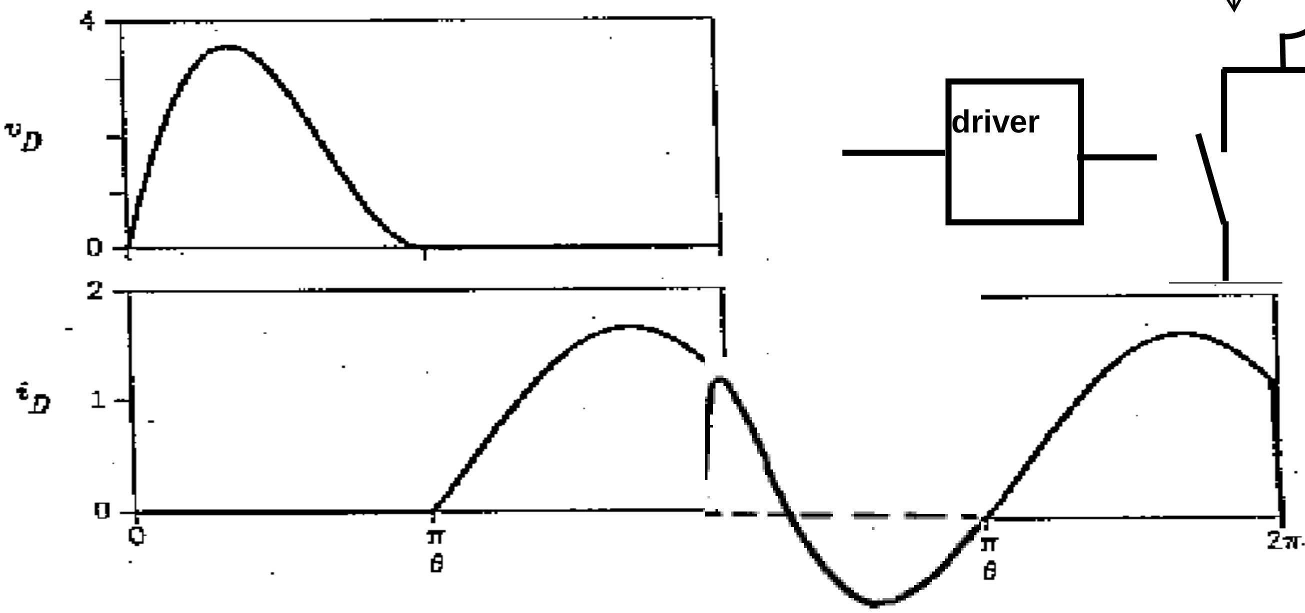


Capacitor current

Class E Amplifier

- Load current is sinusoidal (just fo) due to filter
- Switch and capacitor provide current during different phases

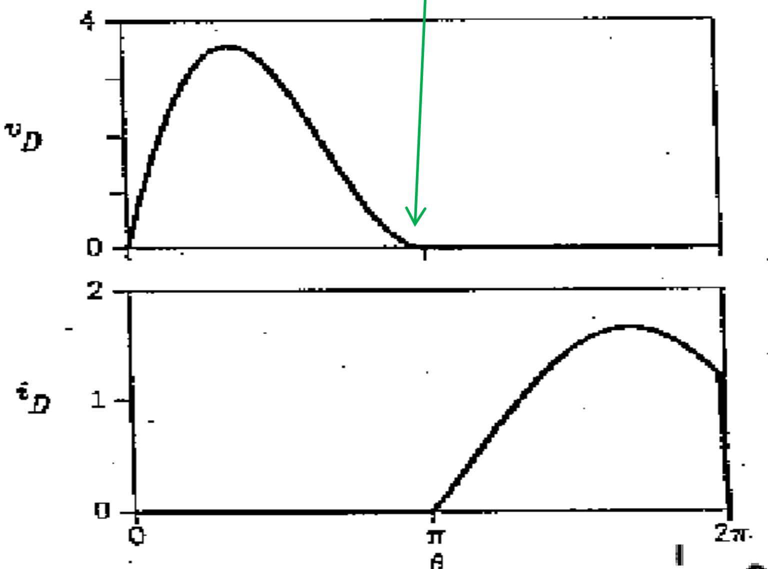




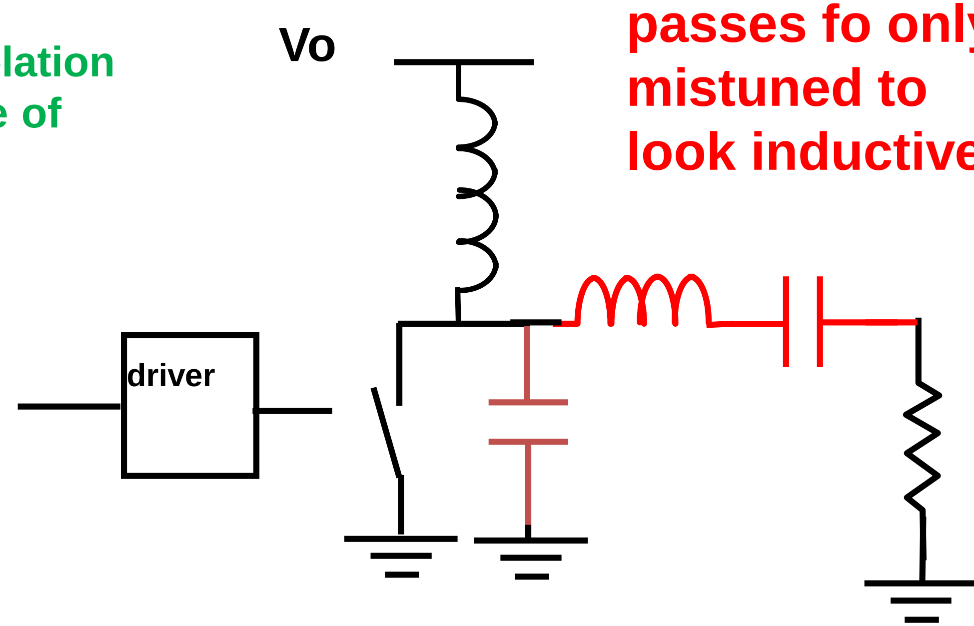
Capacitor current

Class E Amplifier

V=0 and dV/dt =0
are achieved by carefully tuning
Lextra of resonator, Cp and RL in relation
operating frequency (and duty cycle of
switch)



Filter that
passes fo only;
mistuned to
look inductive

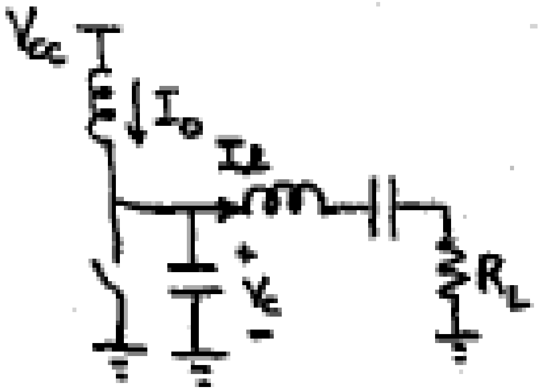


Capacitor C is often just
the output capacitance
of the switch

Capacitor current

Simple Analysis of Class E Amplifier

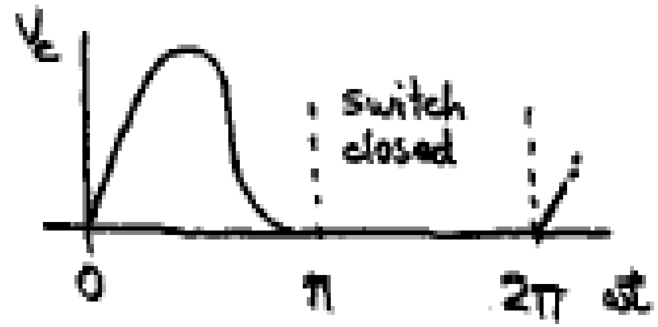
This is done in time domain!



Perfect choke : I_o = constant

Perfect filter : $I_\ell = -I_L \sin(\omega t + \phi)$

$\boxed{\text{Calculate } V_c(t) \text{ when switch is open}}$



$$C \frac{dV_c}{dt} = I_o + I_L \sin(\omega t + \phi)$$

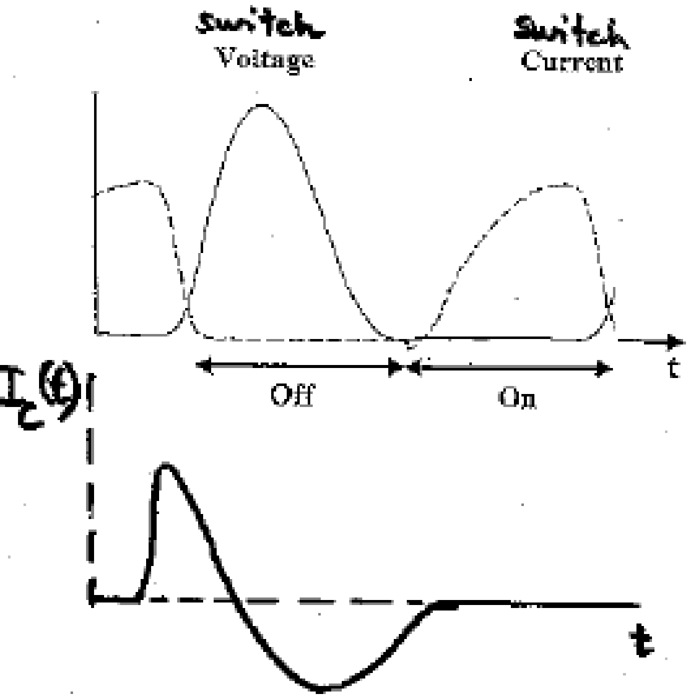
$$V_c(t) = \frac{I_o t}{C} - \frac{I_L}{\omega C}\left[\cos(\omega t + \phi) - \cos\phi\right]$$

Require $V_c = 0$ at $\omega t = \pi$:
$$\frac{I_o}{\omega C}\cdot \pi - \frac{I_L}{\omega C}(-2\cos\phi) = 0$$
$$I_o = -\frac{2}{\pi} I_L \cos\phi$$

Require $\frac{dV_c}{dt} = 0$ at $\omega t = \pi$:
$$I_o + I_L \sin(\pi + \phi) = 0$$
$$I_o = I_L \sin\phi$$

$$-\frac{2}{\pi} = \frac{\sin\phi}{\cos\phi} = \tan\phi$$

Class E Analysis (more)



$$V_c(t) = \frac{I_o t}{C} - \frac{I_L}{\omega C}\left[\cos(\omega t+\phi) - \cos\phi\right] \qquad t<\pi/\omega$$

$$I_o + I_L \sin(\pi+\phi) = 0$$

$$I_o = I_L \sin\phi$$

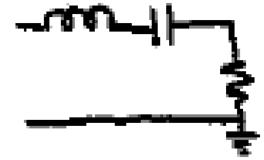
$$-\frac{2}{\pi} = \frac{\sin\phi}{\cos\phi} = \tan\phi$$

$$\phi = -32.5^\circ$$

$$I_L = 1.862\, I_o \qquad I_{peak} = 2.862\, I_o$$

V_{cc} : dc component of $V_c(t) = \dfrac{1}{\pi}\dfrac{I_o}{\omega C}$

V_L : Fourier component at ω of $V_c(t) = \dfrac{0.52\, I_o}{\omega C}$

$Z_L \rightarrow$ 

$$Z_L = \underbrace{\frac{0.18}{\omega C}}_{R_L} + j\frac{0.21}{\omega C}$$

$$P_{out}(\omega) = \frac{1}{2} R_L I_L^2$$

Class E Design Equations

$$Z_{out} = \frac{0.28015}{\omega C} e^{j49.0524^\circ} = \underbrace{\frac{0.18}{\omega C}}_{R_L} + j\frac{0.21}{\omega C}$$

(for fundamental, after Cp)

$$f_{opt} = \frac{I_{\max}}{56.5CV_d}$$

$$\eta_d = \frac{1 + (\pi/2 + \omega C R)^2}{1 + \pi^2/4 \ (1 + \pi \omega C R)^2}$$

Drain efficiency when on-resistance R is included

Class E Features

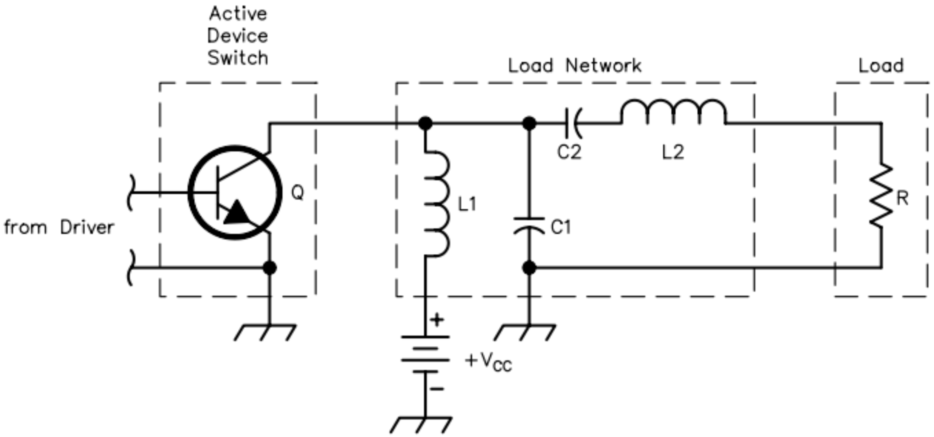
- Efficiency is 100% (ideally) No dissipation in transistor

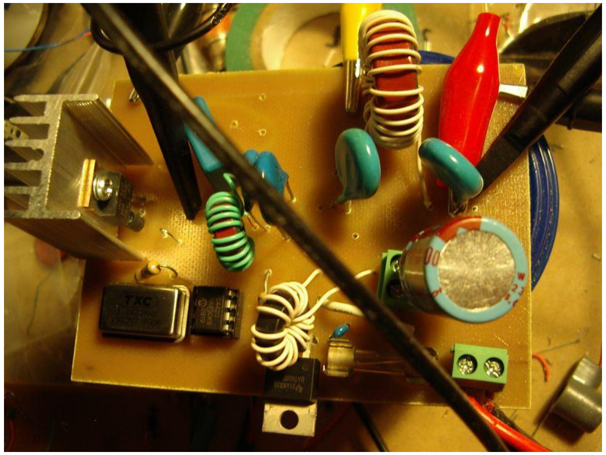
- If frequency changes, then Vce does not quite go to 0
at switching instant => non-zero power dissipation due to $C\Delta V^2$

- Amplitude of output depends on Vcc (not on input amplitude)

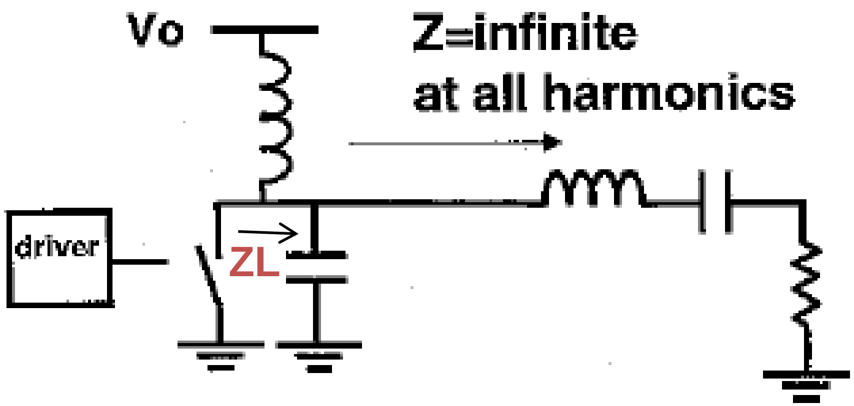
- Pout at fo = 0.78 * 1/8 * Vmax Imax (lower than for Class A)

Nathan Sokal





Another Description of Class E



ZL(f)= RL +jXL

with XL=+0.72 RL

ZL(2f) = - j X2

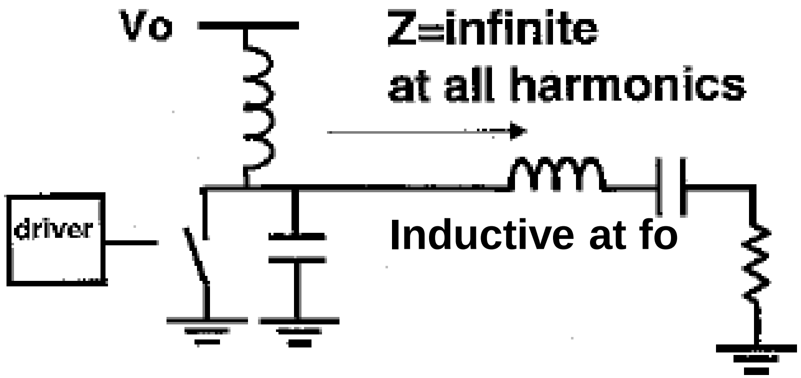
with X2= 1.78 RL

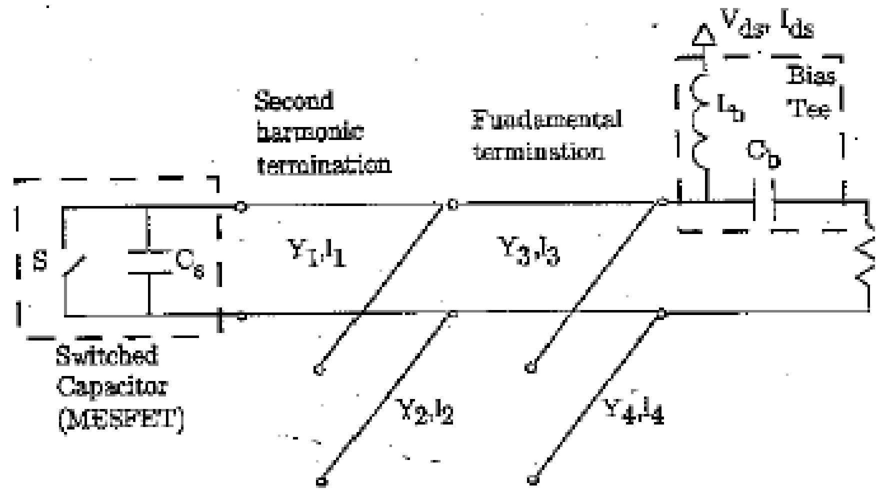
ZL(3f) = -j X3

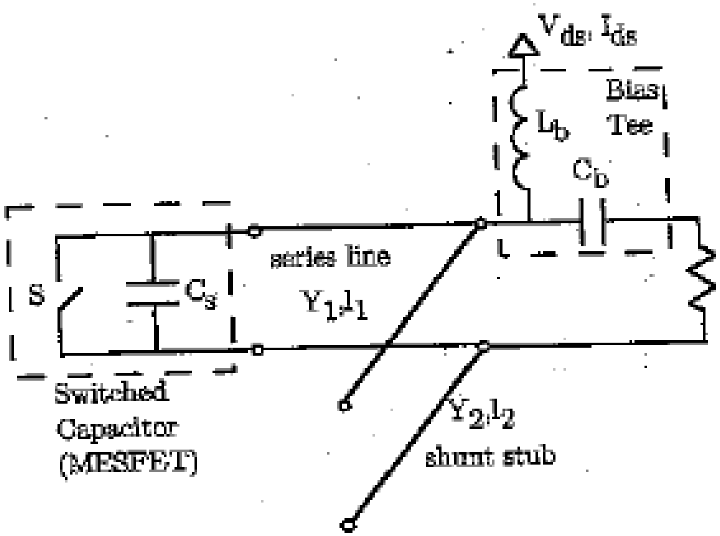
with X3= 1.19 RL

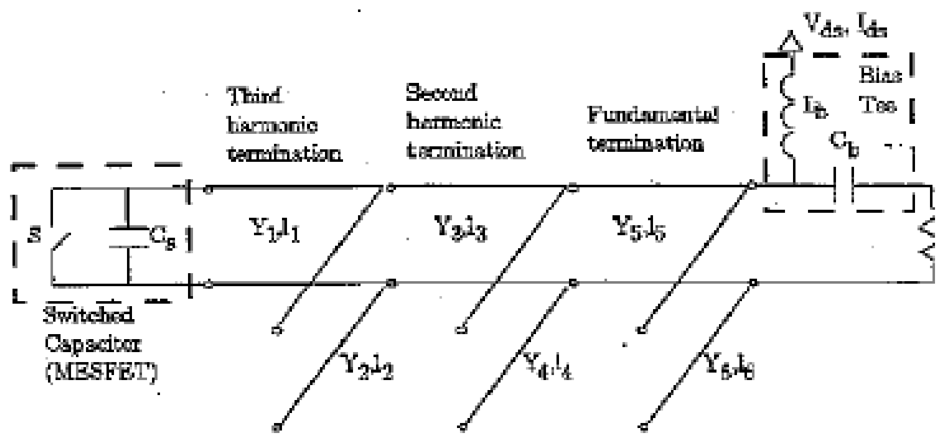
Class E: Additional Implementations

Use transmission lines instead of lumped elements



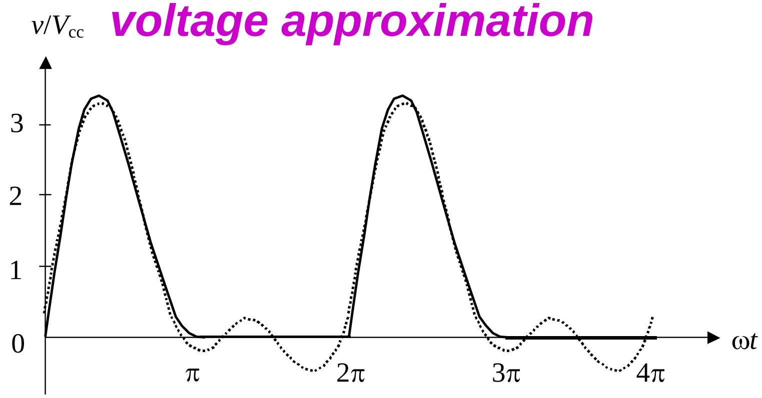


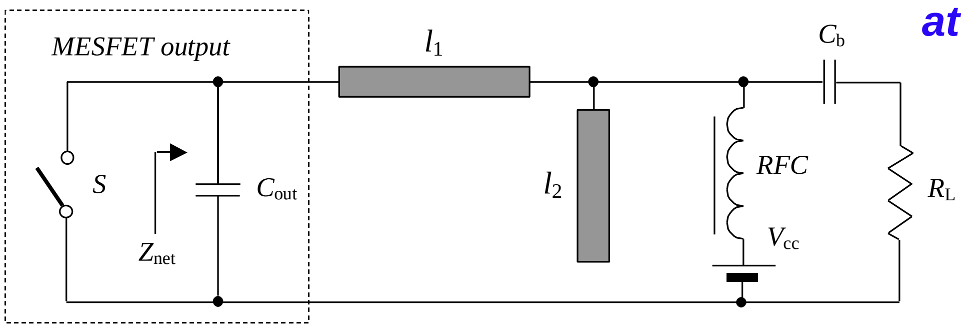


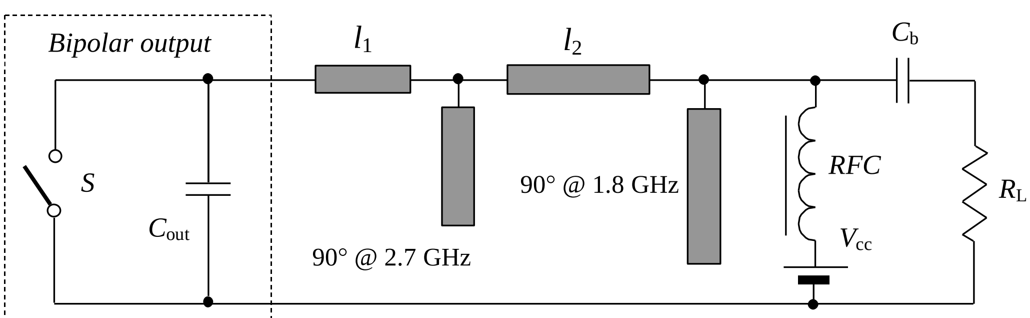


Class E with transmission lines: approximation

Two-harmonic collector voltage approximation







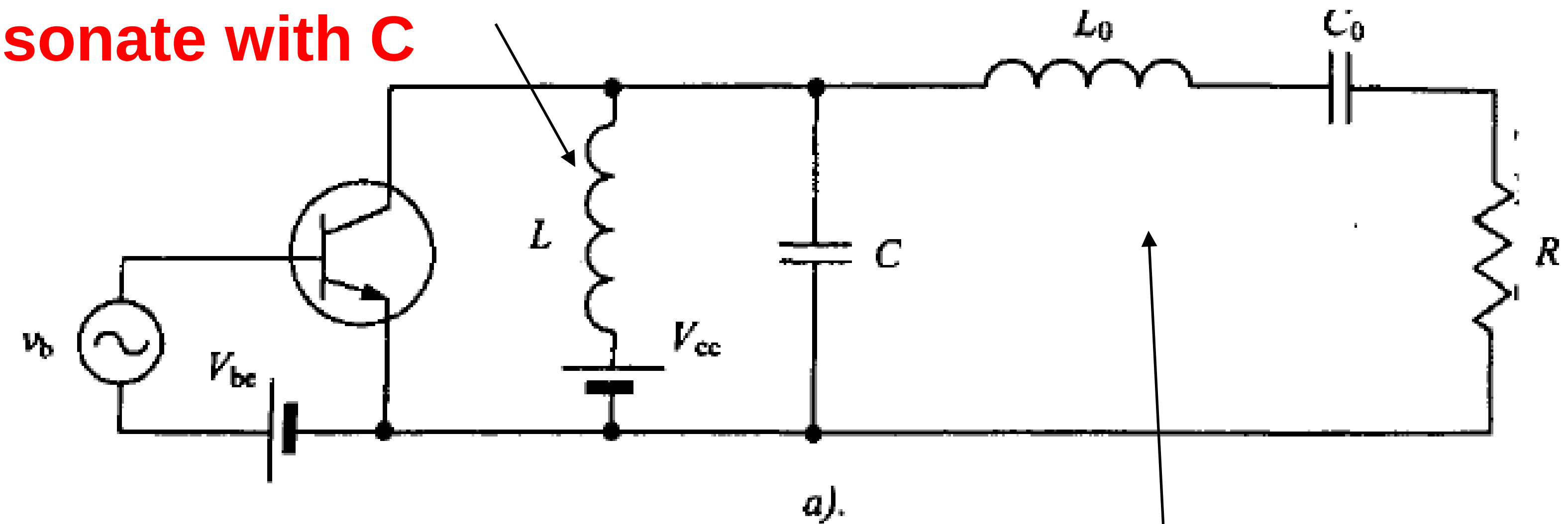
Optimum impedance at fundamental seen by device :

$$Z_{\mathrm{net1}} = R\left(1 + \; j \tan 49.052^{\circ}\right)$$

- ***electrical lengths of transmission lines l_1 and l_2 should be of 45° to provide open circuit seen by device at second harmonic***
- ***their characteristic impedances are chosen to provide optimum inductive impedance seen by device at fundamental***
- ***for three harmonic approximation, additional open circuit transmission line stub with 90-degree electrical length at third harmonic is required (1.5 GHz, 1.5 W, 90%)***

Another Style of Design for Class E

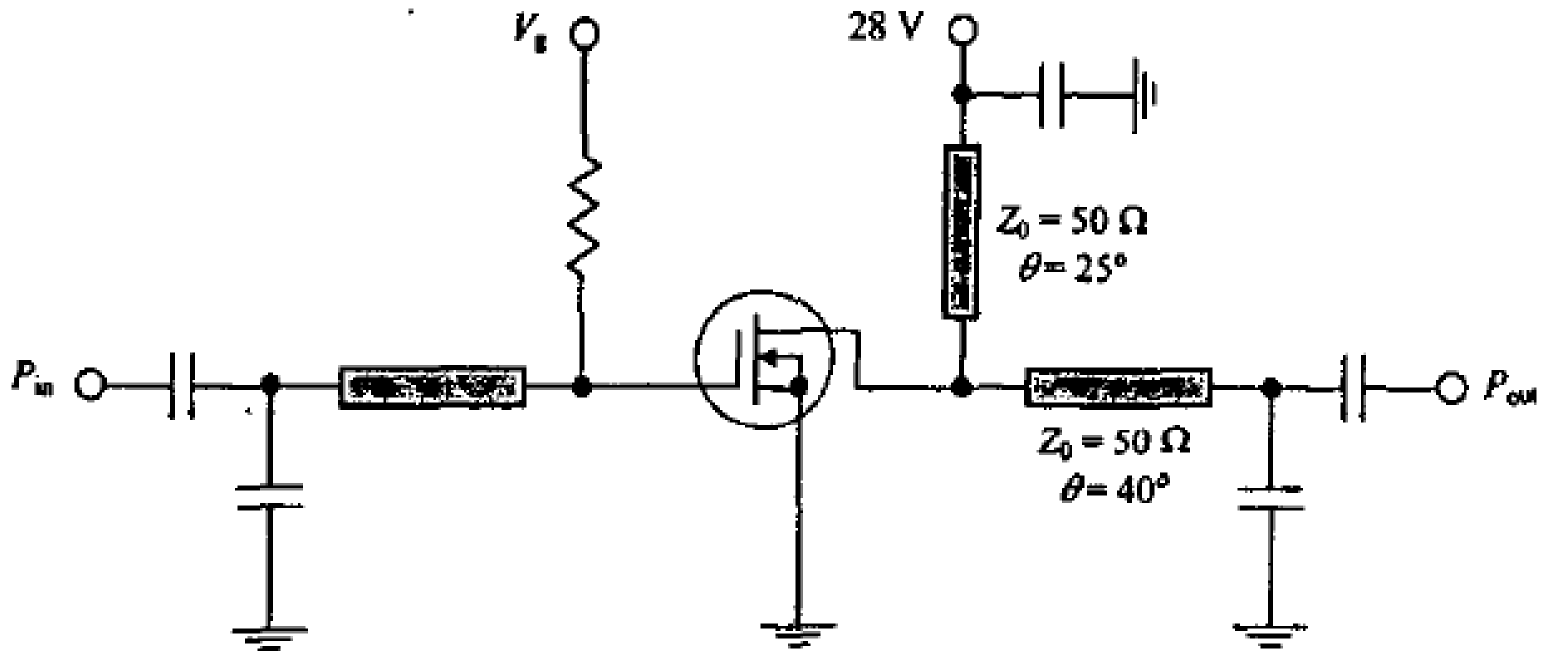
This is not an ideal choke, it is carefully tuned to resonate with C



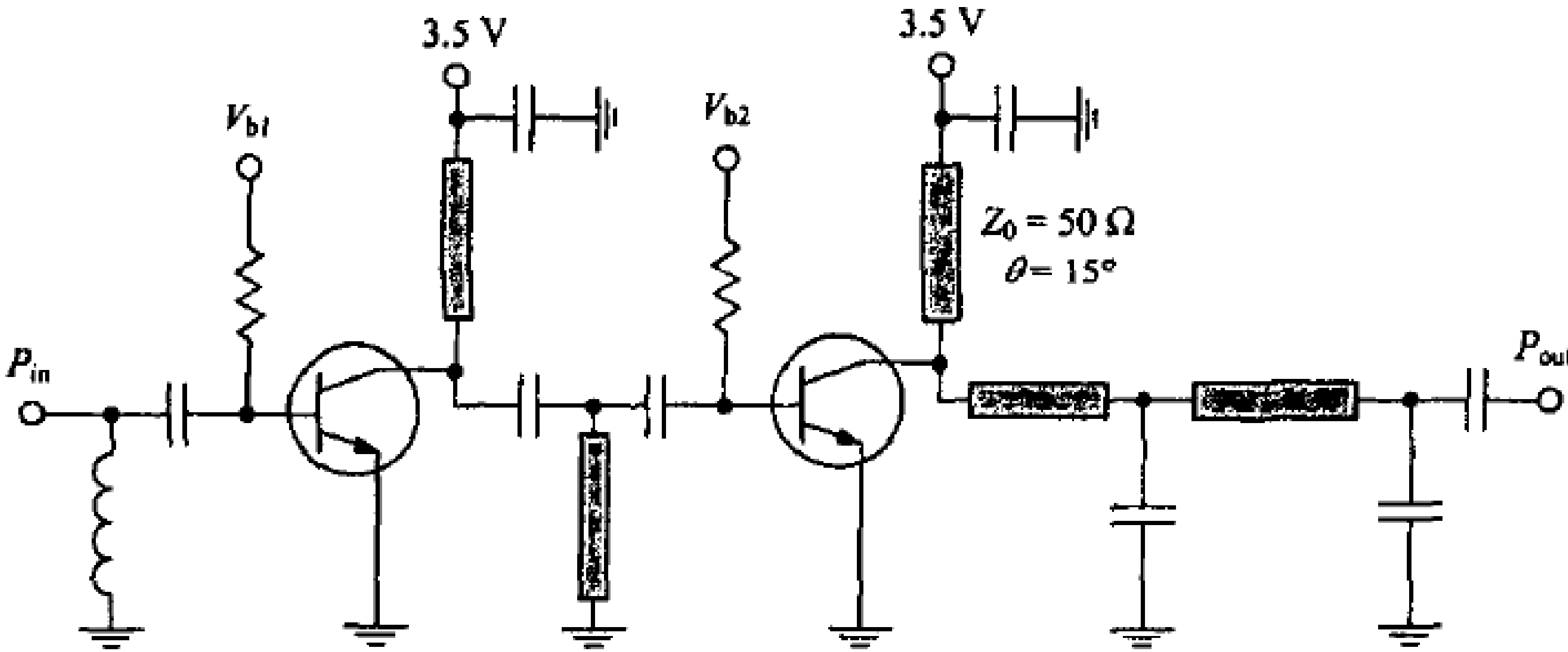
This resonator is tuned to fo
(not mistuned as in classical Class E)

Approach of Grebbenikov and Jaeger

Grebbenikov Design
Implemented with Transmission Lines
for LDMOS Switch



Grebbenikov Design
Implemented with Transmission Lines
And HBTs for handsets

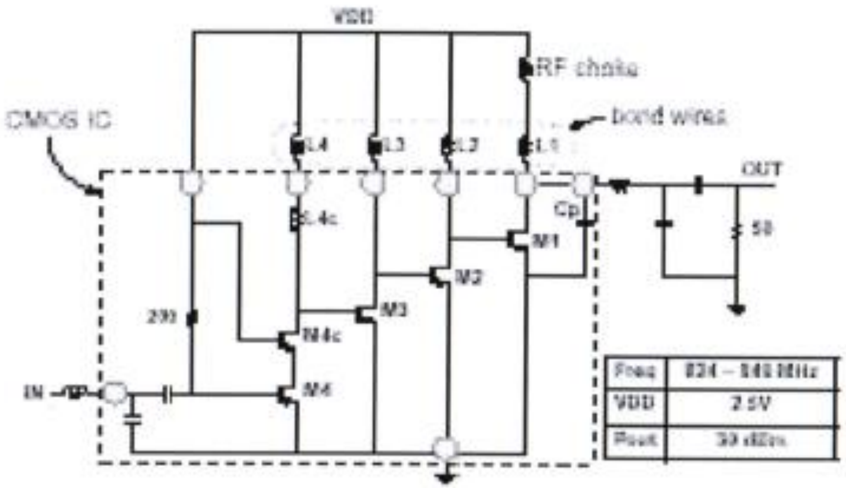


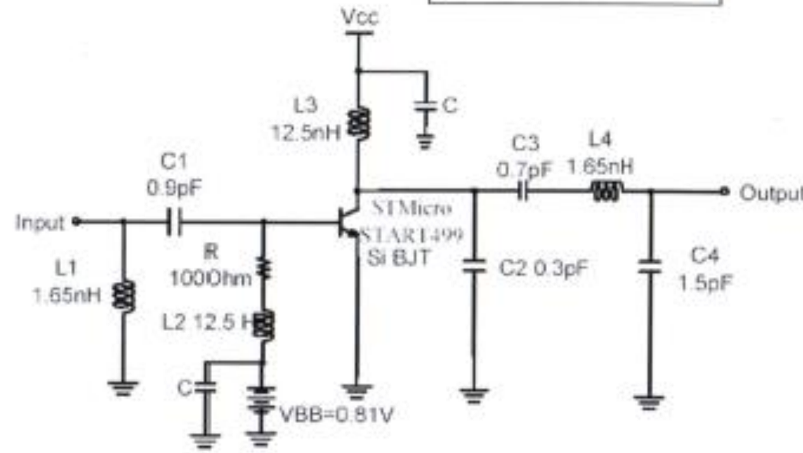
Class E Amplifiers

Experimental Results

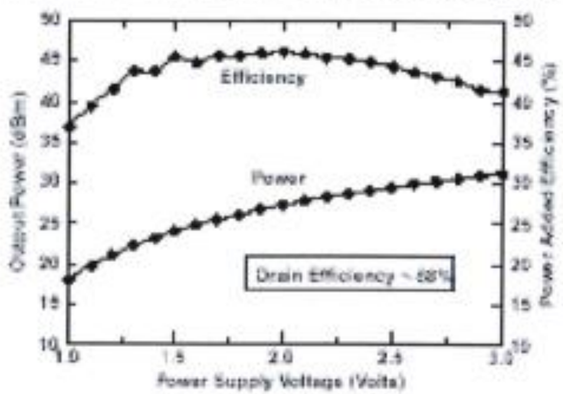
CMOS

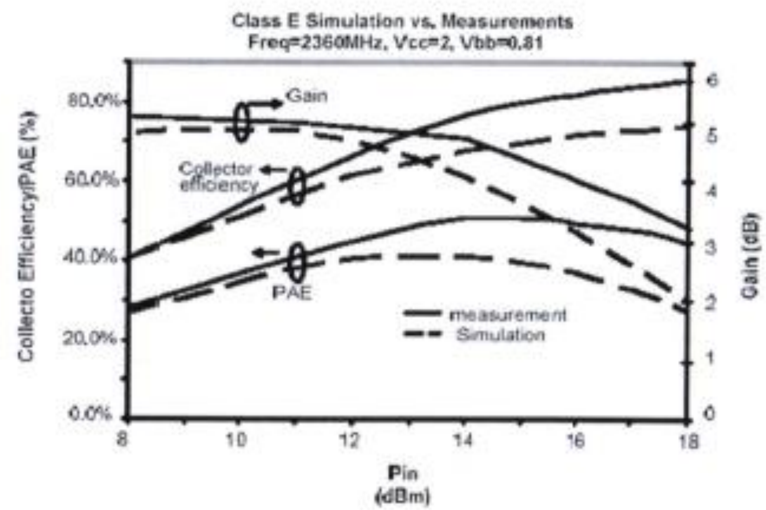
Si BJT





Measured Output Power and Efficiency

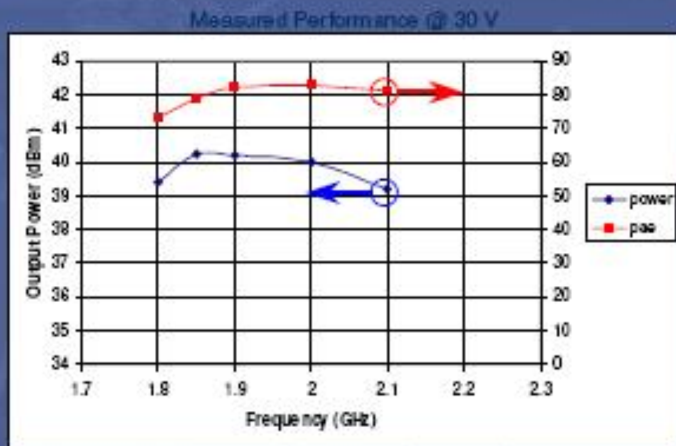


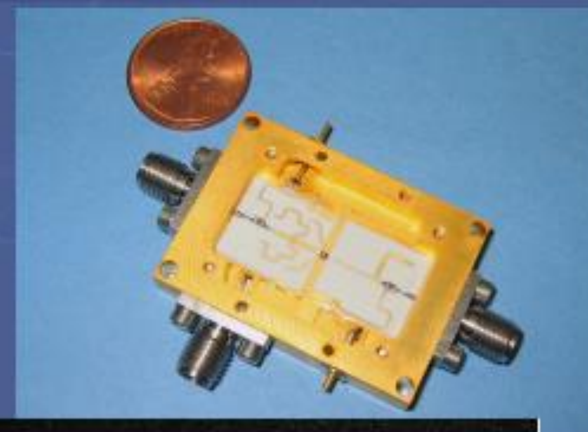


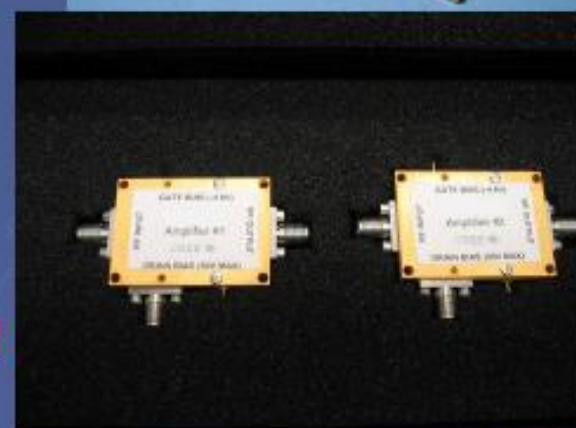
D. Su et al, 1999

Wang, Popp et al IMS2005

World Record 2.0 GHz High Efficiency GaN Amplifier







- Class E Hybrid amplifier
- Vd = 30 volts
- 50Ω input/output
- 10 W P_{OUT}, **88% Drain Efficiency!**
  - 1.9 – 2.1 GHz!

CREE

Design Issues for Class E

1) Peak voltage across switch reaches 3.6 x Vdd for nominal design (so need a high breakdown device)

In presence of output mismatch this can be 5x Vdd or more (it can be risky without an isolator!)

2) There is a maximum frequency possible to achieve class E operation, which depends on Cout and Vdd

For Grebbenikov design, this is

$F_{max} = 0.08 * P_{out} / (C_{out} V_{dd}^2)$

To maximize frequency need to minimize Cout. Chip-on-board could avoid package stray C (but need to get very good die attach for heat sinking)

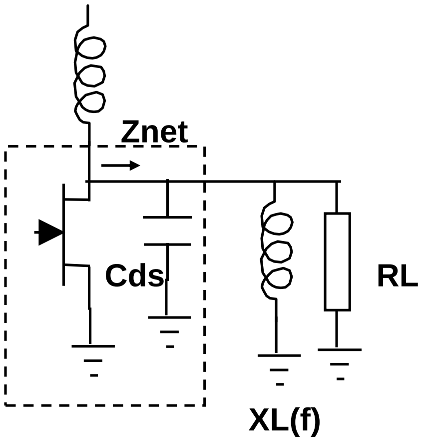
(If try to operate at f above fmax, can get V=0 but not dV/dt=0 when switch closes).

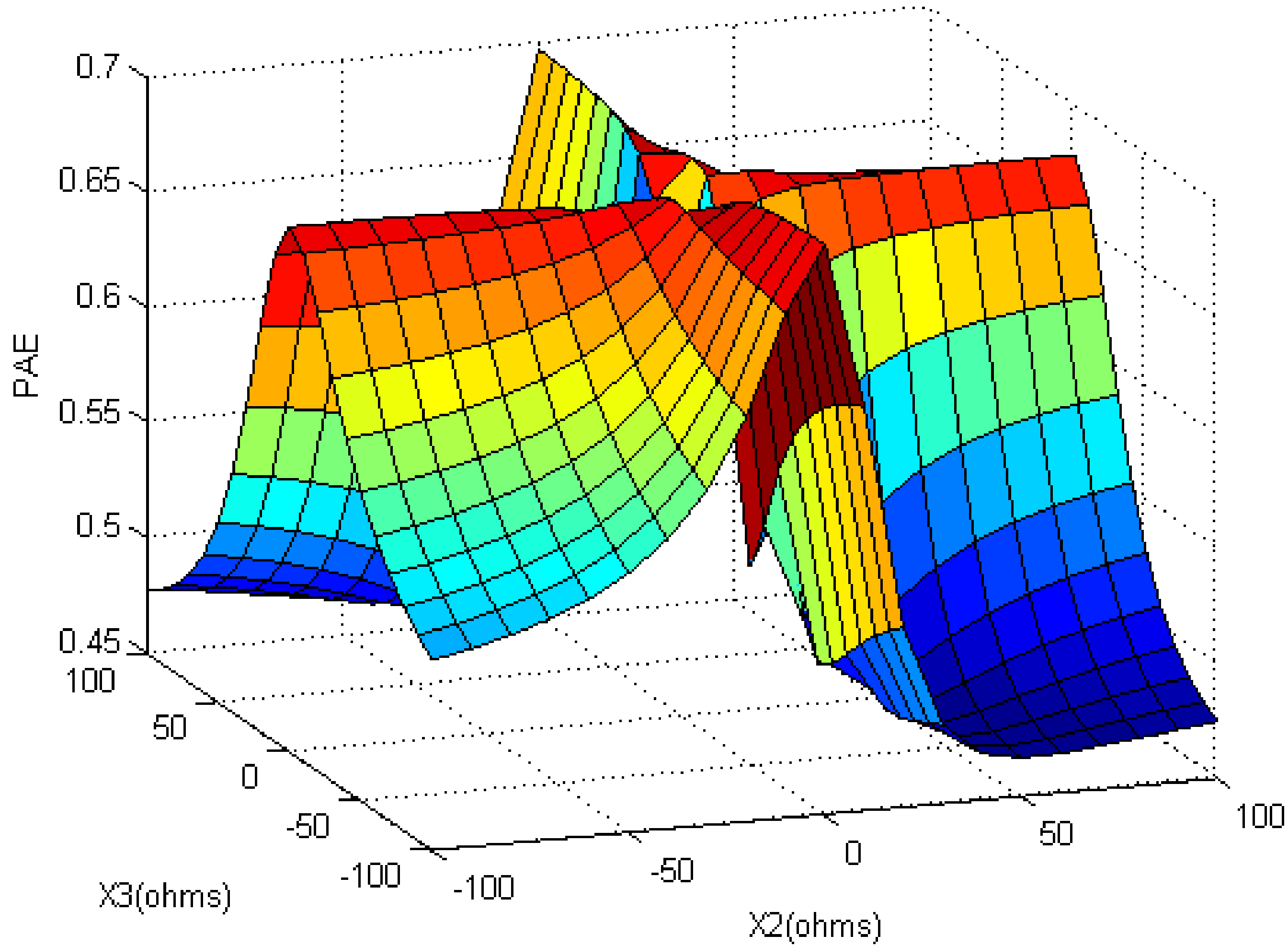
Harmonic Load Tuning

Want to achieve high efficiency mode of operation
Heavy compression - near switching mode

Simulated Efficiency vs Harmonic Load Reactance

X2=Im(Znet) at 2fo
X3=Im(Znet) at 3fo



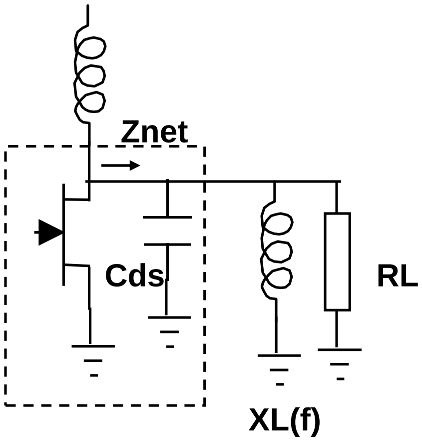


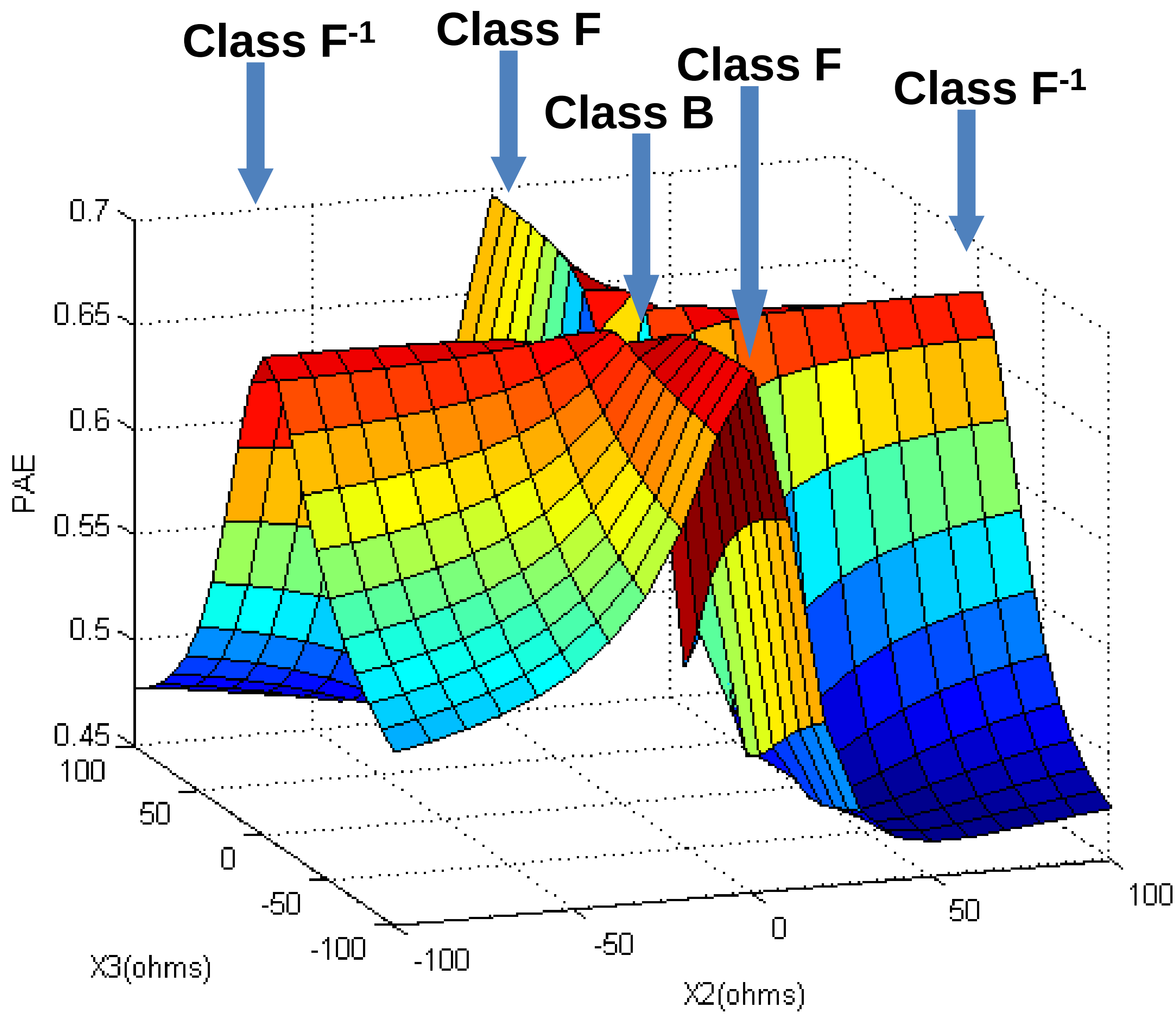
X1=0

Harmonic Load Tuning

Simulated Efficiency vs Harmonic Load Reactance

X2=Im(Znet) at 2fo
X3=Im(Znet) at 3fo

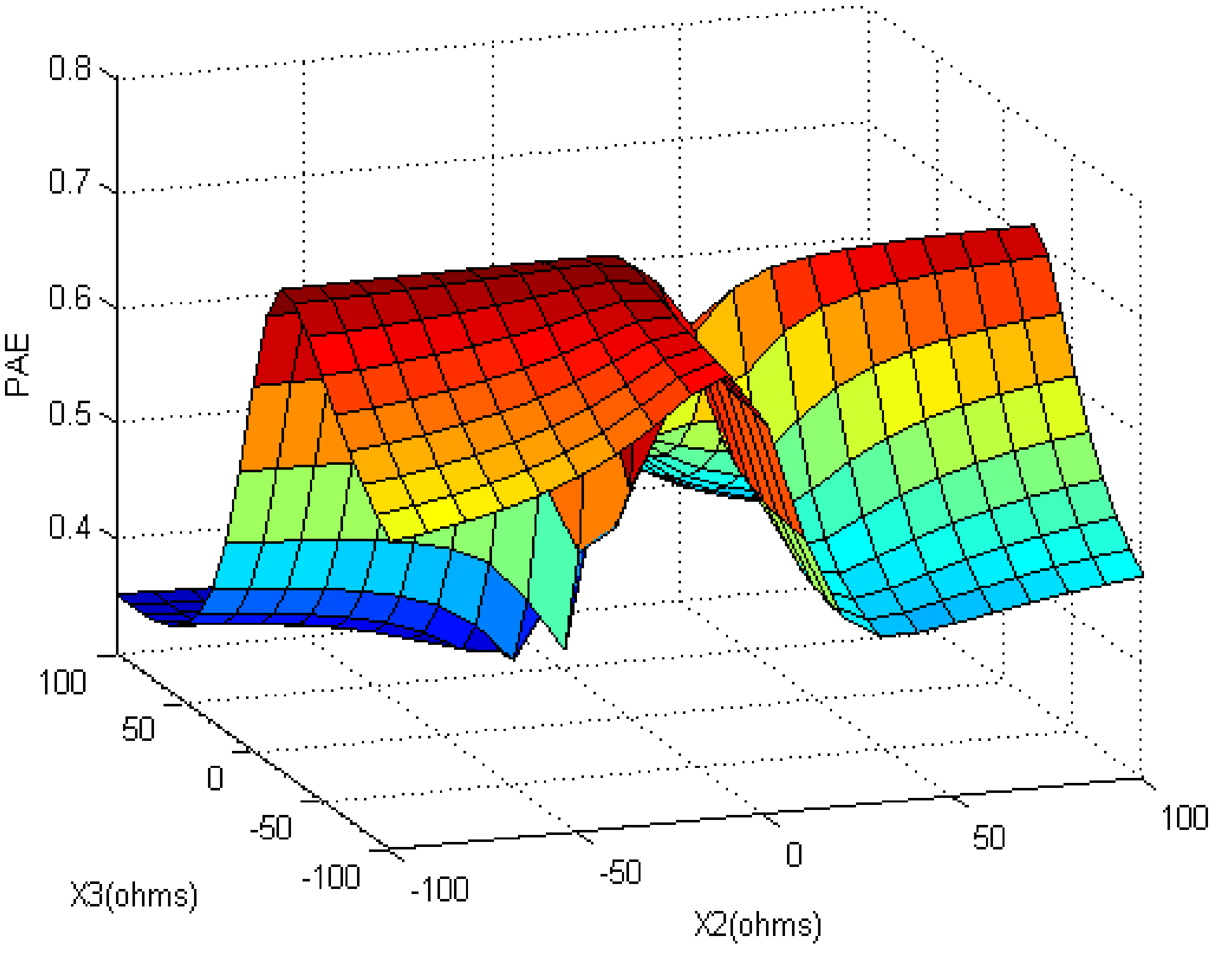




X1=0

Harmonic Load Tuning

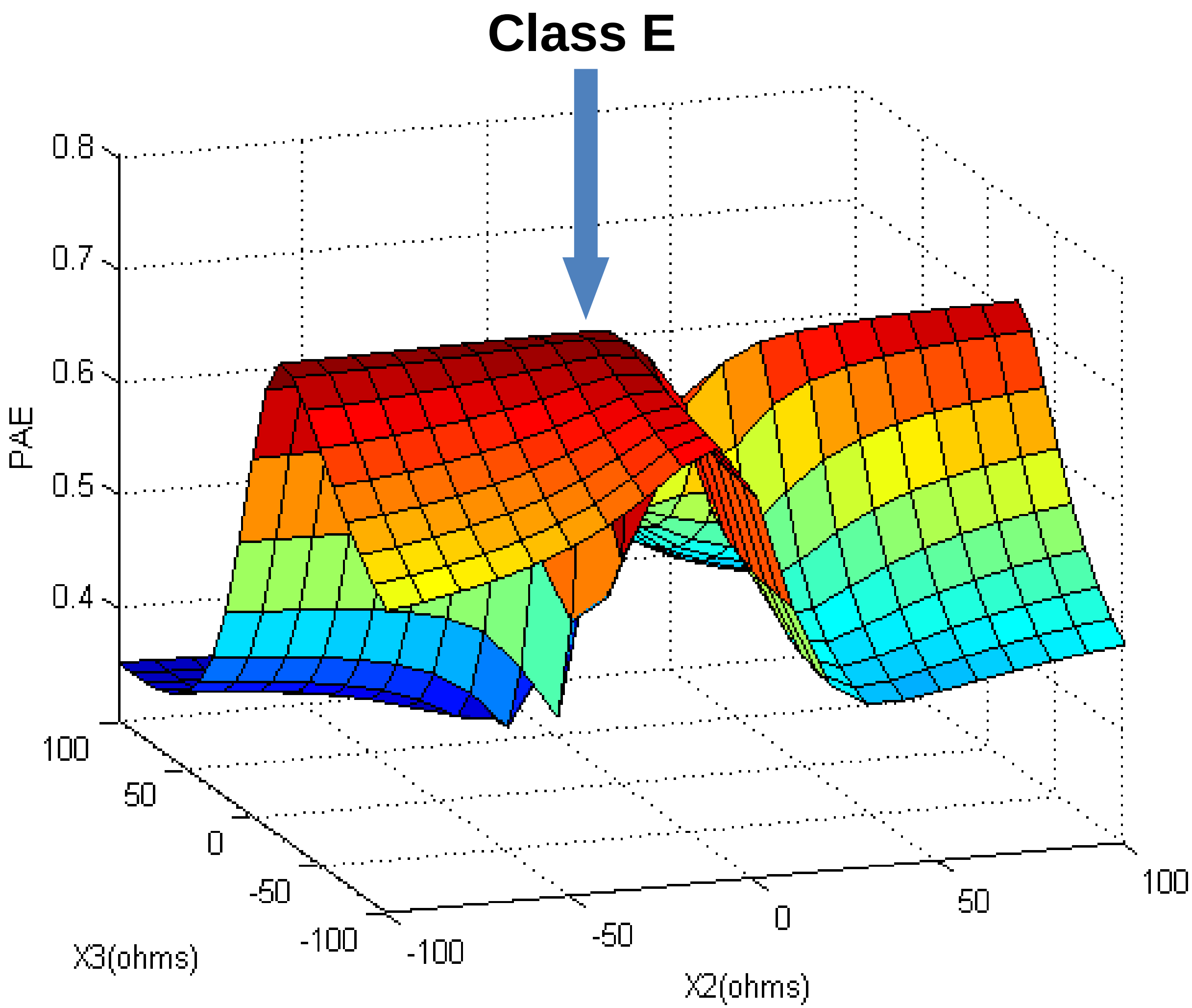
Simulated Efficiency vs Harmonic Load Reactance



X1=RL*0.7

Harmonic Load Tuning

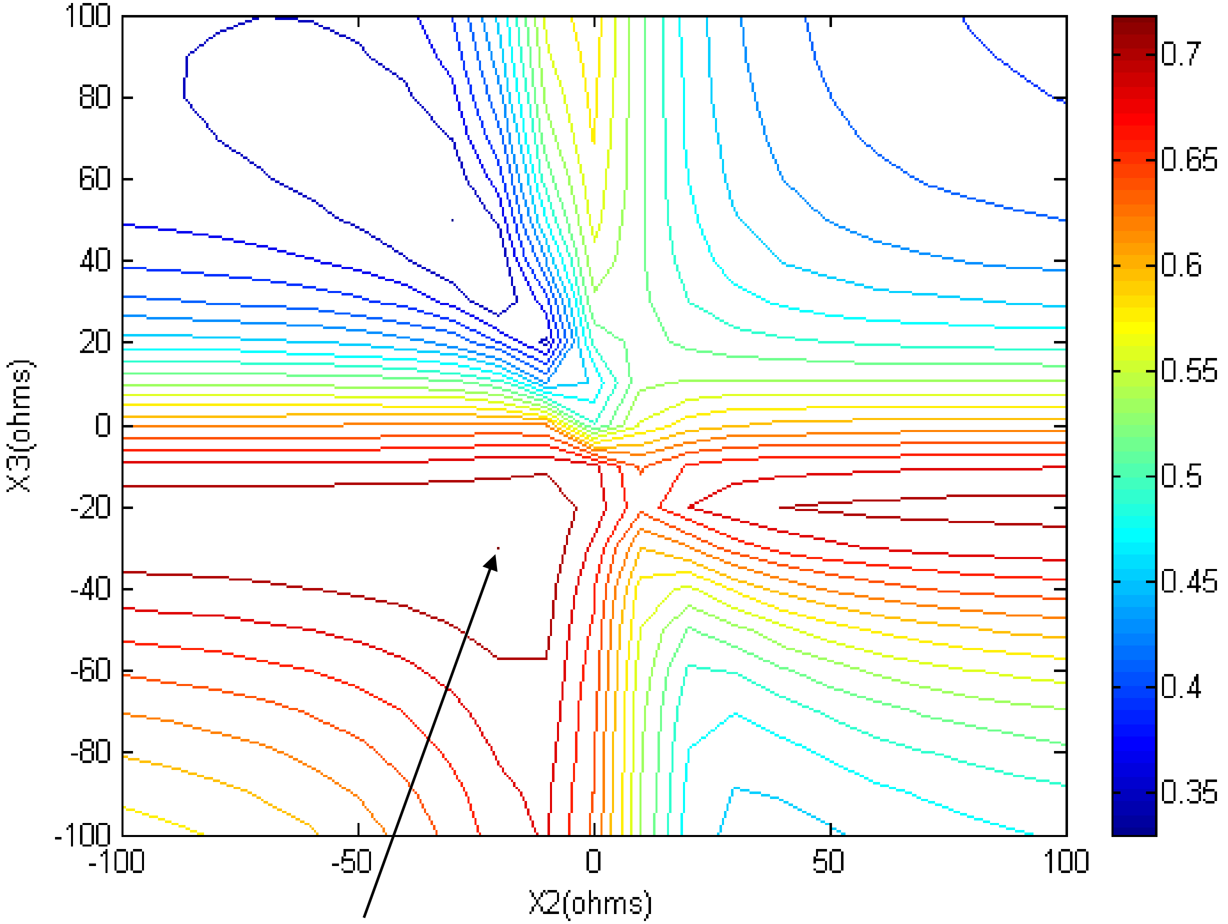
Simulated Efficiency vs Harmonic Load Reactance



X1=RL*0.7

Efficiency Optimization

Contours of PAE Vs X2,X3 (fixed X1)

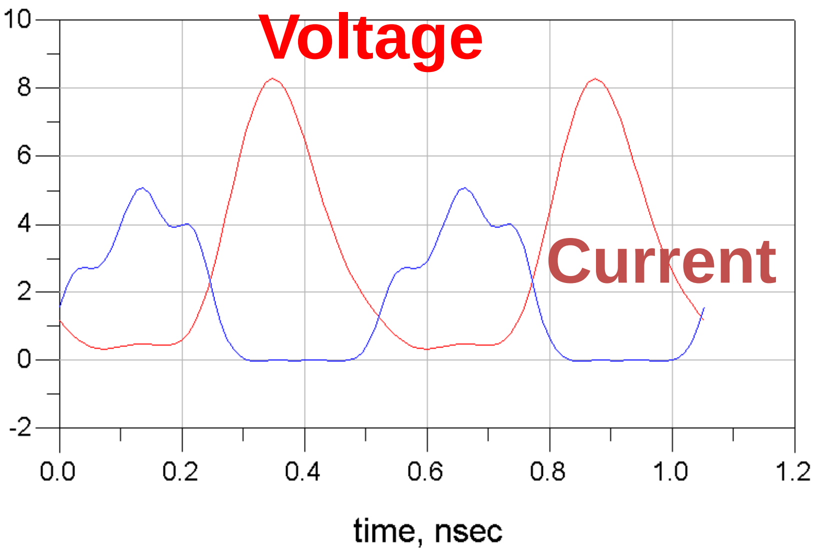


Class E point

X1=RL*0.7

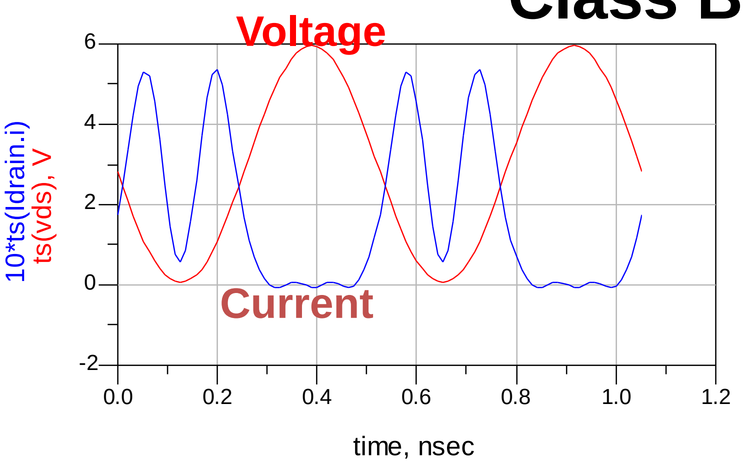
Drain Voltage and Current Waveforms* For Optimal Matching

Waveforms show "switching" behavior - both are near zero during portion of cycle
Requires even harmonics for voltage

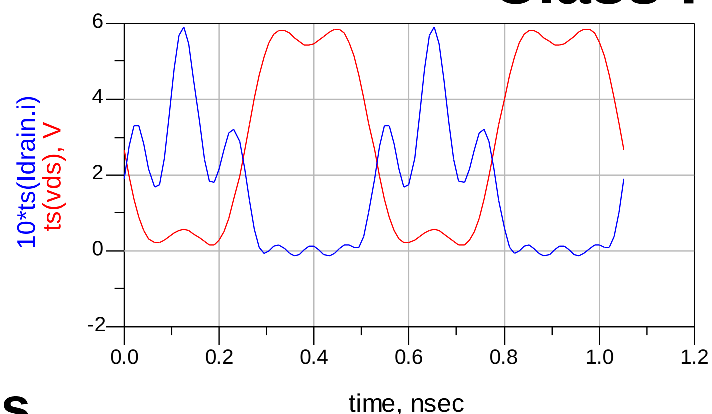


***Best:* Overdriven Class "J"**
Intermediate between Class E and Class F-1

Class B



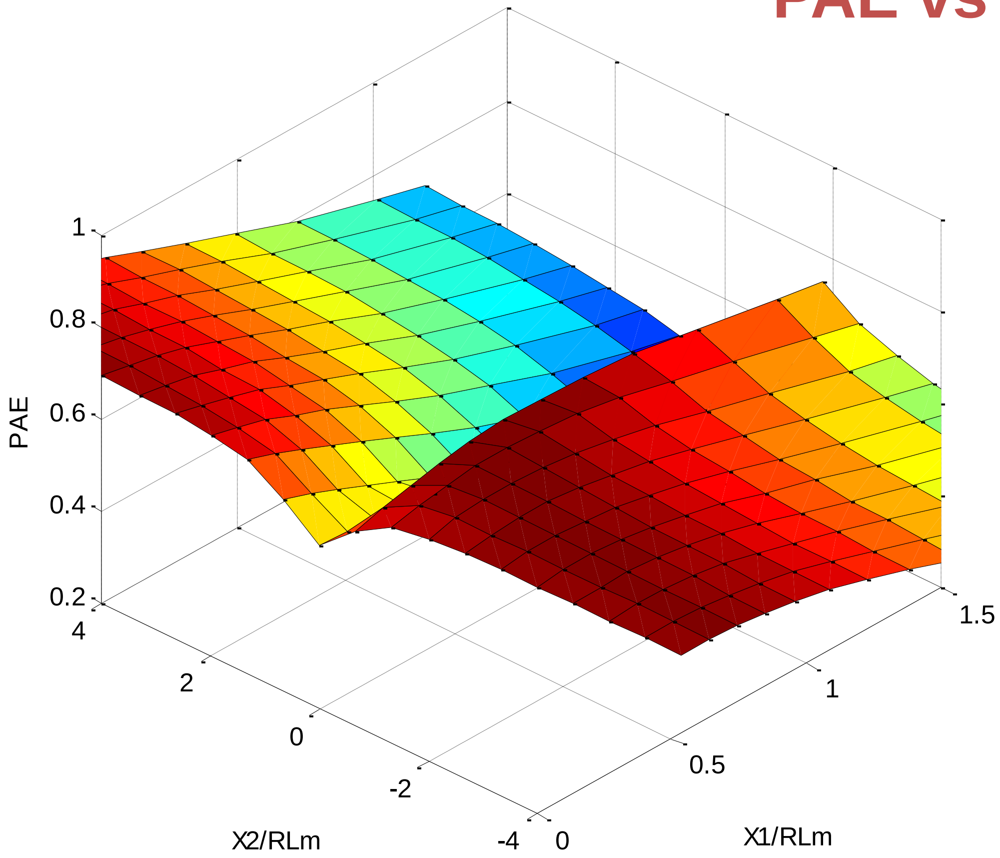
Class F

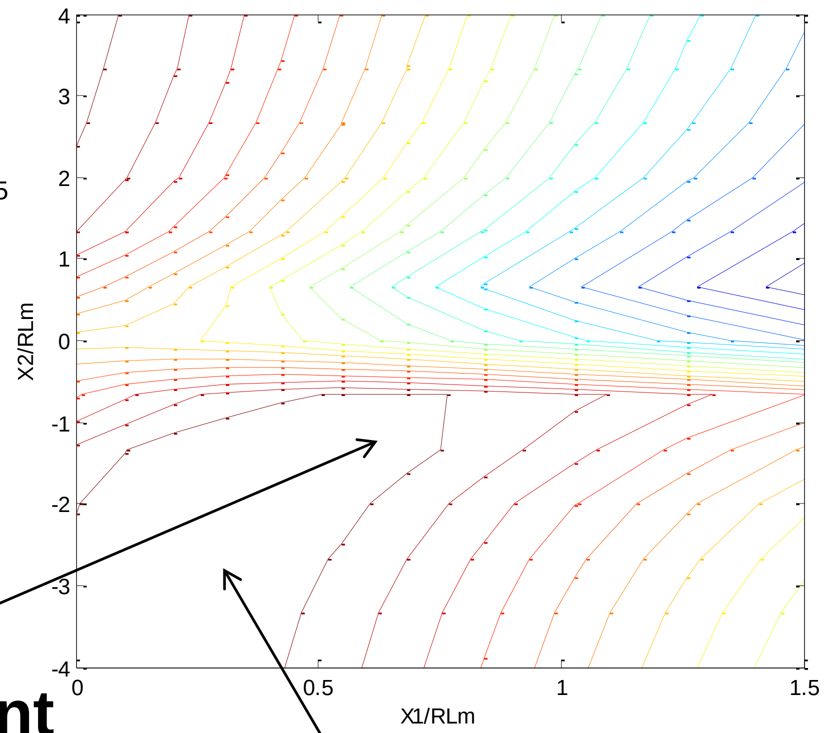


Representative simulated results
****Current is through current generator only;***
Cds capacitive current is de-embedded

PAE vs X1/|ZL1| and X2/|ZL1|

For X3=0 short



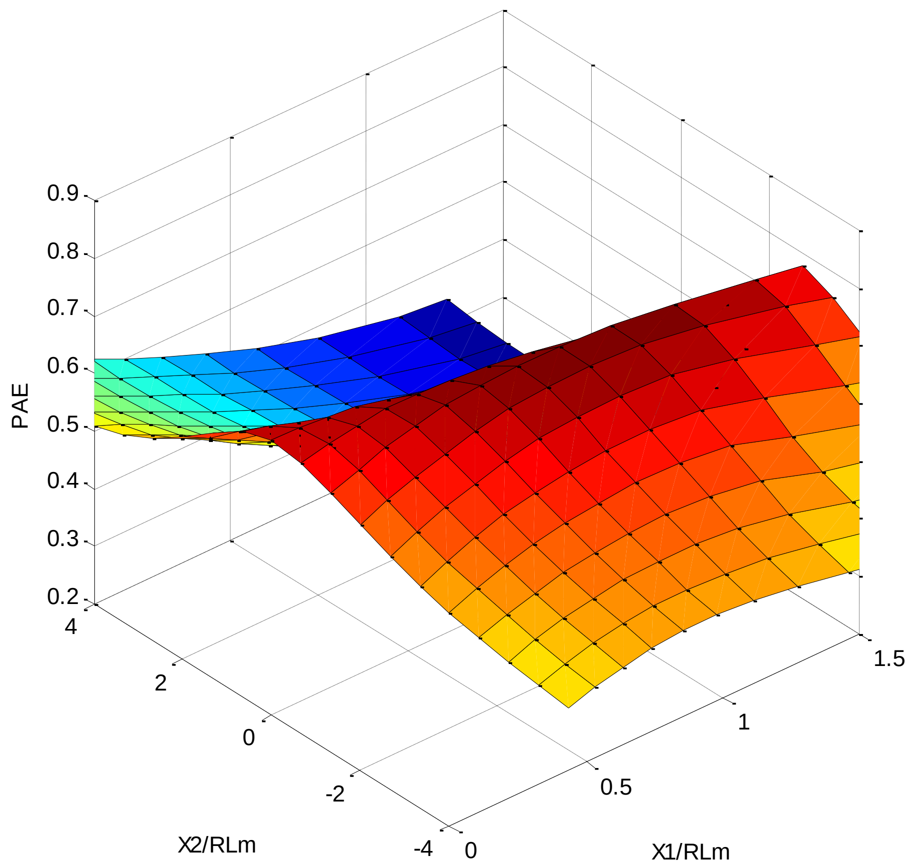


Tradeoff
Inductive ZL at fo
With Capacitive Z at 2fo

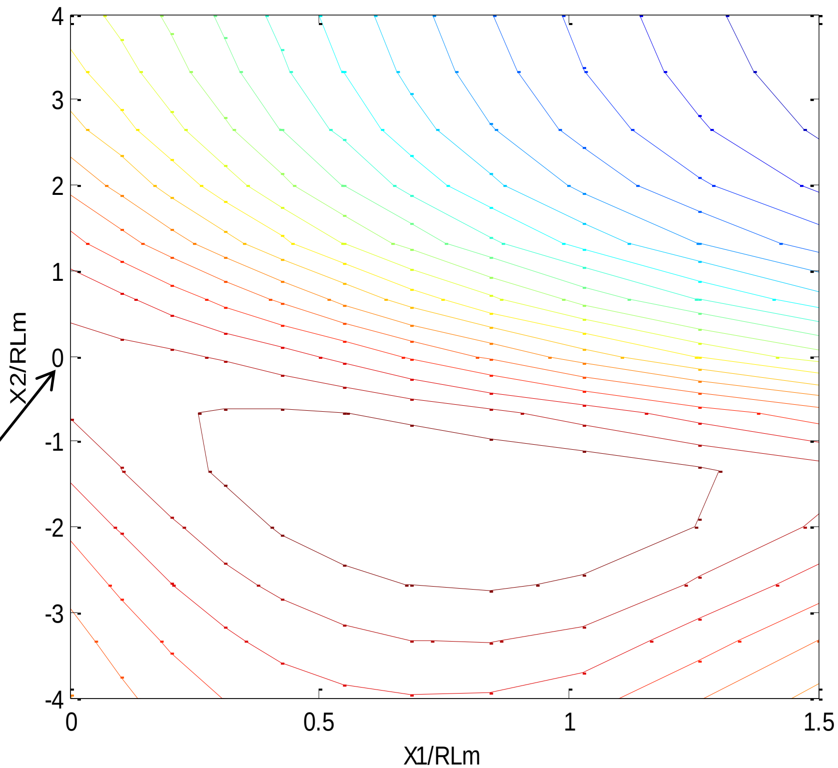
~Class E point
(if X3/magRL=0.96 instead of 0)

Class J region

PAE vs X1/|ZL| and X2/|ZL|



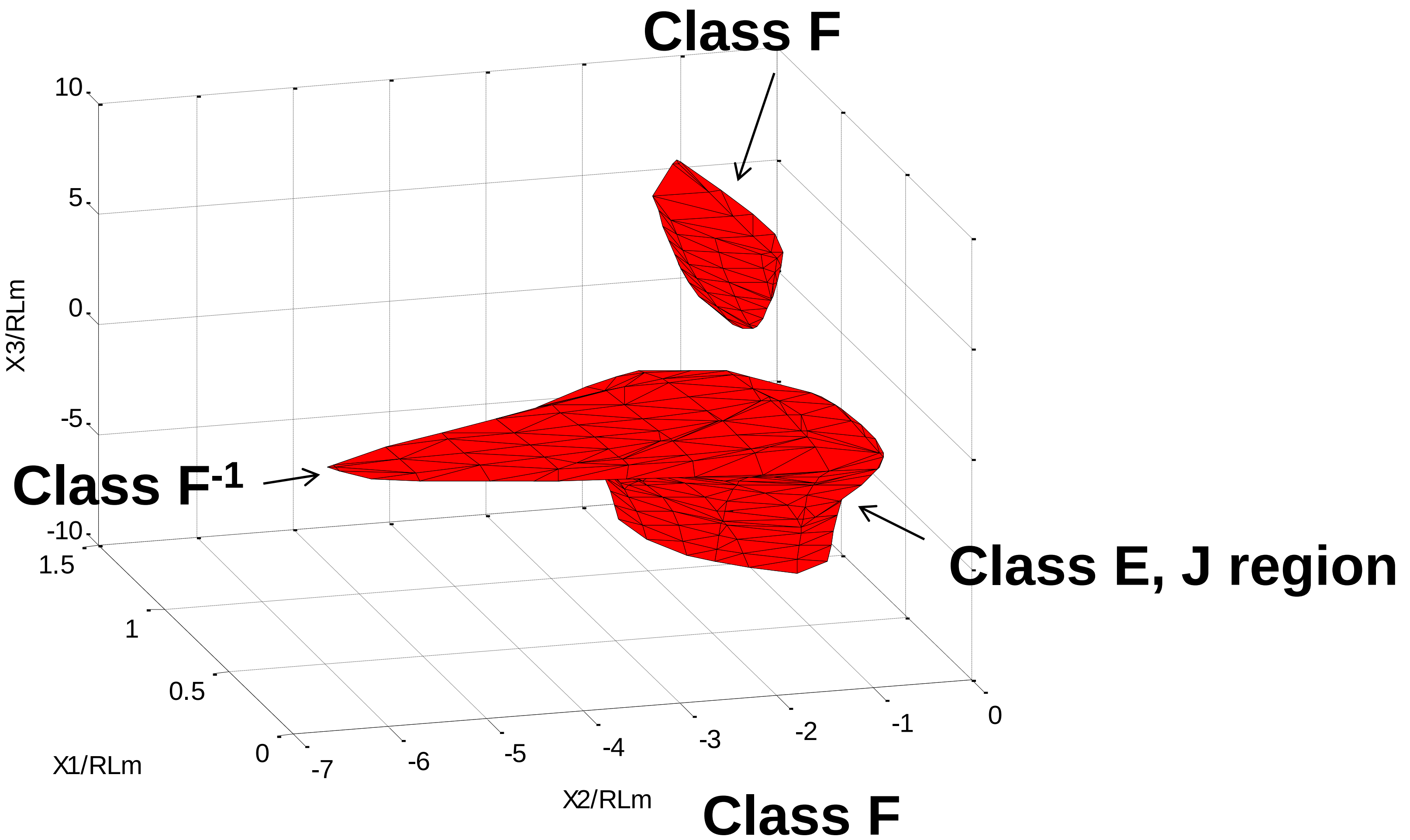
For X3=-6
~open



Tradeoff
Inductive ZL at fo
With Capacitive Z at 2fo

Class F

PAE vs X1 / |ZL| , X2 / |ZL| and |X3| / |ZL|



Performance Dependence on Harmonic Content

- **Efficiency increases with harmonics**

Class F Harmonics	1 (class A)	2	3	4	5
Ideal drain efficiency %	50	71	82	87	91
Power output capability	0.125		0.144		0.151

- **Overdrive the amplifier to generate harmonics**

UCSD

Linearity Issues for High Efficiency Amplifier Modes

Switching mode amplifier output has constant envelope -
determined by power supply, not by switch drive power
=> used for phase modulated signals only

Class F amplifier can have acceptable linearity - but η drops

A key difficulty in optimizing efficiency for waveforms with time varying envelope is:

Need to minimize voltage across transistor,
so want Vt= Vsupply - Vrf =0

How to arrange this if Vrf varies?