T-75-37-05

1. INTRODUCTION

The TMP68681 dual universal asynchronous receiver/transmitter (DUART) is part of the TLCS-68000 Family of peripherals and directly interfaces to the TMP68000 processor via an asynchronous bus structure. The TMP68681 consists of eight major sections internal control logic, timing logic, interrupt control logic, a bidirectional 8-bit data bus buffer, two independent communication channels (A and B), a 6-bit parallel input port, and an 8-bit parallel output port.

The TMP2681 dual asynchronous receiver/transmitter (DUART) is functionally equivalent to the TMP68681 with some minor differences. The description of the TMP68681 applies to the TMP2681 except for the areas described in the Appendix found at the back of this document.

Figure 1.1 illustrates the basic block diagram of the TMP68681 and should be referred to during the discussion of its features which include the following:

- TLCS-68000 Bus Compatible
- Two Independent Full-Duplex Asynchronous Receiver/Transmitter Channels
- Maximum Data Transfer:
  1× – 1 MB/second
  16× – 125 kB/second
- Quadruple-Buffered Receiver Data Registers
- Double-Buffered Transmitter Data Registers
- Independently Programmable Baud Rate for Each Receiver and Transmitter Selectable From:
  18 Fixed Rates: 50 to 38.4k Baud
  One User Defined Rate Derived from a Programmable Timer/Counter
  External 1×Clock or 16×Clock
- Programmable Data Format:
  Five to Eight Data Bits plus Parity
  Odd, Even, No Parity, or Force Parity
  One, One and One-Half, or Two Stop Bits Programmable in One-Sixteenth Bit Increments
- Programmable Channel Modes:
  Normal (Full Duplex)
  Automatic Echo
  Local Loopback
  Remote Loopback

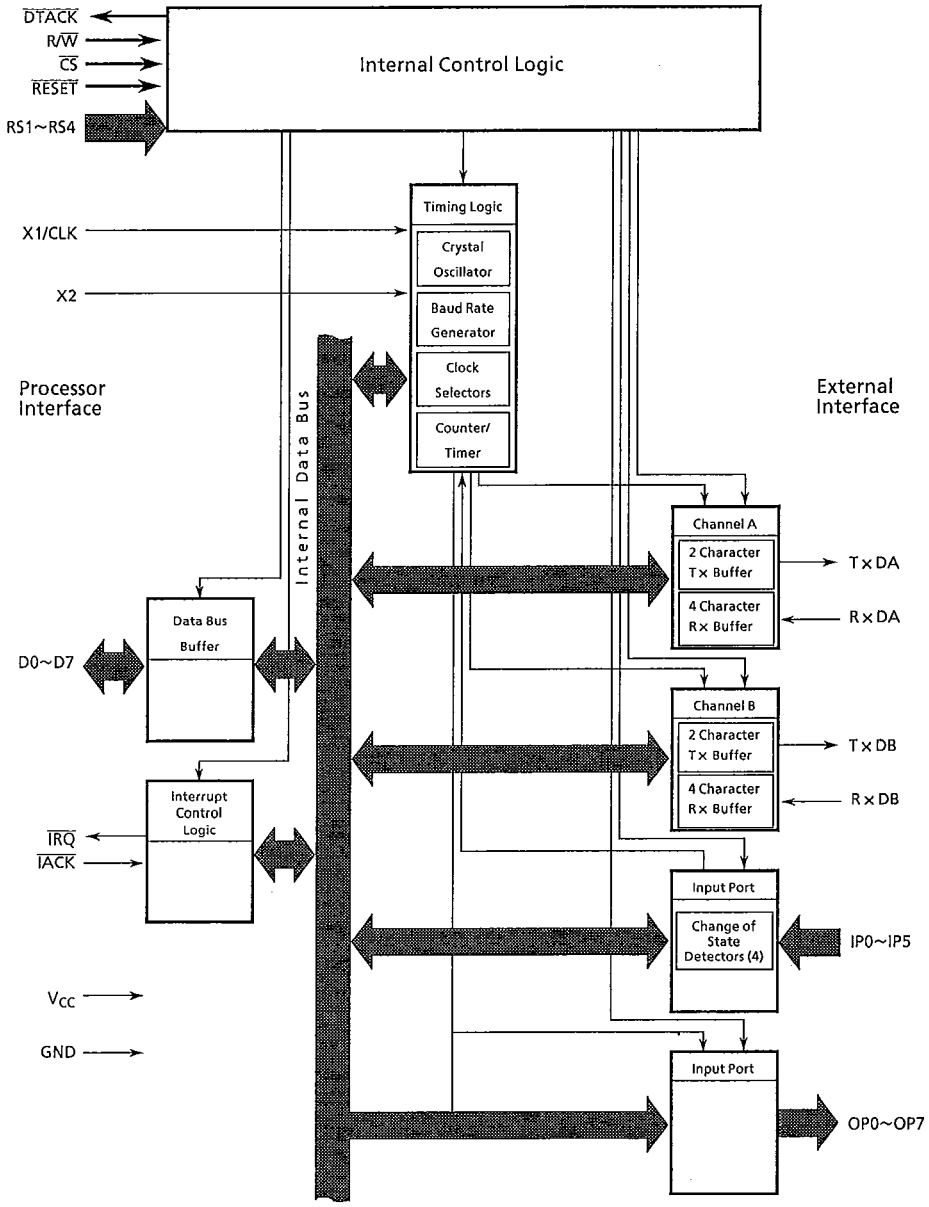


Figure 1.1 Block Diagram

- Automatic Wake-up Mode for Multidrop Applications
- Multi-Function 6-bit Input Port
  - Can Serve as Clock or Control Inputs
  - Change-of-State Detection on Four Inputs

Features (Coninued)

- Multi-Function 8-bit Output Port
  - Individual Bit Set/Reset Capability
  - Outputs can be Programmed to be Status/Interrupt Signals
- Multi-Function 16-bit Programmable Counter/Timer
- Versatile Interrupt System
  - Single Interrupt Output with Eight Maskable Interrupting Conditions
  - Interrupt Vector Output on Interrupt Acknowledge
  - Output Port can be Configured to Provide a Total of Up to Six Separate Wire-ORable Interrupt Outputs
- Parity, Framing, and Overrun Error Detection
- False-State Bit Detection
- Line-Break Detection and Generation
- Detects Break Which Originates in the Middle of a Character
- Start-End Break Interrupt/Status
- On-Chip Crystal Oscillator
- TTL Compatible
- Single +5 V Power Supply

1.1 INTERNAL CONTROL LOGIC

The internal control logic receives operation commands from the central processing unit (CPU) and generates appropriate signals to the internal sections to control device operation. It allows the registers within the DUART to be accessed and various commands to be performed by decoding the four register-select lines (RS1 through RS4). Besides the four register-select lines, there are three other inputs to the internal control logic from the CPU: read/write (R/$\overline{W}$), which allows read and write transfers between the CPU and DUART via the data bus buffer; chip select ($\overline{CS}$), which is the DUART chip select; and reset ($\overline{RESET}$), which is used to initialize or reset the DUART. Output from the internal control logic is the data transfer acknowledge ($\overline{DTACK}$) signal which is asserted during read, write, or interrupt acknowledge cycles. $\overline{DTACK}$ indicates to the CPU that data has been latched on a CPU write cycle or that valid data is present on the data bus during a CPU read cycle or interrupt acknowledge ($\overline{IACK}$) cycle.

1.2 TIMING LOGIC

The timing logic consists of a crystal oscillator, a baud-rate generator (BRG), a programmable 16-bit counter/timer (C/T), and four clock selectors. The crystal oscillator operates directly from a 3.6864 MHz crystal connected across the X1/CLK and X2 inputs or from an external clock of the appropriate frequency connected to X1/CLK. The clock serves as the basic timing reference for the baud-rate generator, the counter/timer, and other internal circuits. A clock signal, within the limits given in SECTION 5 ELECTRICAL SPECIFICATIONS, must always be supplied to the DUART.

The baud-rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communication baud rates ranging from 50 to 38.4k by producing internal clock outputs at 16 times the actual baud rate. The counter/timer can be used in the timer mode to produce a 16× clock for any other baud rate by counting down the crystal clock or external clock. Other baud rates may also be derived by connecting 16× or 1× clocks to certain input port pins which have alternate functions as receiver or transmitter clock inputs. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates.

The 16-bit counter/timer (C/T) included within the DUART and timing logic can be programmed to use one of several timing sources as its input. The output of the counter/timer is available to the internal clock selectors and can also be programmed to be a parallel output at OP3. In the timer mode, the counter/timer acts as a programmable divider and can be used to generate a square-wave output at OP3. In the counter mode, the contents of the counter/timer can be read by the CPU and it can be stopped and started under program control. The counter counts down the number of pulses stored in the concatenation of the counter/timer upper register and counter/timer lower register and produces an interrupt. This is a system oriented feature which may be used to keep track of timeouts when implementing various application protocols.

1.3 INTERRUPT CONTROL LOGIC

The following registers are associated with the interrupt control logic: interrupt mask register (IMR), interrupt status register (ISR), auxiliary control register (ACR), and interrupt vector register (IVR).

Refer to SECTION 4 PROGRAMMING AND REGISTER DESCRIPTION for a more complete description of these registers.

A single active-low interrupt output ($\overline{IRQ}$) is provided which can be used to notify the processor that any of eight internal events has occurred. These eight events are described in the discussion of the interrupt status register (ISR) in SECTION 4 PROGRAMMING AND REGISTER DESCRIPTION.

The interrupt mask register (IMR) can be programmed to select only certain conditions which cause $\overline{IRQ}$ to be asserted while the interrupt status register (ISR) can be read by the CPU to determine all currently active interrupting conditions. When an active-low interrupt acknowledge signal ($\overline{IACK}$) from the processor is asserted while the DUART has an interrupt pending, the DUART will place the contents of the interrupt vector register (IVR) (i.e., the interrupt vector) on the data bus and assert the data transfer acknowledge signal ($\overline{DTACK}$).

In addition, the DUART offers the ability to program the parallel outputs OP3 through OP7 to provide discrete interrupt outputs for the transmitters, the receivers, and the counter/timer.

1.4 DATA BUS BUFFER

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the internal control logic to allow read and write data transfer operations to take place between the controlling CPU and DUART by way of the eight parallel data lines (D0 ~ D7).

1.5 COMMUNICATION CHANNELS A AND B

Each communication channel comprises a full-duplex asynchronous receiver/transmitter (UART).
The operating frequency for each receiver and each transmitter can be selected independently from the baud-rate generator, the counter/timer, or from an external clock.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits, and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for a start bit, stop bit, parity bit (if any), or break condition, and transfers an assembled character to the CPU during read operations.

1.6 INPUT PORT

The inputs to this unlatched 6-bit port (IP0 ~ IP5) can be read by the CPU by performing a read operation. High or low inputs to the input port result in the CPU reading a logic one or logic zero, respectively; that is, there is no inversion of the logic level. Since the input port is a 6-bit port, performing a read operation will result in D7 being read as a logic one and D6 reflecting the logic level of $\overline{IACK}$. Besides general-purpose inputs, the inputs to this port can be individually assigned specific auxiliary functions serving the communication channels.

Four change-of-state detectors, also provided within the input port, are associated with inputs IP0, IP1, IP3, and IP3. A high-to-low or low-to-high transition of these inputs lasting longer than 25 to 30 microseconds (best-to-worst case times) will set the corresponding bit in the input port change register (IPCR). The bits are cleared when the register is read by the CPU. Also, the DUART can be programmed so any particular change of state can generate an interrupt to the CPU. The DUART recognizes a level change on an input pin internally only after it has sampled the new level on the pin for two successive pulses of the sampling clock. The sampling clock is 38.4 MHz and is derived from one of the baud-rate generator taps. The resulting sampling period is slightly more than 25 microseconds (this assumes that the clock input is 3.6864 MHz). Subsequently, if the level change occurs on or just before a sampling pulse, it will be recognized internally after 25 microseconds. However, if the level change occurs just after a sampling pulse, it will be sampled the first time after 25 microseconds. Thus, in this case the level change will not be recognized internally until 50 microseconds after the level change took place on the pin.

1.7 OUTPUT PORT

This 8-bit multi-purpose output port can be used as a general-purpose output port. Associated with the output port is an output port register (OPR).

All bits of the output port register can be individually set and reset. A bit is set by performing a write operation at the appropriate address with the accompanying data specifying the bits to be set (one equals set and zero equals no change). Similarly, a bit is reset by performing a write operation at another address with the accompanying data specifying the bits to be reset (one equal reset and zero equals no change).

The output port register stores data that is to be output at the output port pins. Unlike the input port, if a particular bit of the output port register is set to a logic one or logic zero the output pin will be at a low or high level, respectively. Thus, a logic inversion takes place internal to the DUART with respect to this register. The outputs are complements of the data contained in the output port register. More information on the address location of the output port register and setting and resetting bits of this register can be found in Table 4.1 and in SECTION 4 PROGRAMMING AND REGISTER DESCRIPTION.

Besides general-purpose outputs, the putputs can be individually assigned specific auxiliary functions serving the communication channels. The assignment is accomplished by appropriately programming the channel A and B mode registers (MR1A, MR1B, MR2A, and MR2B) and the output port configuration register (OPCR). More information on the mode registers and output port configuration register can be found in SECTION 4 PROGRAMMING AND REGISTER DESCRIPTION.

2. SIGNAL DESCRIPTION

This section contains a brief description of the input and output signals. Each signal is explained in a brief paragraph about its function with reference (if applicable) to other sections which give greater detail on its use. Table 2.1 provides a quick reference in determining a signal's pin number, its use as an input or output, whether it is active high or low, and the section in which more information can be found about its operation.

Note : The terms assertion and negation will be used extensively. This is done to avoid confusion when dealing with a mixture of "active low" and "active high" signals. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or false.

Table 2.1 Signal Summary (1/2)

Singnal Name	Mnemonic	Pin No.	Input/ Output	Active State	Refer to Para. No.
Power Supply (+ 5V)	Vcc	40	Input	High	2.1
Ground	GND	20	Input	Low	2.1
Crystal Input or External Clock	X1/CLK	32	Input	–	2.2
Crystal Input	X2	33	Input	–	2.3
Reset	$\overline{RESET}$	34	Input	Low	2.4
Chip Select	$\overline{CS}$	35	Input	Low	2.5
Read/Write	R/$\overline{W}$	8	Input	High/Low	2.6
Data Transfer Acknowledge	$\overline{DTACK}$	9	Output*	Low	2.7
Register-Select Bus Bit 4	RS4	6	Input	High	2.8
Register-Select Bus Bit 3	RS3	5	Input	High	2.8
Register-Select Bus Bit 2	RS2	3	Input	High	2.8
Register-Select Bus Bit 1	RS1	1	Input	High	2.8
Bidirectional-Data Bus Bit 7	D7	19	Input/Output	High	2.9
Bidirectional-Data Bus Bit 6	D6	22	Input/Output	High	2.9
Bidirectional-Data Bus Bit 5	D5	18	Input/Output	High	2.9
Bidirectional-Data Bus Bit 4	D4	23	Input/Output	High	2.9
Bidirectional-Data Bus Bit 3	D3	17	Input/Output	High	2.9
Bidirectional-Data Bus Bit 2	D2	24	Input/Output	High	2.9
Bidirectional-Data Bus Bit 1	D1	16	Input/Output	High	2.9

* Requires a pullup registor.

Table 2.1 Signal Summary (2/2)

Signal Name	Mnemonic	Pin No.	Input/ Output	Active State	Refer to Para. No.
Bidirecetional-Data Bus Bit 0 (Least-Significant Bit)	D0	25	Input/Output	High	2.9
Interrupt Request	$\overline{IRQ}$	21	Output*	Low	2.10
Interrupt Acknowledge	$\overline{IACK}$	37	Input	Low	2.11
Channel A Transmitter Serial Data	TxDA	30	Output	–	2.12
Channel A Receiver Serial Data	RxDA	31	Input	–	2.13
Channel B Transmitter Serial Data	TxDB	11	Output	–	2.14
Channel B Receiver Serial Data	RxDB	10	Input	–	2.15
Parallel Input 5	IP5	38	Input	–	2.16.1
Parallel Input 4	IP4	39	Input	–	2.16.2
Parallel Input 3	IP3	2	Input	–	2.16.3
Parallel Input 2	IP2	36	Input	–	2.16.4
Parallel Input 1	IP1	4	Input	–	2.16.5
Parallel Input 0	IP0	7	Input	–	2.16.6
Parallel Output 7	OP7	15	Output**	–	2.17.1
Parallel Output 6	OP6	26	Output**	–	2.17.2
Parallel Output 5	OP5	14	Output**	–	2.17.3
Parallel Output 4	OP4	27	Output**	–	2.17.4
Parallel Output 3	OP3	13	Output**	–	2.17.5
Parallel Output 2	OP2	28	Output	–	2.17.6
Parallel Output 1	OP1	12	Output	–	2.17.7
Parallel Output 0	OP0	29	Output	–	2.17.8

** May require a pullup resistor, depending upon its programmed function.

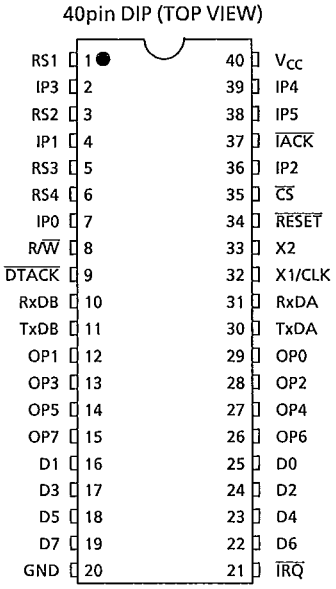


Figure 2.1 Pin Assignments

2.1 Vcc AND GND

Power is supplied to the DUART using these two signals. V_{CC} is power (+5 volts) and GND is the ground connection.

2.2 CRYSTAL INPUT OR EXTERNAL CLOCK (X1/CLK)

This input is one of two connections to a crystal (see 2.3 CRYSTAL INPUT (X2)) or a connection to an external clock. A crystal or a clock, within the specified limits, must be supplied at all times (see SECTION 5 ELECTRICAL SPECIFICATIONS).

If a crystal is used, a capacitor of approximately 10 to 15 picofarads should be connected from this pin to ground.

2.3 CRYSTAL INPUT (X2)

This input is an additional connection to a crystal (see 2.2 CRYSTAL INPUT OR EXTERNAL CLOCK (X1/CLK). If an eternal TTL-level clock is used, this pin should be tied to ground. If a crystal is used, a capacitor of approximately 0 to 5 picofarads should be connected from this pin to ground.

2.4 RESET ($\overline{RESET}$)

The DUART can be reset by asserting the $\overline{RESET}$ signal or by programming the appropriate command register. A hardware reset, assertion of $\overline{RESET}$, clears status registers A and B (SRA and SRB), the interrupt mask register (IMR), the interrupt status register (ISR), the output port register (OPR), and the output port configuration register (OPCR). $\overline{RESET}$ initializes the interrupt vector register (IVR) to $0F_{16}$, places parallel outputs OP0 through OP3 in the high state, places the counter/timer in timer mode, and places channels A and B in the inactive state with the channel A transmitter serial-data output (TxDA) and channel B transmitter serial-data output (TxDB) in the mark (high) state.

Software resets are not as encompassing and are achieved by appropriately programming the channel A and/or B command registers. Reset commands can be programmed through the command register to reset the receiver, transmitter, error status, or break-change interrupts for each channel.

Refer to SECTION 4 PROGRAMMING AND REGISTER DESCRIPTION for further information.

2.5 CHIP SELECT ($\overline{CS}$)

This active low input signal, when low, enables data transfers between the CPU and DUART on the data lines (D0 ~ D7). These data transfers are controlled by read/write (R/$\overline{W}$) and the register-select inputs (RS1 ~ RS4). When chip select is high the D0 ~ D7 data lines are placed in the high-impedance state.

2.6 READ/WRITE (R/$\overline{W}$)

When high, this input indicates a read cycle, and when low, it indicates a write cycle. A cycle is intiated by assertion of the chip-select input.

2.7 DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

This three-state active low open-drain output is asserted in read, write, or interrupt acknowledge ($\overline{IACK}$) cycles to indicate the proper transfer of data between the CPU and DUART.

2.8 REGISTER-SELECT BUS (RS1 ~ RS4)

The register-select bus lines during read/write operations select the DUART internal registers, ports, or commands.

2.9 DATA BUS (D0 ~ D7)

These bidirectional three-state data lines are used to transfer commands, data, and status between the CPU and DUART. D0 is the least-significant bit.

2.10 INTERRUPT REQUEST ($\overline{IRQ}$)

This active low, open-drain output signals the CPU that one or more of the eight maskable interrupting conditions are true.

2.11 INTERRUPT ACKNOWLEDGE ($\overline{IACK}$)

This active low input indicates an interrupt acknowledge cycle. If there is an interrupt pending ($\overline{IRQ}$ asserted) and this pin asserted, the DUART responds by placing the interrupt vector on the data bus and then asserting $\overline{DTACK}$. If these is not an interrupt pending ($\overline{IRQ}$ negated), the DUART ignores the status of this pin.

2.12 CHANNEL A TRANSMITTER SERIAL-DATA OUTPUT (TxDA)

This signal is the transmitter serial-data output for channel A. The least-significant bit is transmitted first. This output is held high (mark condition) when the transmitter is disabled, idle, or operating in the local loopback mode. (Mark is high and space is low.) Data is shifted out this pin on the falling edge of the programmed clock source.

2.13 CHANNEL A RECEIVER SERIAL-DATA INPUT (RxDA)

This signal is the receiver serial-data input for channel A. The least-significant bit is received first.

Data on this pin is sampled on the rising edge of the programmed clock source.

2.14 CHANNEL B TRANSMITTER SERIAL-DATA OUTPUT (TxDB)

This signal is the transmitter serial-data output for channel B. The least-significant bit is transmitted first. This output is held high (mark condition) when the transmitter is disabled, idle, or operating in the local loopback mode. Data is shifted out this pin on the falling edge of the programmed clock source.

2.15 CHANNEL B RECEIVER SERIAL-DATA INPUT (RxDB)

This signal is the receiver serial-data input for channel B. The least-significant bit is received first.

Data on this pin is sampled on the rising edge of the programmed clock source.

2.16 PARALLEL INPUTS (IP0 ~ IP5)

Each of the parallel inputs (IP0 ~ IP5) can be used as general-purpose inputs. However, each one has an alternate function(s) which is described in the following paragraphs.

2.16.1 IP0

This input can be used as the channel A clear-to-send active low input ($\overline{CTSA}$). A change-of-state detector is also associated with this input.

2.16.2 IP1

This input can be used as the channel B clear-to-send active low input ($\overline{CTSB}$). A change-of-state detector is also associated with this input.

2.16.3 IP2

This input can be used as the channel B receiver external clock input (RxCB), or the counter/timer external clock input. When this input is used as the external clock by the receiver, the received data is sampled on the rising edge of the clock. A change-of-state detector is also associated with this input.

2.16.4 IP3

This input can be used as the channel A transmitter external clock input (TxCA). When this input is used as the external clock by the transmitter, the transmitted data is clocked on the falling edge of the clock. A change-of-state detector is also associated with this input.

2.16.5 IP4

This input can be used as the channel A receiver external clock input (RxCA). When this input is used as the external clock by the receiver, the received data is sampled on the rising edge of the clock.

2.16.6 IP5

This input can be used as the cahannel B transmitter external clock (TxCB). When this input is used as the external clock by the transmitter, the transmitted data is clocked on the falling edge of the clock.

2.17 PARALLEL OUTPUTS (OP0 ~ OP7)

Each of the parallel outputs can be used as general-purpose outputs. However, each one has an alternate function(s) which is described in the following paragraphs.

2.17.1 OP0

This output can be used as the cannel A active low request-to-send ($\overline{RTSA}$) output. When used for this function, it is automatically negated and reasserted by either the receiver or transmitter.

2.17.2 OP1

This output can be used as the cahnnel B active low request-to-send ($\overline{RTSB}$) output. When used for this function, it is negated and reasserted automatically by either the receiver or transmitter.

2.17.3 OP2

This output can be used as the channel A transmitter 1×-clock or 16×-clock output, or the channel A receiver 1×-clock output.

2.17.4 OP3

This output can be used as the open-drain active low counter-ready output, the open-drain timer output, the cannel B transmitter 1×-clock output, or the channel B receiver 1×-clock output.

2.17.5 OP4

This output can be used as the channel A open-drain active-low receiver-ready or buffer-full interrupt outputs ($\overline{\text{RxRDYA}}/\overline{\text{FFULLA}}$) by appropriately programming bit 6 of mode register 1A.

2.17.6 OP5

This output can be used as the channel B open-drain active low receiver-ready or buffer-full interrupt outputs ($\overline{\text{RxRDYB}}/\overline{\text{FFULLB}}$) by appropriately programming bit 6 of mode register 1B.

2.17.7 OP6

This output can be used as the channel A open-drain active low transmitter-ready interrupt output ($\overline{\text{TxRDYA}}$) by appropriately programming bit 6 of the output port configuration register.

2.17.8 OP7

This output can be used as the channel B open-drain active low transmitter-ready interrupt output ($\overline{\text{TxRDYB}}$) by appropriately programming bit 7 of the output port configuration register.

3. OPERATION

This section describes the operation of the transmitter, receiver, and operating modes of the TMP68681 DUART.

3.1 TRANSMITTER

The channel A and B transmitters are enabled for data transmission through their respective command registers (refer to SECTION 4 PROGRAMMING AND REGISTER DESCRIPTION). The DUART signals the CPU it is ready to accept a character by setting the transmitter-ready bit in the channel's status register. This condition can be programmed to generate an interrupt request on the $\overline{IRQ}$ output, an interrupt request for channel A's transmitter on parallel output OP6, or for channel B's transmitter on parallel output OP7.

When a character is loaded into the transmit buffer (TB), the above conditions for the respective channel are negated. Data is transferred from the transmit holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The transmitter-ready conditions are then asserted again providing one full character time of buffering. Characters cannot be loaded into the transmit buffer while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the transmitter serial-data output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least-significant bit is sent first. Data is shifted out the transmit serial data output pin on the falling edge of the programmed clock source.

Following the tansmission of the stop bits, if a new character is not available in the tansmit holding register the transmitter serial-data output remains high and the transmitter- empty bit in the status register (SRA and SRB) will be set to a one. Transmission resumes and the transmitter-empty bit is cleared when the CPU loads a new character into the transmit buffer (TBA or TBB). If the transmitter is sent a disable command, it will continue operating until the character in the transmit shift register is completely sent out. The transmitter can be reset through a software command (refer to 2.4 RESET ($\overline{RESET}$)). If it is reset, operation ceases immediately and must be enabled through the command register before resuming operation.

The transmitter can also be forced to send a continuous low condition by issuing a send-break command. If clear-to-send (CTS) operation is enabled, the $\overline{CTS}$ input (alternate function of IP0 or IP1) must be low in order for the character to be transmitted. If it goes high in the middle of a transmission, the character in the shift register is transmitted and TxD then remains in the marking state until $\overline{CTS}$ again goes low. The state of $\overline{CTS}$ is ignored by the transmitter when it is to send a break. The transmitter can be programmed to automatically negate the request-to-send ($\overline{RTS}$) output (alternate function of OP0 and OP1) upon completion of a message transmission.

Note that if the transmitter is programmed to operate in this manner, the $\overline{RTS}$ output must be manually asserted before a message is to be transmitted. In applications where the transmitter is disabled after transmission is complete, and if appropriately programmed, the $\overline{RTS}$ output will be negated one bit time after the character in the transmit shift register is completely transmitted.

3.2 RECEIVER

The channel A and B receivers are enabled for data reception through the respective channel's command register. The channel's receiver looks for a high-to-low (mark-to-space) transition of the start bit on the receiver serial-data input pin. If a transition is detected, the state of the receiver serial-data input pin is sampled each 16× clock for seven and one-half clocks (16×-clock mode) or at the next rising edge of the bit time clock (1×-clock mode). If the receiver serial data is sampled high, the start bit is invalid and the search for a valid start bit begins again. If receiver serial data is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals (at the theoretical center of the bit) until the proper number of data bits and the parity bit (if any) have been assembled and one stop bit has been detected. Data on the receiver serial data input pin is sampled on the rising edge of the programmed clock source.

During this process the least-significant bit is received first. The data is then transferred to a receive holding register (RHR) and the receiver-ready bit in the status register (SRA or SRB) is set to a one (see Figure 4.1). This condition can be programmed to generate an interrupt request on the $\overline{IRQ}$ output, an interrupt request for channel A's receiver on parallel output OP4, or an interrupt request for channel B's receiver on parallel output OP5. If the character length is less than eight bits, the most-significant unused bits in the receive holding register (RHR) are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and receiver serial data remains low for one-half of the bit period after the stop bit was sampled, the receiver operates as if a new start bit transition has been detected.

The parity error, framing error, overrun error, and received-break conditions (if any) set error and break flags in the status register at the received character boundary and are valid only when the receiver-ready bit (RxRDY) in the status register is set.

If a break condition is detected (receiver serial data is low for the entire character including the stop bit), a character consisting of all zeros will be loaded into a receive holding register (RHR) and the received-break bit and the receiver-ready bit in the status register (SRA and SRB) will be set to a one. The receiver serial-data input must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The receiver can detect the beginning of a break in the middle of a character so long as the break persists until at least the next character time. When the break begins in the middle of a character, the receiver will place the damaged character in the receiver FIFO and set the corresponding framing error and receiver-ready status bits. Then, so long as the break persists until the next character time, the receiver will place an all-zeros character in the receiver FIFO and set the corresponding received-break and receiver-ready status bits.

A first-in first-out (FIFO) stack is used in each channel's receive buffer logic and consists of three receive holding registers. The receiver bufer (RBA or RBB) is composed of the FIFO and a receive shift register connected to the receiver serial-data input. Data is assembled in the shift register and loaded into the top-most empty receive holding register position of the FIFO. Thus, data flowing from the receiver to the CPU is quadruply buffered.

The receiver-ready bit in the status register (SRA or SRB) is set whenever one or more characters are available to be read. A read of the receiver buffer produces an output of data from the top of the FIFO stack. After the read cycle, the data at the top of the FIFO stack and its associated status bits are "popped" and new data can be added at the bottom of the stack by the receive shift register.

The FIFO-full status bit set if all three stack positions are filled with data. Either the receiver-ready or the FIFO-full status bits can be selected to cause an interrupt.

In addition to the data byte,three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO (overrun is not). By programming the error-mode control bit in the channel's mode register, status can be provided for "character" or "block" modes.

In the "character" mode, status provided in the status register (SRA or SRB) is given on a character-by-character basis and thus applies only to the character at the top of the FIFO. In the "block" mode, the status provided in the status register for the parity error, framing error, and received-break conditions is the logical OR of these respective bits for all characters coming to the top of the FIFO stack since the last reset error command was issued. That is, beginnig at the last reset error command issued, a continuous logical-OR function of corresponding status bits is produced in the status register as each character comes to the top of the FIFO stack.

The block mode is useful in applications reguiring the exchange of blocks of information where the software overhead of checking each character's error flags cannot be tolerated. In this mode, entire messages can be received and only data integrity check is performed at the end of each message. Although data reception in this manner has speed advantages, there are also disadvantages. Since each character is not individually checked for error conditions by the software, if an error occurs within a message the error will not be recognized until the final check is performed. Also, there is no indication of which character(s) is in error within the message.

In either mode, reading the status register (SR) does not affect the FIFO. The FIFO is "popped" only when the receive buffer (RBA or RBB) is read. Therefore, the status register (SRA or SRB) should be read prior to reading the FIFO.

If all three of the FIFO's receive holding registers are full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected. But, the character previously in the shift register is lost and the overrun-error status bit will be set upon receipt of the start bit of the new overrunning character.

To support control flow capability, a receiver can automatically negate and reassert the request-to-send ($\overline{RTS}$) output. If programmed to operate in this mode, the request-to-send output (alternate function of parallel outputs OP0 and OP1) will automatically be negated by the receiver when a valid start bit is received and the FIFO stack is full. When a FIFO position becomes available, the request-to-send output will be reasserted automatically by the receiver. By connecting the request-to-send output to the clear-to-send ($\overline{CTS}$) input of a transmitting device, overrun errors can be prevented in the receiver. Note that the $\overline{RTS}$ output must be manually asserted the first time. Thereafter the receiver will control the $\overline{RTS}$ output.

If the FIFO stack contains characters and the receiver is then disabled, the characters in the stack can still be read but no additional characters can be received until the receiver is again enabled. If the receiver is reset, the FIFO stack and all of the receiver status bits, the corresponding output prots, and the interrupt request are reset. No additional characters can be received until the receiver is again enabled.

3.3 LOOPING MODES

Besides the normal operation mode, in which the receiver and transmitter operate independently, each DUART channel can be configured to operate in various looping modes which are useful for local and remote system diagnostic functions. These modes are described in the following paragraphs with further information available in SECTION 4 PROGRAMMING AND REGISTER DESCRIPTION.

3.3.1 Automatic-Echo Mode

In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The local CPU-to-receiver communication continues normally but the CPU-to-transmitter link is disabled.

3.3.2 Local-Loopback Mode

In this mode, the transmitter output is internally connected to the receiver input. This mode is useful for testing the operation of a local DUART channel. By sending data to the transmitter and checking that the data assembled by the receiver is the same data

that was sent, correct channel operation can be assured. In this mode the CPU-to-transmitter and CPU-to-receiver communications continue normally.

3.3.3 Remote-Loopback Mode

In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The local CPU-to-receiver link is disabled. This mode is useful in testing the receiver and transmitter operation of a remote channel. For this mode the remote channel must have its receiver enabled.

3.4 MULTIDROP MODE

The channel can be programmed to operate in a wake-up mode used for multidrop or multiprocessor applications. This mode is selected by setting bits three and four in mode register one (MR1). In this mode of operation, a master station's channel, connected to several slave stations (a maximum of 256 unique slave stations), transmits an address character followed by a block of data characters targeted for one of the slave stations. In this mode, the channel receivers within the slave stations are disabled. Even though the channel receivers within the slave stations may be disabled, they continuously monitor the data stream sent out from the master station. When any address character in the data stream is deteced by the slave station's channel receivers, each receiver notifies its respective CPU by setting receiver ready (RxRDY) and generating an interrupt if programmed to do so. Each slave station CPU then compares the received address to its station address and enables its receiver if it wishes to receive the subsequent data characters or block of data from the master station. Slave stations which are not addressed continue monitoring the data stream for the next address character. The end of a previous block of data and the start of another block of data is flagged by an address character. After receiving a block of data, the slave station's CPU may disable the channel receiver and initiate the process again.

A transmitted character from the master station consists of a start bit, the programmed number of data bits, an address/data (A/D) bit flag, and the programmed number of stop bits. The address/data bit identifies to the slave station's channel whether the character should be interpreted as an address character or a data character. The character is interpreted as an address character if the A/D bit is set to a one or interpreted as a data character if it is set to a zero. The polarity of the transmitted address/data bit is selected by programming bit two in mode register one (MR1) to a one for an address character and to a zero for data characters. The mode register should be programmed prior to enabling the transmitter and loading the corresponding data bits into the transmit buffer (TBA or TBB).

In the multidrop mode, the receiver continuously monitors the received data stream regardless of whether it is enabled or disabled. If the receiver is disabled, it sets the receiver ready status bit and loads the character into the FIFO receive holding register stack provided the received address/data bit is a one (address tag).

The received character is discarded if the received address/data bit is a zero (data tag). If the receiver is enabled, all received characters are transferred to the CPU by way of the receive holding register stack during read operations. In either case, the data bits are loaded into the data portion of the FIFO stack while the address/data bit is loaded into the status portion of the FIFO stack normally used for parity error (status register bit five). Framing error, overrun error, and break-detection operate normally regardless of whether the receiver is enabled or disabled.

Note, the address/data bit takes the place of the parity bit and parity is neither calculated nor checked for characters in this mode. Nevertheless, messages in this mode can still contain error detection and correction information. One way to provide error detection, if 8-bit characters are not required, would be to use software to calculate parity and append it to 5-, 6-, or 7-bit characters. Another way to provide error detection for the entire message would be to use cyclic redundancy checks, or Hamming codes similar to those used in synchronous protocols, perform the check in software, and append the check character(s) to the end of the message.

3.5 COUNTER/TIMER

The 16-bit counter/timer can operate in a counter mode or a timer mode. In either mode, the counter/timer input (clock source) can be programmed to come from several sources and the counter/timer output can be programmed to appear on output port pin OP3. The value (preload value) stored in the concatenation of the counter/timer upper register (CTUR) and the counter/timer lower register (CTLR) can be from $0002 ~ $FFFF and changed at any time. In the counter mode, the counter/timer can be started and stopped by the CPU. Thus, this mode allows the counter/timer to be used as a system stopwatch, a real-time single interrupt generator, or a device watchdog. In the timer mode, the counter/timer runs continuously and cannot be started or stopped by the CPU. Instead, the CPU only resets the counter/timer. Thus, this mode allows the counter/timer to be used as a programmable clock source for channels A and B, periodic interrupt generator, or a variable duty cycle square-wave generator. Upon power-up and after reset, the counter/timer operates in timer mode.

3.5.1 Counter Mode

In the counter mode, the counter/timer counts down from the preload value using the programmed counter clock source. The counter clock source can be either the channel A transmitter clock, the channel B transmitter clock, the external clock on the X1/CLK pin divided by sixteen, or an external clock on the input port pin IP2. The CPU can start and stop the counter and can read the count value (CUR : CLR). When a read at the start counter command address is performed, the counter initializes itself with the preload value and begins a countdown sequence. Upon reaching $0000 (terminal count), the counter sets the counter/timer-ready bit in the interrupt status register (ISR [3]), rolls over from $0000 to $FFFF, and continues counting.

The counter can be programmed to generate an interrupt request for this condition on the $\overline{IRQ}$ output pin OP3. If the preload value is changed by the CPU, the counter will not recongnize the new value until it receives the next start counter command (and must reinitialize itself). When a read at the stop counter command address is performed, the counter stops the countdown sequence and clears ISR [3]. The count value should only be read while the counter is stipped. This is because only one of the count registers (either CUR or CLR) can be read at a time and if the counter is running, a decrement of CLR that requires a borrow form the CUR could take place between the two reads.

3.5.2 Timer Mode

In the timer mode, the counter/timer generates a square-wave output derived from the programmed timer input (clock source). The timer clock source can be the external clock on the X1/CLK input pin divided by one or sixteen, or it can be an external input on input port pin IP2 divided by one or sixteen. The square wave generated by the timer has a period of 2× (preload value) × (period of clock source), is available as a clock source for both communications channels, and can be programmed to appear on output pin OP3. The timer runs continuously and cannot be started or stopped by the CPU. Because the timer cannot be stopped, the count value (CUR : CLR) should not be read. When a read at the start counter command address is performed, the timer terminates the current countdown sequence, inverts its output, reinitializes itself with the preload value, and begings a new countdown sequence. Upon reaching $0000 (terminal count), the timer inverts its output, reinitializes itself with the preload value, and repeats the countdown sequence. After reaching terminal count this time, the timer sets the counter/timer-ready bit in the interrupt status register (ISR [3]), inverts its output, reinitializes itself with the preload value, and begins a new countdown sequence. The timer can be programmed to generate an interrupt request for this condition on the $\overline{IRQ}$ output. If the preload value is changed by the CPU, the timer will not recognize the new value until it reaches the next terminal count (and must reinitialize itself). This feature is very useful when generating variable duty cycle square waves. When a read at the stop counter command address is performed, the timer clears ISR [3] but does not stop. Because in timer mode the counter/timer runs continuously, it should be completely configured (preload value loaded and start counter command issued) before programming the timer output to appear on OP3.

4. PROGRAMMING AND REGISTER DESCRIPTION

This section contains a brief discussion on programming certain registers of the DUART with a detailed description of each register and its function.

4.1 PROGRAMMING

The operation of the DUART is progrmmed by writing control words into the appropriate registers. Operational feedback is provided by way of the status registers which can be read by the CPU. The DUART register address and address-triggered commands are described in Table 4.1.

Figure 4.1 (located on foldout page at the end of this document) illustrates a block diagram of the DUART from a programming standpoint and details the register configuration for each block. Table 4.1 and Figure 4.1 should be referred to during the discussion of the programming features of the DUART. The locations marked "do not access" should never be read during normal operation. They are used by the factory for test purposes.

Table 4.1 Register Addressing and Address - Triggered Commands

RS4	RS3	RS2	RS1	Read ($R/\overline{W}=1$)		Write ($R/\overline{W}=0$)	
0	0	0	0	Mode Register A	(MR1A, MR2A)	Mode Register A	(MR1A, MR2A)
0	0	0	1	Status Register A	(SRA)	Clock-Select Register A	(CSRA)
0	0	1	0	Do Not Access*		Command Register A	(CRA)
0	0	1	1	Receiver Buffer A	(RBA)	Transmitter Buffer A	(TBA)
0	1	0	0	Input Port Change Register	(IPCR)	Auxiliary Control Register	(ACR)
0	1	0	1	Interrupt Status Register	(ISR)	Interrupt Mask Register	(IMR)
0	1	1	0	Counter Mode: Current MSB of Counter	(CUR)	Counter/Timer Upper Register	(CTUR)
0	1	1	1	Counter Mode: Current LSB of Counter	(CLR)	Counter/Timer Lower Register	(CTLR)
1	0	0	0	Mode Register B	(MR1B, MR2B)	Mode Register B	(MR1B, MR2B)
1	0	0	1	Status Register B	(SRB)	Clock-Select Register B	(CSRB)
1	0	1	0	Do Not Access*		Command Register B	(CRB)
1	0	1	1	Receiver Buffer B	(RBB)	Transmitter Buffer B	(TBB)
1	1	0	0	Interrupt-Vector Register	(IVR)	Interrupt-Vector Register	(IVR)
1	1	0	1	Input Port (Unlatched)		Output Port Configuration Register	(OPCR)
1	1	1	0	Start-Counter Command**		Output Port Register (OPR)	Bit Set Command**
1	1	1	1	Stop-Counter Command**			Bit Reset Command**

* This address location is used for factory testing of the DUART and should not be read. Reading this location will result in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.

** Address triggered commands.

Table 4.2 is provided to illustrate the various input port pin functions. More detailed information can be obtained from Table 4.5 and 4.2 REGISTER DESCRIPTION.

Table 4.2 Programming of Input Functions

Function	Input Port Pin					
	IP5	IP4	IP3	IP2	IP1	IP0
General Purpose	Default	Default	Default	Default	Default	Default
Change-of-State Detector			Default	Default	Default	Default
External Counter 1X Clock Input				ACR [6:4]* = 000		
External Timer 16X Clock Input				ACR [6:4]* = 100		
External Timer 1X Clock Input				ACR [6:4]* = 101		
RxCA 16X		CSRA [7:4] = 1110				
RxCA 1X		CSRA [7:4] = 1111				
TxCA 16X			CSRA [3:0] = 1110			
TxCA 1X			CSRA [3:0] = 1111			
RxCB 16X				CSRB [7:4] = 1110		
RxCB 1				CSRB [7:4] = 1111		
TxCB 16	CSRB [3:0] = 1110					
TxCB 1X	CSRB [3:0] = 1111					
TxCTSA						MR2A [4] = 1
TxCTSB					MR2B [4] = 1	

Note : Default refers to the function the input port pins perform when not used in one of the other modes. Only those functions which show the register programming are available for use.

* In these modes, because IP2 is used for the counter/timer-clock input, it is not available for use as the channel B receiver-clock input.

Table 4.3 is provided to illustrate the various output port pin functions. More detailed information can be obtained from Table 4.5 and 4.2 REGISTER DESCRIPTION.

Table 4.3 Programming of Output Port Functions

Function	Output Port Pin							
	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
General Purpose	OPCR [7] = 0	OPCR [6] = 0	OPCR [5] = 0	OPCR [4] = 0	OPCR [3:2] = 00	OPCR [1:0] = 00	MR1B [7] = 0 MR2B [5] = 0	MR1A [7] = 0 MR2A [5] = 0
$\overline{\text{CTRDY}}$					OPCR [3:2] = 01, ACR [6] = 0*			
Timer Output					OPCR [3:2] = 01, ACR [6] = 1*			
TxCB × 1					OPCR [3:2] = 10			
RxCB × 1					OPCR [3:2] = 11			
TxCA × 16						OPCR [1:0] = 01		
TxCA × 1						OPCR [1:0] = 10		
TxCA × 1						OPCR [1:0] = 11		
$\overline{\text{TxRDYA}}$		OPCR [6] = 1*						
$\overline{\text{TxRDYB}}$	OPCR [7] = 1*							
$\overline{\text{RxRDYA}}$				OPCR [4] = 1, MR1A [6] = 0*				
$\overline{\text{RxRDYB}}$			OPCR [5] = 1, MR1B [6] = 0*					
$\overline{\text{FFULLA}}$				OPCR [4] = 1, MR1A [6] = 1*				
$\overline{\text{FFULLB}}$			OPCR [5] = 1, MR1B [6] = 1*					
$\overline{\text{RxRTSA}}$								MR1A [7] = 1
$\overline{\text{TxRTSA}}$								MR2A [5] = 1
$\overline{\text{RxRTSB}}$							MR1B [7] = 1	
$\overline{\text{TxRTSB}}$							MR2B [5] = 1	

Note : Only those functions which show the register programming are available for use.
* Pin requires a pullup resistor if used for this function.

Table 4.4 is provided to illustrate the various clock sources which may be selected for the counter and timer. More detailed information can be obtained from Table 4.5 and 4.2 REGISTER DESCRIPTION.

Table 4.4 Selection of Clock Sources for the Counter and Timer Modes

ACR [6]	
= 0	= 1

Counter Mode Clock Sources	ACR [5:4] =
External Input via Input Port Pin 2 (IP2)	00
Channel A 1X Transmitter Clock TxCA	01
Channel B 1X Transmitter Clock TxCB	10
Crystal Oscillator Divide by 16 via X1/CLK and X2 Inputs	11
External Input Divide by 16 via X1/CLK Input Pin	11

Timer Mode Clock Sources	ACR [5:4] =
External Input via Input Port Pin 2 (IP2)	00
External Input Divide by 16 via Input Port Pin 2 (IP2)	01
Crystal Oscillator via X1/CLK and X2 Input	10
Crystal Oscillator Divide by 16 via X1/CLK and X2 Inputs	11
External Input via X1/CLK Input Pin	10
External Input Divide by 16 via X1/CLK Input Pin	11

Note : Only those functios which show the register programming are available for use.

Care should be exercised if the contens of a register is changed during receiver/transmitter operation since certain changes may cause undesired results. For example, changing the number of bit-per-character while the transmitter is active may cause the transmission of an incorrect character. The contents of the mode registers (MR), the clock-select register (CSR), the output port configuration register (OPCR), and bit 7 of the auxiliary control register (ACR [7]) should only be changed after the receiver(s) and transmitter(s) have been issued software Rx and Tx reset commands. Similarly, certain changes to the auxiliary control register (ACR bits six through four) should only be made while the counter/timer (C/T) is not used (i.e, stopped if in counter mode, output and/or interrupt masked timer mode).

Mode registers one and two of each channel are accessed via independent auxiliary pointers. The pointer is set to channel A mode register one (MR1A) and channel B mode register one (MR1B) by RESET or by issuing a "reset pointer" command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1A or MR1B switches the pointer to channel A mode register (MR2A) or channel B mode register two (MR2B). The pointer then remains at MR2A or MR2B. So, subsequent accesses will address MR2A or MR2B, unless the pointer is reset to MR1A or MR1B as described above.

Mode, command, clock-select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 4.5 for descriptions of the register and input and output port bits.

Table 4.5 Register Bit Formats (1/6)

CHANNEL A MODE REGISTER 1 (MR1A) AND CHANNEL B MODE REGISTER 1 (MR1B)

Rx RTS Control	Rx $\overline{IRQ}$ Select	Error Mode	Parity Mode	Parity Type	Bits-per-Character
Bit 7	Bit 6	Bit 5	Bit 4 Bit 3	Bit 2	Bit 1 Bit 0
0 = Disabled 1 = Enabled	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode*	With Parity 0 = Even 1 = Odd Force Parity 0 = LOW 1 = HIGH Multidrop Mode 0 = Data 1 = Address	00 = 5 01 = 6 10 = 7 11 = 8

* The parity bit is used as the address/data bit in multidrop mode.

CHANNEL A MODE REGISTER 2 (MR2A) AND CHANNEL B MODE REGISTER 2 (MR2B)

Channel Mode	Tx RTS Control	CTS Enable Transmitter	Stop Bit Length
Bit 7 Bit 6	Bit 5	Bit 4	Bit 3 Bit 2 Bit 1 Bit 0
00 = Normal 01 = Automatic Echo 10 = Local Loopback 11 = Remote Loopback	0 = Disabled 1 = Enabled	0 = Disabled 1 = Enabled	

	Bit 3 Bit 2 Bit 1 Bit 0	6-8 Bits/ Character	5 Bits/ Character
(0)	0 0 0 0 =	0.563	1.063
(1)	0 0 0 1 =	0.625	1.125
(2)	0 0 1 0 =	0.688	1.188
(3)	0 0 1 1 =	0.750	1.250
(4)	0 1 0 0 =	0.813	1.313
(5)	0 1 0 1 =	0.875	1.375
(6)	0 1 1 0 =	0.938	1.438
(7)	0 1 1 1 =	1.000	1.500
(8)	1 0 0 0 =	1.563	1.563
(9)	1 0 0 1 =	1.625	1.625
(A)	1 0 1 0 =	1.688	1.688
(B)	1 0 1 1 =	1.750	1.750
(C)	1 1 0 0 =	1.813	1.813
(D)	1 1 0 1 =	1.875	1.875
(E)	1 1 1 0 =	1.938	1.938
(F)	1 1 1 1 =	2.000	2.000

Note: If an external 1× clock is used for the transmitter, MR2 bit 3 = 0 selects one stop bit and MR2 bit 3 = 1 selects two stop bits to be transmitted.

Table 4.5 Register Bit Formats (2/6)

CLOCK-SELECT REGISTER A (CSRA)

Receiver-Clock Select						Transmitter-Clock Select					
Bit 7	Bit 6	Bit 5	Bit 4	Baud Rate Set 1 ACR Bit 7 = 0	Baud Rate Set 2 ACR Bit 7 = 1	Bit 3	Bit 2	Bit 1	Bit 0	Baud Rate Set 1 ACR Bit 7 = 0	Baud Rate Set 2 ACR Bit 7 = 1
0	0	0	0	50	75	0	0	0	0	50	75
0	0	0	1	110	110	0	0	0	1	110	110
0	0	1	0	134.5	134.5	0	0	1	0	134.5	134.5
0	0	1	1	200	150	0	0	1	1	200	150
0	1	0	0	300	300	0	1	0	0	300	300
0	1	0	1	600	600	0	1	0	1	600	600
0	1	1	0	1200	1200	0	1	1	0	1200	1200
0	1	1	1	1050	2000	0	1	1	1	1050	2000
1	0	0	0	2400	2400	1	0	0	0	2400	2400
1	0	0	1	4800	4800	1	0	0	1	4800	4800
1	0	1	0	7200	1800	1	0	1	0	7200	1800
1	0	1	1	9600	9600	1	0	1	1	9600	9600
1	1	0	0	38.4K	19.2K	1	1	0	0	38.4K	19.2K
1	1	0	1	Timer	Timer	1	1	0	1	Timer	Timer
1	1	1	0	IP4-X16	IP4-X16	1	1	1	0	IP3-X16	IP3-X16
1	1	1	1	IP4-X1	IP4-X1	1	1	1	1	IP3-X1	IP3-X1

Note: Receiver clock is always a 16× clock except when CSRA seven through four equal 1111.

Note: Transmiter clock is always a 16× except when CSRA bits three zero equal 1111.

CLOCK-SELECT REGISTER B (CSRB)

Receiver-Clock Select						Transmitter-Clock Select					
Bit 7	Bit 6	Bit 5	Bit 4	Baud Rate Set 1 ACR Bit 7 = 0	Baud Rate Set 2 ACR Bit 7 = 1	Bit 3	Bit 2	Bit 1	Bit 0	Baud Rate Set 1 ACR Bit 7 = 0	Baud Rate Set 2 ACR Bit 7 = 1
0	0	0	0	50	75	0	0	0	0	50	75
0	0	0	1	110	110	0	0	0	1	110	110
0	0	1	0	134.5	134.5	0	0	1	0	134.5	134.5
0	0	1	1	200	150	0	0	1	1	200	150
0	1	0	0	300	300	0	1	0	0	300	300
0	1	0	1	600	600	0	1	0	1	600	600
0	1	1	0	1200	1200	0	1	1	0	1200	1200
0	1	1	1	1050	2000	0	1	1	1	1050	2000
1	0	0	0	2400	2400	1	0	0	0	2400	2400
1	0	0	1	4800	4800	1	0	0	1	4800	4800
1	0	1	0	7200	1800	1	0	1	0	7200	1800
1	0	1	1	9600	9600	1	0	1	1	9600	9600
1	1	0	0	38.4K	19.2K	1	1	0	0	38.4K	19.2K
1	1	0	1	Timer	Timer	1	1	0	1	Timer	Timer
1	1	1	0	IP2-X16	IP2-X16	1	1	1	0	IP5-X16	IP5-X16
1	1	1	1	IP2-X1	IP2-X1	1	1	1	1	IP5-X1	IP5-X1

Note: Receiver clock is always a 16× clock except when CSRB bits seven through four equal 1111.

Note: Transmiter clock is always a 16× except when CSRB bits three zero equal 1111.

Table 4.5 Register Bit Formats (3/6)

CHANNEL A COMMAND REGISTER (CRA) AND CHANNEL B COMMAND REGISTER (CRB)

Not Used*	Miscellaneous Commands	Transmitter Commands	Receiver Commands
Bit 7	Bit 6 Bit 5 Bit 4	Bit 3 Bit 2	Bit 1 Bit 0
X	0 0 0 No Command 0 0 1 Reset MR Pointer to MR1 0 1 0 Reset Receiver 0 1 1 Reset Transmitter 1 0 0 Reset Errot Status 1 0 1 Reset Channel's Break-Change Interrupt 1 1 0 Start Break 1 1 1 Stop Break	0 0 No Action, Stays in Present Mode 0 1 Transmitter Enabled 1 0 Transmitter Disabled 1 1 Don't Use, Indeterminated	0 0 No Action, Stays in Present Mode 0 1 Receiver Enabled 1 0 Receiver Disabled 1 1 Don't Use, Indeterminated

* Bit seven is not used and may be set to either zero or one.

CHANNEL A STATUS REGISTER (SRA) AND CHANNEL B STATUS REGISTER (SRB)

Received Bread	Framing Error	Pariaty Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
Bit 7*	Bit 6*	Bit 5*	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

* These status bits are appended to the corresponding data character in the receive FIFO and are valid only when the RxRDY bit set. A read of the status register provides these bits (seven through five) from the top of the FIFO together with bits four through zero. These bits are cleared by a reset error status command. In character mode, they are discarded when the corresponding data character is read from the FIFO.

OUTPUT PORT CONFIGURATION REGISTER (OPCR)

OP7	OP6	OP5	OP4	OP3	OP2
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3 Bit 2	Bit 1 Bit0
0 = OPR [7] 1 = TxRDYB	0 = OPR [6] 1 = TxRDYA	0 = OPR [5] 1 = RxRDYB/ FFULLB	0 = OPR [4] 1 = RxRDYA/ FFULLA	0 0 = OPR [3] 0 1 = C/T Output* 1 0 = TxCB (X1) 1 1 = RxCB (X1)	0 0 = OPR [2] 0 1 = TxCA (X16) 1 0 = TxCA (X1) 1 1 = RxCA (X1)

* IF OP3 is to be used for the timer output, the counter/timer should be programmed for timer (ACR [6]=1), the counter/timer preload registers (CTUR and CTLR) initialized, and the start counter command issued before setting OPCR (3:2)=01.

Note: OP1 and OP0 can be used as transmitter and receiver RTS control lines by appropriately programming the mode registers (MR1 [7] for the receiver RxRTX, and MR2 [5] for the transmitter TxRTS). OP1 is used for channel B's RTS control line and OP0 for channel A's RTS control line. When OP1 and OP0 are not used for RTS control, they may be used as general-purpose outputs. (See Table 4.3.)

Table 4.5 Register Bit Formats (4/6)

OUTPUT PORT REGISTER (OPR)

OPR7	OPR6	OPR5	OPR4	OPR3	OPR2	OPR1	OPR0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

AUXILIARY CONTROL REGISTER (ACR)

BRG SET Select*	Counter/Timer Mode and Source**			Delta*** IP3 $\overline{IRQ}$	Delta*** IP2 $\overline{IRQ}$	Delta*** IP1 $\overline{IRQ}$	Delta*** IP0 $\overline{IRQ}$
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Mode	Clock Source				
0 = Set 1	0 0 0	Counter	External (IP2) * * * *	0 = Disabled	0 = Disabled	0 = Disabled	0 = Disabled
1 = Set 2	0 0 1	Counter	TxCA – 1X Clock of Channel A Transmitter	1 = Enabled	1 = Enabled	1 = Enabled	1 = Enabled
	0 1 0	Counter	TxCB – 1X Clock of Channel B Transmitter				
	0 1 1	Counter	Crystal or External Clock (X1/CLK) Divided by 16				
	1 0 0	Timer	External (IP2) * * * *				
	1 0 1	Timer	External (IP2) Divided by 16* * * *				
	1 1 0	Timer	Crystal or External Clock (X1/CLK)				
	1 1 1	Timer	Crystal or External Clock (X1/CLK) Divided by 16				

* Should only be changed after both channels have been reset and are disabled.

** Should only be afterd while the counter/timer is not in use (i.e, stopped if in counter mode, output and/or interrupt masked if in timer mode).

*** Delta is equivalent to change-of-state.

**** In these modes, because IP2 is used for the counter/timer clock input, it is not available for use as the channel B receiver-clock input.

Tabel 4.5 Register Bit Formats (5/6)

INPUT PORT CHANGE REGISTER (IPCR)

Delta* Detected IP3	Delta* Detected IP2	Delta* Detected IP1	Delta* Detected IP0	Level IP3	Level IP2	Level IP1	Level IP0
Bit 7 0 = No 1 = Yes	Bit 6 0 = No 1 = Yes	Bit 5 0 = No 1 = Yes	Bit 4 0 = No 1 = Yes	Bit 3 0 = Low 1 = High	Bit 2 0 = Low 1 = High	Bit 1 0 = Low 1 = High	Bit 0 0 = Low 1 = High

*Delta is equivalent to change-of-state.

INTERRUPT STATUS REGISTER (ISR)

Input Port Change	Delta Break B	RxRDYB/ FFULLB	TxRDYB	Counter/ Timer Ready	Delta Break A	RxRDYA/ FFULLA	TxRDYA
Bit 7 0 = No 1 = Yes	Bit 6 0 = No 1 = Yes	Bit 5 0 = No 1 = Yes	Bit 4 0 = No 1 = Yes	Bit 3 0 = No 1 = Yes	Bit 2 0 = No 1 = Yes	Bit 1 0 = No 1 = Yes	Bit 0 0 = No 1 = Yes

INTERRUPT MASK REGISTER (IMR)

Input Port Change $\overline{IRQ}$	Delta Break B $\overline{IRQ}$	RxRDYB/ FFULLB $\overline{IRQ}$	TxRDYB $\overline{IRQ}$	Counter/ Timter Ready $\overline{IRQ}$	Delta Break A $\overline{IRQ}$	RxRDYA/ FFULLA $\overline{IRQ}$	TxRDYA $\overline{IRQ}$
Bit 7 0 = Masked 1 = Pass	Bit 6 0 = Masked 1 = Pass	Bit 5 0 = Masked 1 = Pass	Bit 4 0 = Masked 1 = Pass	Bit 3 0 = Masked 1 = Pass	Bit 2 0 = Masked 1 = Pass	Bit 1 0 = Masked 1 = Pass	Bit 0 0 = Masked 1 = Pass

Tabel 4.5 Register Bit Formats (6/6)

COUNTER/TIMER UPPER REGISTER (CTUR)

C/T [15]	C/T [14]	C/T [13]	C/T [12]	C/T [11]	C/T [10]	C/T [9]	C/T [8]
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

COUNTER/TIMER LOWER REGISTER (CTLR)

C/T [7]	C/T [6]	C/T [5]	C/T [4]	C/T [3]	C/T [2]	C/T [1]	C/T [0]
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

INTERRUPT VECTOR REGISTER (IVR)

IVR [7]	IVR [6]	IVR [5]	IVR [4]	IVR [3]	IVR [2]	IVR [1]	IVR [0]
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

INPUT PORT

*	**	IP5	IP4	IP3	IP2	IP1	IP0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

* Bit seven has no external pin. Upon reading the input port, bit seven will always be read as a one.

** Bit six has no external pin. Upon reading the input port, bit six will reflect the current logic level of $\overline{IACK}$.

OUTPUT PORT

PO7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bit 7 / $\overline{OPR}$ [7]	Bit 6 / $\overline{OPR}$ [6]	Bit 5 / $\overline{OPR}$ [5]	Bit 4 / $\overline{OPR}$ [4]	Bit 3 / $\overline{OPR}$ [3]	Bit 2 / $\overline{OPR}$ [2]	Bit 1 / $\overline{OPR}$ [1]	Bit 0 / $\overline{OPR}$ [0]

4.2 REGISTER DESCRIPTION

The following paragraphs provide a detailed description of each register and its function.

4.2.1 Channel A Mode Register1 (MR1A)

The channel A mode register one (MR1A) is accessed when the channel A mode register pointer points to MR1. The pointer is set to MR1 by $\overline{\text{RESET}}$ or by a "set pointer" command applied via control register A. After reading or writing MR1A, the pointer will point to channel A mode register two (MR2A).

4.2.1.1 CHANNEL A RECEIVER REQUEST-TO-SEND CONTROL – MR1A [7]

This bit controls the negation of the channel A request-to-send ($\overline{\text{RTSA}}$) parallel output (OP0) by the receiver. This output is normally asserted by setting OPR [0] and negated by clearing OPR [0]. MR1A [7]=1 causes $\overline{\text{RTSA}}$ to be negated upon receipt of a valid start bit if the channel A FIFO is full. $\overline{\text{RTSA}}$ will be reasserted when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the $\overline{\text{RTSA}}$ output signal to control the clear-to-sent $\overline{\text{CTS}}$ input of the transmitting device.

4.2.1.2 CHANNEL A RECEIVER-INTERRUPT SELECT-MR1A [6]

This bit selects either the channel A receiver-ready status (RxRDY) or the channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on the parallel output OP4 if OP4 is programmed as an interrupt output via the output port configuration register (OPCR).

4.2.1.3 CHANNEL A ERROR MODE SELECT – MR1A [5]

This bit selects the operating mode of the three FIFOed status bit (framing error (FE), parity error (PE), and received break (RB)) for channel A. In the "character" mode, status provided in the status register is given on a character-by-character basis and applies only to the character at the top of the FIFO. In the "block" mode, the status provided in the status register for these bits is the accumulation (logical OR) of the status for all characters coming to the top of the FIFO since the last reset error status command for channel A was issued.

4.2.1.4 CHANNEL A PARITY MODE SELECT – MR1A [4:3]

If "with parity" or "force parity" is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1A [4:3]=11 selects channel A to operate in the multidrop mode described in 3.4 MULTIDROP MODE.

4.2.1.5 CHANNEL A PARITY TYPE SELECT-MR1A [2]

The bit selects the parity type (odd or even) if the "with parity" mode is programmed by MR1A [4:3], and the polarity of the forced parity bit if the "force parity" mode is programmed. It has no effect if the "no parity" mode is programmed. In the multidroup mode, it configures the transmitter for address character transmission or data character transmission.

4.2.1.6 CHANNEL A BITS-PER-CHARACTER SELECT – MR1A [1:0]

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

4.2.2 Channel A Mode Register 2 (MR2A)

The channel A mode register two (MR2A) is accessed when the channel A mode register pointer pints to mode register two (MR2A), which occurs after any access to channel A mode register one (MR1A). Accesses to MR2A do not change the pointer.

4.2.2.1 CHANNEL A MODE SELECT-MR2A [7:6]

Each channel of DUART can operate in one of four modes:normal, automatic echo, local loopback, or remote loopback. MR2A [7:6]=00 is the normal mode, with the transmitter and receiver operating independently. MR2A [7:6]=01 places the channel in the automatic-echo mode, which automatically retransmits the received data. The following conditions are true while in the automatic-echo mode:

1. Received data is reclocked and retransmitted on the channel A transmitter serial-data output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The channel A transmitter ready and transmitter empty status bits are inactive.
5. The received parity is checked, but is not recalculated for transmission, i.e, the transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A [7:6]=10selects the first of these, the local-loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The channel A transmitter serial-data output is held high.
4. The channel A receiver serial-data input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU-to-transmitter and receiver communication continue normally.

The second diagnostic mode is the remote-loopback mode, selected by MR2A [7:6]=11. In this mode:

1. Received data is reclocked and retransmitted on the channel A transmitter serial-data output.
2. The receive clock is used for the transmitter.
3. Received data cannot be read by the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not recalculated for transmission; i.e, the transmitted parity bit is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

Switching between modes should only be done while the channel is disabled. This is because the selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character.

Similarly, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of automatic-echo or remote-loopback modes. If the deselection of these modes occurs just after the receiver has sampled the stop bit (indicated in automatic echo by assertion of receiver ready), and the transmitter is enabled, the transmitter will remain in automatic-echo mode until the entire stop bit has been retransmitted.

4.2.2.2 CHANNEL A TRANSMITTER REQUEST-TO-SEND CONTROL – MR2A [5]

This bit controls the negation of the channel A transmitter request-to-send ($\overline{RTSA}$) paralled output (OP0) by the transmitter. This output is normally asserted by setting OPR [0] and negated by clearing OPR [0]. In applications where the transmitter is disabled after transmission is complete, programming MR2A [5]=1 causes OPR [0] to be cleared automatically one bit time after the characters in the channel A transmit shift register and in the transmit holding register, if any, are completely transmitted, including the programmed number of stop bits. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program the DUART for the automatic-reset mode: MR2A [5]=1.
2. Enable the transmitter.
3. Assert channel A transmitter request-to-send control: OPR [0]=1.
4. Send the message,
5. Disabel the transmitter after the transmitter-ready bit becomes asserted (SRA [2]=1).
6. The last character will be transmitted and OPR [0] will be cleared one bit tiem after the last stop bit, causing the channel A transmitter request-to-send control to be negated.

4.2.2.3 CHANNEL A CLEAR-TO-SEND CONTROL – MR2A [4]

If this bit is zero, channel A clear-to-send control ($\overline{CTSA}$)has no effect on the transmitter. If this bit is a one, the transmitter checks the state of $\overline{CTSA}$ (IP0) each time it is ready to send a character. If IP0 is asserted (low), the character is transmitted. If it is negated (high), the channel A transmitter serial-data output remains in the marking state and the transmission is delayed until $\overline{CTSA}$ goes low. Changes in the $\overline{CTSA}$ while a character is being transmitted do not affect the transmission of that character.

4.2.2.4 CHANNEL A STOP BIT LENGTH SELECT-MR2A [3:0]

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of nine-sexteenths-to-one and one and nine-sexteenths-to-two (1 9/16→2) bits, in increments of one-sixteenth bit, can be programmed for character lengths of six, seven, and eight bits. For a character length of five bits, one and one-sixteenth-to-two (1 1/16→2) stop bits can be programmed in increments of one-sexteenth bit. The receiver, in all cases, only checks for a "mark" condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled).

If an external 1X clock is used for the transmitter, MR2A [3]=0 selects one stop bit and MR2A [3]=1 selects two stop bits to be transmitted.

4.2.3 Channel B Mode Register 1 (MR1B)

The channel B mode register one (MR1B) is accessed when the channel B mode register pointer points to mode register one (MR1). The pointer is set to MR1 by $\overline{\text{RESET}}$ or by a "set pointer" command applied by way of the channel B command register. After reading or writing MR1B, the pointer will point to the channel B mode register two (MR2B).

The bit definitions for this register are identical to the bit definitions for MR1A, except that all control actions apply to the channel B receiver and transmitter and their corresponding inputs and outputs.

4.2.4 Channel B Mode Register 2 (MR2B)

The channel B mode register two (MR2B) is accessed when the channel B mode register pointer points to mode register two (MR2), which occurs after any access to channel B mode register one (MR1B). Accesses to MR2B do not change the pointer.

The bit definitions for this register are identical to the bit definitions for MR2A, except that all control actions apply to the channel B receiver and transmitter and their corresponding input and outputs.

4.2.5 Channel A Clock-Select Register (CSRA)

The following paragraphs provide a detailed description of the channel A clock-select register.

4.2.5.1 CHANNEL A RECEIVER CLOCK-SELECT – CSRA [7:4]

This field selects the baud-rate clock for the channel A receiver form a set of baud rates. There are two sets of baud rates dependent upon bit seven of the auxiliary control register. These sets, with their respective baud rates, are shown in Table 4.5. Set one is selected if ACR [7] = 0 and set two is selected if ACR [7] = 1. The receiver clock is always 16 times the baud rate given in the table except for CSRA [7:4] = 1111, when an external 1× clock is used. When CSRA [7:5] = 111, the external clock connected to parallel input IP4 is used by the receiver.

4.2.5.2 CHANNEL A TRANSMITTER CLOCK SELECT – CSRA [3:0]

This field selects the baud-rate clock for the channel A transmitter from a set of baud rates. As with the receiver clock, there are two sets of baud rates dependent upon bit seven of the auxiliary control register. These sets, with their respective baud rates, are shown in Table 4.5. The transmitter clock is always 16 times the baud rate given in the table except for CSRA [3:0] = 1111, when an external 1× clock is used. When CSRA [3:1] = 111, the external clcok connected to parallel input IP3 is used by the transmitter.

4.2.6 Channel B Clock-Select Register (CSRB)

The follwing paragraphs provide a detailed description of the channel B clock-select register.

4.2.6.1 CHANNEL B RECEIVER CLOCK SELECT – CSRB [7:4]

This field selects the baud-rate clcok for the channel B transmitter from a set of baud rates. There are two sets of baud rates dependent upon bit seven of the auxiliary control register. These sets, with their respective baud rates, are shown in Table 4.5. Set one is selected if ACR [7] = 0 and set two is selected if ACR [7] = 1. The receiver clock is always 16 times the baud rate given in the table except for CSRB [7:4] = 1111, when an external 1× clock is used. When CSRB [7:5] = 111, the external clock connected to parallel input IP2 is used by the receiver.

4.2.6.2 CHANNEL B TRANSMITTER CLOCK SELECT – CSRB [3:0]

The field selects the baud-rate clock for the channel B transmitter from a set of baud rates. As with the receiver clock, there are two sets of baud rates dependent upon bit seven of the auxilary control register. These sets, with their respective baud rates, are shown in Table 4.5. The transmitter clock is always 16 times the baud rate given in the table except of CSRB [3:0] = 111, when an external 1× clock is used. When CSRB [3:1] = 111, the external clock connected to parallel input IP5 is used by the transmitter.

4.2.7 Channel A Command Register (CRA)

The channel A command register (CRA) is a register used to supply commands to channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting; e.g, the "enable transmitter" and "reset transmitter" commands cannot be specified in a single command word.

4.2.7.1 CRA [7]

This bit is not used and may be set to either zero or one.

4.2.7.2 CHANNEL A MISCELLANEOUS COMMANDS – CRA [6:4]

The encoded value of this field may be used to specify a single command as follows:

CRA [6:4]	Command
000	No command.
001	Reset Mode Register Pointer. This command causes the channel A mode register pointer to point to mode register one.
010	Reset Receiver. This command resets the channel A receiver. The receiver is immediately disabled, the RxRDY and FFULL bits in the SRA are cleared, and the RxFIFO pointer is reinitialized. All other registers are unaltered. This command should be used in lieu of the receiver disable command whenever the receiver configuration is to be changed, as it places the receiver in a guaranteed known state.
011	Reset Transmitter. This command resets the channel A transmitter. The transmitter is immediately disabled and the TxRDY and TxEMT bits in the SRA are cleared. All other registers are unaltered. This command should be used in lieu of the transmitter disable command whenever the transmitter configuration is to be changed, as it places the receiver in a guaranteed known state.
100	Reset Error Status. This command clears the channel A received break (RB), parity error (PE), framing error (FE), and overrun error (OE) flags in the status register (SRA [7:4]). This command is used in the character mode to clear OE status (RB, PE, and FE bits will also be cleared) and is used in the block mode to clear all error status flags after a block of data has been received.
101	Reset Channel A Break Change Interrupt. This command causes the channel A break detect change bit in the interrupt status register (ISR [2]) to be cleared to zero.
110	Strat Break. This command forces the channel A transmitter serial-data output (TxDA) low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the transmit holding register, the start of the break will be delayed until that character or any others loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted. The state of the $\overline{CTS}$ input is ignored for this command.

111 Stop Break. The channel A transmitter serial-data output (TxDA) line will go high (marking) within two bit times. TxDA will remain high for one bit time before the next character, if any, is transmitted.

4.2.7.3 CHANNEL A TRANSMITTER COMMANDS – CRA [3:2]

The encoded value of this field specifies commands for the transmitter as follows:

CRA [3:2]	Command
00	No action is taken. The transmitter stays in its present mode. If the transmitter was enabled it remains enabled, if disabled it remains disabled.
01	Enable Transmitter. This command enables operation of the channel A transmitter. The transmitter-ready status bit will be asserted.
10	Disable Transmitter. This command terminates transmitter operation and resets the transmitter-ready and transmitter-empty status bits. However, if a character is being transmitted when the transmitter is disabled, the transmission of the character is completed before assuming the inactive state.
11	Do not use. The result of this is indeterminate.

4.2.7.4 CHANNEL A RECEIVER COMMANDS – CRA [1:0]

The encoded value of this field specifies commands for the receiver as follows:

CRA [1:0]	Command
00	No action is taken. The receiver stays in its present mode. If the receiver was enabled it remains enabled, if disabled it remains disabled.
01	Enable Receiver. This command enables operation of the channel A receiver. If the DUART is not in the multidrop mode, this command also forces the receiver into the search-for-start bit state.
10	Disable Receiver. This command terminates operation of the receiver immediately-a character being received will be lost. The command has no effect on the receiver status bits or any other control register. If the DUART has been programmed to operate in the local loopback or multidrop mode, the receiver operates even if it is disabled. Refer to SECTION 3 OPERATION for further information.
11	Do not use. The result of this is indeterminate.

4.2.8 Channel B Command Register (CRB)

The channel B command register (CRB) is a register used to supply commands to channel B. Multiple commands can be specified in a single write to CRB as long as the commands are nonconflicting; e.g., the "enable transmitter" and "reset transmitter" command cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for channel A command register, except that all control actions apply to the channel B receiver and transmitter and their corresponding inputs and outputs.

4.2.9 Channel A Status Register (SRA)

The following paragraphs provide a detailed description of the channel A status register.

4.2.9.1 CHANNEL A RECEIVED BREAK-SRA [7]

This bit indicates an all zero character of the programmed length has been received without a stop bit. This bit is valid only when the RxRDY bit is set (SRA [0] = 1). Only a single FIFO position is occupied when a break is received;further entries to the FIFO are inhibited until the channel A receiver serial-data input line returns to the marking state for at least one-half a bit time (two successive edges of the internal or external X 1clock).

When this bit becomes set, the channel A "change in break" bit in the interrupt status register (ISR [2]) is also set. Additionally, ISR [2] is set when the end of break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character it must persist until at least the end of the next character time in order for it to be detected.

4.2.9.2 CHANNEL A FRAMING ERROR – SRA [6]

This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position. This bit is valid only when the RxRDY bit is set (SRA [0] = 1).

4.2.9.3 CHANNEL A PARITY ERROR – SRA [5]

This bit becomes set when the "with parity" or "force parity" mode is programmed by mode register one and the correspondign character in the FIFO is received with incorrect parity. In the multidrop mode the parity error bit position is used to store the received address/data bit. This bit is valid only when the RxRDY bit is set (SRA [0] = 1).

4.2.9.4 CHANNEL A OVERRUN ERROR – SRA [4]

This bit when set, indicates one or more characters in the received data stream have been lost. It becomes set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error, and framing error status, if any) is lost. This bit is cleared by a reset error status command.

4.2.9.5 CHANNEL A TRANSMITTER EMPTY – SRA [3]

This bit will be set when the channel A transmitter underruns; i.e., both the transmit holding register and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the transmit holding register awaition transmission. It is cleared when the transmit holding register is loaded by the CPU or when the transmitter is disabled.

4.2.9.6 CHANNEL A TRANSMITTER READY – SRA [2]

This bit, when set, indicates that the transmit holding register is empty and ready to be loaded with a character. Transmitter ready is set when the character is transferred to the transmit shift register. This bit is cleared when the transmit holding register is loaded by the CPU. Transmitter ready is also cleared when the transmitter is disabled and is set when the transmitter is first enabled; i.e., characters loaded into the transmit holding register while the transmitter is disabled will not be transmitted.

4.2.9.7 CHANNEL A FIFO FULL – SRA [1]

This bit is set when a character is transferred from the receive shift register to the receiver FIFO and the transfer causes the FIFO to become full; i.e., all three FIFO holding register positions are occupied. It is cleared when the CPU reads the receiver buffer. If a character is waiting in the receive shift register because the FIFO is full, the channel A FIFO full status bit will not be cleared when the CPU reads the receiver buffer.

4.2.9.8 CHANNEL A RECEIVER READY – SRA [0]

This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the receiver buffer, providing there are no more characters still in the FIFO after this read.

4.2.10 Channel B Status Register (SRB)

The bit definitions for this register are identical to the bit definitions for the channel A status register, except the status applies to the channel B receiver and transmitter and their corresponding inputs and outputs.

4.2.11 Output Port Configuration Register (OPCR)

This register individually configures each bit of the 8-bit parallel output port for general purpose use or an auxiliary function serving the communication channels.

4.2.11.1 OP7 OUTPUT SELECT – OPCR [7]

This bit programs the parallel output OP7 to provide either the complement of OPR [7] or the channel B transmitter interrupt output, which is the complement of the channel B transmitter ready status bit. When configured for the channel B transmitter interrupt, OP7 acts as an open-collector output and is not masked by the contents of the interrupt mask register.

4.2.11.2 OP6 OUTPUT SELECT – OPCR [6]

This bit programs the parallel output OP6 to provide either the complement of OPR [6] or the channel A transmitter interrupt output, which is the complement of the channel A transmitter ready status bit. When configured for the channel A transmitter interrupt, OP6 acts as an open-collector output and is not masked by the contents of the interrupt mask register.

4.2.11.3 OP5 OUTPUT SELECT – OPCR [5]

This bit programs the parallel output OP5 to provide either the complement of OPR [5] or the channel B receiver interrupt output, which is the complement of ISR [5]. When configured for the channel B receiver interrupt, OP5 acts as an opencollector output and is not masked by the contents of the interrupt mask register.

4.2.11.4 OP4 OUTPUT SELECT – OPCR [4]

This bit programs the parallel output OP4 to provide either the complement of OPR [4] or the channel A receiver interrupt output, which is the complement of ISR [1]. When configured for the channel A receiver interrupt, OP4 acts as an opencollector output and is not masked by the contents of the interrupt mask register.

4.2.11.5 OP3 OUTPUT SELECT – OPCR [3:2]

This field programs the parallel output OP3 to provide one of the following:

OPCR [3:2]	OP3 Function
00	In this configuration OP3 becomes the complement of OPR [3].
01	In this configuration OP3 provides the counter/timer output. OP3 acts as an opencollector output and is not masked by the contents of the interrupt mask register. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command. Because the counter/timer, while in timer mode, cannot be stopped, if the counter/timer is to operate in timer mode and its output is programmed to appear on OP3, OPCR [3:2] should be cleared until the counter/timer has been programmed for the desired operation.
10	In this configuration OP3 becomes the 1× clock for the channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a freerunning 1× clock is output.
11	In this configuration OP3 becomes the 1× clock for the channel B receiver, which is the clock that samples the received data. If data is not being received, a free-running 1× clock is output.

4.2.11.6 OP2 OUTPUT SELECT-OPCR [1:0]

This field programs the parallel output OP2 to provide one of the following:

OPCR [1:0]	OP2 Function
00	In this configuration OP2 becomes the complement of OPR [2].
01	In this configuration OP2 becomes the 16× clock for the channel A transmitter. This is the clock selected by CSRA [3:0] and will be a 1× clock if CSRA [3:0]=1111.
10	In this configuration OP2 becomes the 1× clock for the channel A transmitter, which is the clock that shifts the transmitted data. A free running 1× clock is always output in this mode.
11	In this configuration OP2 becomes the 1× clock for the channel A receiver, which is the clock that samples the received data. A free running 1× clock is always output in this mode.

4.2.12 Output Port Register-OPR [7:0]

These bits contain the complement of the logic levels output at the output port pins [OP0-OP7]. Bits of this register are set by performing a bit set command during a write cycle, with data specifying the bits to be set (one equals set, zero equal no change). Bits of this register are cleared by performing a bit reset command during a write cycle, with data specifying the bits to be cleared (one equals reset, zero equals no change).

4.2.13 Auxiliary Control Register (ACR)

The following paragraphs provide a detailed description of the auxiliary control register (ACR).

4.2.13.1 BAUD-RATE GENERATOR SET SELECLT – ACR [7]

This bit selects one of the two sets of baud rates that can be generated by the baud-rate generator:

Set 1 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates available for use by the channel A and B receivers and transmitters are described under 4.2.5 Channel A Clock-Select Register (CSRA) and 4.2.6 Channel B Clock-Select Register (CSRB). Baud-rate generator characteristics are given in Table 4.6.

Table 4.6 Baud-Rate Generator Characteristics
Crystal or Clock = 3.6864 MHz

Nominal Rate (Baud)	Actual 16X Clock (kHz)	Error (Percent)	Nominal Rate (Baud)	Actual 16X Clock (kHz)	Error (Percent)
50	0.8	0	1200	19.2	0
75	1.2	0	1800	28.8	0
100	1.759	−0.069	2000	32.056	0.175
134.5	2.153	0.059	2400	38.4	0
150	2.4	0	4800	76.8	0
200	3.2	0	7200	115.2	0
300	4.8	0	9600	153.6	0
600	9.6	0	19.2k	307.2	0
1050	16.756	−0.260	38.4k	614.4	0

Note : Duty cycle of 16× clocks is 50% ±1%.

4.2.13.2 COUNTER/TIMER MODE AND CLOCK SURCE SELECT – ACR [6:4]

This field seleclts the operating mode of the counter/-timer and its clock source as shown in Table 4.4.

4.2.13.3 IP3, IP2, IP1, AND IP0 CHANGE-OF-STATE INTERRUPT ENABLE – ACR [3:0]

This field seleclts which bits of the input port change register can cause the input change bit in the interrupt status register (ISR [7]) to be set. If a bit of ACR [3:0] is set to the "enabled" state (set to one) and interrupt mask register bit seven in set (IMR [7] = 1) to enable input port change interrupts, then the setting of the corresponding bit in the input port change register by an external transition on that input pin will result in ISR [7] being set and an interrupt output generated. If a bit of ACRC [3:0] is in the "disabled" state (cleared to zero), the setting of that bit in the input port change register has no effect on ISR [7].

4.2.14 Input Port Change Register (IPCR)

The following paragraphs provide a detailed description of the input port change register.

4.2.14.1 IP3, IP2, IP1, AND IP0 CHANGE OF STATE – IPCR [7:4]

These bits are set when a change-of- state, a high-to-low or low-to-high transition, lasting longer than 25-50 microseconds, occurs at their respective input pins. They are cleared when the input port change register is read by the CPU. A read of the input port change register also clears ISR [7], the input change bit in the interrupt status register. The setting of these bits can be programmed by the auxiliary control register to generate an interrupt to the CPU.

4.2.14.2 IP3, IP2, IP1, AND IP0 CURRENT STATE – IPCR [3:0]

These bits provide the current state of their respective inputs. The information is unlatched and reflects the state of the input pins at the time the input port change register is read.

4.2.15 Interrupt Status Register (ISR)

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register. If a bit in the interrupt status register is a one and the corresponding bit in the interrupt mask register is also a one, the $\overline{IRQ}$ output will be asserted. If the correspondigng bit in the interrupt mask register is a zero, the state of the bit in the interrupt status register has no effect on the $\overline{IRQ}$ output.

Note that the interrupt mask register does not mask the reading of the interrupt status register – the true status will be provided regardless of the contents of the intrrupt mask register. The contents of this register are initialized to 0016 when the DUART is reset.

4.2.15.1 INPUT PORT CHANGE STATUS – ISR [7]

This bit is a one when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR [3:0]. This bit is cleared when the CPU reads the input port change register.

4.2.15.2 CHANNEL B CHANGE IN BREAK – ISR [6]

This bit, when set, indicates that the channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel B reset break change interrupt command.

4.2.15.3 CHANNEL B RECEIVER READY OR FIFO FULL – ISR [5]

The function of this bit is programmed by MR1B [6]. If programmed as receiver ready, it indicates that a character has been received in channel B and is waiting in the receiver buffer FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the receiver buffer. If after this read there are more characters still in the FIFO, the bit will be set again after the FIFO is "popped". If programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is cleared when the CPU reads the receiver buffer. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

4.2.15.4 CHANNEL B TRANSMITTER READY – ISR [4]

This bit is a duplicate of channel B transmitter ready (SRB [2]).

4.2.15.5 COUNTER/TIMER READY – ISR [3]

In the counter mode, this bit is set when the counter reaches terminal count and is cleared when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches terminal count). The bit is cleared by a stop counter command. The command, however, does not stop the counter/timer (see 3.5 COUNTER/TIMER).

4.2.15.6 CHANNEL A CHANGE IN BREAK – ISR [2]

This bit, when set, indicates that the channel A receiver has detected the beginning or the end of a received break. It is cleared when the CPU issues a channel A reset break change interrupt command.

4.2.15.7 CHANNEL A RECEIVER READY OR FIFO FULL – ISR [1]

The function of this bit is programmed by MR1A [6]. If programmed as receiver ready, it indicates that a character has been received in channel A and is waiting in the receiver buffer FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the receiver buffer. If after tis read there are more characteers still in the FIFO, the bit will be set again after the FIFO is "popped". If programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is cleared when the CPU reads the receiver buffer. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

4.2.15.8 CHANNEL A TRANSMITTER READY – ISR [0]

This bit is a duplicate of channel A transmitter ready (SRA [2]).

4.2.16 Interrupt Mask Register (IMR)

This register is used to select which bits in the interrupt status register can cause an interrupt output. If a bit in the interrupt status register is a one and the corresponding bit in the interrupt mask register is also a one, the $\overline{IRQ}$ output will be asserted. If the corresponding bit in the interrupt mask register is a zero, the state of the bit in the interrupt status register has no effect on the $\overline{IRQ}$ output.

Note that the intrerrupt mask register does not mask the programmable interrupt outputs OP7 ~ OP3 nor the reading of the interrupt status register.

4.2.17 Count Registers (CUR and CLR)

The count upper register (CUR) and count register (CLR) hold the most-significant byte and the least-significant byte of the current value in the counter/timer, respectively. These registers should only be read when the counter/timer is in counter mode and the counter is stopped. See 3.5 COUNTER/TIMER for further information.

4.2.18 Counter/Timer Preload Registers (CTUR and CTLR)

The counter/timer upper register (CTUR) and counter/timer lower register (CTLR) hold the eight most-significant bits and eight least-significant bits, respectively, of the preload value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the concatenation of CTUR with CTLR is 000216. Note that CTUR and CTLR are write-only registers and cannot be read by the CPU.

4.2.19 Interrupt Vector Register (IVR)

This register contains the interrupt vector. When the DUART responds to a valid interrupt acknowledge ($\overline{IACK}$) cycle the contents of this register are placed on the data bus. Upon reset, this register will contain OF16, which is the TMP68000 exception vector assignment for uninitialized interrupt vectors.

5. ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the TMP68681.

5.1 ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 ~ + 6.0	V
Input Voltage	V_{in}	−0.5 ~ + 6.0	V
Operating Temperature Range	T_a	0 ~ + 70	℃
Storage Temperature	T_{stg}	−65 ~ + 150	℃

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

5.2 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, T_a = 0°C~70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, Except X1/CLK	V_{IH}	2.0	–	–	V
Input High Voltage, X1/CLK	V_{IH}	4.0	–	–	V
Input Low Voltage	V_{IL}	–	–	0.8	V
Output High Voltage, Except Open-Collector Outputs (I_{OH} = – 400 μA)	V_{OH}	2.4	–	–	V
Output Low Voltage (I_{OL} = 2.4mA)	V_{OL}	–	–	0.4	V
Input Leakage Current (V_{in} = 0 to V_{CC})	I_{IL}	– 10	–	10	μA
Data Bus Hi-Z Leakage Current (V_{OUT} = 0 to V_{CC})	I_{LL}	– 10	–	10	μA
Open-Collector Output Leakage Current (V_{OUT} = 0 to V_{CC})	I_{OC}	– 10	–	10	μA
Power Supply Current	I_{CC}	–	–	150	mA
Capacitance (V_{in} = 5V, Ta = 25°C, f = 1MHz)	C_{in}	–	–	15	pF
X1/CLK Low Input Current Vin = 0, X2 Grounded Vin = 0, X2 Floated	I_{X1L}	 – 4.0 – 3.0	 – 2.0 – 1.5	 0 0	mA
X1/CLK High Input Current Vin = Vcc, X2 Grounded Vin = Vcc, X2 Floated	I_{X1H}	 – 1.0 0	 0.2 3.5	 1.0 10.0	mA
X2 Low Input Current Vin = 0, X1/CLK Floated	I_{X2L}	– 100	– 30	0	μA
X2 High Input Current Vin = Vcc, X1/CLK Floated	I_{X2H}	0	+ 30	100	μA

5.3 AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, T_a = 0°C~70°C, See Note 1)

Characteristic	Symbol	Min	Max	Unit
X1/CLK Frequency (See Note 2)	f_{CLK}	2.0	4.0	MHz
Counter/Timer Clock Frequency	f_{CTC}	0	4.0	MHz
Receiver Clock Frequency (RxC) 16X Clock 1X Clock	f_{RX}	 0 0	 2.0 1.0	MHz
Transmitter Clock Frequency (TxC) 16X Clock 1X Clock	f_{TX}	 0 0	 2.0 1.0	MHz

Note 1 : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for outputs:

C_L = 150 picofarads, R_L = 750 ohm to V_{CC}.

2 : To use the standard baud rates selected by the clock-select register given in Table 4.5, the X1/CLK frequency shold be set to 3.6864 MHz or a 3.6864 MHz crystal should be connected across pins X1/CLK and X2.

5.4 AC ELECTRICAL CHARACTERISTICS – $\overline{\text{RESET}}$ TIMING

(See Figure 5.1 and Note 1)

Characteristic	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ Pulse Width	t_{RES}	1.0	–	μs

Note 1 : All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: C_L = 150 picofarads, R_L = 750 ohms to V_{CC}. Test conditions for interrupt outputs: C_L = 50 picofarads, R_L = 27 kilohms to V_{CC}.

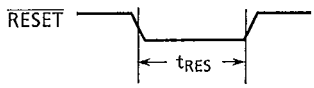


Figure 5.1 $\overline{\text{RESET}}$ Timing

5.5 AC ELECTRICAL CHARACTERISTECS – READ CYCLE BUS TIMING

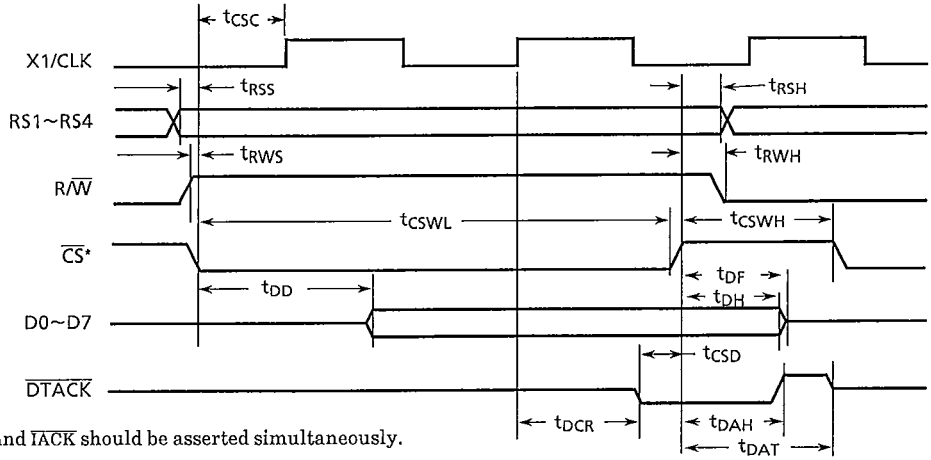
(See Figure 5.2 and Note 1)

Characteristic	Symbol	Min	Max	Unit
$\overline{CS}$ Setup Time to X1/CLK High (See Note 2)	t_{CSC}	90	–	ns
RS1~RS4 Setup Timer to $\overline{CS}$ Asserted	t_{RSS}	10	–	ns
R/$\overline{W}$ Setup Timer to $\overline{CS}$ ASsserted	t_{RWS}	0	–	ns
$\overline{CS}$ Pulse Width Asserted (See Note 3)	t_{CSWL}	205	–	ns
Data Valid from $\overline{CS}$ Asserted	t_{DD}	–	175	ns
$\overline{DTACK}$ Asserted from X1/CLK High	t_{DCR}	–	125	ns
$\overline{CS}$ Negated from $\overline{DTACK}$ Asserted (See Note 3)	t_{CSD}	20	–	ns
RS1~RS4 Hold Time from $\overline{CS}$ Negated	t_{RSH}	0	–	ns
R/$\overline{W}$ Hold Time from $\overline{CS}$ Negated	t_{RWH}	0	–	ns
Data Hold Time from $\overline{CS}$ Negated	t_{DH}	0	–	ns
Data Bus Floating from $\overline{CS}$ Negated	t_{DF}	–	100	ns
$\overline{DTACK}$ Negated from $\overline{CS}$ Negated	t_{DAH}	–	100	ns
$\overline{DTACK}$ Hi-Z from $\overline{CS}$ Negated	t_{DAT}	–	125	ns
$\overline{CS}$ Pulse Width Negated	t_{CSWH}	90	–	ns

Note 1: All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nonoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: C_L=150 picofarads, R_L=750 ohms to V_{CC}. Test conditions for interrupt outputs: C_L=50 picofarads, R_L=27 kilohms to V_{CC}.

2: This specification is made only to insure $\overline{DTACK}$ is asserted with respect to the rising edge of X1/CLK as shown in Figure 5.2, not to guarantee operation of the part. If the setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

3: The t_{CSD} specification is made only to insure that $\overline{DTACK}$ will be asserted. If $\overline{CS}$ is negated before $\overline{DTACK}$ is asserted, $\overline{DTACK}$ may not be asserted.



* $\overline{CS}$ and $\overline{IACK}$ should be asserted simultaneously.

Figure 5.2 Read Cycle Bus Timing

5.6 ELECTRICAL CHARACTERISTICS – WRITE CYCLE BUS TIMING

(See Figure 5.3 and Note 1)

Characteristic	Symbol	Min	Max	Unit
$\overline{CS}$ Setup Time to X1/CLK High (See Note 2)	t_{CSC}	90	–	ns
RS1~RS4 Setup Time to $\overline{CS}$ Asserted	t_{RSS}	10	–	ns
R/$\overline{W}$ Setup Time to $\overline{CS}$ Asserted	t_{RWS}	0	–	ns
$\overline{CS}$ Pulse Width Asserted (See Note 3 and 4)	t_{CSWL}	205	–	ns
Data Setup Time to X1/CLK High (See Note 4)	t_{DS}	100	–	ns
Data Setup Time to $\overline{CS}$ Negated (See Note 4)	t_{DSCS}	100	–	ns
$\overline{DTACK}$ Asserted from X1/CLK High	t_{DCW}	–	125	ns
$\overline{CS}$ Negated from $\overline{DTACK}$ Asserted (See Note 3)	t_{CSD}	20	–	ns
RS1~RS4 Hold Time from $\overline{CS}$ Negated	t_{RSH}	0	–	ns
R/$\overline{W}$ Hold Time from $\overline{CS}$ Negated	t_{RWH}	0	–	ns
Data Hold Time from $\overline{CS}$ Negated	t_{DH}	0	–	ns
$\overline{DTACK}$ Negated from $\overline{CS}$ Negated	t_{DAH}	–	100	ns
$\overline{DTACK}$ Hi-Z from $\overline{CS}$ Negated	t_{DAT}	–	125	ns
$\overline{CS}$ Pulse Width Negated (See Note 5)	t_{CSWH}	90	–	ns

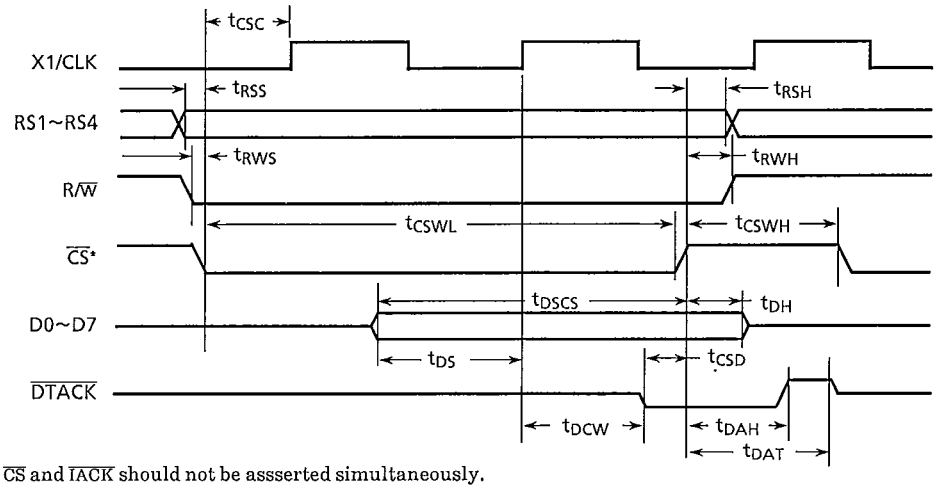
Note 1 : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: C_L=150 picofarads, R_L=750 ohms to V_{CC}. Test conditions for interrupt outputs: C_L=50 picofarads, R_L=27 kilohms to V_{CC}.

2 : This specification is made only to insure $\overline{DTACK}$ is asserted with respect to the rising edge of X1/CLK as shown in Figure 5.2, not to guarantee operation of the part. If the setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

3 : The t_{CSD} specification is made only to insure that $\overline{DTACK}$ will be asserted. If $\overline{CS}$ is negated before $\overline{DTACK}$ is asserted, $\overline{DTACK}$ may not be asserted.

4 : During write cycles, data is latched on either the asserting edge of $\overline{DTACK}$ or the negating edge of CS, whichever occurs first. If CS is negated within one clock cycle after $\overline{CS}$ has been recognized (i.e., first rising edge of X1/CLK where $\overline{CS}$ is asserted), then $\overline{DTACK}$ may not be generated. In this case, data will be latched on the negating edge of $\overline{CS}$. Thus, t_{DS} can be ignored but t_{DSCS} must be observed.

5 : Consecutive write operations to the same command register (CRA or CRB) require at least three transitions of X1/CLK between write cycles. Typically, a processor is incapable of accessing the same command register a second time prior to three transitions on the X1/CLK pin.



* $\overline{CS}$ and $\overline{IACK}$ should not be assserted simultaneously.

Figure 5.3 Write Cycle Bus Timing

5.7 AC ELECTRICAL CHARACTERISTICS – INTERRUPT CYCLE BUS TIMING*

(See Figure 5.4 and Note 1)

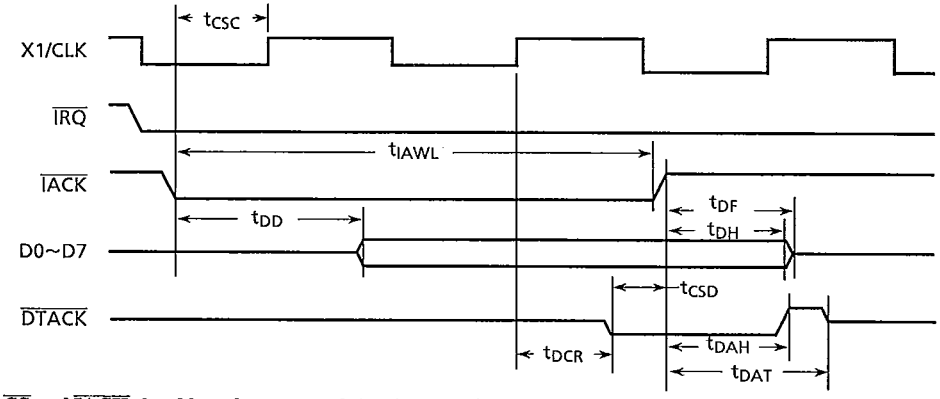
Characteristic	Symbol	Min	Max	Unit
$\overline{IACK}$ Setup Time to X1/CLK High (See Note 2)	t_{CSC}	90	–	ns
$\overline{IACK}$ Pulse Width Asserted (See Note 3)	t_{IAWL}	205	–	ns
Data Valid from $\overline{IACK}$ Asserted	t_{DD}	–	175	ns
$\overline{DTACK}$ Asserted form X1/CLK High	t_{DCR}	–	125	ns
$\overline{IACK}$ Negated from $\overline{DTACK}$ Asserted (See Note 3)	t_{CSD}	0	–	ns
Data Hold Time from $\overline{IACK}$ Negated	t_{DH}	0	–	ns
Data Bus Floating from $\overline{IACK}$ Negated	t_{DF}	–	100	ns
$\overline{DTACK}$ Negated from $\overline{IACK}$ Negated	t_{DAH}	–	100	ns
$\overline{DTACK}$ Hi-Z from $\overline{IACK}$ Negated	t_{DAT}	–	125	ns

* During $\overline{IACK}$ cycles, the status of the R/W line is ignored.

Note 1 : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: $C_L=150$ picofarads, $R_L=750$ ohms to V_{CC}. Test conditions for interrupt outputs: $C_L=50$ picofarads, $R_L=27$ kilohms to V_{CC}.

2 : This specification is made only to insure $\overline{DTACK}$ is asserted with respect to the rising edge of X1/CLK as shown in Figure 5.2, not to guarantee operation of the part. If the setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

3 : The t_{CSD} specification is made only to insure that $\overline{DTACK}$ will be asserted. If $\overline{CS}$ is negated before $\overline{DTACK}$ is asserted, $\overline{DTACK}$ may not be asserted.



* $\overline{CS}$ and $\overline{IACK}$ should not be assserted simultaneously.

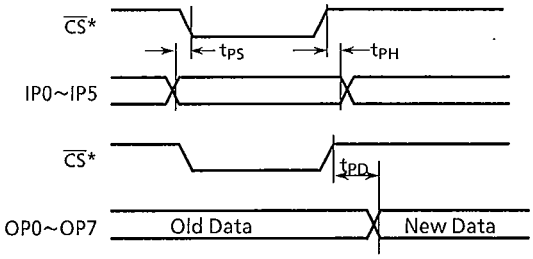
Figure 5.4 Interrupt Cycle Bus Timing

5.8 AC ELECTRICAL CHARACTERISTICS – PORT TIMING

(See Figure 5.5 and Note 1)

Characteristic	Symbol	Min	Max	Unit
Port Input Setup Time to $\overline{CS}$ Asserted	t_{PS}	0	–	ns
Port Input Hold Time from $\overline{CS}$ Negated	t_{PH}	0	–	ns
Port Output Valid from $\overline{CS}$ Negated	t_{PD}	–	400	ns

Note : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 folts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: $C_L = 150$ picofarads, $R_L = 750$ ohms to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ picofarads, $R_L = 27$ kilohms to V_{CC}.



* $\overline{CS}$ and $\overline{IACK}$ should not be assserted simultaneously.

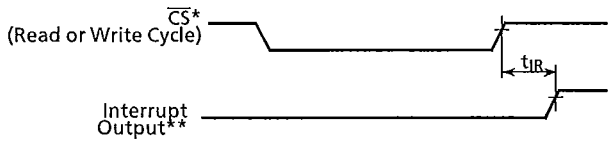
Figure 5.5 Port Timing

5.9 AC ELECTRICAL CHARACTERISTICS – INTERRUPT RESET TIMING

(See Figure 5.6 and Note 1)

Characteristic	Symbol	Min	Max	Unit
$\overline{IRQ}$ Negated or OP3~OP7 High from $\overline{CS}$ Negated When Used as Interrupts From:	t_{IR}			
Read RB (RxRDY/FFULL Interrupt)		–	300	ns
Write TB (TxRDY Interrupt)		–	300	ns
Reset Command (Delta Break Interrupt)		–	300	ns
Stop C/T Command (Counter Interrupt)		–	300	ns
Read IPCR (Input Port Change Interrupt)		–	300	ns
Write IMR (Clear-of-Interrupt Mask Bit)		–	300	ns

Note : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transiiton time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: $C_L = 150$ picofarads, $R_L = 750$ ohms to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ picofarads, $R_L = 27$ kilohms to V_{CC}.



* $\overline{CS}$ and $\overline{IACK}$ should not be asserted simultaneously.
** $\overline{IRQ}$ or OP3~OP7 when used as interrupt outputs.

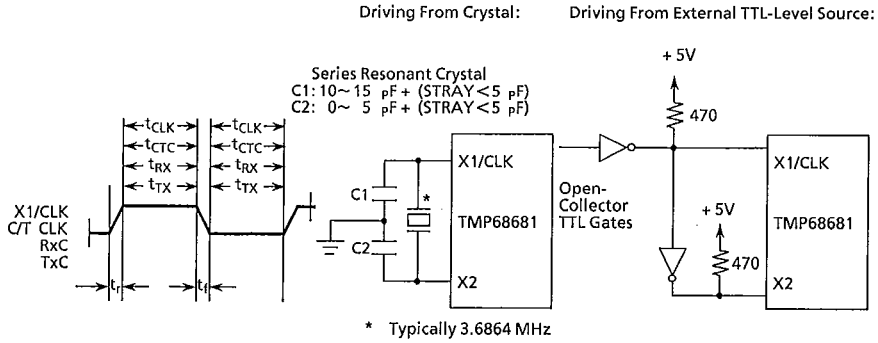
Figure 5.6 Interrupt Reset Timing

5.10 AC ELECTRICAL CHARACTERISTICS – CLOCK TIMING

(See Figure 5.7 and Note 1)

Characteristic	Symbol	Min	Max	Unit
X1/CLK High or Low Time	t_{CLK}	100	–	ns
Counter/Timer Clock High or Low Time	t_{CTC}	100	–	ns
Receive Clock (RxC) High or Low Time	t_{Rx}	220	–	ns
Transmit Clock (TxC) High or Low Time	t_{Tx}	220	–	ns
Clock Rise Time	t_r	–	20	ns
Clock Fall Time	t_f	–	20	ns

Note : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: C_L=150 picofarads, R_L 750 ohms TO V_{CC}. Test conditions for interrupt outputs: C_L=50 picofarads, R_L=27 kilohms to V_{CC}.



Note : Board layout should be such that the crystal and capacitor(s) are as close as possible to the pins of the DUART to minimize stray capacitance. Also, crystal series resistance should be less than 180 ohms.

Figure 5.7 Clock Timing

5.11 AC ELECTRICAL CHARACTERISTICS – TRANSMITTER TIMING

(See Figure 5.8 and Note 1)

Characteristic	Symbol	Min	Max	Unit
TxC Output Valid from TxC Low	t_{TxD}	–	350	ns
TxC Low to TxD Output Valid	t_{TCS}	–	150	ns

Note : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltalges of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: $C_L = 150$ picofarads, $R_L = 750$ ohms to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ picofarads, $R_L = 27$ kilohms to V_{CC}.

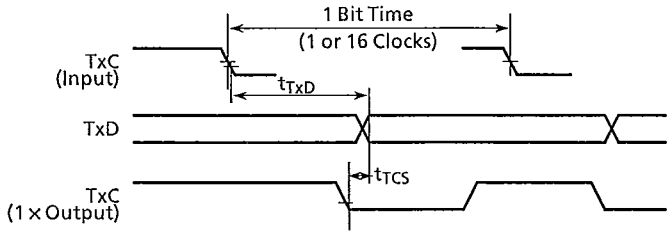


Figure 5.8 Transmit Timing

5.12 AC ELECTRICAL CHARACTERISTICS – RECEIVER TIMING

(See Figure 5.9 and Note 1)

Characteristic	Symbol	Min	Max	Unit
RxC Data Setup Time to RxC High	t_{RxS}	240	–	ns
RxC Data Hold Time from RxC High	t_{RxH}	200	–	ns

Note : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltalges of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: $C_L = 150$ picofarads, $R_L = 750$ ohms to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ picofarads, $R_L = 27$ kilohms to V_{CC}.

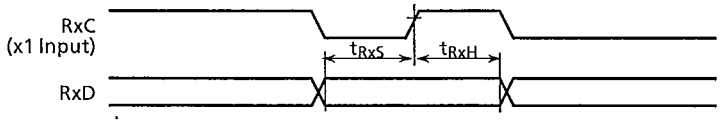
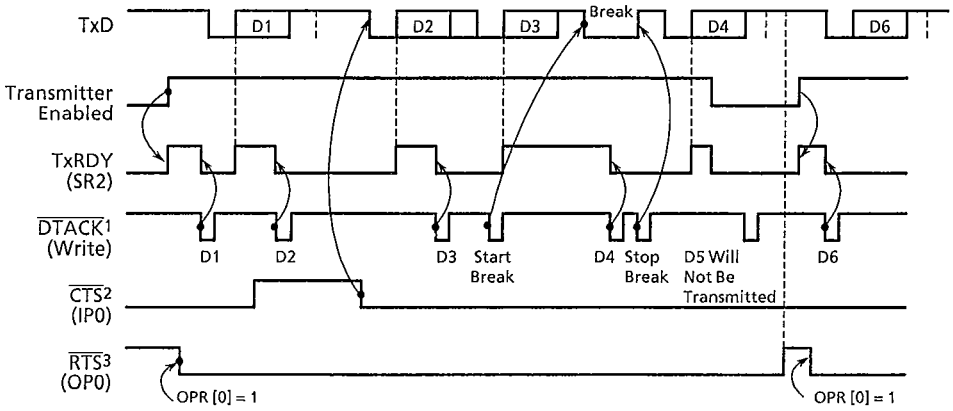


Figure 5.9 Receive Timing

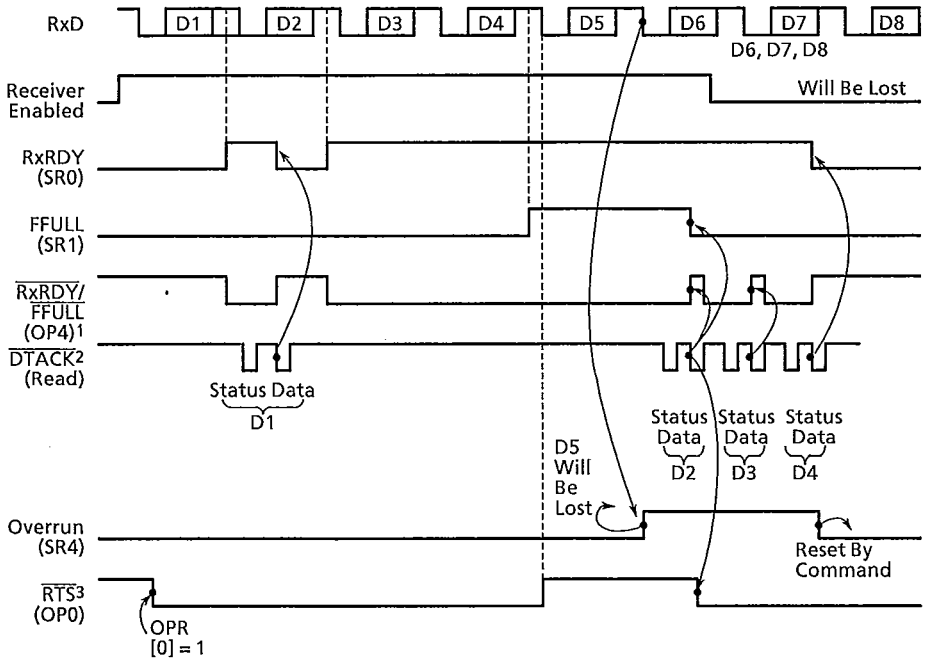


Note 1 : If $\overline{CS}$ is negated within one clock cycle after $\overline{CS}$ is recognized, $\overline{DTACK}$ will not be asserted. In this case the negation of $\overline{CS}$ will cause the transitions.

2 : Timing shown for MR2 (4) = 1.

3 : Timing shown for MR2 (5) = 1.

Figure 5.10 Transmitter Timing

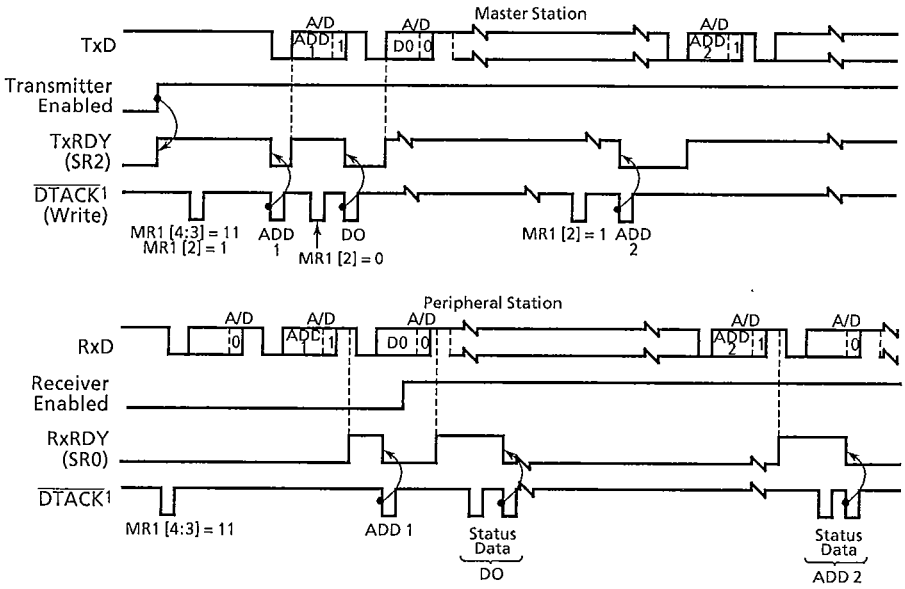


Note 1 : Shown for OPCR (4) = 1 and MR1(6) = 0.

2 : If CS is negated within one clock cycle after $\overline{CS}$ is recognized, $\overline{DTACK}$ will not be asserted. In this case the negation of $\overline{CS}$ will cause the transitions.

3 : Timing shown for MR1 (7) = 1.

Figure 5.11 Receiver Timing



Note: If $\overline{CS}$ is negated within one clock cycle after $\overline{CS}$ is recognized, $\overline{DTACK}$ will not be asserted. In this case the negation of $\overline{CS}$ will cause the transitions.

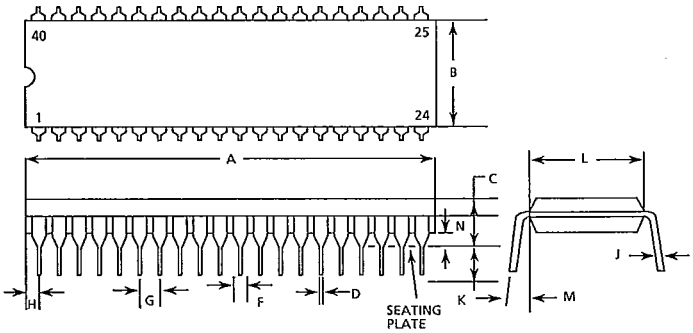
Figure 5.12 Wake-Up Mode Timing

6. MECHANICAL DATA

This section contains package dimensions for the TMP68681/2681.

6.1 PACKAGE DIMENSIONS

PLASTIC PACKAGE



Unit : mm

Dim	MILLMETERS	
	Min	Max
A	51.69	52.45
B	13.72	14.22
C	3.94	5.08
D	0.36	0.56
F	1.02	1.52
G	2.54 BSC	
H	1.65	2.16
J	0.20	0.38
K	2.92	3.43
L	15.24 BSC	
M	0°	15°
N	0.51	1.02

APPENDIX
TMP2681

The TMP2681 dual asynchronous receiver/transmitters (DUARTs) are functionally equivalent to the TMP68681 with some minor differences. The description of the TMP68681 applies to the TMP2681 except for the areas described below.

A.1 INTRODUCTION

Unlike the TMP68681 which has an TLCS-68000 bus interface, the TMP2681 have a general purpose interface which may be used with both synchronous and asynchronous microprocessors. This devices have a multipurpose 7-bit input port and a multipurpose 8-bit output port. These ports can be used as general purpose I/O ports or can be assigned specific functions (such as inputs or status/interrupt outputs) under program control. A block diagram for the TMP2681 is given in Figure A.1.

The TMP2681 differ in that the TMP2681 is available in a 40-pin dual-in-line package is available in a 28-pin dual-in-line package. This option is given to satisfy system requirements.

A.1.1 INTERNAL CONTROL LOGIC

The internal control logic receives operation commands from the central processing unit (CPU) and generates appropriate signals to the internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

A.1.2 INTERRUPT CONTROL LOGIC

A single active-low interrupt output ($\overline{IRQ}$) is provided which is activated upon the occurrence of any of eight internal events. Associated with th einterrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR may be programmed to select only certain conditions to cause $\overline{IRQ}$ to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

In addition, the DUARTs offer the ability to program the parallel outputs OP3 through OP7 to provide discrete interrupt outputs for the transmitters, the receivers, and the counter/timer.

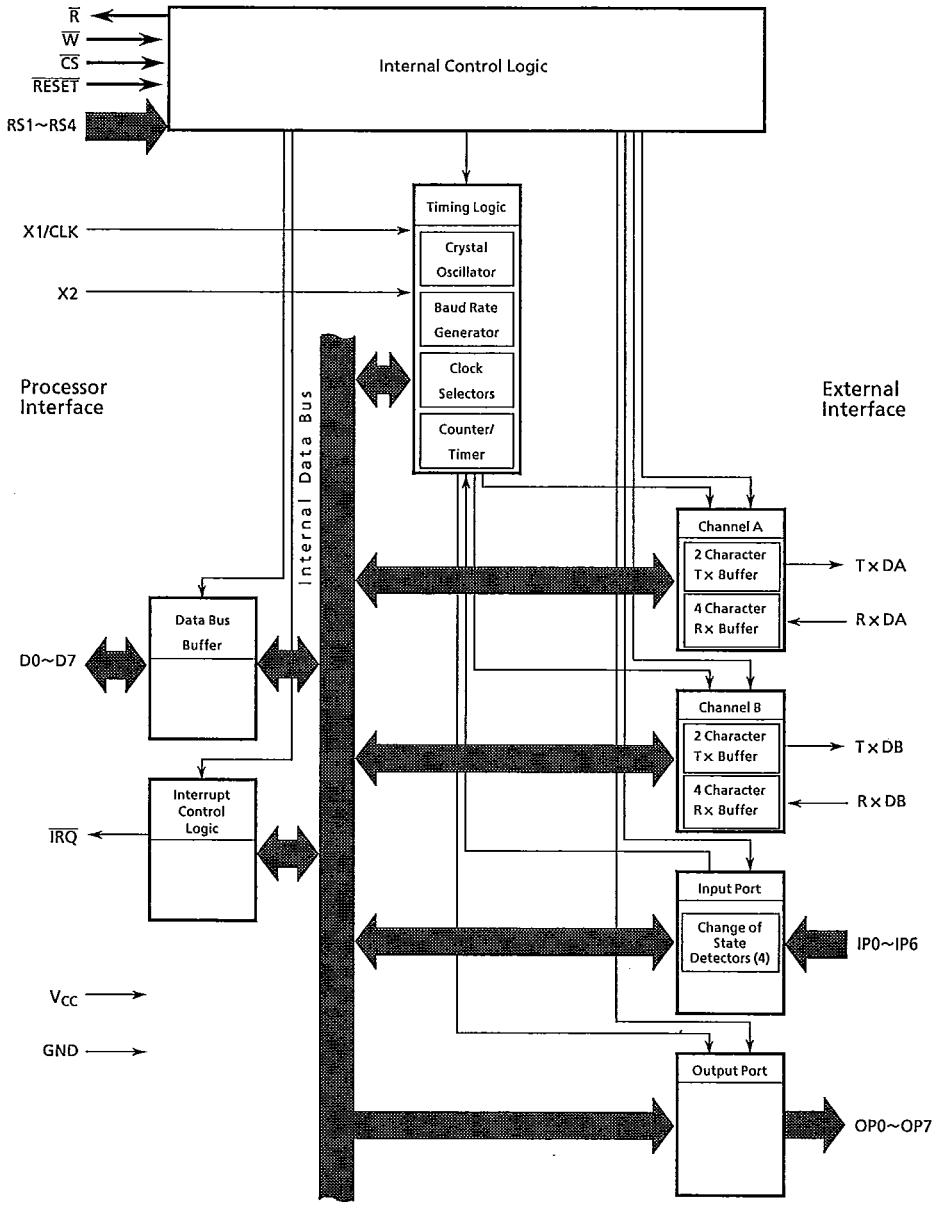


Figure A.1 TMP2681 Block Diagram

A.1.3 INPUT PORT

The inputs to the unlatched 7-bit port (IPO ~ IP6) can be read by the CPU by performing a read operation. A high input results in a logic one while a low input results in a logic zero. D7 will always be read as a logic one. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors, also provided within the input port, are associated with inputs IP0, IP1, IP2, and IP3. A high-to-low or low-to-high transition of these inputs lasting longer than 25 to 50 microseconds (best-to-worst case times) will set the corresponding bit in the input port change register (IPCR). The bits are cleared when the register is read by the CPU. Also, the DUART can be programmed so any particular change of state can generate an interrupt to the CPU.

A.2 SIGNAL DESCRIPTION

Table A.1, like that for the TMP68681 found in Section 2, Signal Description, provides a quick reference in determining a signal's pin number, its use as an input or output, whether it is active high or low, and the section in which more information can be found about its operation. Note that the signal description given for the TMP68681 applies to the TMP2681 except for the areas described in this appendix.

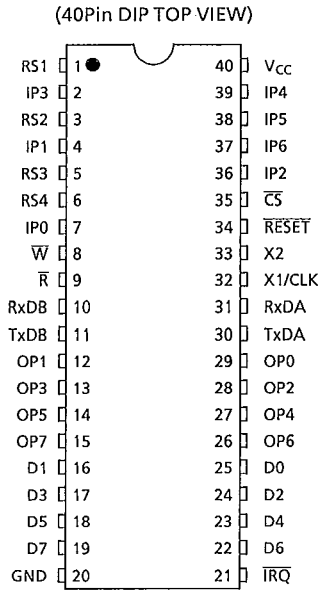


Figure A.2 TMP2681 Pin Assignments

A.2.1 RESET (RESET)

When active high, this input clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0~OP7 in the high state, stops the counter/timer, and puts channel A and B in the inactive state with the TxDA and TxDB outputs in the mark (high) state.

A.2.2 CHIP SELECT ($\overline{CS}$)

This active low signal, when low, enables data transfers between the CPU and DUART on the date lines (D0 ~ D7). These data transfers are controlled by write ($\overline{W}$), read ($\overline{R}$), and the register-select inputs (RS1 ~ RS4). When chip enable is high, the D0 through D7 data line are placed in the high-impedance state.

A.2.3 WRITE STROBE ($\overline{W}$)

When this signal and chip enable are low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the rising edge of the signal.

A.2.4 READ STROBE ($\overline{R}$)

When this signal and chip enable are low, the contents of the addressed register are pressented on the data bus. The read cycle begins on the falling edge of the signal.

A.2.5 PARALLEL INPUT 6 (IP6)

This signal can be used as a general purpose input or a channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.

Table A.1 TMP2681 Signal Summary (1/2)

Signal Name	Mnemonic	Pin No.	Input/Output	Active State	Refer to Para. No.
Power Supply (+5V)	V_{CC}	40	Input	High	2.1
Ground	GND	20	Input	Low	2.1
Crystal Input or External Clock	X1/CLK	32	Input	–	2.2
Crystal Input	X2	33	Input	–	2.3
Reset	$\overline{RESET}$	34	Input	Low	A. 2.1
Chip Select	$\overline{CS}$	35	Input	Low	A. 2.2
Write Strobe	$\overline{W}$	8	Input	Low	A. 2.3
Read Strobe	$\overline{R}$	9	Input	Low	A. 2.4
Register Select Bus Bit 4	RS4	6	Input	High	2.8
Register Select Bus Bit 3	RS3	5	Input	High	2.8
Register Select Bus Bit 2	RS2	3	Input	High	2.8
Register Select Bus Bit 1	RS1	1	Input	High	2.8

Table A.1 TMP2681 Signal Summary (2/2)

Signal Name	Mnemonic	Pin No.	Input/Output	Active State	Refer to Para. No.
Bidirectional-Data Bus Bit 7	D7	19	Input/Output	High	2.9
Bidirectional-Data Bus Bit 6	D6	22	Input/Output	High	2.9
Bidirectional-Data Bus Bit 5	D5	18	Input/Output	High	2.9
Bidirectional-Data Bus Bit 4	D4	23	Input/Output	High	2.9
Bidirectional-Data Bus Bit 3	D3	17	Input/Output	High	2.9
Bidirectional-Data Bus Bit 2	D2	24	Input/Output	High	2.9
Bidirectional-Data Bus Bit 1	D1	16	Input/Output	High	2.9
Bidirectional-Data Bus Bit 0	D0	25	Input/Output	High	2.9
Interrupt Request	$\overline{IRQ}$	21	Output*	Low	2.10
Channel A Transmitter Serial Data	TxDA	30	Output	–	2.12
Channel A Receiver Serial Data	RxDA	31	Input	–	2.13
Channel B Transmitter Serial Data	TxDB	11	Output	–	2.14
Channel B Receiver Serial Data	RxDB	10	Input	–	2.15
Parallel Input 6 (TMP2681 Only)	IP6	37	Input	–	A. 2.5
Parallel Input 5 (TMP2681 Only)	IP5	38	Input	–	2.16.1
Parallel Input 4 (TMP2681 Only)	IP4	39	Input	–	2.16.2
Parallel Input 3 (TMP2681 Only)	IP3	2	Input	–	2.16.3
Parallel Input 2 (TMP2681 Only)	IP2	36	Input	–	A. 2.6
Parallel Input 1 (TMP2681 Only)	IP1	4	Input	–	2.16.5
Parallel Input 0 (TMP2681 Only)	IP0	7	Input	–	2.16.6
Parallel Output 7 (TMP2681 Only)	OP7	15	Output**	–	2.17.1
Parallel Output 6 (TMP2681 Only)	OP6	26	Output**	–	2.17.2
Parallel Output 5 (TMP2681 Only)	OP5	14	Output**	–	2.17.3
Parallel Output 4 (TMP2681 Only)	OP4	27	Output**	–	2.17.4
Parallel Output 3 (TMP2681 Only)	OP3	13	Output**	–	2.17.5
Parallel Output 2 (TMP2681 Only)	OP2	28	Output	–	2.17.6
Parallel Output 1	OP1	12	Output	–	2.17.7
Parallel Output 0	OP0	29	Output	–	2.17.8

* Requires a pullup resistor.

** May require a pullup resistor depending upon its programmed function.

A.2.6 PARALLEL INPUT 2 (IP2)

This signal can be used as a general purpose input or a counter/timer external clock input.

A.3 PROGRAMMING AND REGISTER DESCRIPTION

Table A.2 describes the register addresses and address-triggered commands for the TMP2681. The detailed description of each register and its function, given for the TMP68681 in Section 4 Programming and Register Description, applies to the TMP2681.

Table A.2 TMP2681 Register Addressing and Address - Triggered Commands

RS4	RS3	RS2	RS1	Read ($\overline{R}=0$)	Write ($\overline{W}=0$)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Stauts Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Do Not Access *	Command Register A (CRA)
0	0	1	1	Receiver Buffer A (RBA)	Transmit Buffer A (TBA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter Mode: Current MSB of Counter (CUR)	Counter/Timer Upper Register (CTUR)
0	1	1	1	Counter Mode: Current LSB of CounterB (CLR)	Counter/Timer Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Do Not Access*	Command Register B (CRB)
1	0	1	1	Receiver Buffer B (RBB)	Transmit Buffer B (TBB)
1	1	0	0	Do Not Access	Do Not Access*
1	1	0	1	Input Port (Unlatched)	Output Port Register (OPCR)
1	1	1	0	Start Counter Command**	Output Port Register (OPR): Bit Set Command**
1	1	1	1	Stop Counter Command**	Output Port Register (OPR): Bit Reset Command**

* This address location is used for factory testing of the DUARTs and should not be read. Reading this location will result in undesired effects and possible incorrect transmission or reception of characters. Reigster contents may also be changed.

** Address Triggered commands.

A.4 ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the TMP2681.

A.4.1 ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 ~ + 6.0	V
Input Voltage	V_{in}	−0.5 ~ + 6.0	V
Operating Temperature Range	T_a	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

A.4.2 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, T_a = 0°C~70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, Except X1/CLK*	V_{IH}	2.0	–	–	V
Input High Voltage, X1/CLK	V_{IH}	4.0	–	–	V
Input Low Voltage	V_{IL}	–	–	0.8	V
Output High Voltage, Except Open-Collector Outputs (I_{OH} = −400 μA)	V_{OH}	2.4	–	–	V
Output Low Voltage (I_{OL} = 2.4mA)	V_{OL}	–	–	0.4	V
Input Leakage Current (V_{in} = 0 to V_{CC})	I_{IL}	−10	–	10	μA
Data Bus Hi-Z Leakage Current (V_{OUT} = 0 to V_{CC})	I_{LL}	−10	–	10	μA
Open-Collector Output Leakage Current (V_{OUT} = 0 to V_{CC})	I_{OC}	−10	–	10	μA
Power Supply Current	I_{CC}	–	–	150	mA
Capacitance (V_{in} = 5V, Ta = 25°C, f = 1MHz)	C_{in}	–	–	15	pF
X1/CLK Low Input Currnet Vin = 0, X2 Grounded Vin = 0, X2 Floated	I_{X1L}	 −4.0 −3.0	 −2.0 −1.5	 0 0	mA
X1/CLK High Input Current Vin = Vcc, X2 Grounded Vin = Vcc, X2 Floated	I_{X1H}	 −1.0 0	 0.2 3.5	 1.0 10.0	mA
X2 Low Input Current Vin = 0, X1/CLK Floated	I_{X2L}	−100	−30	0	μA
X2 High Input Current Vin = Vcc, X1/CLK Floated	I_{X2H}	0	+30	100	μA

A.4.3 AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V±5%, GND=0V, T_a=0°C~70°C, See Note 1)

Characteristic	Symbol	Min	Max	Unit
X1/CLK Frequency*	f_{CLK}	2.0	4.0	MHz
Counter/Timer Clock Frequency	f_{CTC}	0	4.0	MHz
Receiver Clock Frequency (RxC) 16X Clock 1X Clock	f_{RX}	 0 0	 2.0 1.0	MHz
Transmitter Clock Frequency (TxC) 16X Clock 1X Clock	f_{TX}	0	 2.0 1.0	MHz

* To use the standard baud rates selected by the clock-select register given in Table 4-5, the X1/CLK frequency should be set at 3.6864 MHz.

A.4.4 AC ELECTRICAL CHARACTERISTICS – RESET TIMING (See Figure A.2)

Characteristic	Symbol	Min	Max	Unit
RESET Pulse Width	t_{RES}	1.0	–	μs

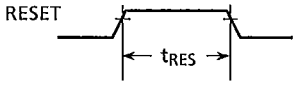


Figure A.2 RESET Timing

A.4.5 AC ELECTRICAL CHARACTERISTICS – BUT TIMING (See Figure A.3)

Characteristic	Symbol	Min	Max	Unit
RS1~RS4 Setup Time to $\overline{R}$, $\overline{W}$ Asserted	t_{RSS}	10	–	ns
RS1~RS4 Hold Time from $\overline{R}$, $\overline{W}$ Negated	t_{RSH}	0	–	ns
$\overline{CS}$ Setup Time to $\overline{R}$, $\overline{W}$ Asserted	t_{CS}	0	–	ns
$\overline{CS}$ Hold Time from $\overline{R}$, $\overline{W}$ Negated	t_{CH}	0	–	ns
$\overline{R}$, $\overline{W}$ Pulse Width Asserted	t_{RW}	205	–	ns
Data Valid after $\overline{R}$ Asserted	t_{DD}	–	175	ns
Data Bus Floating after $\overline{R}$ Negated	t_{DF}	–	100	ns
Data Setup Time before $\overline{W}$ Negated	t_{DS}	100	–	ns
Data Hold Time after $\overline{R}$ or $\overline{W}$ Negated	t_{DH}	10	–	ns
High Time Between Reads and/or Writes*	t_{RWD}	200	–	ns

* If $\overline{CS}$ is used as the "strobing" input, this parameter defines theminimum high time between one $\overline{CS}$ and the next. $\overline{CS}$ and R ($\overline{W}$) are ANDed internally. Subsequently, the signal asserted last initiates the cycle and the signal negated first terminates the cycle. $\overline{R}$ must be negated for t_{RWD} to guarantee that any status register changes are valid. Consecutive write operations to the same command register require at last three edges of the X1 clock between writes. Typically, a processor is incapable of accessing the same command register a second time prior to three transitions on the X1/CLK pin.

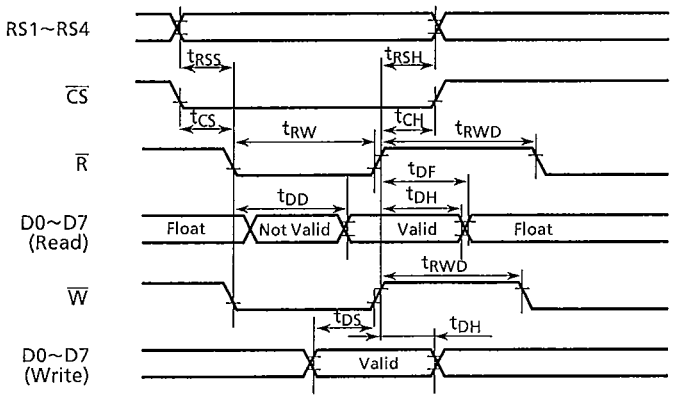


Figure A.3 Bus Timing

A.4.6 AC ELECTRICAL CHARACTERISTICS – PORT TIMING (See Figure A.4)

Charactereistic	Symbol	Min	Max	Unit
Port Input Setup Time to $\overline{R}$ Asserted	t_{PS}	0	–	ns
Port Input Hold Time from $\overline{R}$ Negated	t_{PH}	0	–	ns
Port Output Valid from $\overline{W}$ Negated	t_{PD}	0	400	ns

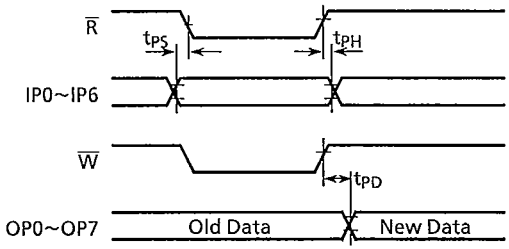


Figure A.4 Port Timing

A.4.7 AC ELECTRICAL CHARACTERISTICS – INTERRUPT TIMING (See Figure A.5)

Characteristic	Symbol	Min	Max	Unit
$\overline{IRQ}$ Negated or OP3~OP7 High for $\overline{R}$ or $\overline{W}$ Negated When Used as Interrupts From:	t_{IR}			
Read RHR (RxRDY/FFULL Interrupt)		–	300	ns
Write THR (TxRDY Interrupt)		–	300	ns
Reset Command (Delta Break Interrupt)		–	300	ns
Stop C/T Command (Counter Interrupt)		–	300	ns
Read IPCR (Inpur Port Change Interrupt)		–	300	ns
Write IMR (Clear-of-Interrupt Mask Bit)		–	300	ns

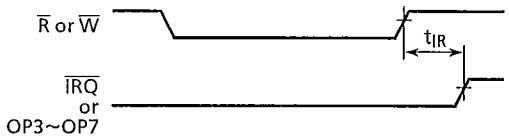
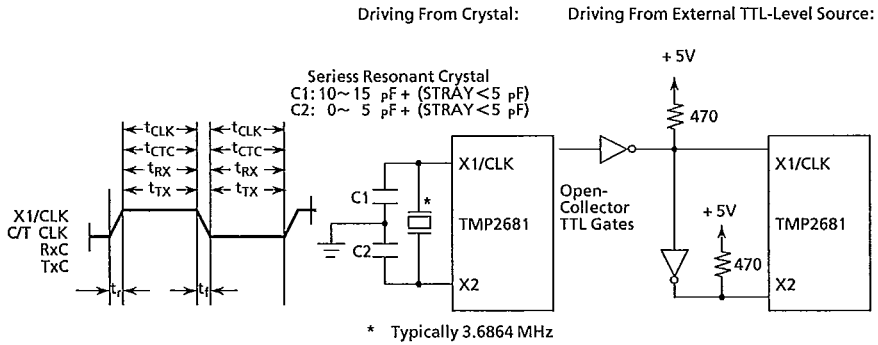


Figure A.5 Interrupt Timing

A.4.8 AC ELECTRICAL CHARACTERISTICS – CLOCK TIMING (See Figure A.6 and Note 1)

Characteristic	Symbol	Min	Max	Unit
X1/CLK High or Low Time	t_{CLK}	100	–	ns
Counter/Timer Clock High or Low Time	t_{CTC}	100	–	ns
Receive Clock (RxC) High or Low Time	t_{Rx}	220	–	ns
Transmit Clock (TxC) High or Low Time	t_{Tx}	220	–	ns
Clock Rise Time	t_r	–	20	ns
Clock Fall Time	t_f	–	20	ns

Note : All voltage measurements are referenced to ground (GND). For testing, all input signals exept X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transtion time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test condition for non-interrupt outputs: $C_L = 150$ picofarads, $R_L = 750$ ohms to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ picofarads, $R_L = 27$ kilohms to V_{CC}.



Note : Board layout should be such that the crystal and capacitor(s) are as close as possible to the pins of the DUART to minimize stray capacitance Also, crystal series resistance should be less than 180 ohms.

Figure A.6 Clock Timing

A.4.9 AC ELECTRICAL CHARACTERISTICS – TRANSMITTER TIMING

(See Figure A.7 and Note1)

Characteristic	Symbol	Min	Max	Unit
TxC Output Valid from TxC Low	t_{TxD}	–	350	ns
TxC Low to TxD Output Valid	t_{TCS}	–	150	ns

Note : All voltage measurements are referenced to ground (GND). For testing, all input signals except X1/CLK swing between 0.4 volt and 2.4 volts with a maximum transition time of 20 nanoseconds. For X1/CLK, this swing is between 0.4 volt and 4.4 volts. All time measurements are referenced at input and output voltages of 0.8 volt and 2.0 volts as appropriate. Test conditions for non-interrupt outputs: C_L=150 picofarads, R_L=750 ohms to V_{CC}. Test conditions for interrupt outputs: C_L=50 picofarads, R_L=27kilohms to V_{CC}.

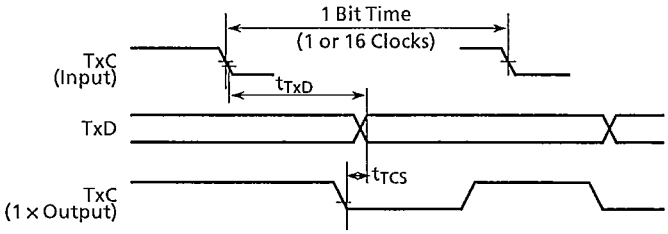


Figure A.7 Transmit Timing

A.4.10 AC ELECTRICAL CHARACTERISTICS – RECEIVER TIMING

(See Figure A.8)

Characteristic	Symbol	Min	Max	Unit
RxC Data Setup Time to RxC High	t_{RxS}	240	–	ns
RxC Data Hold Time from RxC High	t_{RxH}	200	–	ns

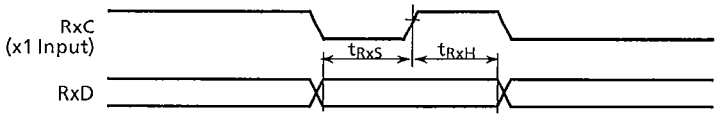


Figure A.8 Receive Timing

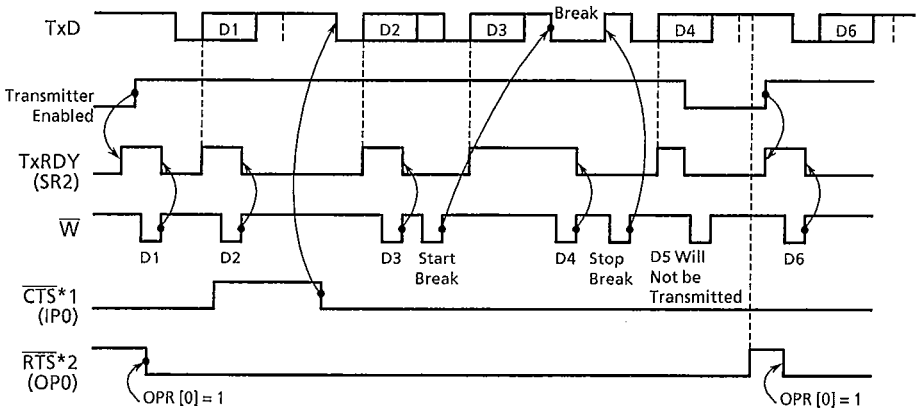


Figure A.9 Transmitter Timing

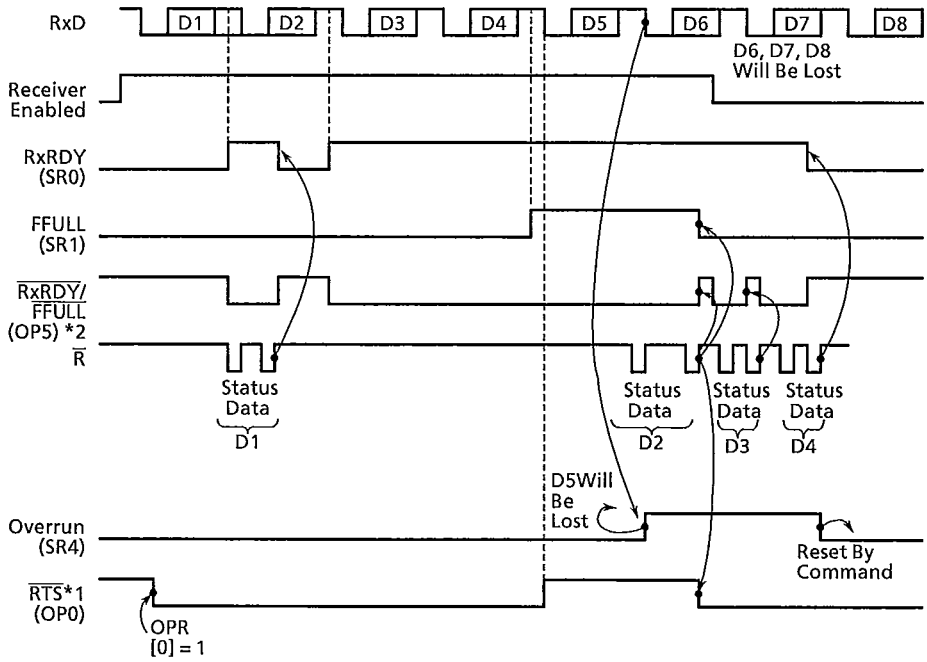


Figure A.10 Receiver Timing

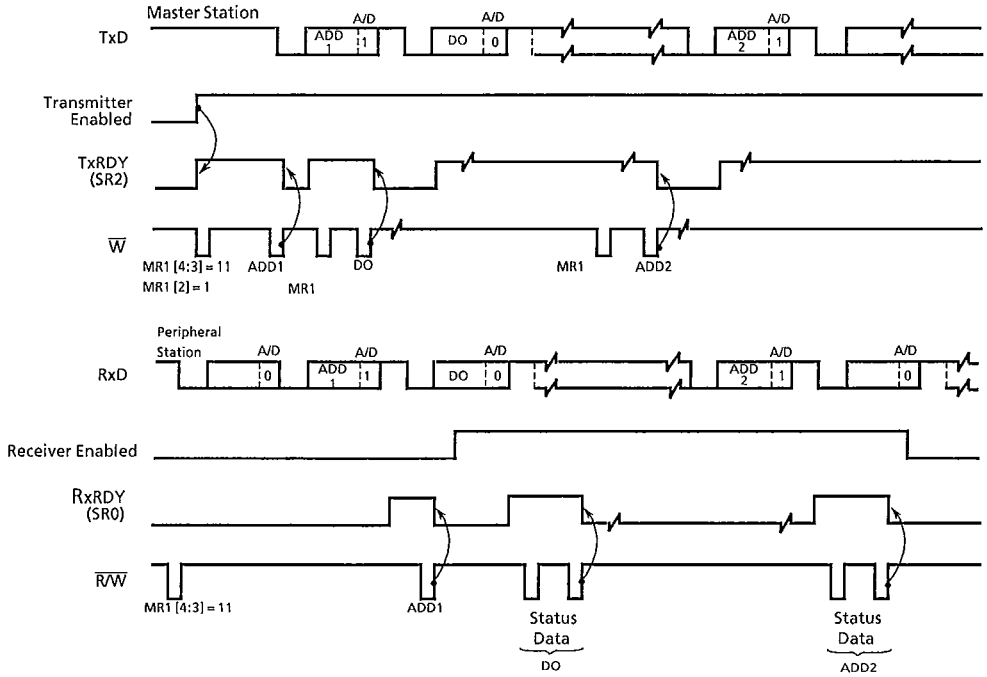


Figure A.11 Wake-Up Mode Timing