Description of a library gate

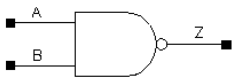
Let's consider a *NAND2* gate. A whole description of it includes many kind of views, to be used by designers or tools or both in different designing steps:

Documentation A documentation of the gate performance should be given to the designer as in figure 5.1:

ND2LL
ND2LLP
ND2LLX4
ND2LLX6
ND2LLX8

Function: Function = 2 Input NAND

Boolean Expression: Z = !(A•B)



Physical Dimensions

Property	ND2LL	ND2LLP	ND2LLX4	ND2LLX6	ND2LLX8
Area(um2)	6.052	8.069	12.103	16.138	20.172
Width(um)	1.23	1.64	2.46	3.28	4.1
Height(um)	4.920	4.920	4.920	4.920	4.920

Capacitance

picoFarads

Property	ND2LL	ND2LLP	ND2LLX4	ND2LLX6	ND2LLX8
Z Max Load	0.160	0.320	0.640	0.960	1.280
A Input	0.0027	0.0051	0.0106	0.0153	0.0208
B Input	0.0026	0.0048	0.0093	0.0142	0.0188

Propagation Delay

nanoSeconds, as a function of C (load in pF) and Tr (input transition time in nS)

Cell	Path	Event	Best P 1.32 V -40 C	Worst P 1.08 V 125 C	Nominal P 1.2 V 25 C
ND2LL	A-Z	A_F_Z_R	0.013 + 2.22C + 0.372Tr	0.029 + 4.68C + 0.388Tr	0.019 + 3.19C + 0.388Tr
		A_R_Z_F	0.010 + 1.67C + 0.272Tr	0.027 + 4.28C + 0.303Tr	0.015 + 2.52C + 0.294Tr
	B-Z	B_F_Z_R	0.010 + 2.22C + 0.371Tr	0.022 + 4.68C + 0.388Tr	0.015 + 3.19C + 0.387Tr
		B_R_Z_F	0.008 + 1.67C + 0.330Tr	0.021 + 4.28C + 0.355Tr	0.012 + 2.52C + 0.349Tr

Leakage Power

picoWatts at Best P 1.32 V 25 C

Cell	minimum	median	maximum
ND2LL	464.37	549.98	754.37

Figure 5.1: Performance description for a nand2 gate.

Symbol the logic symbol representing input/output pins and logic function, as in figure 5.2

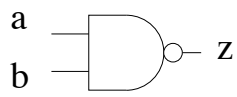


Figure 5.2: Symbol view of the cell

Schematic the schematic realized by a network of transistor symbols (NMOS or PMOS) as in figure 5.3

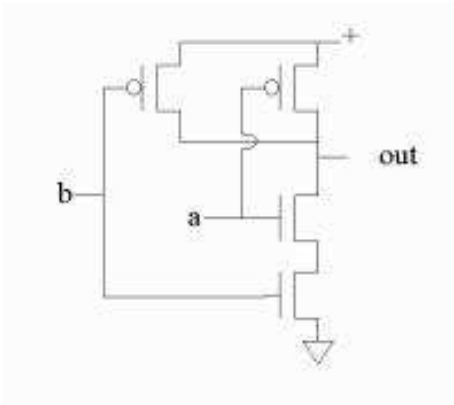


Figure 5.3: Schematic view of the cell

Layout the view describing the masks necessary for fabrication, as in figure 5.4. This view is used mainly for use in tools which need to display the layout to a designer.

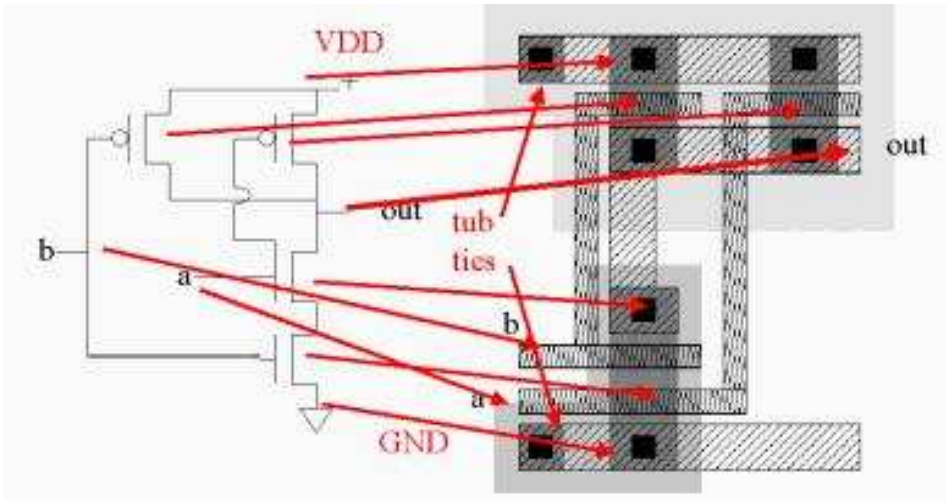


Figure 5.4: Layout view of the cell (in this contest relations between the schematic and the layout masks are given.)

LEF Library Exchange Format, this is the real layout description used by physical design tools, in which masks are described as polygons and coordinates are given for defining their positions and shapes; the types of mask is underlined by predefined keywords. An example of a NAND2 gate LEF view is below:

```
MACRO ND2HS
    CLASS CORE ;
    FOREIGN ND2HS 0.000 0.000  ;
    ORIGIN 0.000 0.000 ;
    SIZE 1.230 BY 4.920 ;
    SYMMETRY x y ;
    SITE CORE ;
    PIN Z
        DIRECTION OUTPUT ;
        PORT
        LAYER M1 ;
                POLYGON  1.130 1.540 0.720 1.540 0.720 4.040 0.510 4.040 0.510 1.540 0.470 1.540
                 0.470 1.330 1.130 1.330 ;
        END
    END Z
    PIN B
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT  0.900 2.110 1.130 2.810 ;
        END
    END B
    PIN A
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT  0.100 1.700 0.330 2.400 ;
        END
    END A
    PIN vdd
        DIRECTION INOUT ;
        USE power ;
        SHAPE ABUTMENT ;
        PORT
        LAYER M1 ;
        RECT  0.000 4.220 1.230 5.000 ;
        END
    END vdd
    PIN vdd
        DIRECTION INOUT ;
        USE power ;
        SHAPE ABUTMENT ;
        PORT
        LAYER M1 ;
        RECT  0.000 4.220 1.230 5.000 ;
        END
    END vdd
    PIN gnd
        DIRECTION INOUT ;
        USE ground ;
        SHAPE ABUTMENT ;
        PORT
        LAYER M1 ;
        RECT  0.000 -0.080 1.230 0.700 ;
```

```
        END
    END gnd
END ND2HS
```

Spice A spice view is given based on the extraction of devices and parasitics having the layout as a reference point and performed by extraction tools: they are able to understand the polygon shape and their overlapping, and to extract MOS devices, diodes, resistance and capacitance, on the basis of given rules and technological informations. An example of the spice view is given below (read it carefully as you will use it later on):

```
.subckt ND2HS A B Z gnd vdd
XMN0 net15 A gnd gnd ENHSGP_BS3JU W=0.640U L=0.130U AD=0.061P AS=0.305P PD=0.190U PS=2.870U
XMN1 Z B net15 gnd ENHSGP_BS3JU W=0.640U L=0.130U AD=0.218P AS=0.061P PD=1.320U PS=0.190U
XMP0 Z A vdd vdd EPHSGP_BS3JU W=0.770U L=0.130U AD=0.192P AS=0.471P PD=1.130U PS=4.130U
XMP1 Z B vdd vdd EPHSGP_BS3JU W=0.770U L=0.130U AS=0.471P AD=0.192P PS=4.130U PD=1.130U
C1 vdd gnd 0.142f
C2 gnd gnd 0.897f
C4 Z gnd 0.108f
C5 A gnd 0.129f
C6 B gnd 0.132f
C1-2 vdd gnd 0.132f
C1-4 vdd Z 0.018f
C1-5 vdd A 0.002f
C1-6 vdd B 0.002f
C2-4 gnd Z 0.178f
C2-5 gnd A 0.067f
C2-6 gnd B 0.063f
C4-5 Z A 0.099f
C4-6 Z B 0.132f
C5-6 A B 0.131f
.ends ND2HS
```

Timing-Power Library A timing description is given to be used by Back-end tools as timing analysers. One of the most used kind of description is below.

```
cell(ND2HS) {

   area : 4.3904;
   cell_leakage_power : 6127.1;
   drc_celltype : "combinational";
   drc_ground_pin_drives : "gnd none";
   drc_ground_pin_provides : "";
   drc_ground_pin_requires : "";
   drc_ground_pins : "gnd";
   drc_maxparallel : 1;
   drc_power_pin_drives : "vdd none";
   drc_power_pin_provides : "";
   drc_power_pin_requires : "";
   drc_power_pins : "vdd";
   drc_restriction : "none";
   leakage_power(){
    value : 7135.3;
    when : "A*B";
```

```
}
leakage_power(){
 value : 4263.9;
 when : "!A*B";
}
leakage_power(){
 value : 5973.9;
 when : "A*!B";
}
pin(A){
 capacitance : 0.00228;
 direction : input;
 drc_pindrive : "none";
 drc_pinfunction : "normal";
 drc_pinkind : "internal";
 drc_pinpolarity : "high";
 drc_pinsigtype : "signal";
 max_transition : 0.6649;
}
pin(B){
 capacitance : 0.00216;
 direction : input;
 drc_pindrive : "none";
 drc_pinfunction : "normal";
 drc_pinkind : "internal";
 drc_pinpolarity : "high";
 drc_pinsigtype : "signal";
 max_transition : 0.6649;
}
pin(Z){
 capacitance : 0;
 direction : output;
 drc_pindrive : "always";
 drc_pinfunction : "normal";
 drc_pinkind : "internal";
 drc_pinpolarity : "low";
 drc_pinsigtype : "signal";
 function : "! (A*B)";
 max_capacitance : 0.0828;
 max_transition : 0.6649;
 internal_power(){
  related_pin : "A";
  fall_power(power_table_9){
   values("0.00042, 0.00044",\
        "0.00069, 0.00041",\
        "0.00614, 0.00187",\
        "0.01520, 0.00593");
  }
  rise_power(power_table_9){
   values("0.00456, 0.00490",\
        "0.00532, 0.00512",\
        "0.01104, 0.00720",\
        "0.02019, 0.01207");
  }
```

```
}
internal_power(){
 related_pin : "B";
 fall_power(power_table_9){
  values("0.00040, 0.00044",\
       "0.00092, 0.00044",\
       "0.00685, 0.00220",\
       "0.01632, 0.00668");
 }
 rise_power(power_table_9){
  values("0.00331, 0.00376",\
       "0.00400, 0.00399",\
       "0.00976, 0.00585",\
       "0.01915, 0.01044");
 }
}
timing(){
 drc_charcond : "0_1 B 1_0 B";
 intrinsic_fall : 0.05367;
 intrinsic_rise : 0.1096;
 related_pin : "A";
 timing_label : "A_Z";
 timing_sense : negative_unate;
 cell_fall(table_5){
  values("0.01327, 0.04768, 0.08275, 0.15338",\
       "0.03086, 0.07144, 0.10662, 0.17726",\
       "0.06357, 0.13550, 0.18456, 0.26485",\
       "0.09767, 0.19545, 0.26205, 0.36506");
 }
 cell_rise(table_5){
  values("0.01736, 0.06286, 0.10926, 0.20273",\
       "0.04511, 0.09353, 0.13966, 0.23257",\
       "0.12012, 0.19645, 0.25537, 0.35102",\
       "0.21398, 0.31133, 0.38527, 0.50861");
 }
 fall_transition(table_5){
  values("0.01455, 0.07493, 0.13668, 0.26108",\
       "0.02413, 0.07658, 0.13684, 0.26109",\
       "0.06493, 0.11972, 0.17053, 0.27673",\
       "0.11166, 0.18171, 0.23555, 0.33784");
 }
 rise_transition(table_5){
  values("0.02441, 0.11246, 0.20277, 0.38381",\
       "0.03467, 0.11296, 0.20292, 0.38382",\
       "0.07264, 0.15972, 0.23302, 0.39319",\
       "0.11664, 0.22233, 0.30702, 0.45533");
 }
}
timing(){
 drc_charcond : "0_1 A 1_0 A";
 intrinsic_fall : 0.0569;
 intrinsic_rise : 0.09732;
 related_pin : "B";
 timing_label : "B_Z";
```

```
    timing_sense : negative_unate;
    cell_fall(table_5){
     values("0.01189, 0.04636, 0.08146, 0.15215",\
         "0.03093, 0.07347, 0.10833, 0.17887",\
         "0.06749, 0.14437, 0.19774, 0.28178",\
         "0.10718, 0.20943, 0.28122, 0.39331");
    }
    cell_rise(table_5){
     values("0.01539, 0.06119, 0.10763, 0.20088",\
         "0.04105, 0.09137, 0.13756, 0.23098",\
         "0.10870, 0.19128, 0.25185, 0.34859",\
         "0.19187, 0.30017, 0.37768, 0.50395");
    }
    fall_transition(table_5){
     values("0.01456, 0.07487, 0.13662, 0.26106",\
         "0.02744, 0.07761, 0.13684, 0.26107",\
         "0.07399, 0.13519, 0.18486, 0.28421",\
         "0.12928, 0.20974, 0.26747, 0.36904");
    }
    rise_transition(table_5){
     values("0.02059, 0.10867, 0.19917, 0.38099",\
         "0.03204, 0.10919, 0.19918, 0.38100",\
         "0.07180, 0.15774, 0.23037, 0.39059",\
         "0.11945, 0.22245, 0.30620, 0.45314");
    }
   }
  }
 }
```

Timing values are given in Look-Up-Table format, where the index used are referred to as for example 'table_5', defined previously in the same file containing the LUT description:

```
lu_table_template( table_5 ) {
  variable_1 : input_net_transition ;
  variable_2 : total_output_net_capacitance ;
  index_1 (" 0.0048, 0.1088, 0.2608, 0.5248, 1 ");
  index_2 (" 0.004, 0.012, 0.028, 0.08, 0.16 ");
}
```

Power table, ex. powe_table_9 gives in the values agianst which the power value have been characterized:

```
  power_lut_template(power_table_9){
   index_1(" 0.0029, 0.0689, 0.3155, 0.6649 ");
   index_2(" 0.0027, 0.0828 ");
   variable_1 : input_transition_time;
   variable_2 : total_output_net_capacitance;
  }
```