

5.1.1) There can be 4 32-bit integers in a 16-byte cache line because $16 \times 8 = 128 \rightarrow 128/32 = 4$

5.1.2) Variables I and J and B[I][O] are used consistently so they exhibit temporal locality.

5.1.3) A[J][I] and A[I][J] change with J so it exhibits spatial locality.

5.2.1)

Reference	Binary Word Address	Tag	Index	Hit or Miss
0x03	00000011	0	3	Miss
0xb4	10110100	B	3	Miss
0x2b	00101011	2	B	Miss
0x02	00000010	0	2	Miss
0xbf	10111111	B	F	Miss
0x58	01011000	5	8	Miss
0xbe	10111110	B	E	Miss
0x0e	00001110	0	E	Miss
0xb5	10110101	B	5	Miss
0x2c	00101100	2	C	Miss
0xba	10111010	B	A	Miss
0xfd	11111101	F	D	Miss

5.2.2)

Reference	Binary Word Address	Tag	Index	Offset	Hit or Miss
0x03	00000011	0	1	1	Miss
0xb4	10110100	B	2	0	Miss

0x2b	00101011	2	5	1	Miss
0x02	00000010	0	1	0	Hit
0xbf	10111111	B	7	1	Miss
0x58	01011000	5	8	0	Miss
0xbe	10111110	B	E	0	Hit
0x0e	00001110	0	E	0	Miss
0xb5	10110101	B	5	1	Hit
0x2c	00101100	2	C	0	Miss
0xba	10111010	B	5	0	Miss
0xfd	11111101	F	6	1	Miss

5.3.1) The block size in words is 32 because $2^5 = 32$

5.3.2) Cache has 32 entries because $2^5 = 32$ with 5 blocks

5.3.3) 704 bits because $32 * 22 = 704$

5.6.1) $P1 = 1/0.66 = 1.515 \text{ GHz}$

$$P2 = 1/0.9 = 1.11 \text{ GHz}$$

5.6.2) $P1 = 0.66 + (0.08 * 70) = 6.26 \text{ ns}$

$$P2 = 0.9 + (0.06 * 70) = 5.1 \text{ ns}$$

5.6.3) $P1 = 1 + ((0.08 * 70) / 0.66) * 0.36 = 4.054 \text{ CPI}$

$$P2 = 1 + ((0.06 * 70) / 0.9) * 0.36 = 2.68 \text{ CPI}$$

P2 is faster because it has less CPI

5.12.1) PTE's for a single level page table = $2^{43}/2^{12} = 2^{31}$ PTE's

2^{33} bytes needed to store the page table because $2^{31} * 2^2 = 2^{33}$