CSCE 3953

Project Report 1

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**OBJECTIVE**

Project 1’s main purpose is to further gain familiarity with the Verilog language and simulating designs in ModelSim, but also to design and simulate a seven to one multiplexer (7to1 MUX). Project 0 was a basic, cursory view of what ModelSim has to offer. As Project 1 utilizes the background knowledge gained from each chapter of the tutorial, navigating the directory, project, code, and waveform interfaces was no issue. However, the programming of the design and testbench provided the most difficulty.

**DESIGN METHODOLOGY / CIRCUIT DIAGRAM**

Building on review in lectures and from previous classes, understanding the design structure of a MUX was simple. It has seven one-bit inputs, three select bits, and one output bit. The three select bits relate to the number of input bits (seven) by being the closest estimation to two raised to the third power. The key function of a MUX comes from the select bits. The output is almost entirely dependent on the state of the select bits. This allows many input signals to share one device.

Illustrated below is the circuit diagram for a 7to1 MUX.

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**SIMULATION METHOD**

The simulation method chosen for Project 1 is a waveform. Waveforms provide an intuitive, graphical interface to analyze the function of the simulated design as it progresses through time. A testbench is a way to test the validity of the design. This is done by providing each input with a value and allowing it to interact with the design to produce an accurate output. In Project 1’s case, the specific values provided were concerned with the state of the select bits. These values were reflected in the waveform.

**RESULT**

The resulting waveform shows the output changing in value based on the state of the select bits.

Below is a screenshot of the simulated 7to1 MUX as a waveform.

A screenshot of a computer

Description automatically generated

**ANALYSIS AND CONCLUSION**

In conclusion, designing, testing, and simulating a 7to1 MUX aids in the ultimate purpose of Project 1, to gain more familiarity with Verilog and ModelSim. By relying on past knowledge from previous courses, Project 0, and lectures, a waveform consistent with the design structure of the MUX was generated. The only difficulties experienced in the completion of Project 1 related to programming in Verilog. Overall, more practice in the setup process for the simulation streamlined the project time significantly.