CSCE 3953

Project Report 2

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**PART 1: Count and output the number of 1’s in a parallel 8-bit input**

**OBJECTIVE**

The purpose of Part 1 of Project 2 is to create a combinational design that counts the number of 1’s in an 8-bit input. The assumptions made whilst programming the testbench ran through the 256 combinations there are for an 8-bit number and modulated the output accordingly.

**DESIGN METHODOLOGY / CIRCUIT DIAGRAM**

This design needs to be specifically combinational; this means there are no reset or clock signals. The 8-bit inputs are generated by incrementing the given value by one 256 times. For each input case, the program runs through each bit, checks if it is a 1, and increments the output value. Otherwise, the output stays the same.

**SIMULATION METHOD**

Yet again, the simulation method for this part of Project 2 is a waveform. This waveform captures each of the 256 cases to verify the efficacy of the testbench.

**RESULT**

Below are each of the 256 cases (divided into 16 screen shots).

A computer screen with green lines

Description automatically generated

A computer screen shot of a black and green screen

Description automatically generated

A screenshot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated

A computer screen with green lines

Description automatically generated

A computer screen shot of a black screen

Description automatically generated

A computer screen with green lines

Description automatically generated

A screenshot of a computer

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A screenshot of a computer

Description automatically generated

A computer screen with green lines

Description automatically generated

A screenshot of a computer

Description automatically generated

**ANALYSIS AND CONCLUSION**

The purpose of Part 1 was to create a design that counts the number of 1’s in an 8-bit input. As the design was required to be combinational as opposed to sequential, this altered both the design and testbench code. The design code did not require a clock and reset; this was replaced by a for loop that simply increments the input before checking the whole input for 1’s.

**PART 2: BCD counter whose initial count is 5**

**OBJECTIVE**

The purpose of Part 2 of Project 2 is to create a BCD (binary coded decimal) counter. This specific counter works in a range of zero to nine; this classifies it as a decade counter. Where most BCD counters start from zero, the one made for Part 2 is required to start at five. Because of this added feature, one cycle of the output should start at five, loop to zero after nine, and end at four. This cycle is displayed graphically in a waveform which can be seen under the result section of this part of the report.

**DESIGN METHODOLOGY / CIRCUIT DIAGRAM**

With each positive edge of the clock, the 4-bit output is increased by one. Once the counter reaches 9, the reset signal then resets the count to zero. Being a sequential circuit design, the use of “=” in always blocks creates race conditions and is overall poor praxis. This issue is remedied when “<=” is used instead as shown in the source code.

Below is the circuit diagram for a BCD or decade counter.

A diagram of a circuit

Description automatically generated

**SIMULATION METHOD**

Much like Part 1 of this Project, the testbench is simulated via waveform. This is used to verify the functionality of the design using the clock timing and reset configuration written in the testbench.

**RESULT**

The waveform shows the clock, reset, and 4-bit output of the design. With each positive edge of the clock, the output value is incremented until it reaches the maximum value in a decade counter (9) where reset will reset the count value to zero.

Below is the waveform simulation of the BCD counter with an initial value of five.

A computer screen shot of a black and green screen

Description automatically generated

**ANALYSIS AND CONCLUSION**

The goal of Part 2 was an introduction to a BCD counter with an additional feature being the initial value is five. Additionally, this was the first time as sequential circuits were coded in Verilog; this aspect seemed like it was going to increase difficulty, but in practice made the code make more sense. Simulating the testbench by waveform showed the counting cycle required for the design. The idea of two different types of circuits in one report was daunting at first, but after writing the code and stimulating each design, the work was not as intensive.