CSCE 3953

Project Report 3

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Landon Reynolds

010975968

SEC001

10/9/23

**PART 1: Count and output the number of 1’s in a parallel 8-bit input**

**OBJECTIVE**

The purpose of this part one of this project is to synthesize part one of project two’s circuit. Project two’s circuit counted and outputted the number of 1’s present in each given 8-bit input. The process is much the same, however the implementation of Synopsys creates a circuit more accurate to reality.

**SYNTHESIS PROCESS**

The design is the same as part one of project two, but a virtual clock and modules with delay are added to the circuit. A virtual clock is needed to implement delay to combinational circuits. This delay can be seen in the waveform of the “Results” section of this report.

**SIMULATION METHOD**

The method of simulation is the same as part one of the previous project.

**RESULT**

Below is the synthesized version of a circuit that outputs the number of 1’s in a given 8-bit input.

A screenshot of a computer

Description automatically generated

**ANALYSIS AND CONCLUSION**

In conclusion, synthesizing project two part one’s design in Synopsys creates a version of the circuit that has delays and glitches which align more with what is seen in the real world. Virtual clocks are needed for combination designs as they give the modified gates a means to be delayed.

**PART 2: BCD counter whose initial count is 5**

**OBJECTIVE**

The purpose of part two of this project is to synthesize part two of project two’s circuit. Project two’s second design was a BCDcounter with the added feature of resetting when the counter reaches 5. The process is much the same, however the implementation of Synopsys creates a circuit more accurate to reality.

**SYNTHESIS PROCESS**

The design is the same as part two of project two, but a clock and modules with delay are added to the circuit. In contrast to part one’s clock, the BCD counter requires a generated clock. This generated clock has a set period that can be altered to meet various needs for power and area. By my discretion, the clock period is set to 20 MHz. This can be seen in the “Results” section of this part of the report.

**SIMULATION METHOD**

The simulation of this design is the same as the process undergone by part two of project twos design.

**RESULT**

Below is one cycle of the BCD counter with added delay.

A screenshot of a computer

Description automatically generated

Below is a zoomed-in section of the BCD counter to graphically represent delay.

A screenshot of a computer

Description automatically generated

**ANALYSIS AND CONCLUSION**

Part two of this project was my first experience in generating and modulating a clock for a synthesized circuit. Although the period chosen may not have been the most efficient for area and power consumption, the waveform still accurately displays the functionality of the design.