CSCE 3953

Project Report 4

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**OBJECTIVE**

The purpose of this project is to create a race light (which I have incorrectly called stoplight) circuit, synthesize it, and create a waveform. This race light is supposed to cycle between red, yellow, green, and then back to red.

**DESIGN METHODOLOGY / STATE TRANSITION GRAPH**

Below is the State Transition Graph for the race light.

A graph on lined paper

Description automatically generated

**SIMULATION METHOD**

The synthesized circuit was simulated via waveform.

**RESULT**

Below is a cycle of the circuit design (st1 is the red light, st2 is the yellow light, and st3 is the green light).

A screenshot of a computer

Description automatically generated

**ANALYSIS AND CONCLUSION**

In conclusion, the tasks of Project 4 consisted of creating a race light with a state transition graph, synthesizing the design, and simulating it. When the start button is on its negative edge, the race light cycle goes from Red-off-Yellow-off-Green-off-Red. The most challenging part of this project was writing the Verilog code of both the design and testbench in state transition graph form.