CSCE 3953

Project Report 5

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Landon Reynolds

010975968

SEC001

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**OBJECTIVE**

The purpose of Project 5 is to design a circuit with two 4-bit registers and 2 4-bit tri-state buffers to analyze the functionality of bus masters and bus slaves. These registers and tri-state buffers were then connected structurally to a top level design.

**DESIGN METHODOLOGY**

The first step in meeting the requirements for this design is designing a 4-bit D flip-flop. This process was issueless. Same goes with creating the 4-bit tri-state buffer, the behavior was quite simple to program. Then came the structuring of the bus. Although this part is just a wire, the inputs and outputs from the registers play a critical part in bus mastering and slaving.

**SIMULATION METHOD**

The design was synthesized in Design Vision and Simulated via waveform in ModelSim.

**RESULT**

Below is the waveform of the synthesized design displaying the state of each bit of the registers’ inputs and outputs.

A screenshot of a computer program

Description automatically generated

Below is a zoomed-in image of the synthesized waveform showing delay.

A screenshot of a computer

Description automatically generated

Below is the nonsynthesized version of the top-level design (see Analysis and Conclusion for elaboration)

A screenshot of a computer program

Description automatically generated

**ANALYSIS AND CONCLUSION**

In a general view of Project 5, about half of the requirements were familiar and nonchallenging; these parts include designing the D flip-flop and tristate buffer. However, constructing the bus structurally and creating the waveform were the most challenging and time-consuming tasks as they required some tweaking to achieve the required result. The main issue was the post synthesis bus was not asserting high impedance at dead time as it should have but was simply not asserting any signal at all. I am unsure as to why this is the case and would appreciate a hint as to where there could be an error in the synthesizing process.