CSCE 3953

Project Report 6

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Landon Reynolds

010975968

SEC001

10/31/23

**OBJECTIVE**

The main objective of Project 6 is to execute static timing analysis on Project 4’s Moore Machine design. This is done by utilizing PrimeTime as our analysis software. PrimeTime first reads the Verilog code written for written for Project 4, sets up operations conditions, defines constraints, and finally runs a static timing analysis. This analysis can run through every combination of input pins and output pins.

**LOGIC SYNTHESIS CONSTRAINTS**

Regarding logic synthesis, there were not too many modifications made to the design. The constraint applied to the circuit in Design Vision was instantiating a clock that had a period of 40 ns.

**TIMING CONSTRAINTS IN PRIMETIME**

The constraints applied during static timing analysis needed to induce a design that violated the slack value. Initially, I thought decreasing the period of the design would suffocate it and result in a violated slack value; however, the design still managed to meet the slack requirement. Changing the uncertainty of the clock resulted in a violated slack value.

**RESULT**

Below and left is the version of the design that met slack with only the logic synthesis constraints. Below and on the right is the design with violated slack and modified clock period and uncertainty.

A screenshot of a computer program

Description automatically generatedA screenshot of a computer screen

Description automatically generated

**ANALYSIS AND CONCLUSION**

The main objective of Project 6 was to demonstrate the effects of modifying values like uncertainty, setup time, and hold time of a design during static timing analysis. This resulted in a design put under such critical constraints that it violated timing and slack. Speeding up a design’s operating speed could lead to violations in slack as there are limitations to how fast gates can function and incorporating their respective delays further widens room for violation. Increasing uncertainty also makes slack violation more probable as it changes the arrival time of a clock drastically. Gaining familiarity with PrimeTime allows circuits to be stress tested and optimized under certain conditions.