October 26, 2020 2:18 PM

Objective

- More exposure to decoders
- To familiarize the student with the Xilinx Vivado development environment.
- To create a VHDL project containing VHDL source fles and a simulaton testbench.
- To run a simulaton and verify the operaton of a decoder specifed using VHDL.**Prelab Notes**

Might be a good idea to plug every aldm cable to the test header. For organization's sake.

Equipment used:

- **Vivado and Xilinx**

RAMS

This lab is done entirely on our pc/vpn. Do not keep food/drink around hardware. Avoid spillage, protecting from damage or electrical harm. Digital safety measures should be taken into account - save often, make backups.

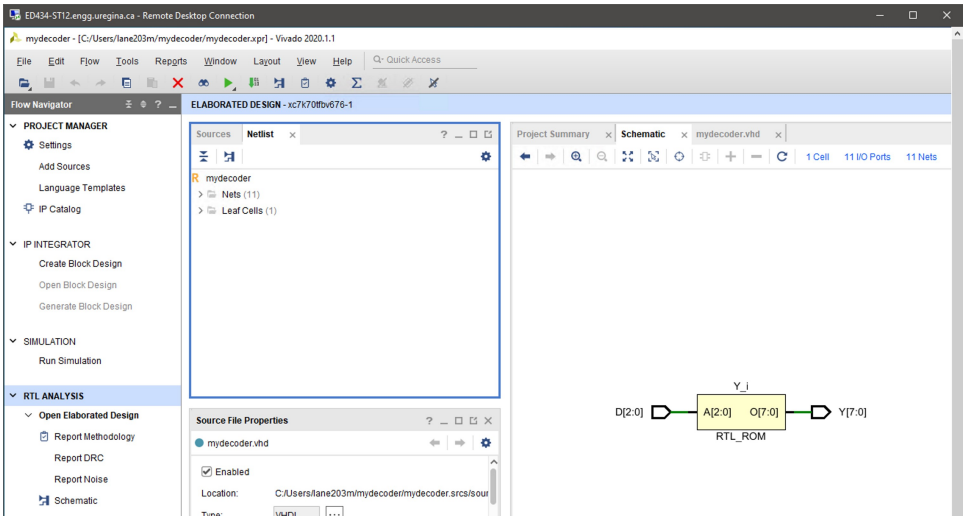
Pre-Work Plan

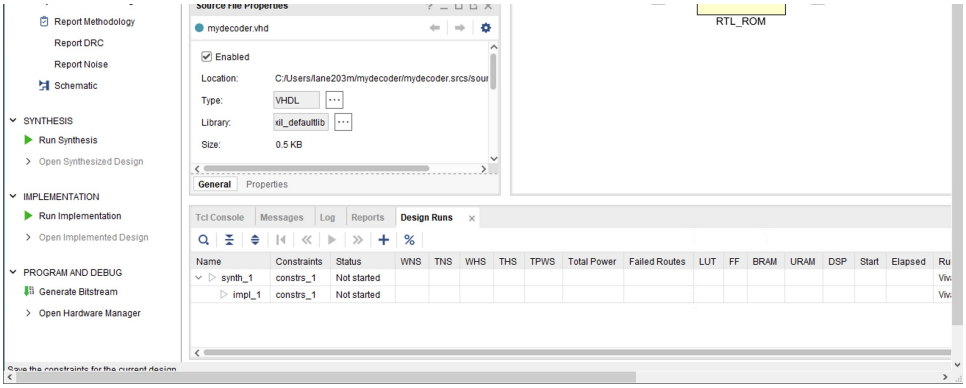
I started with this initial model, but quickly changed to a new design as seen in the work result

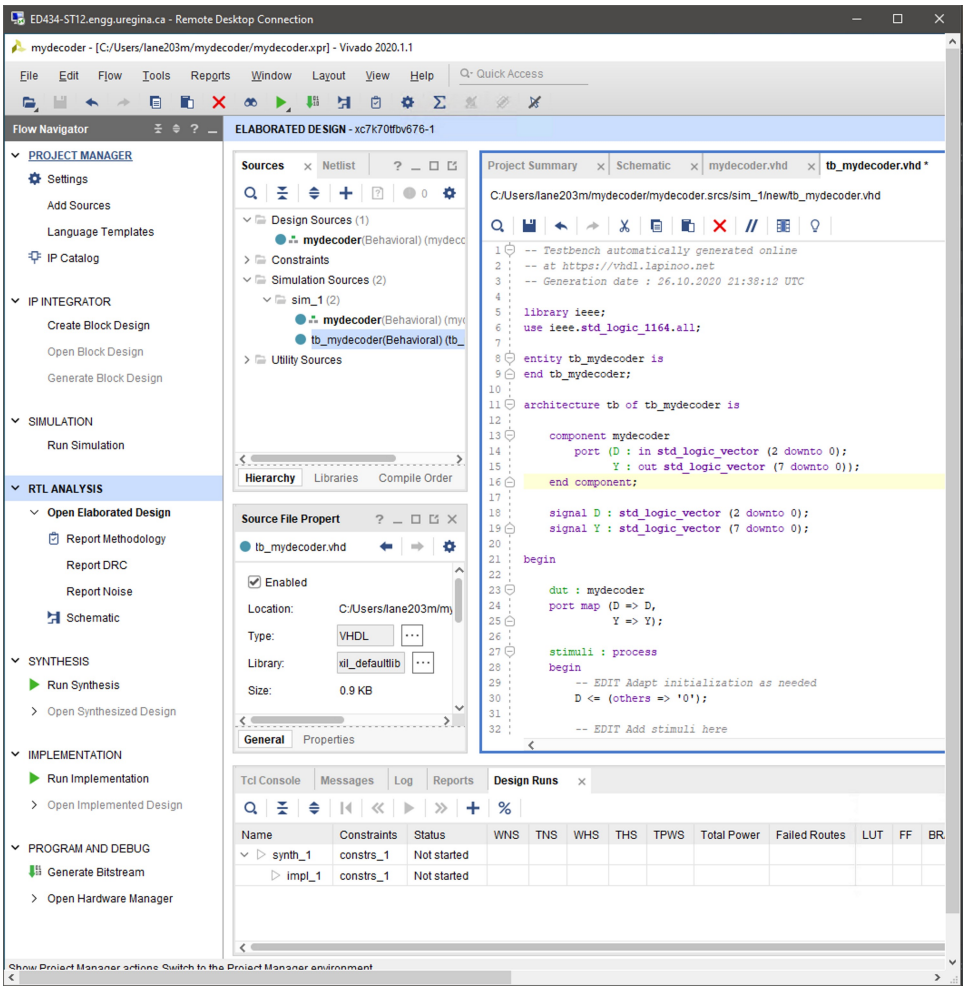
Process

We create our file/project as myDecoder in vivado. Everything so far is in VHDL

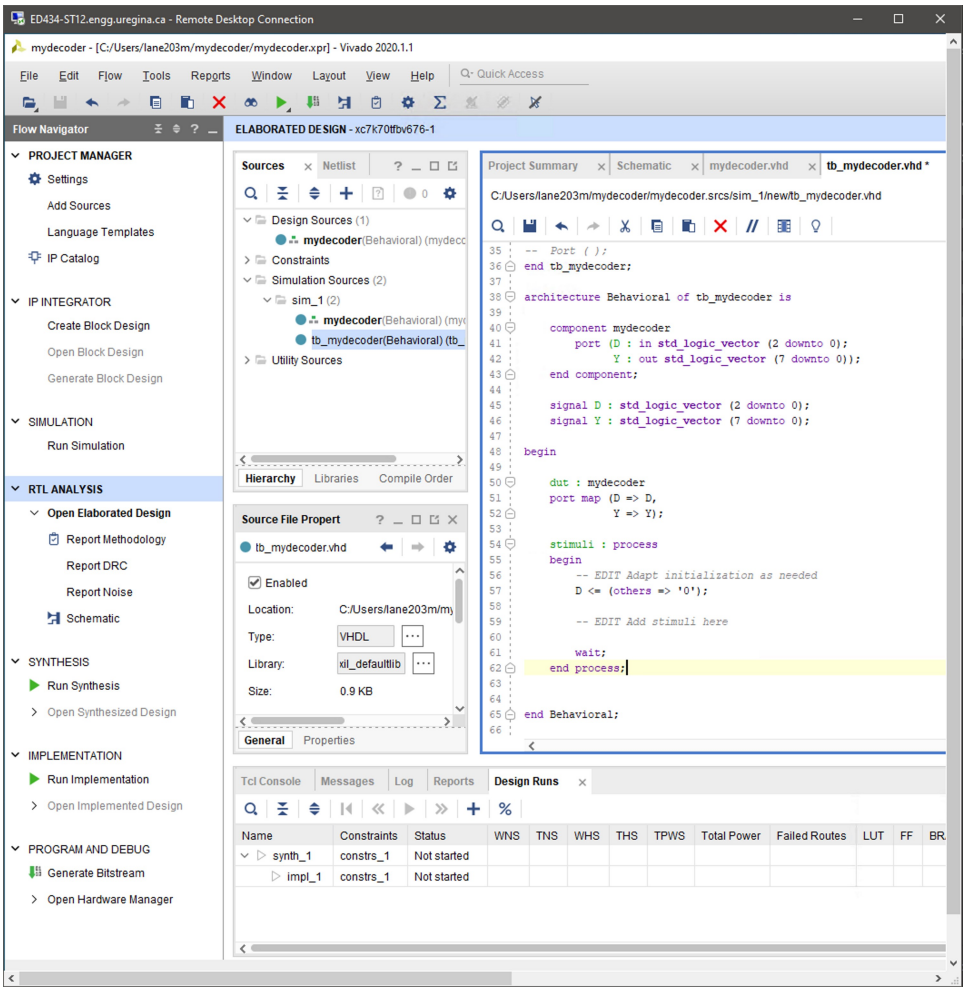
From flow navigator, we open elaborated design



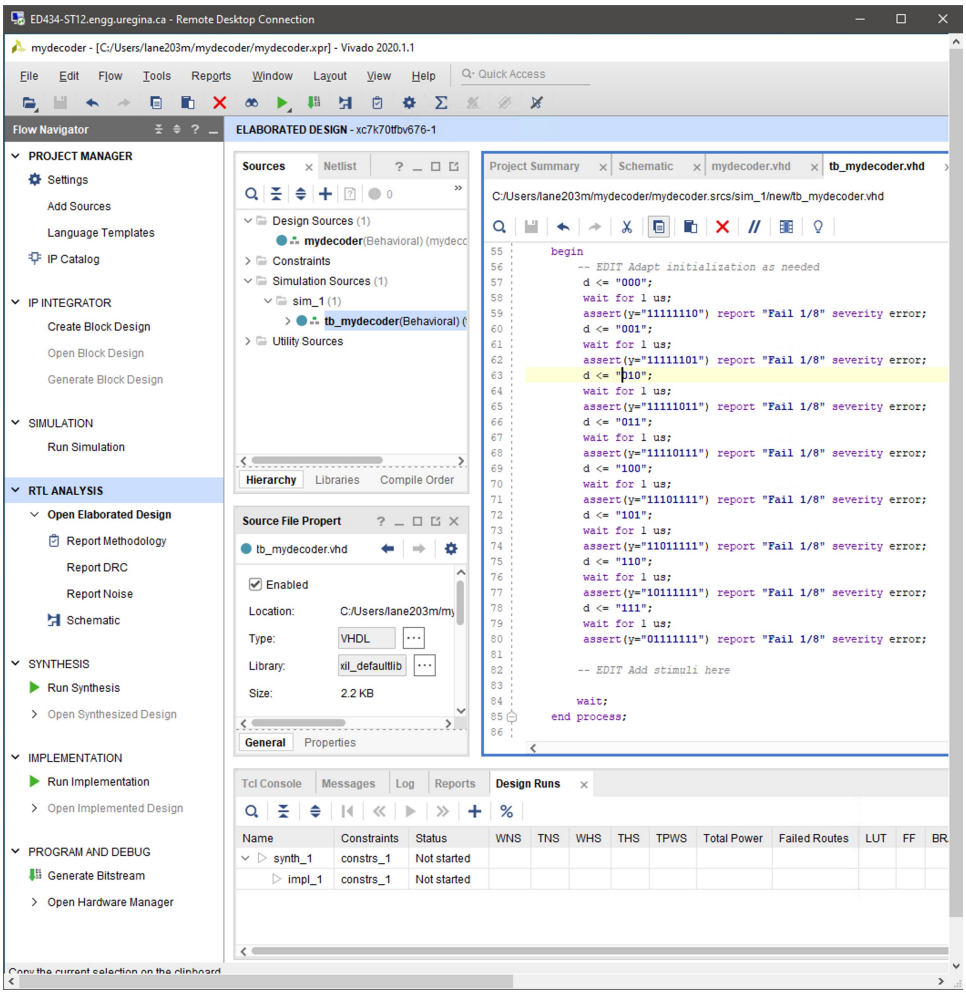


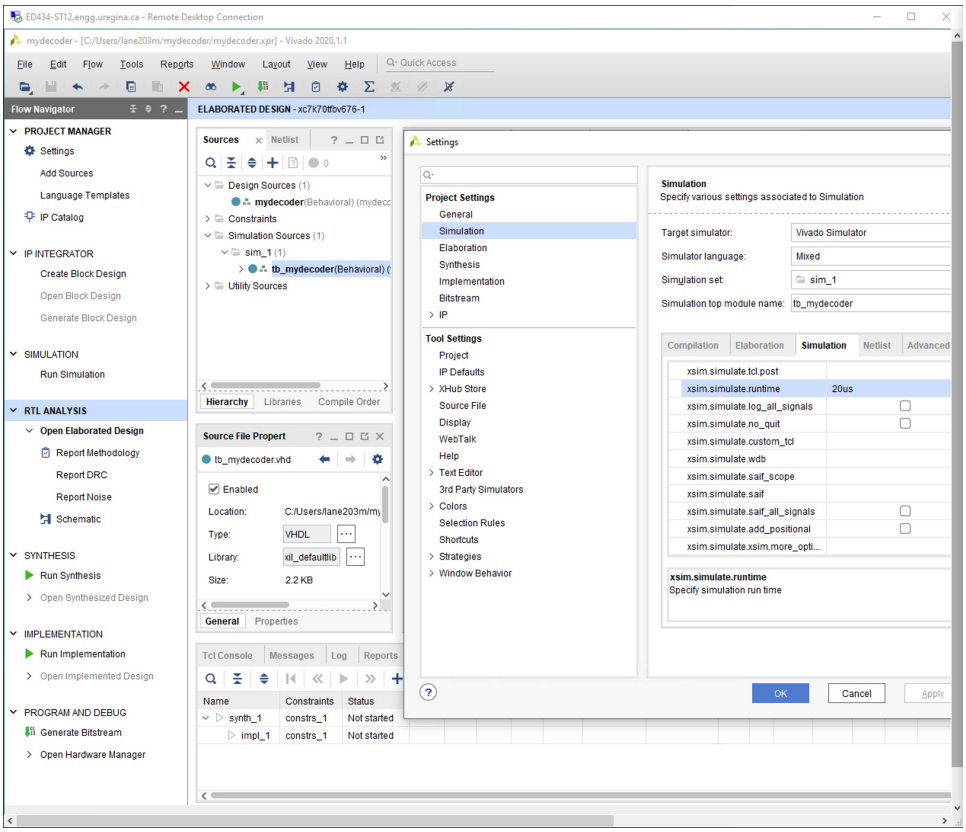


We setup our test bench

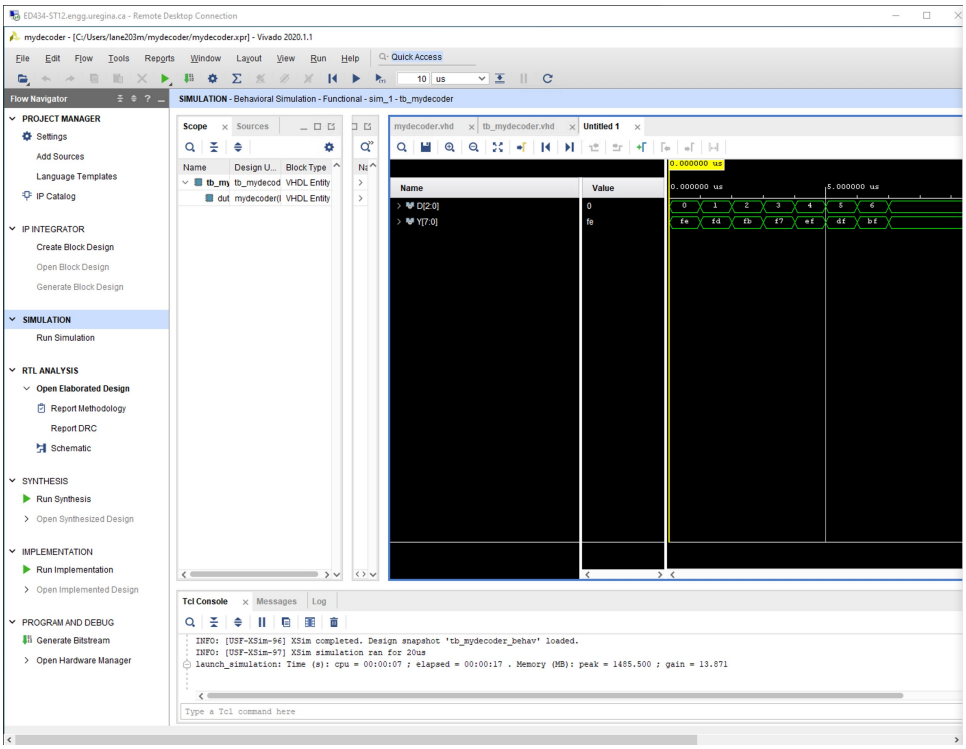


These are our tests for the simulation





Our result is a 3 to 8 decoder. This is similar to lab 4's decoder 74HC138



Analysis

2

Notice, our entries in the define module has created the entity for us. So we have our 3 input d, and 8 input y.

3

When using with select, we are saying with a given d, give y. So, when d is 000, give 11111110

4

"A port map maps signals in an architecture to ports on an instance within that architecture. Port maps can also appear in a block or in a configuration. The connections can be listed via positional association or via named association."

I believe this allows us to access the entities d,y declared in mydecoder.vhd.

I believe wait for x us is what creates the slight pauses or breaks in our simulation. Here we can easily see which test is which. So, every 1us, our simulation dips and gives us the rectangular hexagons. We wait before another answer appears.

5

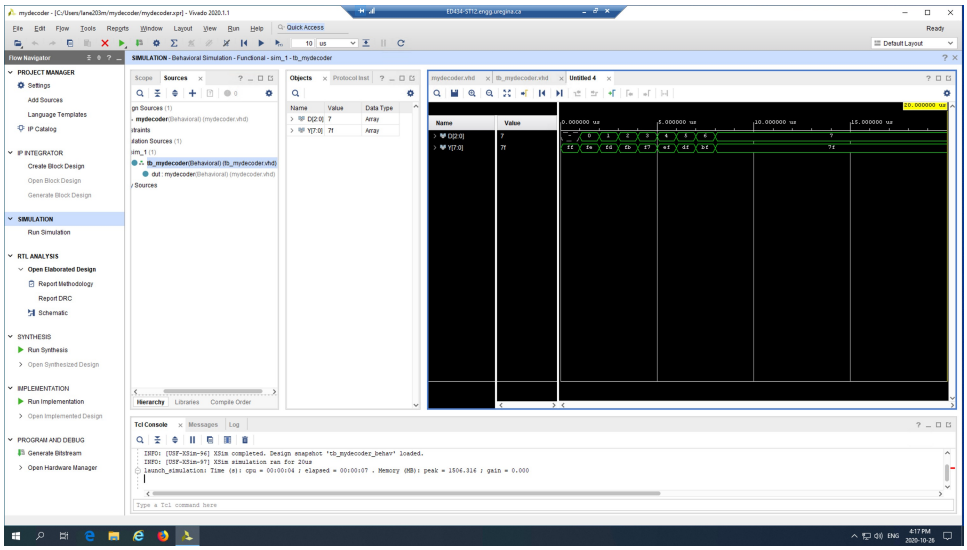
Note, if we made a test for

d <= "---";

wait for 1 us;

assert(y="11111111") report "Fail 1/8" severity error;

Our result would be ff, or 11111111 - as expected for values of "other"


mydecoder - [C:/Users/lana203m/mydecoder/mydecoder.xpr] - Vivado 2020.1.1
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_mydecoder
Sources
Objects
Protocol Inst
mydecoder.vhd
tb_mydecoder.vhd
Untitled 4
Name
Value
Data Type
D[2:0]
Y[7:0]
Hierarchy
Libraries
Compile Order
Tcl Console
Messages
Log
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_mydecoder_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 20us
launch_simulation: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1504.316 ; gain = 0.000
Type a Tcl command here
ENG
4:17 PM
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